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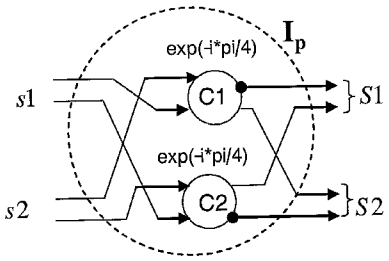
(54) **Title:** CORDIC-BASED FFT AND IFFT APPARATUS AND METHOD

FIG. 6



(57) **Abstract:** Disclosed is an apparatus for performing a 2-point FFT, comprising two CORDIC processors (C1 and C2), each including: two input ports (p1 and P2) that respectively represent real input port and imaginary input port; and two output ports (P1 and P2) that respectively represent real output port and imaginary output port for outputting rotated data; wherein real part of a first input signal (s1) is applied to the imaginary input port (p2) of the first CORDIC processor(C1); imaginary part of a first input signal (s1) is applied to the imaginary input port (p2) of the second CORDIC processor(C2); real part of a second input signal (s2) is applied to the real input port (p1) of the first CORDIC processor (C1); imaginary part of the second input signal (s2) is applied to the real input port (p1) of the second CORDIC processor (C2); the first and second CORDIC processors rotate the respective input signals applied thereto by 45 degrees in the clockwise direction; data from the real output port (P1) of said first CORDIC processor (C1), and data from the real output port (P2) of the second CORDIC processor (C2), constitute respectively real part and imaginary part of a first output signal (S1); and data from the imaginary output port (P2) of said first CORDIC processor (C1), and data from the imaginary output port (P2) of said second CORDIC processor constitute respectively real part and imaginary part of a second output signal (S2).

WO 2009/040957 A2

DESCRIPTION

CORDIC-BASED FFT AND IFFT APPARATUS AND METHOD

FIELD OF THE INVENTION

This invention relates to a CORDIC-based digital signal processing system and, more particularly, to CORDIC-BASED FFT AND IFFT apparatus and method.

BACKGROUND OF THE INVENTION

In general, an N-point FFT (Fast Fourier Transform) is expressed mathematically as [1]

$$X_k = \sum_{n=0}^{N-1} x_n e^{\frac{-i2\pi nk}{N}}, \qquad (1)$$

where x_n is the nth element of a discrete time signal vector $\mathbf{x} = [x_0 \ \cdots \ x_{N-1}]$ with N data samples, and X_k is the kth element of vector $\mathbf{X} = [X_0 \ \cdots \ X_{N-1}]$ that corresponds to FFT of $\mathbf{x}$. In general, both x_n and X_k can be considered as complex numbers. Direct implementation of an FFT using (1) is always avoided due to its extremely high computation load especially when N is large. Thus, instead of directly implementing (1), an N-point FFT or IFFT (Inverse Fast Fourier Transform) is always implemented using stages of small-sized FFT or IFFT units. As an example, an 8-point FFT can be implemented using three stages each comprising four 2-point FFT operations.

Further, in order to reduce processing latency while increasing throughput of a device that implements FFT/IFFT operations, a number of processors are used in parallel. Fig.1 shows a typical parallel-based mode of implementing an 8-point IFFT/FFT [1]. In Fig.1, circled regions represent processors that operate in parallel. Of these regions, the shaded ones, "●", represent multiplication by twiddle factor, while regions marked with un-shaded "○" represents addition operations.

FFT has conventionally been implemented using DSP (Digital Signal Processor), parameterized ASIC(Application Specific Integrated Circuit), IP(intellectual property) cores, FPGA(Field Programmable Gate Array) and reconfigurable processors. It has been noted that when a processor is based on CORDIC(coordinate rotation digital computer) [2], the resulting FFT utilizes less hardware resources in comparison to MAC (Multiply and Accumulate) based processors. This is especially so when the size of FFT is large. Whereas there are hybrid processors based on a combination of CORDIC and ADDER units [3], or CORDIC and FFT/IFFT Kernel [2][P1], this patent consider processors which are purely based on CORDIC [4][5][6].

As an example, Fig.2 shows a conventional FFT based on CORDIC for processing FFT of a vector with two data samples "s1" and "s2", and generating two output data samples "S1" and "S2". An intermediate signal S'2 is generated by a pair of CORDIC processors. This pair of CORDIC processors has been labeled I.

The intermediate signal S'2 is given by

$$S'2 = -2^{-0.5}(s1 - s2) \quad (2)$$

Therefore, output signals "S1" and "S2" are related to the input samples "s1" and "s2" by the following equations:

$$\begin{aligned} S1 &= 2^{-0.5}(s1 + s2) \\ S2 &= 2^{-0.5}(s1 - s2) \end{aligned} \quad (3)$$

From (1), FFT $[S1'\ S2']$ of $[s1\ s2]$ is given by

$$\begin{aligned} S1' &= (s1 + s2) \\ S2' &= (s1 - s2) \end{aligned} \quad (4)$$

[Non-Patent Document 1]

J.G. Proakis and D.G. Manolakis, Introduction to Digital Signal Processing, Maxwell Macmillan, 1989

[Non-Patent Document 2]

Y.H. Hu, "CORDIC-Based VLSI Architecture for Digital Signal Processing," IEEE Signal Processing Magazine, pp.16-July 1992

[Non-Patent Document 3]

R. Sarmineto, F. Tobajas, et.al, "A CORDIC Processor for FFT Computations and Its Implementation Using Gallium Arsenide Technology," IEEE Trans. on VLSI Systems, pp.18-30, vol.6, no.1, March 1998

[Non-Patent Document 4]

C. Ying, S.Chen and J. Chih, "Efficient CORDIC Designs for Multi-Mode OFDM FFT," ICASSP Page(s): 1036 -1039, vol.3, May

2006

[Non-Patent Document 5]

B. Heyne, J. Gotze, "A Pure CORDIC based FFT for Reconfigurable Digital Signal Processing," 12th European Signal Processing Conference (EUSIPCO2004), Vienna, Austria, 2004

[Non-Patent Document 6]

B. Heyne, J. Gotze, "CORDIC-Based algorithms for software defined Radio (SDR) baseband Processing," Adv. Radio Sci., 4, 179-184, 2006

[Patent Document 1]

Kulkarni et al., "Reconfigurable Vector-FFT/IFFT, Vector-Multiplier/Divider," Patent US 7,082,451 B2

SUMMARY OF THE DISCLOSURE

The entire disclosures of the above mentioned Non-Patent Documents and Patent Document are herein incorporated by reference thereto. The analysis below described is given by the present invention.

From the equations (2) and (3), it can be said that conventional purely CORDIC based FFT requires a processor that perform only sign reversal operation.

For large size radix-2 based FFT or IFFT, the sign reversal operation ends up consuming significant amount or resources.

Another example is given in Fig.3 for the case of an 8-point FFT [5][6]. With reference to Fig.3, there are provide first, second

and third stages, each including four pairs of CORDIC processors. In Fig.3, the pairs of CORDIC processors that have been labeled as I, II and III, are given in Figs.2, 4 and 5, respectively.

As in the case of a 2-point FFT that has been explained above, additional CORDIC processors are used to perform sign reversal in order to generate scaled results of an 8-point FFT.

As described above, the conventional purely CORDIC based FFT or IFFT requires additional processing steps or processors for performing sign reversal.

The minimization of computational load in a purely CORDIC-based processor that is used to implement FFT or IFFT is demanded.

Accordingly, it is an object of the present invention to provide an apparatus and method which may reduce hardware resources or processing steps in a CORDIC-based FFT or IFFT.

In one aspect (first) of the present invention, there is provided an apparatus for performing a 2-point FFT (Fast Fourier Transform) wherein first and second complex input signals ('s1' and 's2') are evaluated to generate 2-point FFT's first and second complex output signals ("S1" and "S2"), said apparatus comprising first and second CORDIC processors (C1 and C2), each of the first and second CORDIC processors including:

first and second input ports ('p1' and 'p2') that respectively represent real input port and imaginary input port; and

first and second output ports ('P1' and 'P2') that respectively

represent real output port and imaginary output port for outputting rotated data; wherein real part of the first input signal ('s1') is applied to the imaginary input port ('p2') of the first CORDIC processor (C1);

imaginary part of the first input signal ('s1') is applied to the imaginary input port ('p2') of the second CORDIC processor (C2);

real part of the second input signal ('s2') is applied to the real input port ('p1') of the first CORDIC processor (C1);

imaginary part of the second input signal ('s2') is applied to the real input port ('p1') of the second CORDIC processor (C2);

the first and second CORDIC processors (C1 and C2) rotate the respective input signals by 45 degrees in the clockwise direction;

data from real output port ('p1') of said first CORDIC processor (C1), and data from real output port ('p1') of the second CORDIC processor (C2), constitute respectively real part and imaginary part of the 2-point FFT's first output signal ("S1"); and

data from the imaginary output port ('p2') of said first CORDIC processor (C1), and data from the imaginary output port ('p2') of said second CORDIC processor (C2) constitute respectively real part and imaginary part of the 2-point FFT's second output signal (" S2 ").

In another aspect (second aspect) of the present invention, there is provided an apparatus for performing a 2-point FFT (Fast Fourier Transform), first and second complex input signals ('s1' and 's2') are evaluated to generate 2-point FFT's first and second

complex output signals ("S1" and "S2"), said apparatus comprising first and second CORDIC processors (C1 and C2), each of said first and second CORDIC processors comprising at least first and second input ports ('p1' and 'p2') that respectively represent real input port and imaginary input port; and

at least first and second output ports ('P1' and 'P2') that respectively represent real output port and imaginary output port for outputting rotated data; wherein

real part of said first input signal ('s1') is applied to the real input port of the first CORDIC processor (C1);

imaginary part of said first input signal ('s1') is applied to the real input port of the second CORDIC processor (C2);

real part of the second input signal ('s2') is applied to the imaginary input port of the first CORDIC processor (C1);

imaginary part of the second input signal ('s2') is applied to the imaginary part of the second CORDIC processor (C2);

the first and second CORDIC processors (C1 and C2) rotate respective input signals applied thereto by 45 degrees in the anticlockwise direction;

data from imaginary output port of the second CORDIC processor (C2), and data from the imaginary output port of the first CORDIC processor (C1), constitute respectively real part and imaginary part of the 2-point FFT's first output signal ("S1"); and

data from real output port of the second CORDIC processors (C2), and data from the real output port of the first CORDIC

processors (C1), constitute respectively real part and imaginary part of the 2-point FFT's second output signal ("S2").

In a third aspect of the present invention, there is provided an apparatus for performing a 4-point FFT, said apparatus comprising first and second stages for processing FFT of four complex data samples,

the first stage comprising two 2-point FFT for processing four input signals of complex data (x1,x2,x3,x4);

a second stage for processing the output of the first stage using two 2-point FFT;

wherein in the first stage, data is processed as set forth in first or second aspect.

In a fourth aspect of the present invention, there is provided an apparatus for performing a 4-point FFT, said apparatus comprising first and second stages for processing FFT of four complex data samples,

the first stage comprising two 2-point FFT for processing input signals of complex data (x1,x2,x3,x4);

the second stage for processing the output of the first stage using first and second pair of CORDIC processors;

each of the first and second CORDIC processors including at least first and second input ports ('p1' and 'p2') that respectively represent real input port and imaginary input port; and

at least first and second output ports ('P1' and 'P2') that respectively represent real output port and imaginary output port for

outputting rotated data;

wherein in the second stage of the FFT,

input signals (a1, a2) into the first pair of CORDIC processors is processed as stated in the first or second aspect;

input signals (a3, a4) into the second pair of CORDIC processors is processed as follows:

applying real part of the first input signal ('a3') to the real input port of the first CORDIC processor (C1) of the second pair of CORDIC processors;

applying imaginary part of the first input signal ('a3)' to the real input port of the second CORDIC processor (C2) of the second pair of CORDIC processors;

applying real part of the second input signal ('a4') to the imaginary input port of the first CORDIC processor (C1) of the second pair of CORDIC processors; and

applying imaginary part of the second input signal ('a4') to the imaginary input port of the second CORDIC processor (C2) of the second pair of CORDIC processors;

two CORDIC processors (C1 and C2) of the second pair of CORDIC processors, rotate respective input signals applied thereto by 45 degrees in the anticlockwise direction;

imaginary output port of first CORDIC processor (C1), and real output port of the second CORDIC processor (C2) in the second pair of CORDIC processors, constitute respectively real part and imaginary part of the third output signal ("S2") from the second

stage of the FFT;

real output port of first CORDIC processor (C1), and data from the imaginary output port of the second CORDIC processor (C2) in the second pair of CORDIC processors, constitute respectively real part and imaginary part of the fourth output signal ("S3") from the second stage of the FFT.

In a fifth aspect of the present invention, there is provided an apparatus for performing an 8-point FFT, comprising three stages for processing FFT of eight complex data samples;

the first stage comprising two pairs of 4-point FFT for processing eight complex input signals (s1,s2,...,s8) and generate eight complex output signals;

the output of said two pairs of 4-point FFT being multiplied by twiddle factors in the second stage to generate an output for being processed by the third stage of the 8-point FFT;

the third stage comprising four pairs of 2-point FFT, wherein the 2-point FFT in the third stage, data is processed has as set forth in first aspect or second aspect.

In a sixth aspect of the present invention, there is provided an apparatus for performing an 8-point FFT comprising three stages for processing FFT of eight complex data samples;

the first stage comprising two pairs of 4-point FFT for processing the eight samples of complex input signals (s1,s2,...,s8) and generate eight samples of complex output signals;

the output of said pairs of 4-point FFT being selectively

multiplied by twiddle factors or rotated by an equivalent rotational angle in the second stage to generate an output for being processed by the third stage of the 8-point FFT;

the third stage comprising four pairs of CORDIC processors;

each of the CORDIC processors in the four pairs of CORDIC processors comprising at least two input ports ('p1' and 'p2') that respectively represent real input port and imaginary input port; and

at least first and second output ports ('P1' and 'P2') that respectively represent real output port and imaginary output port for outputting rotated data;

wherein the third stage, one of the pairs of CORDIC processors process two input signals (a8 and a9) of complex data applied thereto to generate two output signals (A8 and A9) as follows:

applying real part of the first input signal ('a8') to the real input port of the first CORDIC processor (C1) of the pair of CORDIC processors;

applying imaginary part of the first input signal ('a8)' to the real input port of the second CORDIC processor (C2) of the pair of CORDIC processors;

applying real part of second input signal ('a9') to the imaginary input port of the second CORDIC processor (C2) of the pair of CORDIC processors;

applying imaginary part of second input signal ('a9') to the imaginary input port of the first CORDIC processor (C1) of the pair

of CORDIC processors;

wherein two CORDIC processors (C1 and C2), of the pair of CORDIC processors, rotate respective input signals applied thereto by 45 degrees in the anticlockwise direction;

data from the imaginary output port of first CORDIC processor (C1), and data from the real output port of the second CORDIC processor (C2) in the second pair of real number CORDIC processors, constitute respectively real part and imaginary part of the first output signal;

data from the real output port of first CORDIC processor (C1), and data from the imaginary output port of the second CORDIC processor (C2) in the second pair of CORDIC processors, constitute respectively real part and imaginary part of the second output signal.

In a seventh aspect of the present invention, there is provided an apparatus for performing an FFT comprising multiple stages for processing FFT of complex data samples, with at least one stage implemented using at least one 2-point FFT, wherein in the stage implementing 2-point FFT, at least one of the 2-point FFT will process data as set forth in first or second aspect.

In an eighth aspect of the present invention, there is provided an apparatus for performing an FFT comprising multiple stages for processing FFT of complex data samples with at least one stage implemented using 4-point FFT, wherein the stage, at least one of the 4-point FFT data will be processed as set forth in third aspect or fourth aspect.

In a ninth aspect of the present invention, there is provided an apparatus for performing an FFT comprising multiple stages for processing FFT of complex data samples with at least one stage implemented using 8-point FFT, wherein the stage, at least one of the 8-point FFT data will be processed as set forth in fifth aspect or sixth aspect.

In a tenth aspect of the present invention, there is provided a processor for processing four complex data samples (a1, a2, a3 and a4), said processor comprising two pairs of CORDIC processors with at least two CORDIC processors (C1 and C2) for rotating second (a4) complex input signals applied thereto in the clockwise direction by 90 degrees and evaluating a 2-point FFT of the first input signal sample (a3) and rotated second input signal sample;

each the CORDIC processors comprising at least first and second input ports ('p1' and 'p2') that respectively represent real input port and imaginary input port; and

at least first and second output ports ('P1' and 'P2') that respectively represent real output port and imaginary output port for outputting rotated data,

where in the processor,

first and second input signals into the first pair of CORDIC processors are processed as defined in the first aspect or second aspect and

third and fourth input signals ('a3' and 'a4') into the second pair of CORDIC processors are processed as follows:

applying real part of the third input signal ('a3') to the real input port of the first CORDIC processor (C1) of the second pair of CORDIC processors;

applying imaginary part of the third input signal ('a3') to the real input port of the second CORDIC processor (C2) of the second pair of CORDIC processors;

applying real part of the fourth input signal ('a4') to the imaginary input port of the second CORDIC processor (C2) of the second pair of CORDIC processors;

applying imaginary part of the fourth input signal ('a4') to the imaginary input port of the second CORDIC processor (C2) of the second pair of CORDIC processors;

two CORDIC processors (C1 and C2) of the second pair of CORDIC processors, rotate respective input signals applied thereto by 45 degrees in the anticlockwise direction;

data from the imaginary output port of the first CORDIC processor (C1), and data from the real output port of the second CORDIC processor (C2) in the second pair of real number CORDIC processors, constitute respectively real part and imaginary part of a first output signal;

data from the real output port of first CORDIC processor (C1), and data from the imaginary output port of the second CORDIC processor (C2) in the second pair of CORDIC processors, constitute respectively real part and imaginary part of a second output signal.

In an eleventh aspect of the present invention, there is

provided an apparatus for performing a 2-point IFFT comprising two CORDIC processors (C1 and C2), each comprising at least first and second input ports ('p1' and 'p2') that respectively represent real input port and imaginary input port; and

at least first and second output ports ('P1' and 'P2') that respectively represent real output port and imaginary output port for outputting rotated data;

wherein in the 2-point IFFT, IFFT of two samples of complex input signals ('s1' and 's2') is evaluated to generate two output signal ("S1" and "S2"),

real part of the first input signal ('s1') is applied to imaginary port ('p2') of the first CORDIC processor (C1);

imaginary part of the first input signal ('s1') is applied to imaginary port ('p2') of the second CORDIC processor (C2);

real part of second input signal ('s2') is applied to the real input port of the first CORDIC processor (C1);

imaginary part of second input signal ('s2') is applied to the real input port of the second CORDIC processor (C2);

two CORDIC processors (C1 and C2) rotate respective input signals applied thereto by 45 degrees in the clockwise direction;

data from the real output port ('p1') of first CORDIC processor (C1), and data from the real output port ('P1') of the second CORDIC processor (C2), constitute respectively real part and imaginary part of the 2-point IFFT's first output signal ("S1";

data from the imaginary output port ('P2') of first CORDIC

processor (C1), and data from the imaginary output port of the second CORDIC processor (C2), constitute respectively real part and imaginary part of the 2-point IFFT's second output signal ("S2").

In a twelfth aspect of the present invention, there is provided an apparatus for performing a 2-point IFFT comprising two CORDIC processors (C1 and C2), each including at least first and second input ports ('p1' and 'p2') that respectively represent real input port and imaginary input port; and

at least first and second output ports ('P1' and 'P2') that respectively represent real output port and imaginary output port for outputting rotated data;

wherein IFFT of two samples of complex input signals ('s1' and 's2') is evaluated as follows:

applying the real part of the first input signal ('s1') to the real input port of the first CORDIC processor (C1);

applying imaginary part of the first input signal ('s1') to the real input port of the second CORDIC processor (C2);

applying real part of second input signal ('s2') to the imaginary input port of the first CORDIC processor (C1); and

applying imaginary part of second input signal ('s2') to the imaginary part of the second CORDIC processor (C2);

and generates two output signals ('S1' and 'S2'),

wherein in the 2-point IFFT,

the two CORDIC processors (C1 and C2) rotate respective input signals applied thereto by 45 degrees in the anticlockwise

direction;

data from the imaginary output port of second CORDIC processor (C2), and data from the imaginary output port of the first CORDIC processor (C1), constitute respectively real part and imaginary part of the 2-point IFFT's first output signal ("S1"); and

data from the real output port of second CORDIC processors(C2), and data from the real output port of the first CORDIC processors (C1), constitute respectively real part and imaginary part of the 2-point IFFT's second output signal ("S2").

In a thirteenth aspect of the present invention, there is provided an apparatus for performing a 4-point IFFT comprising two stages for processing IFFT of four complex data samples,

the first stage comprising two 2-point IFFT for processing complex input signals (x1,x2,x3,x4);

the second stage processing the output of the first stage using two 2-point IFFT, where in the first stage of the 4-point IFFT:

data is processed as set forth in the eleventh aspect or twelfth aspect.

In a fourteenth aspect of the present invention, there is provided an apparatus for performing a 4-point IFFT comprising two stages for processing IFFT of four complex data samples,

the first stage comprising two 2-point IFFT for processing complex input signals (x1,x2,x3,x4);

the second stage processing the output of the first stage using two pairs of CORDIC processors;

each of the CORDIC processors including at least first and second input ports ('p1' and 'p2') that respectively represent real input port and imaginary input port; and

at least first and second output ports ('P1' and 'P2') that respectively represent real output port and imaginary output port for outputting rotated data;

wherein in the second stage of the IFFT,

input signals (a1, a2) into the first pair of CORDIC processors is processed as set forth in the eleventh aspect or twelve aspect;

input signals (a3, a4) into the second pair of CORDIC processors is processed as follows:

applying real part of the first input signal ('a3') to the real input port of the first CORDIC processor (C1) of the second pair of CORDIC processors;

applying imaginary part of the first input signal ('a3') to the real input port of the second CORDIC processor (C2) of the second pair of CORDIC processors;

applying real part of second input signal ('a4') to the imaginary input port of the second CORDIC processor (C2) of the second pair of CORDIC processors;

applying imaginary part of second input signal ('a4') to the imaginary input port of the first CORDIC processor (C1) of the second pair of CORDIC processors; and

two CORDIC processors (C1 and C2) of the second pair of CORDIC processors, rotating respective input signals applied thereto

by 45 degrees in the anticlockwise direction;

wherein data from the real output port of first CORDIC processor (C1), and data from the imaginary output port of the second CORDIC processor (C2) in the second pair of CORDIC processors, constitute respectively real part and imaginary part of the third output signal ("X3") from the second stage of the IFFT; and

data from the imaginary output port of first CORDIC processor (C1), and data from the real output port of the second CORDIC processor (C2) in the second pair of CORDIC processors, constitute respectively real part and imaginary part of the fourth output signal ("X4") from the second stage of the IFFT.

In a fifteenth aspect of the present invention, there is provided an apparatus for performing an 8-point IFFT comprising three stages for processing IFFT of eight complex data samples;

the first stage comprising two pairs of 4-point IFFT for processing the eight samples of complex input signals (s1,s2,...,s8) and generate eight complex output signals;

wherein the output of said two pairs of 4-point IFFT are multiplied by twiddle factors in the second stage to generate an output for being processed by the third stage of the 8-point IFFT;

the third stage comprising four pairs of 2-point IFFT, wherein in the 2-point IFFT in the third stage, data is processed as set forth in the eleventh aspect or twelfth aspect.

In a sixteenth aspect of the present invention, there is provided an apparatus for performing an 8-point IFFT comprising

three stages for processing IFFT of eight complex data samples;

the first stage comprising two pairs of 4-point IFFT for processing the eight complex input signals (s1,s2,...,s8) and generate eight complex output signals;

the output of said pairs of 4-point IFFT being selectively multiplied by twiddle factors or rotated by an equivalent rotational angle in the second stage to generate an output for being processed by the third stage of the 8-point IFFT;

the third stage comprising four pairs of CORDIC processors;

each of the CORDIC processors in the four pairs of CORDIC processors comprising at least first and second input ports ('p1' and 'p2') that respectively represent real input port and imaginary input port; and

at least first and second output ports ('P1' and 'P2') that respectively represent real output port and imaginary output port for outputting rotated data;

wherein in the third stage, one of the pairs of CORDIC processors process two input samples (a3 and a4) of complex data applied thereto as follows:

applying real part of the first input signal ('a3') to the real input port of the first CORDIC processor (C1) of the pair of CORDIC processors;

applying imaginary part of the first input signal ('a3') to the real input port of the second CORDIC processor (C2) of the pair of CORDIC processors;

applying real part of the second input signal ('a4') to the imaginary input port of the second CORDIC processor (C2) of the pair of CORDIC processors;

applying imaginary part of the second input signal ('a4') to the imaginary input port of the first CORDIC processor (C1) of the pair of CORDIC processors; and

two CORDIC processors (C1 and C2) of the pair of CORDIC processors, rotating respective input signals applied thereto by 45 degrees in the anticlockwise direction;

wherein data from the real output port of first CORDIC processor (C1), and data from the imaginary output port of the second CORDIC processor (C2) in the second pair of real number CORDIC processors, constitute respectively real part and imaginary part of the first output signal; and

data from the imaginary output port of first CORDIC processor (C1), and data from the real output port of the second CORDIC processor (C2) in the second pair of CORDIC processors, constitute respectively real part and imaginary part of the second output signal.

In a seventeenth aspect of the present invention, there is provided an apparatus for performing an IFFT comprising multiple stages for processing IFFT of complex data samples with at least one stage implemented using at least one 2-point IFFT, wherein in the stage implementing 2-point IFFT, at least one of the 2-point IFFT processes data as set forth in the eleventh or twelfth aspect.

In an eighteenth aspect of the present invention, there is provided an apparatus for performing an IFFT comprising multiple stages for processing IFFT of complex data samples with at least one stage implemented using 4-point IFFT, wherein in the stage, at least one of the 4-point IFFT processes data as set forth in the thirteenth or fourteenth aspect.

In a nineteenth aspect of the present invention, there is provided an apparatus for performing an IFFT comprising multiple stages for processing IFFT of complex data samples with at least one stage implemented using 8-point IFFT, wherein in the stage, at least one of the 8-point IFFT processes data as set forth in the fifteenth or sixteenth aspect.

In a twentieth aspect of the present invention, there is provided a processor for processing four samples of complex input signals (a1, a2, a3 and a4), the processor comprising two pairs of CORDIC processors with at least two CORDIC processors (C1 and C2) for rotating the second signal (a4) in the clockwise direction by 90 degrees and evaluating a 2-point IFFT of the first input signal (a3) and the rotated second input signal;

each the CORDIC processors comprising at least first and second input ports ('p1' and 'p2') that respectively represent real input port and imaginary input port; and

first and second output ports ('P1' and 'P2') that respectively represent real output port and imaginary output port for outputting rotated data;

where in the processor,

first and second input signals into the first pair of CORDIC processors are processed as defined in the twelfth aspect or thirteenth aspect; and

third and fourth input signals ('a3' and 'a4') into the second pair of CORDIC are processed as follows:

applying real part of the first input signal ('a3') to the real input port of the first CORDIC processor (C1) of the second pair of CORDIC processors;

applying imaginary part of the first input signal ('a3') to the real input port of the second CORDIC processor (C2) of the second pair of CORDIC processors;

applying real part of second input signal ('a4') to the imaginary input port of the second CORDIC processor (C2) of the second pair of CORDIC processors;

applying imaginary part of second input signal ('a4') to the imaginary input port of the first CORDIC processor (C1) of the second pair of CORDIC processors; and

two CORDIC processors (C1 and C2), of the second pair of CORDIC processors, rotating respective input signals applied thereto by 45 degrees in the anticlockwise direction;

wherein data from the real output port of first CORDIC processor (C1), and data from the imaginary output port of the second CORDIC processor (C2) in the second pair of CORDIC processors, constitute respectively real part and imaginary part of

the first output signal; and

data from the imaginary output port of first CORDIC processor (C1), and data from the real output port of the second CORDIC processor (C2) in the second pair of CORDIC processors, constitute respectively real part and imaginary part of the second output signal.

In a twenty-first aspect of the present invention, there is provided an apparatus for performing an IFFT comprising multiple stages for processing IFFT of complex data samples with at least one stage implemented using two CORDIC processors as set forth in the thirteen aspect.

In further aspects of the present invention, there are provided methods for performing FFT and IFFT, respectively, which will become apparent from the entire disclosure including claims and drawings.

Meritorious effect of the present invention is that FFT or IFFT result is obtained using only CORDIC processors, thus achieving reduction in operations or hardware resources.

Still other features and advantages of the present invention will become readily apparent to those skilled in this art from the following detailed description in conjunction with the accompanying drawings wherein examples of the invention are shown and described, simply by way of illustration of the mode contemplated of carrying out this invention. As will be realized, the invention is capable of other and different examples, and its several details are capable of

modifications in various obvious respects, all without departing from the invention. Accordingly, the drawing and description are to be regarded as illustrative in nature, and not as restrictive.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig.1 is a diagram illustrating an example of 8-point FFT with parallel processing.

Fig.2 is a diagram illustrating an example of 2-point FFT with an additional processor for sign reversal.

Fig.3 is a diagram illustrating the configuration of related art for implementing an 8-point FFT using pairs of CORDIC processors (labeled I,II and III) that have been illustrated in Figs.1, 4 and 5, respectively.

Fig.4 is a diagram illustrating the configuration of related art for using a pair of CORDIC processors (II) in an 8-point FFT described in Fig.3.

Fig.5 is a diagram illustrating the configuration of related art for using a pair of CORDIC processors (III) in an 8-point FFT described in Fig.3.

Fig.6 is a diagram illustrating an example of the 2-point FFT using a pair of CORDIC processors according to the present invention.

Fig.7 is a diagram illustrating an example of two CORDIC processors, C1 and C2, which constitute a pair of CORDIC processors.

Fig.8 is a diagram illustrating another example for implementing a 2-point FFT using a pair of CORDIC processors according to the present invention.

Fig.9 is a diagram illustrating the configuration of an example of the present invention, using the second pair of CORDIC processors in the second stage of a 4-point FFT illustrated in Fig.12.

Fig.10 is a diagram illustrating the configuration of a system of an example for computing 2-point FFT of data that is pre-multiplied with a twiddle factor.

Fig.11 is a diagram illustrating the configuration of an example according to the present invention, using a pair of CORDIC processors (IIIp) in an 8-point IFFT in Fig.14.

Fig.12 is a diagram illustrating the configuration of an example according to the present invention for implementing a 4-point FFT.

Fig.13 is a diagram illustrating the configuration of an example according to the present invention, for implementing an 8-point FFT, using Ip and IIp that has been described in Figs.6 and 9, respectively.

Fig.14 is a diagram illustrating the configuration of an example according to the present invention for implementing an 8-point IFFT, using Ip and IIIp that has been described in Figs.6 and 11, respectively.

EXPLANATION OF NUMERALS

C1, C2: CORDIC processor

Ip: 2-point FFT

Ip1: 2-point FFT

IIp:2-point processor (or method) for rotating one input by 90 degrees in clockwise direction then perform a 2-point FFT

IIIp:2-point processor (or method) for rotating one input by 90 degrees in anticlockwise direction then perform a 2-point FFT

p1: input port(Real data)

p2: input port(Imaginary data)

P1: output port(Real data)

P2: output port(Imaginary data)

s1, s2: input signal

S1, S2: output signal

π : An equivalent of 180^0 in radians

W_N^k: Twiddle factor

PREFERRED MODES OF THE INVENTION

<A 2-point FFT>

Fig.6 shows the configuration of an example for implementing a 2-point FFT or IFFT using a pair of CORDIC processors according to the present invention. Fig. 7 is a diagram illustrating these two inputs and output ports .of CORDIC processors (C1 and C2). With reference to Fig.7, each of the CORDIC processors (C1 and C2) has at least two inputs (p1 and p2). Although the relative position of these inputs can always be changed, we assume that the top input

(p1) represents a real number or the x-coordinate, while the bottom input port (p2) represents an imaginary number or the y-coordinate on the x-y plane. Similarly, there are at least two output ports with the top port (P1) and bottom port (P2) representing respectively the real part or x-coordinate and the imaginary part or y-coordinate.

Assume that we are given a vector (u1,u2) on the x-y plane with x-coordinate data (real data) u1 and a y-coordinate data (imaginary data) u2.

The CORDIC processor (C1) rotates (u1, u2) by an angle θ in the clockwise direction to generate an output (U1,U2), where U1 is the x-coordinate data and U2 is the resulting y-coordinate data.

$$\begin{aligned} U_1 &= u_1\cos(\theta) - u_2\sin(\theta) \\ U_2 &= u_2\cos(\theta) + u_1\sin(\theta) \end{aligned} \qquad (5)$$

Alternatively,

$$U_1 + iU_2 = (u_1 + iu_2)e^{i\theta} \qquad (6)$$

Now, consider a case where we need to calculate FFT of a vector with two complex data samples (input signals) s1 and s2. In the present invention, as shown in Fig.6, real part of second data sample s2 and real part of first data sample s1 are respectively applied to real input port (p1) and imaginary input port (p2) of the first CORDIC processor (C1). Imaginary part of second data sample (s2) and imaginary part of the first data sample (s1) are respectively applied to real input port (p1) and imaginary input port (p2) of the second CORDIC processor (C2).

The respective inputs to each of the two CORDIC processors

(C1) and (C2) are then rotated 45 degrees in the clockwise direction. Resulting output signals from CORDIC processors (C1 and C2) are then routed as follows:

As in the conventional method, output data from real port (p1) of first CORDIC processor (C1) and output data from real port (p1) of second CORDIC processor respectively constitute real and imaginary part of the first output data (S1) of a 2-point FFT data. The output data from imaginary port (p2) of first CORDIC processor (C1) and output data from imaginary port (p2) of second CORDIC processor (C2) respectively constitute real and imaginary part of the second output data (S2) of a 2-point FFT data.

<A 2-point FFT>

Fig.8 shows an alternative example of the present invention which implements a 2-point FFT or IFFT. With reference to Fig.8, real part of the first input signal s1 and real part of second input signal s2 are respectively applied to real input port (p1) and imaginary input port (p2) of the first CORDIC processor (C1). Further, imaginary part of the first input signal s1 and imaginary part of second input signal s2 are respectively applied to imaginary input port (p2) of the first CORDIC processor and imaginary input port (p2) of the second CORDIC processor (C2). The respective inputs to each of the two CORDIC processors (C1 and C2) are then rotated 45 degrees in theanticlockwise direction. Resulting output data (signal) from each of the two CORDIC processor (C1 and C2) are

the routed as follows:

Output data from imaginary port (p2) of the second CORDIC processor (C2) and output data from imaginary port (p2) of the first CORDIC processor (C1) respectively constitute real and imaginary part of the first output data (S1) of a 2-point FFT data.

The output data from real port (p1) of first CORDIC processor (C1) and output data from real port (p1) of second CORDIC processor (C2) respectively constitute imaginary and real part of the second output data (S2) of a 2-point FFT data.

<A 2-point FFT with Twiddle factor at one of its input>

In an N-point FFT or IFFT that can be factored, FFT or IFFT implementation can be done in stages. The results of a previous stage are multiplied by twiddle factors before being applied to the next stage. Typical twiddle factors are expressed as $Tw_{n,k} = e^{2i\pi nk/N}$. As an example, for a 4-point FFT, n={0,1} and k={0,1}.

Fig.10 illustrates a system where two complex data samples are first multiplied with a twiddle factor before computing a 2-point FFT. In this case, the twiddle factor corresponds to $e^{2i\pi/4}$.

Another aspect of the present invention is described for implementing the system described in Fig.10 using a pair of CORDIC processors.

Fig.9 shows the configuration of another example for performing the 2-point FFT using two CORDIC processors. In Fig.9, for two input complex data samples a_3 and a_4, the aim is to

evaluate 2-point FFT of samples a_3 and $a_4 e^{i\pi/2}$.

With reference to Fig.9, real part of first data a_3 and imaginary part of second data a_4 are respectively applied to real input port (p1) and imaginary input port (p2) of the first CORDIC processor (C1). Further, imaginary part of first data a_3 and real part of second data a_4 are respectively applied to real input port (p1) and imaginary input port (p2) of the second CORDIC processor (C2).

The respective inputs to each of the two CORDIC processors (C1) and (C2) are then rotated by 45 degrees in the anticlockwise direction. Resulting output data (signal) from each CORDIC processor are then routed as follows:

Output data from imaginary port (p2) of the first CORDIC processor (C1) and output data from real port (p1) of second CORDIC (C2) processor respectively constitute real and imaginary part of the first output data (A_3).

The output data from real port (p1) of first CORDIC processor (C1) and output data from imaginary port (p2) of second CORDIC processor (C2) respectively constitute real and imaginary part of the second output data (A_4).

In IFFT, twiddle factors takes on complex conjugate of equivalent twiddle factors in an FFT. Thus, rather than use $e^{2i\pi/4}$, a 4-point IFFT uses $e^{-2i\pi/4}$ as its twiddle factor.

Fig.11 illustrates an example or the present invention for evaluating 2-point IFFT of samples a_3 and $a_4 e^{-i\pi/2}$ given two inputs

a_3 and a_4 samples of data. In Fig.11, real part of first data a_8 and imaginary part of second data a_9 are respectively applied to real input port (p1) and imaginary input port (p2) of the first CORDIC processor (C1). Further, imaginary part of first data a_8 and real part of second data a_9 are respectively applied to real input port (p1) of the first CORDIC processor (C1) and imaginary input port (p2) of the second CORDIC processor (C2). The respective inputs to each of the two CORDIC processors (C1) and (C2) are then rotated 45 degrees in the anticlockwise direction. Resulting output data (signal) from each CORDIC processor are the routed as follows:

Output data from real port (p1) of the first CORDIC processor (C1) and output data from imaginary port (p2) of second CORDIC (C2) processor respectively constitute real and imaginary part of the first output data (A_8).

The output data from imaginary port (p2) of first CORDIC processor (C1) and output data from imaginary port (p2) of second CORDIC processor (C2) respectively constitute real and imaginary part of the second output data (A_9).

Performance of the proposed ideas can be explained as follows:

In a 2-point FFT proposed in Fig.6, output will given by

$$S_1 = 2^{-0.5}(s_1 + s_2)$$
$$S_2 = 2^{-0.5}(s_1 - s_2) \qquad (7)$$

This is equivalent to scaled FFT of a vector $[s_1 \quad s_2]$. It clear from Fig.6 that FFT result is obtained using only two CORDIC

processors which then results is a reduction in complexity. Output from an alternative CORDIC based 2-point FFT that has been illustrated in Fig.8, is also given by (7).

<A 4-point FFT>

Fig.12 shows one example of FFT where the present invention can be applied. With reference to Fig.12, 4-point FFT of four samples of data $[x_1 \quad x_2 \quad x_3 \quad x_4]$ is implemented using two stages of processing.

In the first stage, there are two pairs of CORDIC processors. First stage FFT-1 includes two CORDIC processors configured as shown in Fig. 6 or Fig.8. First stage FFT-2 includes two CORDIC processors configured as shown in Fig. 6 or Fig.8. Each pair of the CORDIC processors has input and output ports as described in Fig.7.

The first pair FFT-1 computes 2-point FFT of data samples $[x_1 \quad x_3]$ while the second pair of CORDIC processors FFT-2 computes 2-point FFT of $[x_2 \quad x_4]$.

Computation of 2-point FFT is based on the design proposed in Fig.6 or Fig.8.

Outputs from these two pairs of CORDIC processors are $[a_1 \quad a_3]$ and $[a_2 \quad a_4]$, respectively. The output data from the first stage is then processed in the second stage as follows:

Evaluate 2-point FFT of two samples of data, $[a_1 \quad a_2]$, using the first pair of CORDIC processors (FFT-3) in second stage of a 4-point FFT. Once again, the 2-point FFT can be implemented using

the design proposed in Fig.6 or Fig.8.

Next, 2-point FFT of two samples of data $\begin{bmatrix} a_3 & a_4 e^{-i\pi/2} \end{bmatrix}$ is evaluated using the second pair of CCORDIC processors (FFT-4) in the second stage of a 4-point FFT.

This operation is implemented using the design presented in Fig.9.

The first stage of 4-point FFT implements 2-point FFT of $\begin{bmatrix} x_1 & x_3 \end{bmatrix}$ and $\begin{bmatrix} x_2 & x_4 \end{bmatrix}$ then generates $\begin{bmatrix} a_1 & a_3 \end{bmatrix}$ and $\begin{bmatrix} a_2 & a_4 \end{bmatrix}$ as output data. From (7) $\begin{bmatrix} a_1 & a_3 \end{bmatrix}$ and $\begin{bmatrix} a_2 & a_4 \end{bmatrix}$ are given by

$$\begin{bmatrix} a_1 \\ a_3 \end{bmatrix} = 2^{0.5} \begin{bmatrix} x_1 + x_3 \\ x_1 - x_3 \end{bmatrix}$$

$$\begin{bmatrix} a_2 \\ a_4 \end{bmatrix} = 2^{0.5} \begin{bmatrix} x_2 + x_4 \\ x_2 - x_4 \end{bmatrix}, \quad (8)$$

respectively. The second stage implements two 2-point FFT operations on $\begin{bmatrix} a_1 & a_2 \end{bmatrix}$ and $\begin{bmatrix} a_3 & a_4 e^{-i\pi/2} \end{bmatrix}$, respectively. Using (7) or (8), output data will therefore be given by

$$\begin{bmatrix} X_1 \\ X_3 \end{bmatrix} = 2 \begin{bmatrix} x_1 + x_3 + x_2 + x_4 \\ x_1 + x_3 - x_2 - x_4 \end{bmatrix}$$

$$\begin{bmatrix} X_2 \\ X_4 \end{bmatrix} = 2 \begin{bmatrix} x_1 - x_3 + x_2 - x_4 \\ x_2 - x_4 - (x_2 - x_4) e^{-i\pi/2} \end{bmatrix}. \quad (9)$$

From (1), it can be said that (9) represents scaled FFT of $\begin{bmatrix} x_1 & x_2 & x_3 & x_4 \end{bmatrix}$. Thus, the proposed method enables the implementation of a 4-point FFT using purely CORDIC based

processors. The 4-point FFT can also be used to implement a scaled 4-point IFFT. As an example, if one is interested in evaluating the IFFT of $[x_1 \quad x_2 \quad x_3 \quad x_4]$, then the scaled IFFT results $F[x_1 \quad x_2 \quad x_3 \quad x_4]$ will be given by

$$F[x_1 \quad x_2 \quad x_3 \quad x_4] = [X_1 \quad X_4 \quad X_3 \quad X_2] \tag{10}$$

where X_1, X_2, X_3 and X_4 are the scaled FFT results that have been given in (8).

<A 8-point FFT>

Fig.13 shows another example of FFT where the present invention can be applied. With reference to Fig.13, a system for evaluating an 8-point FFT of eight samples of data $[s_1 \quad s_2 \quad \cdots \quad s_8]$ is implemented using three stages of processing.

First and second stage can be considered as performing two 4-point FFT operations. These are the FFT of $[s_1 \quad s_5 \quad s_3 \quad s_7]$ and $[s_2 \quad s_6 \quad s_4 \quad s_8]$, respectively. These two 4-point FFT are implemented as explained with reference to Fig.12.

The output of the two 4-point FFT are then multiplied by two twiddle factors w_8^1, w_8^2 and w_8^3, where

$$w_8^1 = e^{i2\pi/8}, \tag{11}$$

$$w_8^2 = e^{i2\pi 2/8} \tag{12}$$

and

$$w_8^3 = e^{i2\pi 3/8} \tag{13}$$

respectively.

Third Stage of implementing an 8-point FFT involves four

pairs of CORDIC for performing 2-point FFT operations. Note that in this figure, it is possible to combine the twiddle factor multiplication with w_8^2 and the 2-point FFT (3P-S3). When these two operations are combined, the pair of CORDIC processors (3P-S3) will be implemented using IIp that has been illustrated in Fig.9.

< 8-point IFFT>

Fig.14 shows the configuration of an IFFT where the present invention can also be applied. The general structure of implementation is similar to an 8-point FFT explained above. In this figure, an 8-point IFFT of eight samples of data $[S_1 \quad S_2 \quad \cdots \quad S_8]$ is implemented using three stages of processing. First and second stage can be considered as performing two 4-point IFFT operations. These are the IFFT of $[S_1 \quad S_5 \quad S_3 \quad S_7]$ and $[S_2 \quad S_6 \quad S_4 \quad S_8]$, respectively. The output of the two 4-point IFFT are multiplied by two twiddle factors w_8^{-1} and w_8^{-3}, where

$$w_8^{-1} = e^{-i2\pi/8} \tag{14}$$

and

$$w_8^{-3} = e^{-i2\pi 3/8}, \tag{15}$$

respectively.

<4-point IFFT>

As in the case of FFT, a 4-point IFFT consist of two stages. In the first stage, there are two pairs of CORDIC processors. The first pair computes 2-point IFFT of data samples $[S_1 \quad S_5]$ while the

second pair of CORDIC processors computes 2-point IFFT of $[S_3 \quad S_7]$. The computation of 2-point IFFT is based on design proposed in Fig.6 or Fig.8. The outputs from these two pairs of CORDIC processors are $[a_1 \quad a_3]$ and $[a_2 \quad a_4]$, respectively. The output data from the first stage, are then processed in the second stage as follows:

Evaluate 2-point IFFT of two samples of data, $[a_1 \quad a_2]$, using the first pair of CORDIC processors in second stage of a 4-point FFT. Once again, the 2-point IFFT can be implemented using the design proposed in Fig.6 or Fig.8. Next, evaluate 2-point IFFT of two samples of data $[a_3 \quad a_4 e^{-i\pi/2}]$ using the second pair of CCORDIC processors in the second stage of a 4-point IFFT. This operation is implemented using the design presented in Fig.11.

Third Stage of implementing an 8-point IFFT involves three pairs of CORDIC for performing 2-point IFFT operations and one pair of CORDIC for evaluating 2-point IFFT of $[b_5 \quad b_6 e^{-i\pi/2}]$. The later one-pair of CORDIC is implemented as shown in Fig.11.

INDUSTRIAL APPLICABILITY

It is possible to apply this technology to any signal processing system that evaluates FFT or IFFT using a stage with 2-point FFT or IFFT.

It should be noted that other objects, features and aspects of the present invention will become apparent in the entire disclosure and that modifications may be done without departing the gist and

scope of the present invention as disclosed herein and claimed as appended herewith.

Also it should be noted that any combination of the disclosed and/or claimed elements, matters and/or items may fall under the modifications aforementioned.

CLAIMS:

1. An apparatus for performing a 2-point FFT, wherein first and second complex input signals are evaluated to generate 2-point FFT's first and second complex output signals, said apparatus comprising first and second CORDIC processors,

each of the first and second CORDIC processors including:

first and second input ports that respectively represent real input port and imaginary input port; and

first and second output ports that respectively represent real output port and imaginary output port for outputting rotated data;

wherein real part of the first input signal is applied to the imaginary input port of the first CORDIC processor;

imaginary part of the first input signal is applied to the imaginary input port of the second CORDIC processor;

real part of the second input signal is applied to the real input port of the first CORDIC processor;

imaginary part of the second input signal is applied to the real input port of the second CORDIC processor; and

the first and second CORDIC processors rotate the respective input signals applied thereto by 45 degrees in the clockwise direction;

wherein data from the real output port of said first CORDIC processor, and data from the real output port of the second CORDIC processor constitute respectively real part and imaginary part of the 2-point FFT's first output signal; and

data from the imaginary output port of said first CORDIC processor, and data from the imaginary output port of said second CORDIC processor constitute respectively real part and imaginary part of the 2-point FFT's second output signal.

2. An apparatus for performing a 2-point FFT, wherein first and second complex input signals are evaluated to generate 2-point FFT's first and second complex output signals, said apparatus comprising first and second CORDIC processors, each of said first and second CORDIC processors including:

first and second input ports that respectively represent real input port and imaginary input port; and

first and second output ports that respectively represent real output port and imaginary output port for outputting rotated data;

wherein real part of the first input signal is applied to the real input port of the first CORDIC processor;

imaginary part of the first input signal is applied to the real input port of the second CORDIC processor;

real part of the second input signal is applied to the imaginary input port of the first CORDIC processor;

imaginary part of the second input signal is applied to the imaginary input port of the second CORDIC processor; and

the first and second CORDIC processors rotate respective input signals applied thereto by 45 degrees in the anticlockwise direction;

wherein data from the imaginary output port of the second CORDIC

processor, and data from the imaginary output port of the first CORDIC processor, constitute respectively real part and imaginary part of the 2-point FFT's first output signal; and

data from the real output port of the second CORDIC processors, and data from the real output port of the first CORDIC processors, constitute respectively real part and imaginary part of the 2-point FFT's second output signal.

3. An apparatus for performing a 4-point FFT, comprising first and second stages that process FFT of four complex data samples;

wherein the first stage includes two 2-point FFT units that process four complex input signals; each of said two 2-point FFT units processing data as defined in claim 1 or claim 2; and

the second stage processes the output of the first stage using two 2-point FFT.

4. An apparatus for performing a 4-point FFT, comprising first and second stages that process FFT of four complex data samples;

wherein the first stage includes two 2-point FFT units that process four complex input signals; and

the second stage processes the output of the first stage using first and second pair of CORDIC processors; each CORDIC processor including:

first and second input ports that respectively represent real input port and imaginary input port; and

first and second output ports that respectively represent real output port and imaginary output port for outputting rotated data;

wherein in the second stage of the FFT,

first and second input signals into a first pair of CORDIC processors are processed as defined in claim 1 or claim 2; and

the second pair of CORDIC processors process third and fourth input signals applied thereto as follows:

applying real part of the third input signal to the real input port of a first CORDIC processor of the second pair of CORDIC processors;

applying imaginary part of the third input signal to the real input port of a second CORDIC processor of the second pair of CORDIC processors;

applying real part of the fourth input signal to the imaginary input port of the second CORDIC processor of the second pair of CORDIC processors;

applying imaginary part of the fourth input signal to the imaginary input port of the first CORDIC processor of the second pair of CORDIC processors; and

the first and second CORDIC processors of the second pair of CORDIC processors, rotating respective input signals applied thereto by 45 degrees in the anticlockwise direction;

wherein data from the imaginary output port of the first CORDIC processor, and data from the real output port of the second CORDIC processor in the second pair of CORDIC processors, constitute respectively real part and imaginary part of a third output signal from the second stage of the FFT; and

the data from real output port of first CORDIC processor, and data from the imaginary output port of the second CORDIC processor in the second pair of CORDIC processors, constitute respectively real part and imaginary part of a fourth output signal from the second stage of the FFT.

5. An apparatus for performing an 8-point FFT, comprising three stages for processing FFT of eight complex data samples;

wherein the first stage includes two pairs of 4-point FFT that process eight complex input signals to generate eight complex output signals;

in the second stage, the output signals of the two pairs of said 4-point FFT are multiplied by twiddle factors to generate an output for being processed by the third stage of the 8-point FFT; and

the third stage comprises four pairs of 2-point FFT units, each of which processes data as defined in claim 1 or claim 2.

6. An apparatus for performing an 8-point FFT, comprising three stages for processing FFT of eight complex data samples;

wherein the first stage includes two pairs of 4-point FFT units that process eight complex input signals to generate eight samples of complex output signals;

in the second stage, the outputs of said two pairs of 4-point FFT units are selectively multiplied by twiddle factors or rotated by an equivalent rotational angle to generate an output for being processed by the third stage of the 8-point FFT; and

the third stage includes four pairs of CORDIC processors;

each CORDIC processor in the four pairs of CORDIC processors including:

first and second input ports that respectively represent real input port and imaginary input port; and

first and second output ports that respectively represent real output port and imaginary output port for outputting rotated data;

wherein in the third stage,

one pair of said four pairs of CORDIC processors process first and second complex input signals applied thereto to generate first and second output signals as follows:

applying real part of the first input signal to the real input port of a first CORDIC processor of the pair of CORDIC processors;

applying imaginary part of the first input signal to the real input port of a second CORDIC processor of the pair of CORDIC processors;

applying real part of the second input signal to the imaginary input port of the second CORDIC processor of the pair of CORDIC processors;

applying imaginary part of the first input signal to the imaginary input port of the first CORDIC processor of the pair of CORDIC processors; and

the first and second CORDIC processors of the pair of CORDIC processors, rotating respective input signals applied thereto by 45 degrees in the anticlockwise direction;

wherein data from the imaginary output port of first CORDIC

processor, and data from the real output port of the second CORDIC processor in the second pair of real number CORDIC processors, constitute respectively real part and imaginary part of a first output signal; and

data from real output port of first CORDIC processor, and data from the imaginary output port of the second CORDIC processor in the second pair of CORDIC processors, constitute respectively real part and imaginary part of a second output signal.

7. An apparatus for performing an FFT, comprising a plurality of stages that process FFT of complex data samples, with at least one stage implemented using at least one 2-point FFT unit;

wherein in the stage implementing 2-point FFT, at least one 2-point FFT unit processes data as defined in claim 1 or claim 2.

8. An apparatus for performing an FFT, comprising a plurality of stages for processing FFT of complex data samples with at least one stage implemented using at least one 4-point FFT unit;

wherein in the stage implementing 4-point FFT, at least one 4-point FFT unit processes data as defined in claim 3 or claim 4.

9. An apparatus for performing an FFT, comprising a plurality of stages for processing FFT of complex data samples with at least one stage implemented using at least 8-point FFT unit;

wherein in the stage implementing 8-point FFT, at least one 8-point FFT unit processes data as defined in claim 5 or claim 6.

10. A processor for processing first, second, third and fourth complex input signals, comprising first and second pairs of CORDIC

processors that rotate the fourth input signal applied thereto in the clockwise direction by 90 degrees and evaluate a 2-point FFT of the third input signal and the rotated fourth input signal;

each CORDIC processor of the first and second pairs of CORDIC processors including:

first and second input ports that respectively represent real input port and imaginary input port; and

first and second output ports that respectively represent real output port and imaginary output port for outputting rotated data;

where in the processor,

first and second input signals into the first pair of CORDIC processors are processed as defined in claim 1 or claim 2; and

third and fourth input signals into the second pair of CORDIC processors are processed as follows:

applying real part of the third input signal to the real input port of the first CORDIC processor of a second pair of CORDIC processors;

applying imaginary part of the third input signal to the real input port of the second CORDIC processor of the second pair of CORDIC processors;

applying real part of the fourth input signal to the imaginary input port of the second CORDIC processor of the second pair of CORDIC processors;

applying imaginary part of the fourth input signal to the imaginary input port of the second CORDIC processor of the second

pair of CORDIC processors; and

the first and second CORDIC processors of the second pair of CORDIC processors, rotating respective input signals applied thereto by 45 degrees in the anticlockwise direction;

wherein data from the imaginary output port of the first CORDIC processor, and data from the real output port of the second CORDIC processor in the second pair of CORDIC processors, constitute respectively real part and imaginary part of a first output signal; and

data from the real output port of the first CORDIC processor, and data from the imaginary output port of the second CORDIC processor in the second pair of CORDIC processors, constitute respectively real part and imaginary part of a second output signal.

11. An apparatus for performing a 2-point IFFT, comprising two CORDIC processors;

each CORDIC processor including:

first and second input ports that respectively represent real input port and imaginary input port; and

first and second output ports that respectively represent real output port and imaginary output port for outputting rotated data;

wherein IFFT of two samples of complex input signals is evaluated to generate 2-point IFFT's first and second output signals as follows:

applying real part of the first input signal to the imaginary input port of the first CORDIC processor;

applying imaginary part of the first input signal to the imaginary input port of the second CORDIC processor;

applying real part of second input signal to the real input port of the first CORDIC processor;

applying imaginary part of second input signal to the real input port of the second CORDIC processor; and

the first and second CORDIC processors rotating respective input signals applied thereto by 45 degrees in the clockwise direction; wherein data from the real output port of first CORDIC processor, and data from the real output port of the second CORDIC processor, constitute respectively real part and imaginary part of the 2-point IFFT's first output signal; and

data from the imaginary output port of first CORDIC processor, and the imaginary output port of the second CORDIC processor, constitute respectively real part and imaginary part of the 2-point IFFT's second output signal.

12. An apparatus for performing a 2-point IFFT comprising first and second CORDIC processors;

each CORDIC processor including:

first and second input ports that respectively represent real input port and imaginary input port; and

first and second output ports that respectively represent real output port and imaginary output port for outputting rotated data;

wherein IFFT of two samples of complex input signals are evaluated to generate 2-point IFFT's first and second output signals

as follows:

applying the real part of a first input signal to the real input port of the first CORDIC processor;

applying imaginary part of the first input signal to the real input port of the second CORDIC processor;

applying real part of a second input signal to the imaginary input port of the first CORDIC processor; and

applying imaginary part of the second input signal to the imaginary input port of the second CORDIC processor; and

the first and second CORDIC processors rotating respective input signals applied thereto by 45 degrees in the anticlockwise direction;

wherein data from the imaginary output port of second CORDIC processor, and data from the imaginary output port of the first CORDIC processor, constitute respectively real part and imaginary part of the 2-point IFFT's first output signal; and

data from the real output port of second CORDIC processors, and data from the real output port of the first CORDIC processors, constitute respectively real part and imaginary part of the 2-point IFFT's second output signal.

13. An apparatus for performing a 4-point IFFT, comprising two stages that process IFFT of four complex data samples,

wherein the first stage includes two 2-point IFFT units that process four complex input signals; and

the second stage processes the output of the first stage using

two 2-point IFFT,

wherein in the first stage, the 4-point IFFT unit process data as defined in claim 11 or claim 12.

14. An apparatus for performing a 4-point IFFT, comprising two stages that process IFFT of four complex data samples,

wherein the first stage includes two 2-point IFFT units that process complex input signals; and

the second stage processes the output of the first stage using two pairs of CORDIC processors;

each CORDIC processor including:

first and second input ports that respectively represent real input port and imaginary input port; and

first and second output ports that respectively represent real output port and imaginary output port for outputting rotated data;

wherein in the second stage of the IFFT, first and second input signals into the first pair of CORDIC processors are processed as defined in claim 11 or claim 12; and

third and fourth input signals into the second pair of CORDIC processors is processed as follows:

applying real part of the third input signal to the real input port of the first CORDIC processor of the second pair of CORDIC processors;

applying imaginary part of the third input signal to the real input port of the second CORDIC processor of the second pair of CORDIC processors;

applying real part of the fourth input signal to the imaginary input port of the second CORDIC processor of the second pair of CORDIC processors;

applying imaginary part of the fourth input signal to the imaginary input port of the first CORDIC processor of the second pair of CORDIC processors; and

the first and second CORDIC processors of the second pair of CORDIC processors, rotating respective input signals applied thereto by 45 degrees in the anticlockwise direction;

wherein data from the real output port of first CORDIC processor, and data from the imaginary output port of the second CORDIC processor in the second pair of CORDIC processors, constitute respectively real part and imaginary part of the third output signal from the second stage of the IFFT; and

data from the imaginary output port of first CORDIC processor, and data from the real output port of the second CORDIC processor in the second pair of CORDIC processors, constitute respectively real part and imaginary part of the fourth output signal from the second stage of the IFFT.

15. An apparatus for performing an 8-point IFFT, comprising three stages that process IFFT of eight complex data samples;

wherein the first stage includes two pairs of 4-point IFFT units that process eight complex input signals to generate eight complex output signals;

in the second stage, the outputs of said two pairs of 4-point

IFFT are multiplied by twiddle factors to generate an output for being processed by the third stage of the 8-point IFFT; and

the third stage comprises four pairs of 2-point IFFT units, at least one of which processes data as defined in claim 11 or claim 12.

16. An apparatus for performing an 8-point IFFT, comprising three stages that process IFFT of eight complex data samples;

wherein the first stage includes two pairs of 4-point IFFT that process eight complex input signals to generate eight complex output signals;

in the second stage, the outputs of said pairs of 4-point IFFT are selectively multiplied by twiddle factors or rotated by an equivalent rotational angle to generate an output for being processed by the third stage of the 8-point IFFT; and

the third stage includes four pairs of CORDIC processors;

each CORDIC processor of the four pairs of CORDIC processors including:

first and second input ports that respectively represent real input port and imaginary input port; and

first and second output ports that respectively represent real output port and imaginary output port for outputting rotated data;

wherein in the third stage, one of the pairs of CORDIC processors process first and second input samples of complex data applied thereto as follows:

applying real part of the first input signal to the real input port of the first CORDIC processor of the pair of CORDIC

processors;

applying imaginary part of the first input signal to the real input port of the second CORDIC processor of the pair of CORDIC processors;

applying real part of the second input signal to the imaginary input port of the second CORDIC processor of the pair of CORDIC processors;

applying imaginary part of the second input signal to the imaginary input port of the first CORDIC processor of the pair of CORDIC processors; and

the first and second CORDIC processors of the pair of CORDIC processors, rotating respective input signals applied thereto by 45 degrees in the anticlockwise direction;

wherein data from the real output port of first CORDIC processor, and data from the imaginary output port of the second CORDIC processor in the second pair of real number CORDIC processors, constitute respectively real part and imaginary part of a first output signal; and

data from the imaginary output port of first CORDIC processor, and data from the real output port of the second CORDIC processor in the second pair of CORDIC processors, constitute respectively real part and imaginary part of a second output signal;

17. An apparatus for performing an IFFT, comprising multiple stages that process IFFT of complex data samples with at least one stage implemented using at least one 2-point IFFT unit,

wherein in the stage implementing 2-point IFFT, at least one 2-point IFFT unit processes data as defined in claim 11 or claim 12.

18. An apparatus for performing an IFFT, comprising a plurality of stages that process IFFT of complex data samples with at least one stage implemented using 4-point IFFT unit;

wherein in the stage implementing 4-point IFFT, at least one 4-point IFFT processes data as defined in claim 13 or claim 14.

19. An apparatus for performing an IFFT comprising multiple stages that process IFFT of complex data samples with at least one stage implemented using at least 8-point IFFT units;

wherein in the stage implementing 8-point IFFT, at least one 8-point IFFT processes data as defined in claim 15 or claim 16.

20. A processor for processing four samples of complex input signals, the processor comprising first and second pairs of CORDIC processors for rotating the fourth signal in the clockwise direction by 90 degrees and evaluating a 2-point IFFT of the third input signal and the rotated fourth input signal;

each CORDIC processor including:

first and second input ports that respectively represent real input port and imaginary input port; and

first and second output ports that respectively represent real output port and imaginary output port for outputting rotated data;

wherein in the processor,

first and second input signals into the first pair of CORDIC processors are processed as defined in claim 11 or claim 12; and

third and fourth input signals into the second pair of CORDIC processors are processed as follows:

applying real part of the first input signal to the real input port of the first CORDIC processor of the second pair of CORDIC processors;

applying imaginary part of the first input signal to the real input port of the second CORDIC processor of the second pair of CORDIC processors;

applying real part of the second input signal to the imaginary input port of the second CORDIC processor of the second pair of CORDIC processors;

applying imaginary part of the second input signal ('a4') to the imaginary input port of the second CORDIC processor of the second pair of CORDIC processors; and

the first and second CORDIC processors of the second pair of CORDIC processors, rotating respective input signals applied thereto by 45 degrees in the anticlockwise direction;

wherein data from the real output port of first CORDIC processor, and data from the imaginary output port of the second CORDIC processor in the second pair of real number CORDIC processors, constitute respectively real part and imaginary part of a first output signal; and

data from the imaginary output port of first CORDIC processor, and data from the real output port of the second CORDIC processor in the second pair of CORDIC processors, constitute

respectively real part and imaginary part of a second output signal.

21. An apparatus for performing an IFFT comprising a plurality of stages that process IFFT of complex data samples, with at least one stage processing two complex input data using first and second CORDIC processors as defined in claim 13.

22. A method of performing a 2-point FFT, wherein first and second complex input signals are evaluated to generate 2-point FFT's first and second complex output signals, using first and second CORDIC processors,

each of the first and second CORDIC processors including: first and second input ports that respectively represent real input port and imaginary input port; and first and second output ports that respectively represent real output port and imaginary output port for outputting rotated data, said method comprising:

applying real part of the first input signal to the imaginary input port of the first CORDIC processor;

applying imaginary part of the first input signal to the imaginary input port of the second CORDIC processor;

applying real part of the second input signal to the real input port of the first CORDIC processor;

applying imaginary part of the second input signal to the real input port of the second CORDIC processor; and

rotating by the first and second CORDIC processors the respective input signals applied thereto by 45 degrees in the clockwise direction;

wherein data from the real output port of said first CORDIC processor, and data from the real output port of the second CORDIC processor, constitute respectively real part and imaginary part of the 2-point FFT's first output signal; and

data from the imaginary output port of said first CORDIC processor, and data from the imaginary output port of said second CORDIC processor constitute respectively real part and imaginary part of the 2-point FFT's second output signal.

23. A method of performing a 2-point FFT, using first and second CORDIC processors, each of said first and second CORDIC processors including: first and second input ports that respectively represent real input port and imaginary input port; and first and second output ports that respectively represent real output port and imaginary output port for outputting rotated data, said method comprising:

applying the real part of a first input signal to the real input port of the first CORDIC processor;

applying imaginary part of the first input signal to the real input port of the second CORDIC processor;

applying real part of a second input signal to the imaginary input port of the first CORDIC processor; and

applying imaginary part of the second input signal to the imaginary input port of the second CORDIC processor; and

rotating by first and second CORDIC processors respective input signals applied thereto by 45 degrees in the anticlockwise

direction;

wherein data from the imaginary output port of the second CORDIC processor, and data from the imaginary output port of the first CORDIC processor, constitute respectively real part and imaginary part of the 2-point FFT's first output signal; and

data from the real output port of the second CORDIC processors, and data from the real output port of the first CORDIC processors, constitute respectively real part and imaginary part of the 2-point FFT's second output signal.

24. A method of performing a 4-point FFT, using first and second stages that process FFT of four complex data samples,

wherein the first stage includes two 2-point FFT for processing four complex input signals; and

the second stage processing the output of the first stage using two 2-point FFT;

wherein in the first stage, data is processed as defined in claim 22 or claim 23.

25. A method of performing a 4-point FFT, using first and second stages that process FFT of four complex data samples;

wherein the first stage with two 2-point FFT process four complex input signals; and

the second stage processes the output of the first stage using first and second pair of CORDIC processors;

each of the first and second CORDIC processors including: first and second input ports that respectively represent real input

port and imaginary input port; and first and second output ports that respectively represent real output port and imaginary output port for outputting rotated data;

the second stage comprising:

processing first and second input signals in the first pair of CORDIC processors as defined in claim 22 or claim 23; and

processing third and fourth input signals in the second pair of CORDIC processors as follows:

applying real part of third input signal to the real input port of the first CORDIC processor of the second pair of CORDIC processors;

applying imaginary part of the third input signal to the real input port of the second CORDIC processor of the second pair of CORDIC processors;

applying real part of fourth input signal to the imaginary input port of the second CORDIC processor of the second pair of CORDIC processors;

applying imaginary part of the fourth input signal to the imaginary input port of the first CORDIC processor of the second pair of CORDIC processors; and

the first and second CORDIC processors of the second pair of CORDIC processors, rotating respective input signals applied thereto by 45 degrees in the anticlockwise direction;

wherein data from the imaginary output port of the first CORDIC processor, and data from the real output port of the second

CORDIC processor in the second pair of real number CORDIC processors, constitute respectively real part and imaginary part of the third output signal from the second stage; and

the data from real output port of first CORDIC processor, and data from the imaginary output port of the second CORDIC processor in the second pair of CORDIC processors, constitute respectively real part and imaginary part of the fourth output signal from the second stage.

26. A method of performing an 8-point FFT, using three stages that process FFT of eight complex data samples, said method comprising:

the first stage with two pairs of 4-point FFT processing eight complex input signals to generate eight complex output signals;

the second stage multiplying the output signals of the two pairs of said 4-point FFT by twiddle factors to generate an output for being processed by the third stage of the 8-point FFT; and

the third stage with four pairs of 2-point FFT that process data as defined in claim 22 or claim 23.

27. A method of performing an 8-point FFT, using three stages that process FFT of eight complex data samples, said method comprising:

the first stage with two pairs of 4-point FFT processing eight complex input signals to generate eight samples of complex output signals;

the second stage selectively multiplying the output of said

pairs of 4-point FFT by twiddle factors or rotating the output of said pairs of 4-point FFT by an equivalent rotational angle to generate an output for being processed by the third stage of the 8-point FFT; and

the third stage with four pairs of CORDIC processors; each including: first and second input ports that respectively represent real input port and imaginary input port; and first and second output ports that respectively represent real output port and imaginary output port for outputting rotated data;

wherein processing by one of the pairs of CORDIC processors first and second complex input signals applied thereto to generate first and second output signals is as follows:

applying real part of the first input signal to the real input port of the first CORDIC processor of the pair of CORDIC processors;

applying imaginary part of the first input signal to the real input port of the second CORDIC processor of the pair of CORDIC processors;

applying real part of the second input signal to the imaginary input port of the second CORDIC processor of the pair of CORDIC processors;

applying imaginary part of the first input signal to the imaginary input port of the first CORDIC processor of the pair of CORDIC processors; and

the first and second CORDIC processors of the pair of CORDIC processors, rotating respective input signals applied thereto

by 45 degrees in the anticlockwise direction;

wherein data from the imaginary output port of first CORDIC processor, and data from the real output port of the second CORDIC processor in the second pair of CORDIC processors, constitute respectively real part and imaginary part of a first output signal; and

data from real output port of first CORDIC processor, and data from the imaginary output port of the second CORDIC processor in the second pair of CORDIC processors, constitute respectively real part and imaginary part of a second output signal.

28. A method of performing an FFT, using a plurality of stages that process FFT of complex data samples, with at least one stage implemented using at least one 2-point FFT;

wherein in the stage implementing 2-point FFT, at least one 2-point FFT processes data as defined in claim 22 or claim 23.

29. A method of performing an FFT, using a plurality of stages that process FFT of complex data samples with at least one stage implemented using 4-point FFT;

wherein in the stage implementing 4-point FFT, at least one 4-point FFT processes data as defined in claim 24 or claim 25.

30. A method of performing an FFT, using a plurality of stages that process FFT of complex data samples with at least one stage implemented using 8-point FFT;

wherein in the stage implementing 8-point FFT, at least one 8-point FFT processes data as defined in claim 26 or claim 27.

31. A method of performing a 2-point IFFT, using two CORDIC

processors, each comprising first and second input ports that respectively represent real input port and imaginary input port; and first and second output ports that respectively represent real output port and imaginary output port for outputting rotated data;

said method comprising:

applying real part of the first input signal to the imaginary input port of the first CORDIC processor;

applying imaginary part of the first input signal to the imaginary input port of the second CORDIC processor;

applying real part of second input signal to the real input port of the first CORDIC processor;

applying imaginary part of second input signal to the real input port of the second CORDIC processor; and

the first and second CORDIC processors rotating respective input signals applied thereto by 45 degrees in the clockwise direction;

wherein data from the real output port of first CORDIC processor, and data from the real output port of the second CORDIC processor, constitute respectively real part and imaginary part of a first output signal of the 2-point IFFT; and

data from the imaginary output port of first CORDIC processor, and the imaginary output port of the second CORDIC processor, constitute respectively real part and imaginary part of a second output signal of the 2-point IFFT.

32. A method of performing a 2-point IFFT, using two CORDIC

processors, each including: first and second input ports that respectively represent real input port and imaginary input port; and first and second output ports that respectively represent real output port and imaginary output port for outputting rotated data;

said method comprising:

applying the real part of the first input signal to the real input port of the first CORDIC processor;

applying imaginary part of the first input signal to the real input port of the second CORDIC processor;

applying real part of second input signal to the imaginary input port of the first CORDIC processor; and

applying imaginary part of second input signal to the imaginary input port of the second CORDIC processor; and

the first and second CORDIC processors rotating respective input signals applied thereto by 45 degrees in the anticlockwise direction;

wherein data from the imaginary output port of second CORDIC processor, and data from the imaginary output port of the first CORDIC processor, constitute respectively real part and imaginary part of a first output signal of the 2-point IFFT; and

data from the real output port of second CORDIC processors, and data from the real output port of the first CORDIC processors, constitute respectively real part and imaginary part of a second output signal of the 2-point IFFT.

33. A method of performing a 4-point IFFT, using two stages that

process IFFT of four complex data samples, said method comprising:

the first stage with two 2-point IFFT processing four complex input signals; and

the second stage processing the output of the first stage using two 2-point IFFT;

where in the first stage of the 4-point IFFT, data is processed as defined in claim 31 or claim 32.

34. A method of performing a 4-point IFFT using two stages that process IFFT of four complex data samples, said method comprising:

the first stage with two 2-point IFFT processing complex input signals;

the second stage processing the output of the first stage using two pairs of CORDIC processors;

each of the CORDIC processors including first and second input ports that respectively represent real input port and imaginary input port; and first and second output ports that respectively represent real output port and imaginary output port for outputting rotated data;

wherein in the second stage of the IFFT,

first and second input signals into the first pair of CORDIC processors are processed as defined in claim 31 or claim 32;

third and fourth input signals into the second pair of CORDIC processors is processed as follows:

applying real part of the third input signal to the real input port of the first CORDIC processor of the second pair of CORDIC

processors;

applying imaginary part of the third input signal to the real input port of the second CORDIC processor of the second pair of CORDIC processors;

applying real part of the fourth input signal to the imaginary input port of the second CORDIC processor of the second pair of CORDIC processors;

applying imaginary part of the fourth input signal to the imaginary input port of the first CORDIC processor of the second pair of CORDIC processors;

the first and second CORDIC processors of the second pair of CORDIC processors, rotating respective input signals applied thereto by 45 degrees in the anticlockwise direction;

data from the real output port of first CORDIC processor, and data from the imaginary output port of the second CORDIC processor in the second pair of CORDIC processors, constitute respectively real part and imaginary part of the third output signal from the second stage of the IFFT; and

data from the imaginary output port of first CORDIC processor, and data from the real output port of the second CORDIC processor in the second pair of CORDIC processors, constitute respectively real part and imaginary part of the fourth output signal from the second stage of the IFFT.

35. A method of performing an 8-point IFFT, using three stages that process IFFT of eight complex data samples, said method

comprising:

the first stage with two pairs of 4-point IFFT processing eight complex input signals to generate eight complex output signals;

the second stage multiplying the output of said two pairs of 4-point IFFT by twiddle factors to generate an output for being processed by the third stage of the 8-point IFFT; and

the third stage with four pairs of 2-point IFFT processing the output of the second stage;

wherein the 2-point IFFT in the third stage, data is processed as defined in claim 31 or claim 32.

36. A method of performing an 8-point IFFT, using three stages that process IFFT of eight complex data samples, said method comprising:

the first stage with two pairs of 4-point IFFT processing eight complex input signals to generate eight complex output signals;

the output of said pairs of 4-point IFFT being selectively multiplied by twiddle factors or rotated by an equivalent rotational angle in the second stage to generate an output for being processed by the third stage of the 8-point IFFT; and

the third stage with four pairs of CORDIC processors processing the output of the second stage;

each of the CORDIC processors in the four pairs of CORDIC processors comprising first and second input ports that respectively represent real input port and imaginary input port; and first and second output ports that respectively represent real output port and

imaginary output port for outputting rotated data;

wherein in the third stage,

one of the pairs of CORDIC processors processes first and second input samples of complex data applied thereto as follows:

applying real part of the first input signal to the real input port of the first CORDIC processor of the pair of CORDIC processors;

applying imaginary part of the first input signal to the real input port of the second CORDIC processor of the pair of CORDIC processors;

applying real part of the second input signal to the imaginary input port of the first CORDIC processor of the pair of CORDIC processors;

applying imaginary part of the second input signal to the imaginary input port of the second CORDIC processor of the pair of CORDIC processors; and

the first and second CORDIC processors of the pair of CORDIC processors, rotating respective input signals applied thereto by 45 degrees in the anticlockwise direction;

wherein data from the real output port of first CORDIC processor, and data from the imaginary output port of the second CORDIC processor in the second pair of CORDIC processors, constitute respectively real part and imaginary part of a first output signal; and

data from the imaginary output port of first CORDIC

processor, and data from the real output port of the second CORDIC processor in the second pair of CORDIC processors, constitute respectively real part and imaginary part of a second output signal.

37. A method of performing an IFFT using a plurality of stages that process IFFT of complex data samples with at least one stage implemented using at least one 2-point IFFT;

wherein in the stage implementing 2-point IFFT, at least one 2-point IFFT processes data as defined in claim 31 or claim 32.

38. A method of performing an IFFT using a plurality of stages that process IFFT of complex data samples with at least one stage implemented using 4-point IFFT;

wherein in the stage implementing 2-point IFFT, at least one 4-point IFFT processes data as defined in claim 33 or claim 34.

39. A method of performing an IFFT using a plurality of stages that process IFFT of complex data samples with at least one stage implemented using 8-point IFFT;

wherein in the stage implementing 8-point IFFT, at least one 8-point IFFT processes data as defined in claim 35 or claim 36.

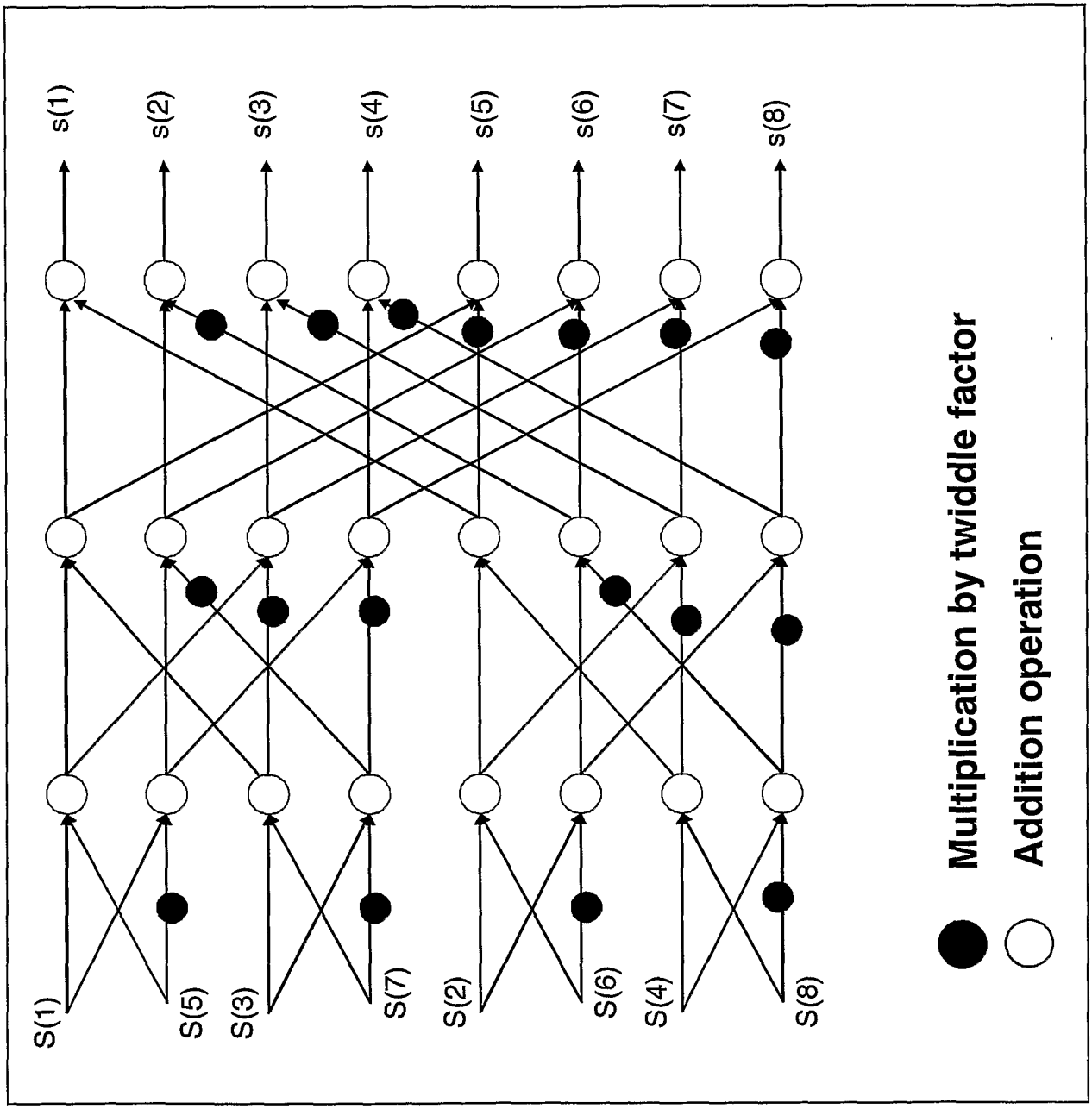

s(1)
s(2)
s(3)
s(4)
s(5)
s(6)
s(7)
s(8)
S(1)
S(5)
S(3)
S(7)
S(2)
S(6)
S(4)
S(8)
Multiplication by twiddle factor
Addition operation

FIG. 1

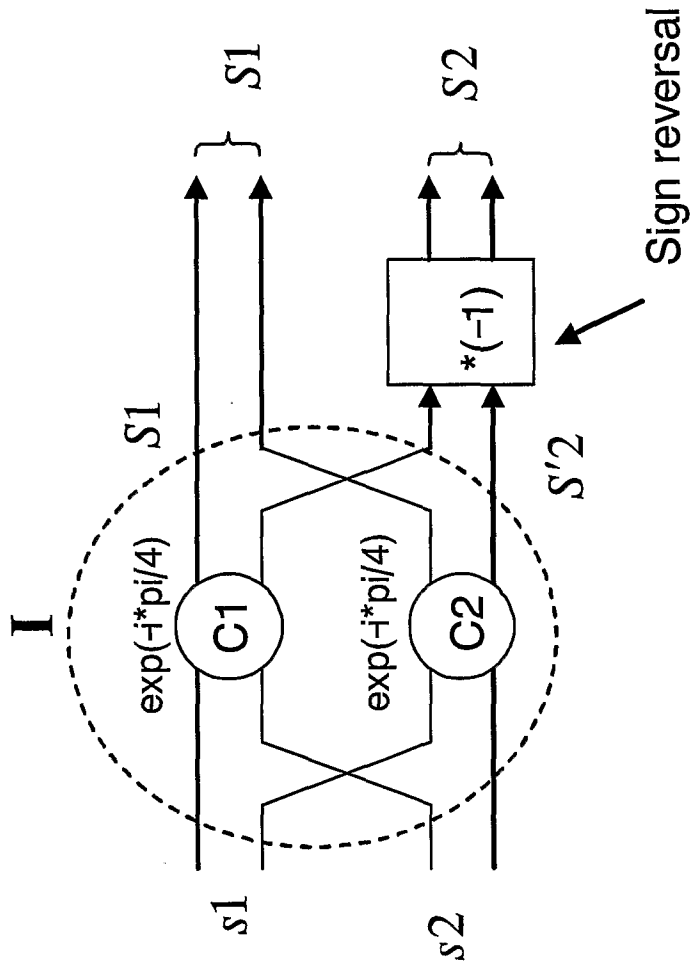


FIG. 2

FIG. 3 RELATED ART

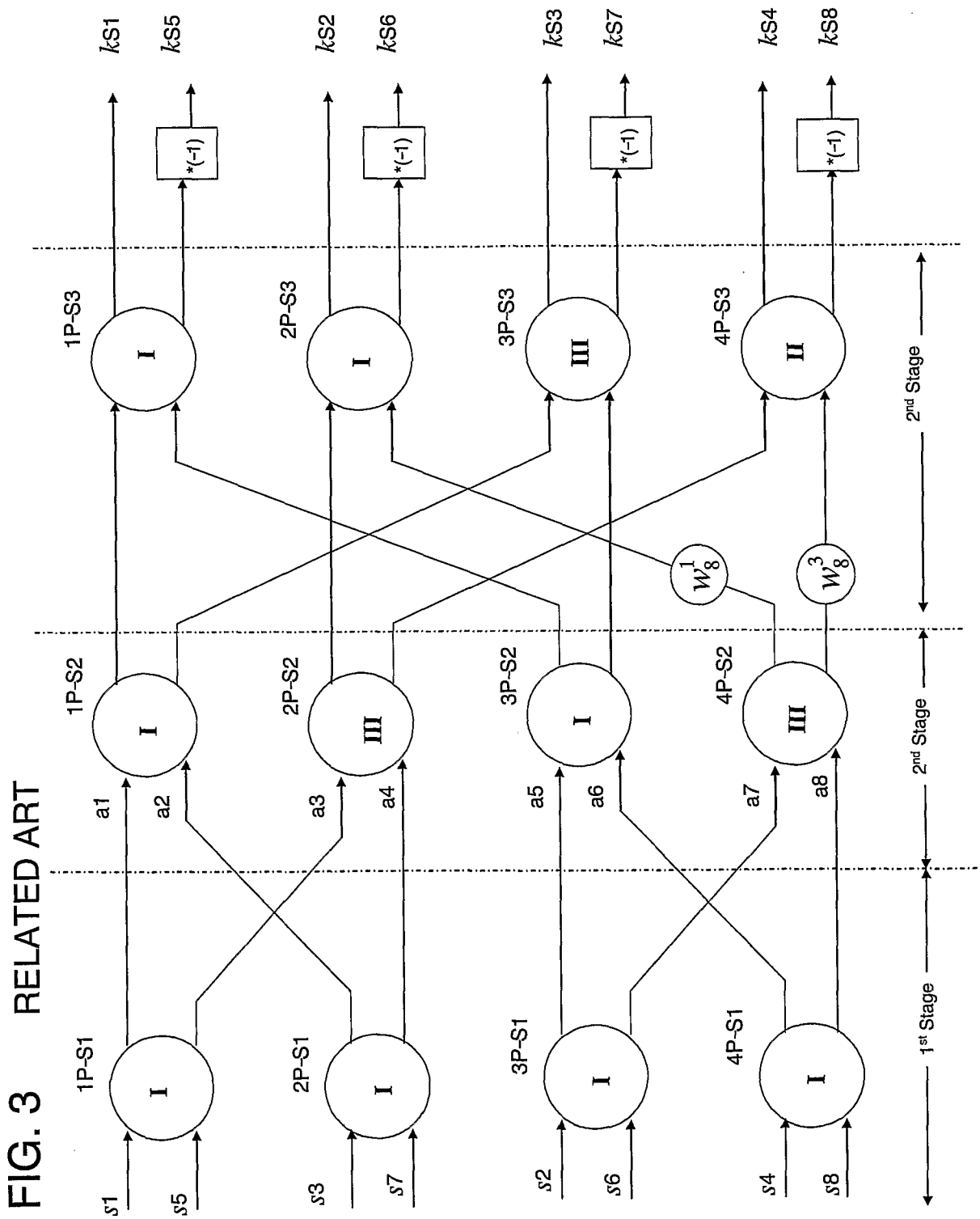


FIG. 4 RELATED ART

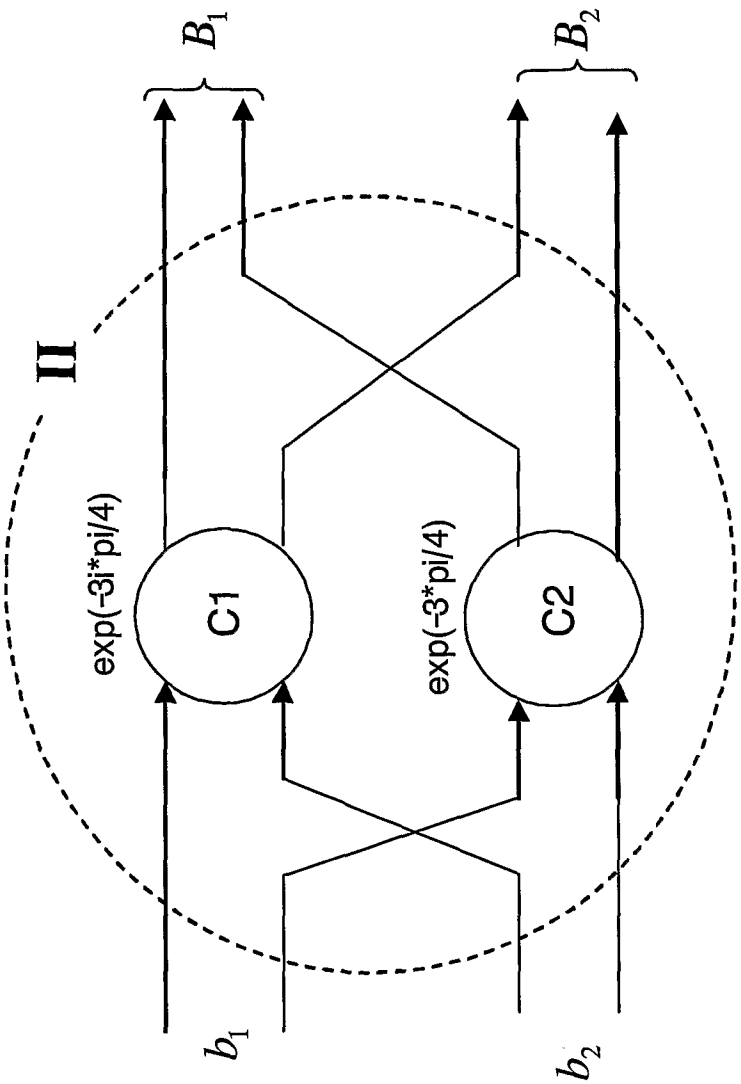
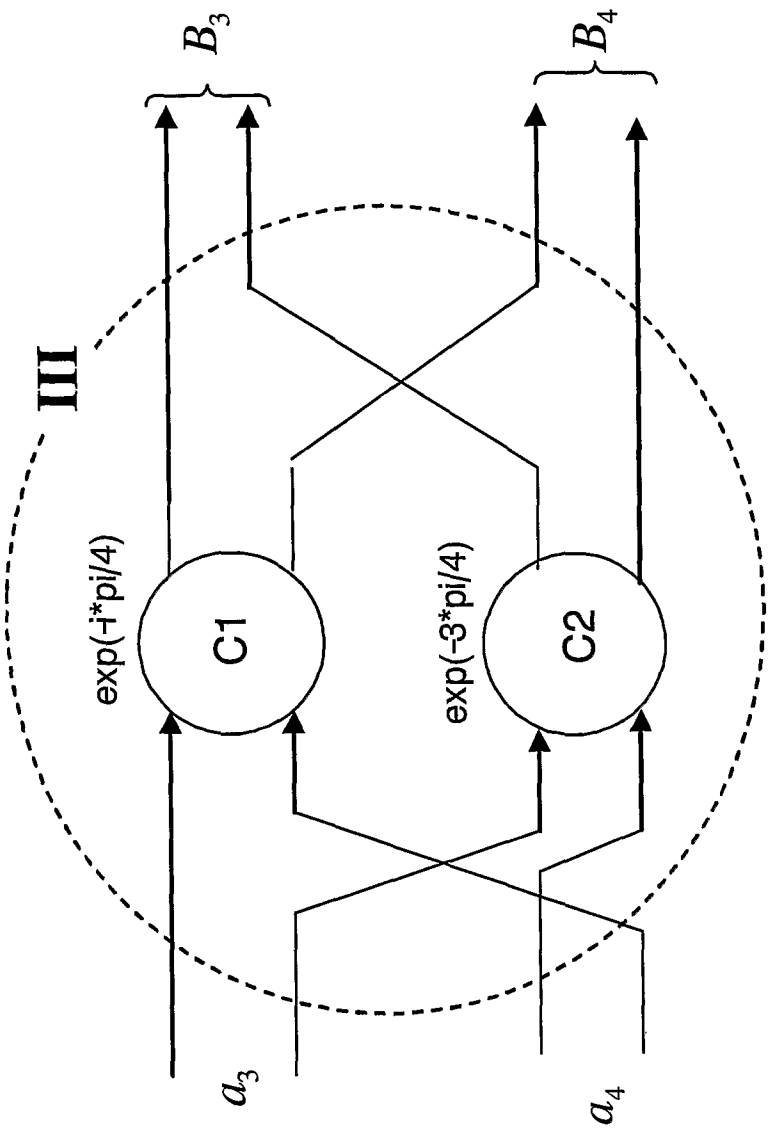


FIG. 5 RELATED ART



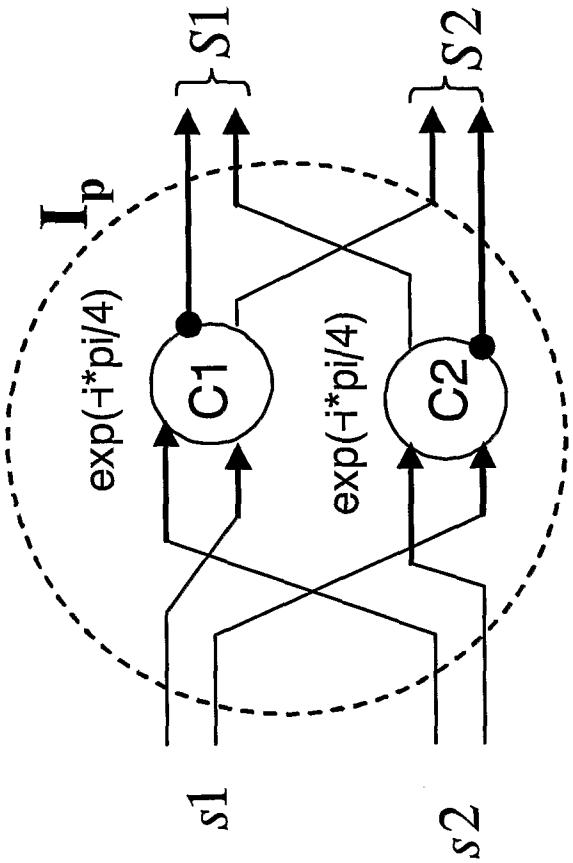
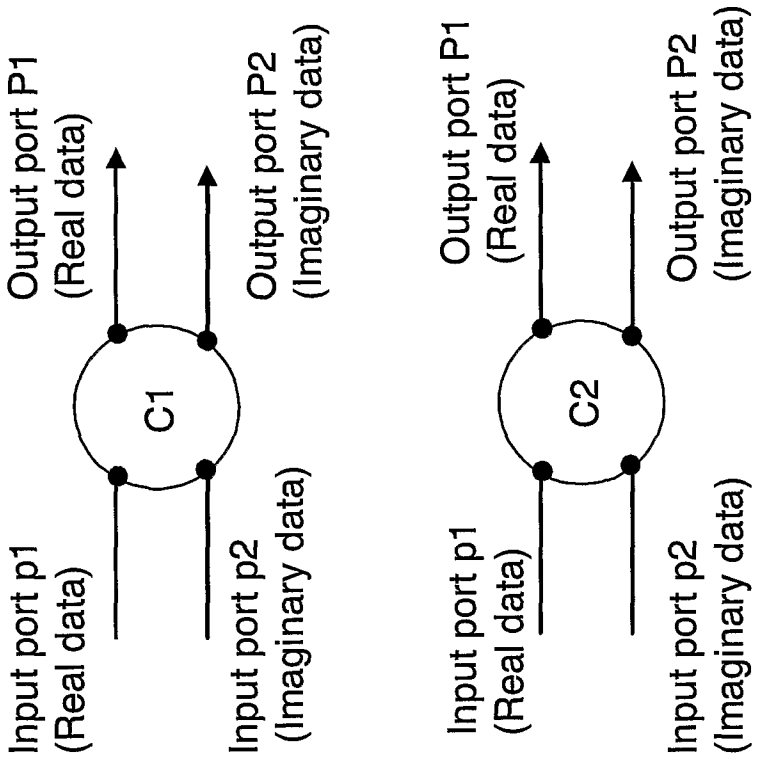


FIG. 6

FIG. 7


Output port P1
(Real data)
Output port P2
(Imaginary data)
C1
Input port p1
(Real data)
Input port p2
(Imaginary data)
Output port P1
(Real data)
Output port P2
(Imaginary data)
C2
Input port p1
(Real data)
Input port p2
(Imaginary data)

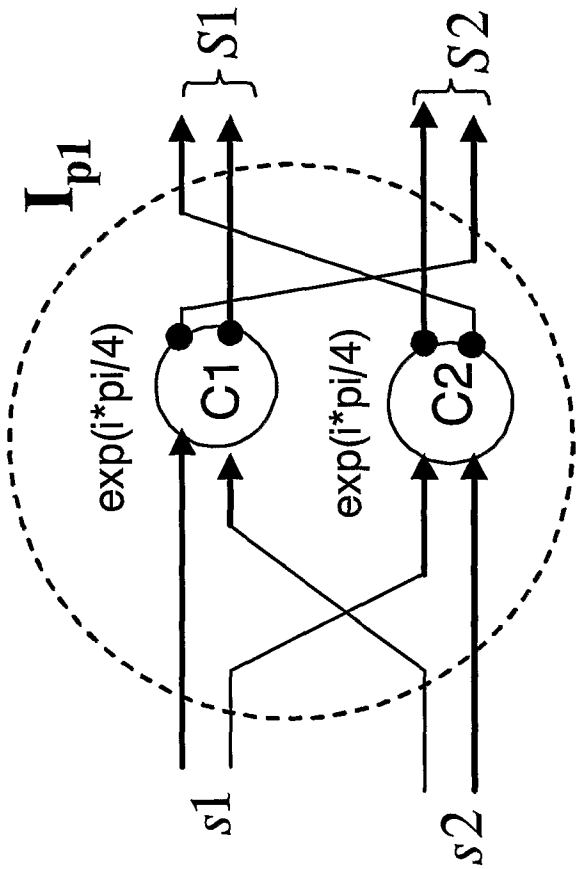
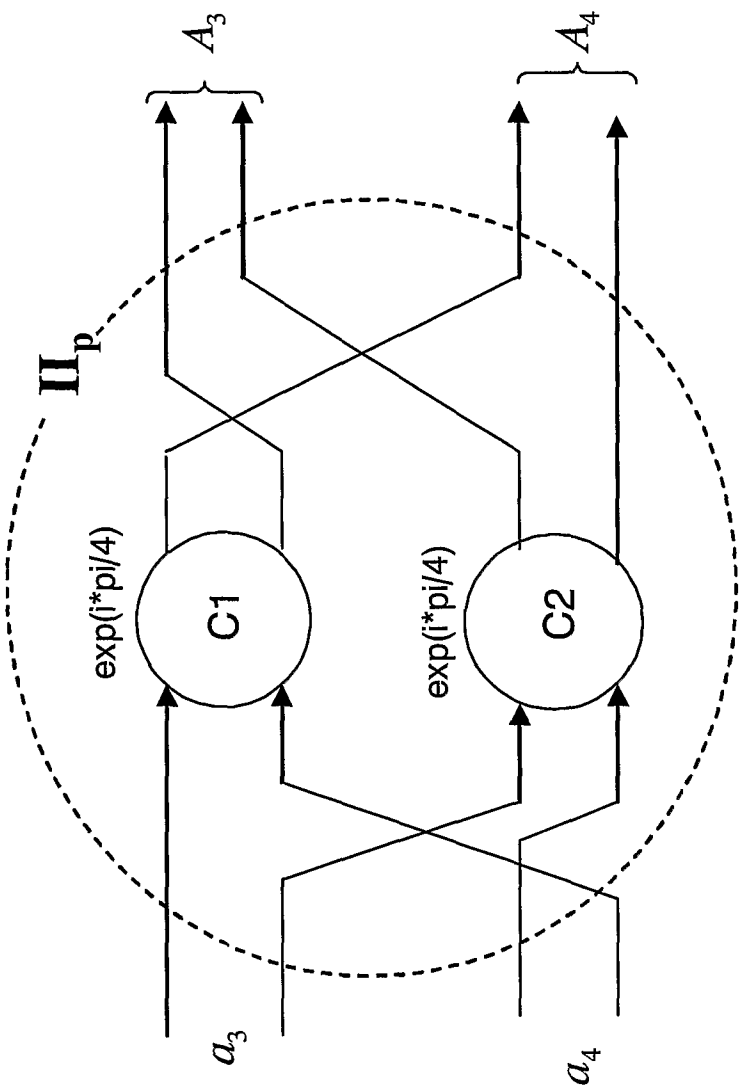


FIG. 8

FIG. 9



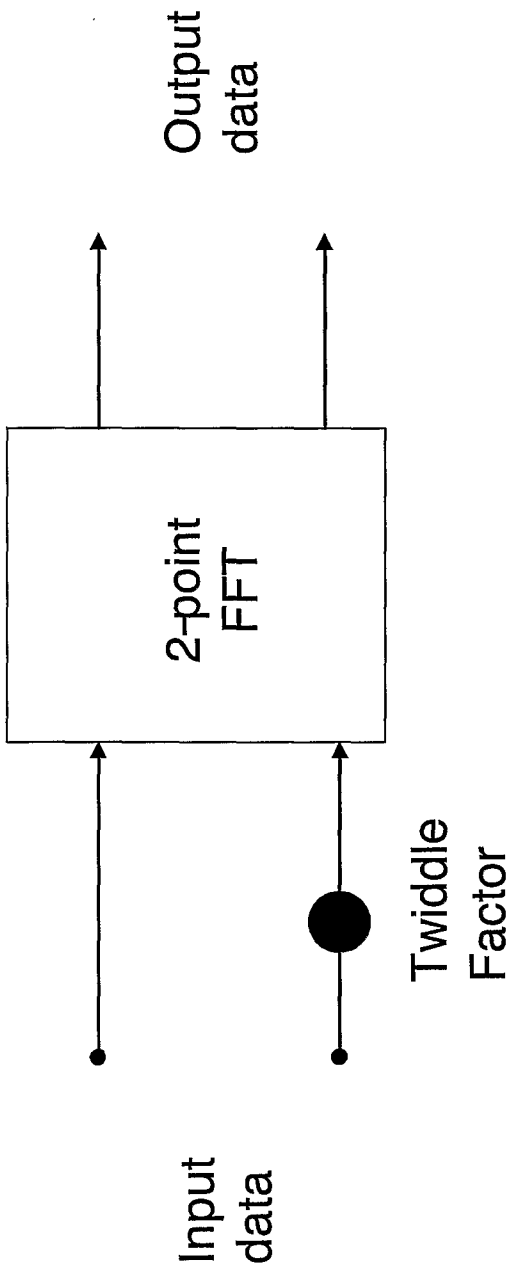


FIG. 10

FIG. 11

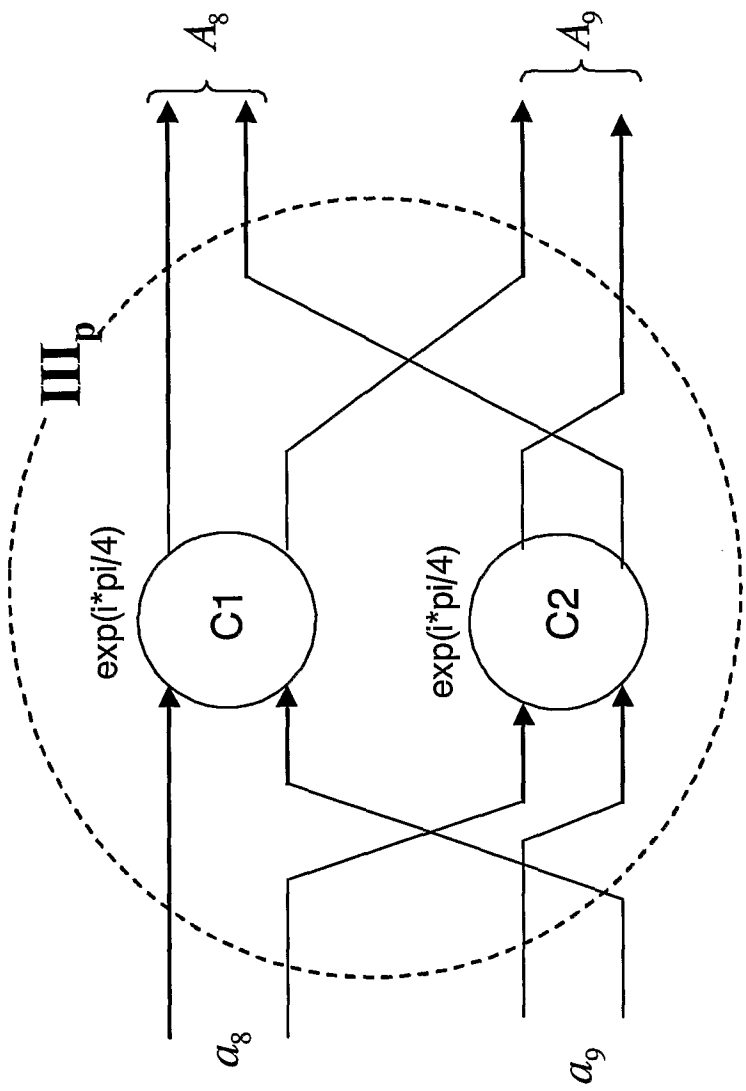


FIG. 12

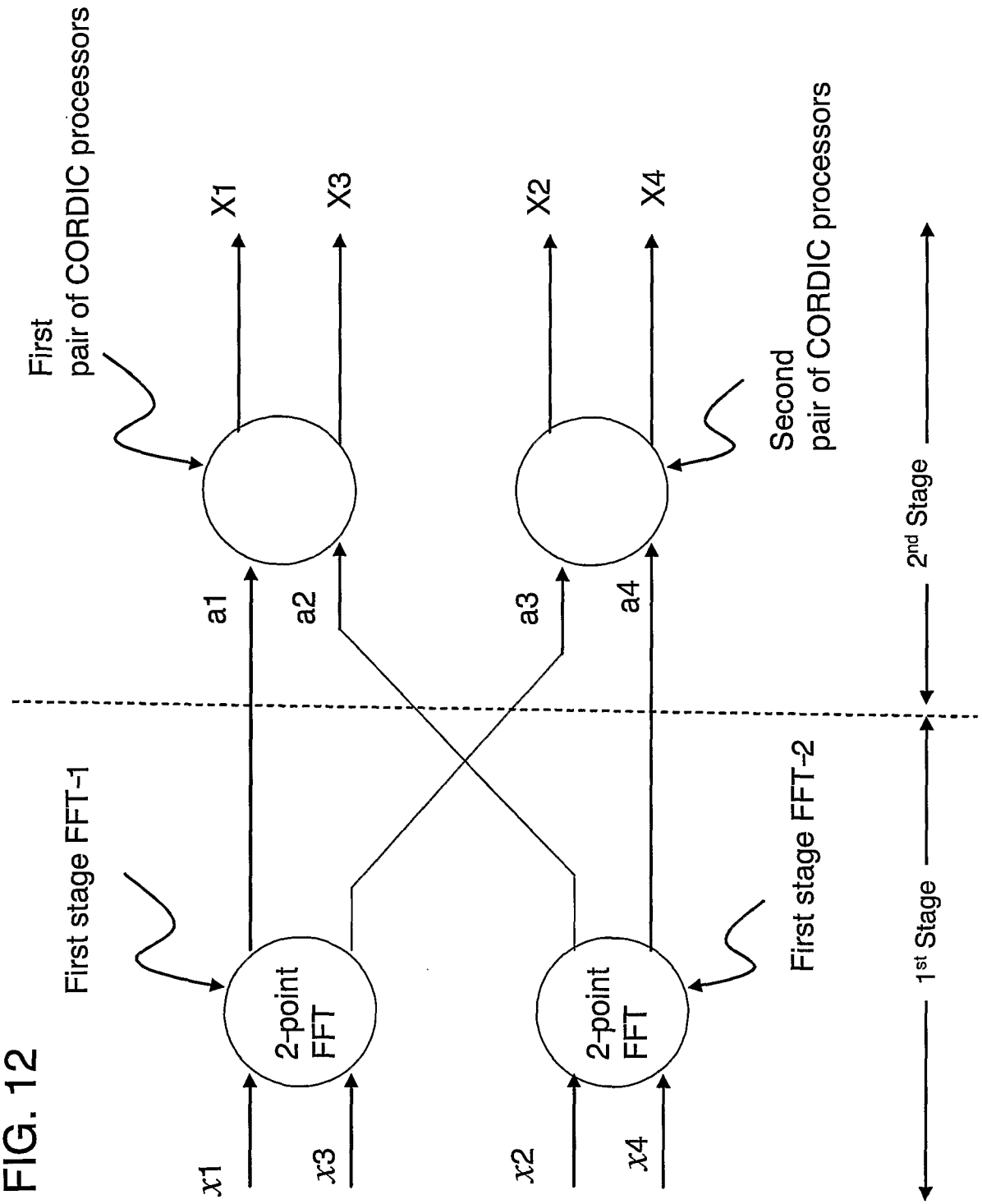

First stage FFT-1
First stage FFT-2
First pair of CORDIC processors
Second pair of CORDIC processors
2-point FFT
2-point FFT
x1
x3
x2
x4
a1
a2
a3
a4
X1
X3
X2
X4
1st Stage
2nd Stage

FIG. 13

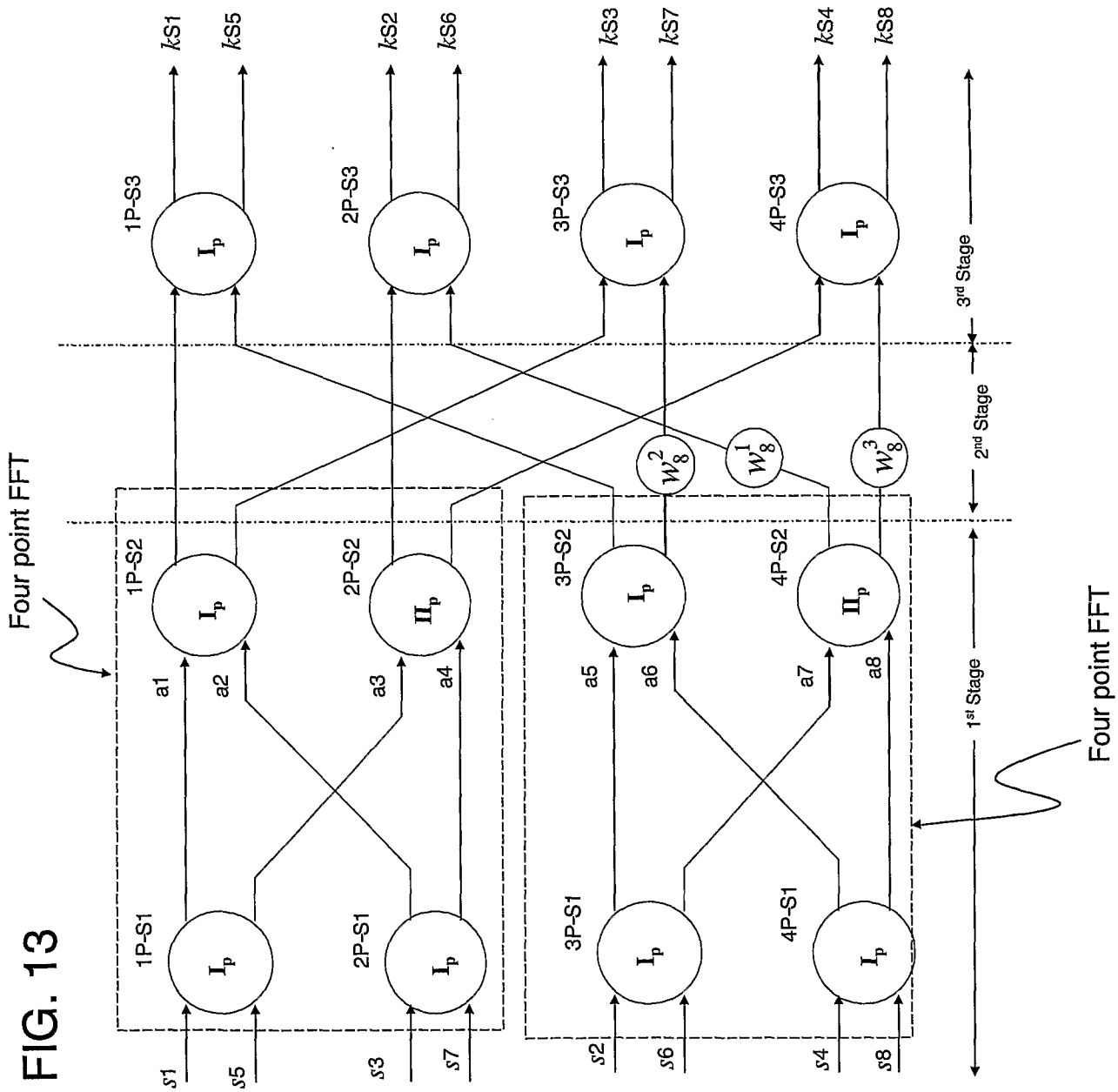
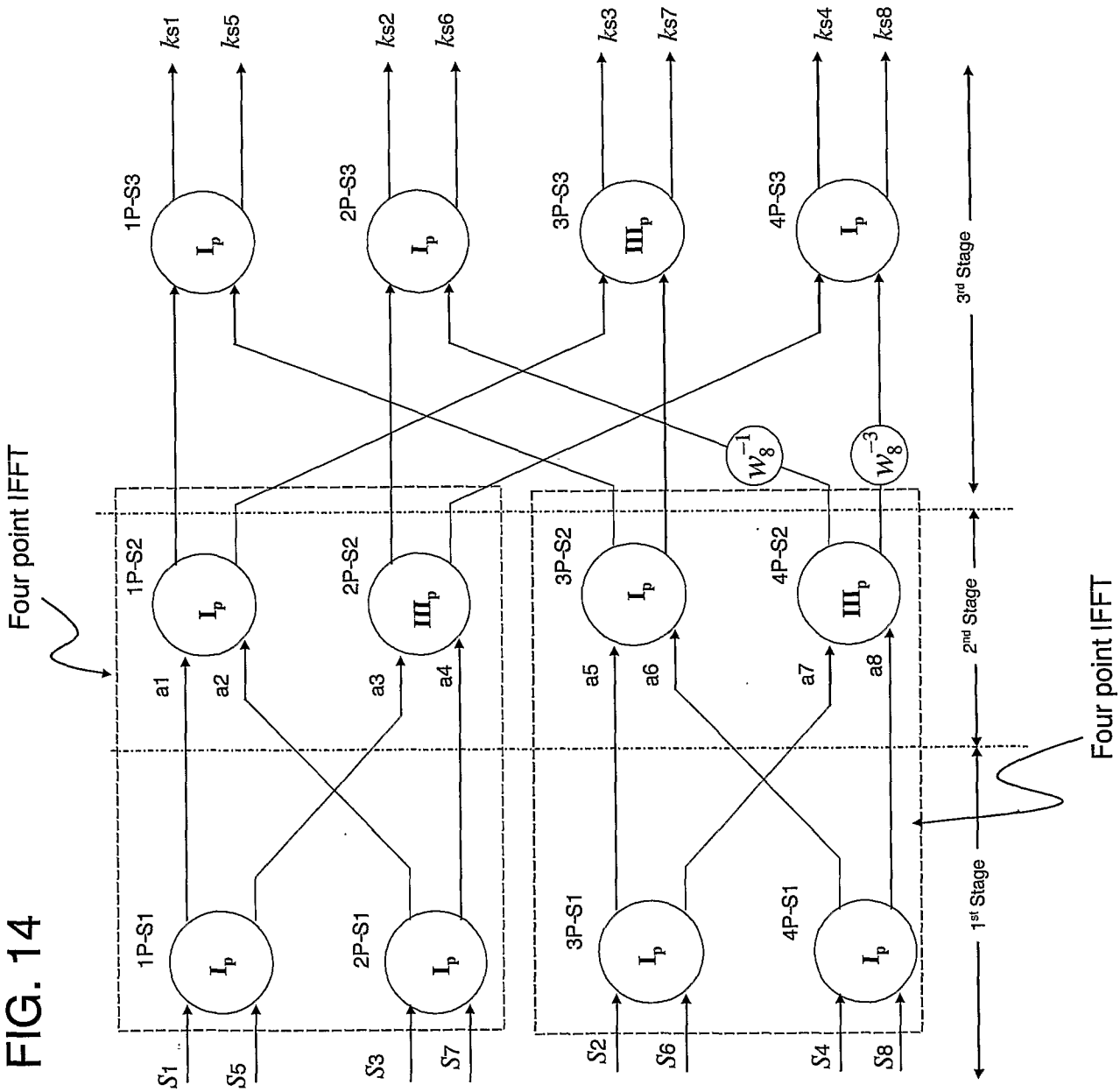

Four point FFT
1P-S1
1P-S2
1P-S3
2P-S1
2P-S2
2P-S3
3P-S1
3P-S2
3P-S3
4P-S1
4P-S2
4P-S3
I_p
II_p
s1
s5
s3
s7
s2
s6
s4
s8
a1
a2
a3
a4
a5
a6
a7
a8
kS1
kS5
kS2
kS6
kS3
kS7
kS4
kS8
W_8^2
W_8^1
W_8^3
1st Stage
2nd Stage
3rd Stage
Four point FFT

FIG. 14


Four point IFFT
1P-S1
1P-S2
1P-S3
2P-S1
2P-S2
2P-S3
3P-S1
3P-S2
3P-S3
4P-S1
4P-S2
4P-S3
I_p
III_p
a1
a2
a3
a4
a5
a6
a7
a8
S1
S5
S3
S7
S2
S6
S4
S8
ks1
ks5
ks2
ks6
ks3
ks7
ks4
ks8
W_8^{-1}
W_8^{-3}
1st Stage
2nd Stage
3rd Stage
Four point IFFT