

[54] **ELECTRONIC SCORING SYSTEM FOR BOWLING ESTABLISHMENTS**

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[51] Int. Cl.² **A63D 5/00; A63D 5/04**

[58] Field of Search **340/172.5, 323 B; 235/92 GA, 151; 273/54 C**

[56]

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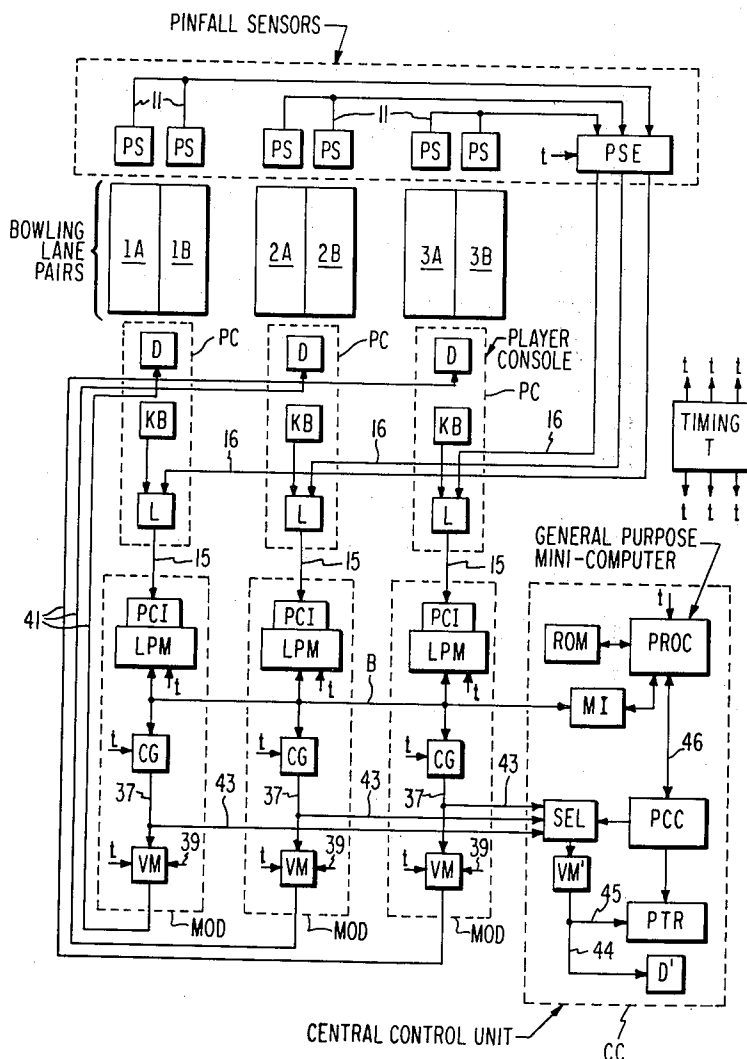
Attorney, Agent, or Firm—Edward J. Norton; Carl V. Olson

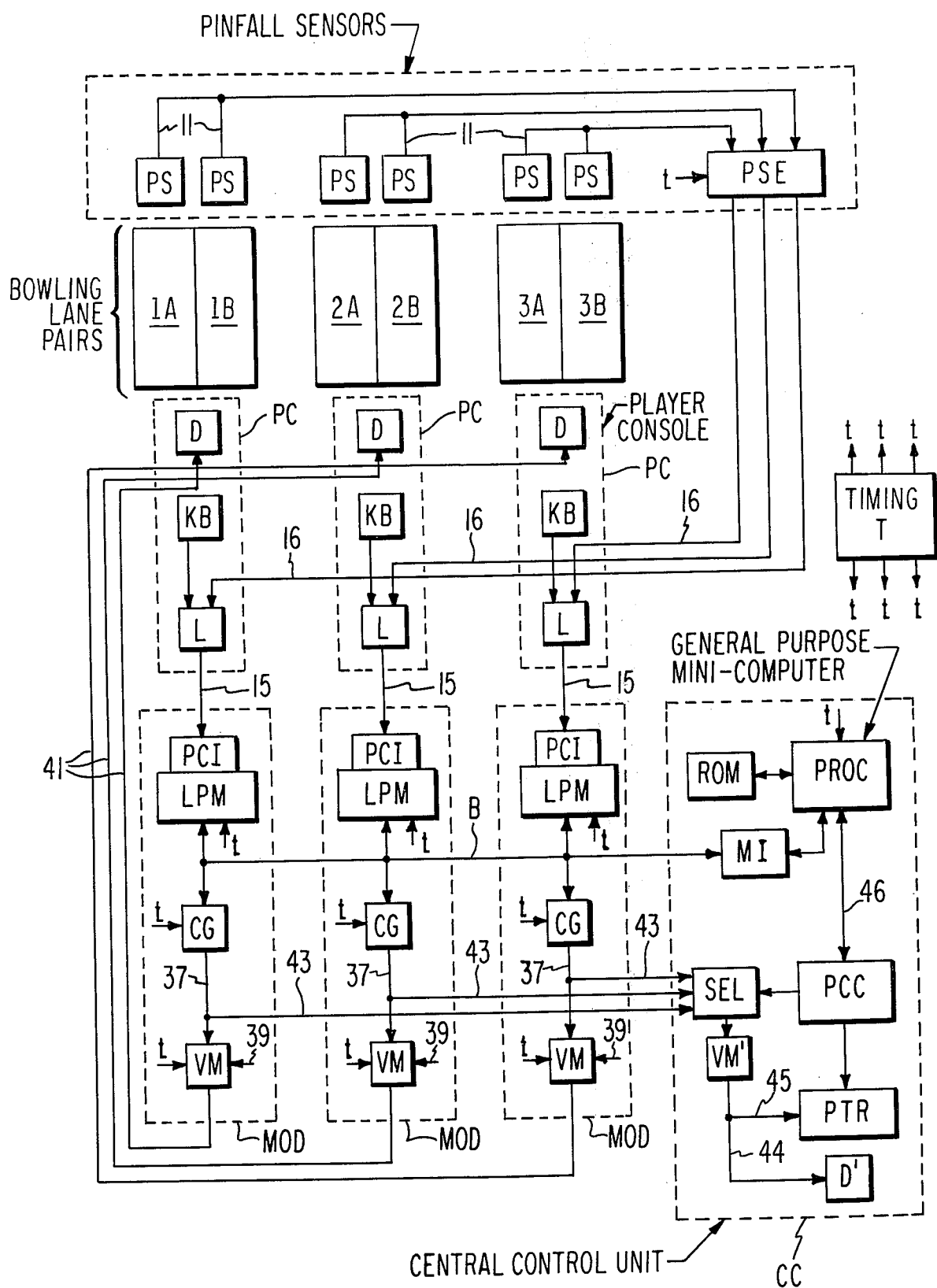
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ABSTRACT

An automatic scoring system for a plurality of bowling lanes is disclosed which employs a central control unit including a general purpose mini-computer having a read-only memory programmed to control the processor in the computation and display of bowling scores. The system is constructed to be easily expanded by adding a player console and an electronic module for each added pair of bowling lanes. Bowling score sheet information is displayed on cathode ray tube display devices at player and proprietor locations. Pinfall information may be introduced manually or by automatic pinfall sensors.

2 Claims, 4 Drawing Figures





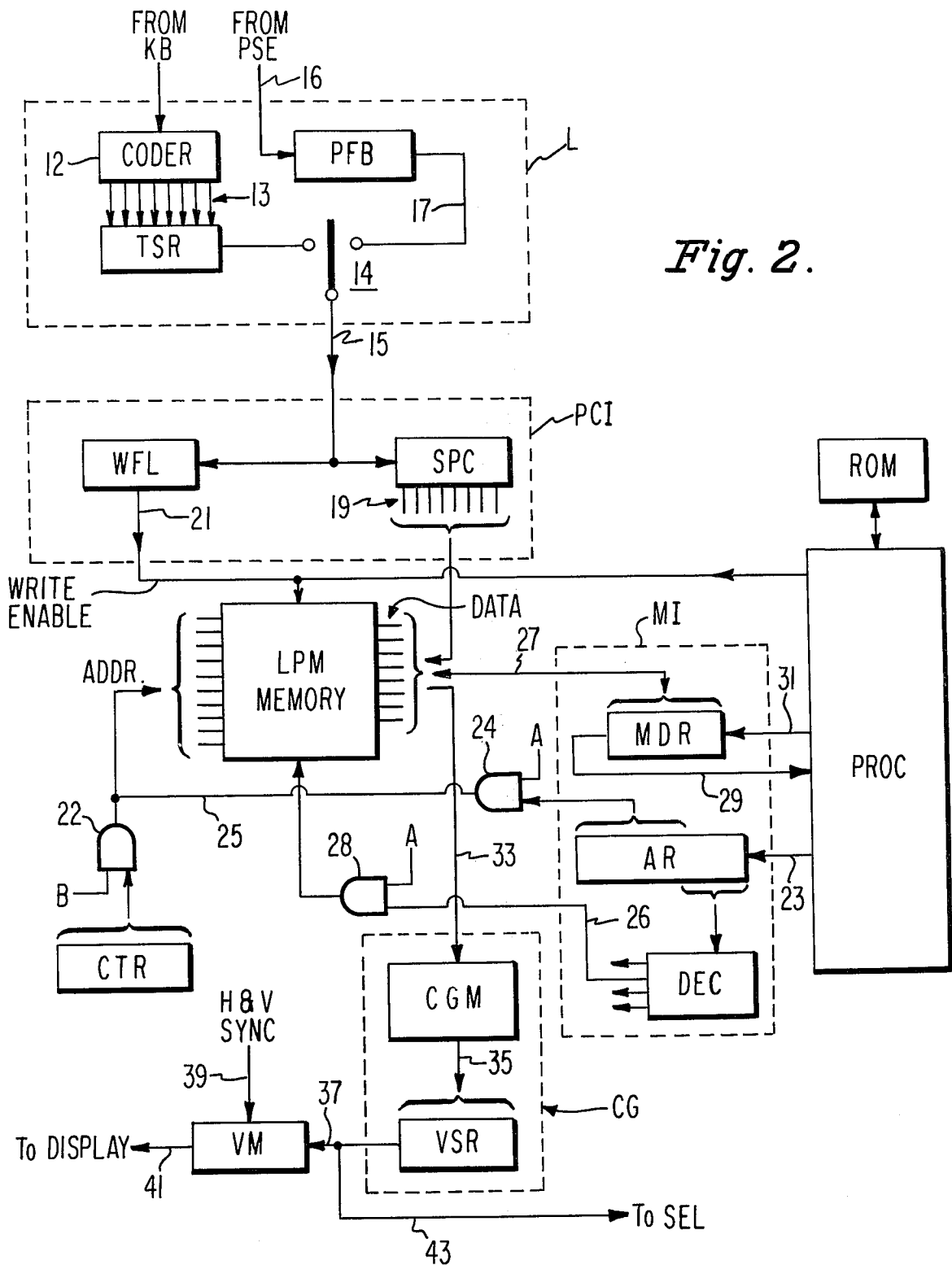
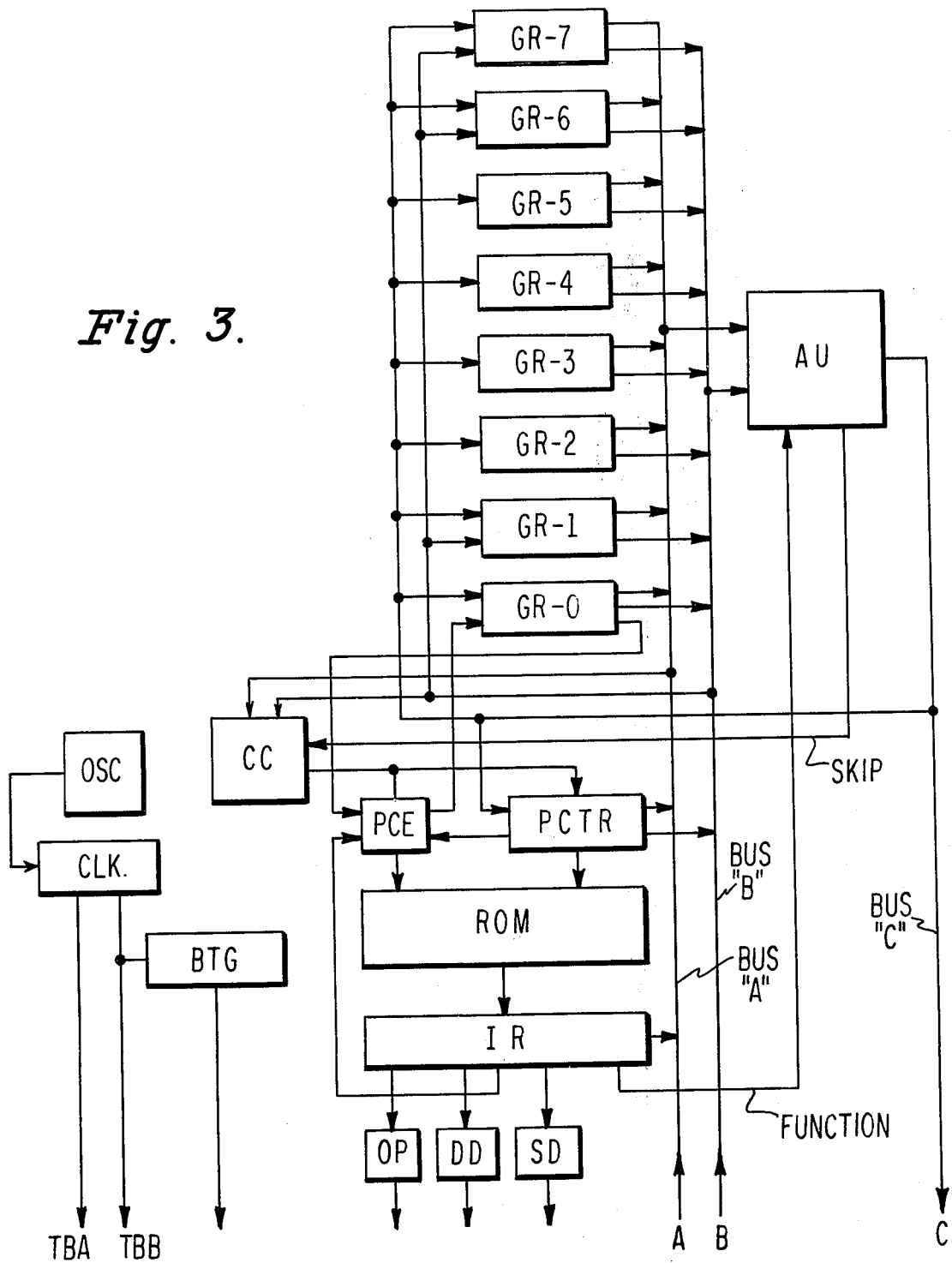


Fig. 3.



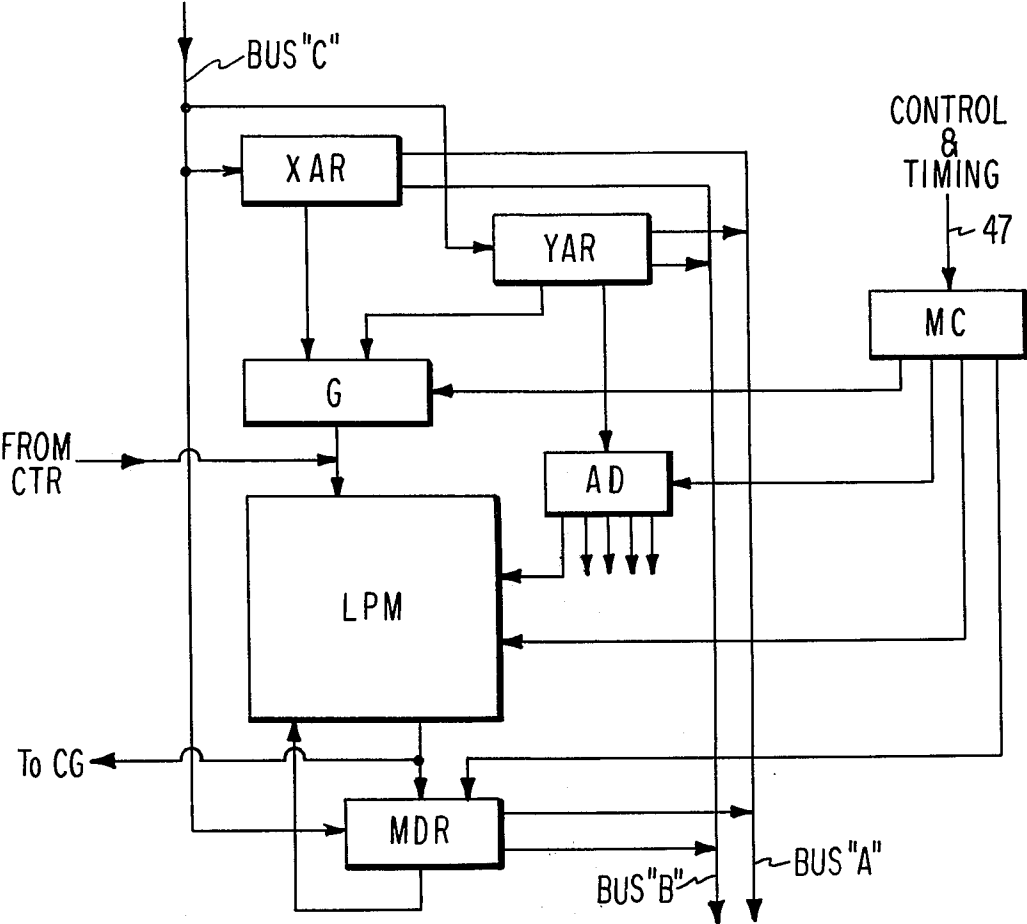


Fig. 4.

ELECTRONIC SCORING SYSTEM FOR BOWLING ESTABLISHMENTS

BACKGROUND OF THE INVENTION

Many electro-mechanical and some electronic systems have been proposed for accomplishing the automatic computation and display of bowling scores. The rules by which scores are computed in bowling contests are not simple, and demands for inexpensive and reliable automatic scoring equipment have yet to be satisfied. The approach that has been followed in the past has been to design a system in which every component is a special-purpose device useful solely in cooperation with the other special-purpose devices for computing bowling scores. This seemingly logical approach has resulted in scoring systems which are unnecessarily complex and unnecessarily expensive to build and maintain.

SUMMARY OF THE INVENTION

According to an example of the present invention, an improved electronic automatic scoring system for a plurality of bowling lanes is constructed using a general-purpose mini-computer having an alterable read-only memory containing a computer program. The program consists of sequences of instructions written to control the calculation and display of bowling scores. An electronic module is provided for each pair of bowling lanes, each module includes a lane pair memory, and all lane pair memories are connected to operate as the main memory of the mini-computer. Electronic modules, and player consoles, can be added to the system without complication whenever it may be desired to expand the system to handle additional pairs of bowling lanes.

BRIEF DESCRIPTION OF THE DRAWING

FIG. 1 is a schematic diagram of an automatic bowling score computing and display system constructed according to the teachings of the invention;

FIG. 2 is a more detailed block diagram of a portion of the system shown in FIG. 1;

FIG. 3 is a block diagram of a general-purpose mini-computer suitable for use in the system of FIG. 1; and

FIG. 4 is a block diagram of a lane pair memory used as a memory by the computer of FIG. 3 in the system of FIG. 1.

DESCRIPTION OF A PREFERRED EMBODIMENT

Referring in greater detail to FIG. 1 of the drawing, three pairs of bowling lanes are represented at 1A, 1B; 2A, 2B; and 3A, 3B. A pinfall sensor PS is located at the remote end of each bowling lane. Each pinfall sensor PS provides a clocked series of binary units on its output conductor 11 which indicates the numbers of the pins which have been knocked down after a ball has been rolled down the bowling lane or alley. While any pinfall sensor equipment may be employed, a suitable equipment is described in detail in a U.S. patent application Ser. No. 318,550 filed by Hugo Logemann, Jr. and Harold F. Dion on Dec. 26, 1972 now U.S. Pat. No. 3,847,394, issued on Nov. 12, 1974, entitled "Bowling Pin Detector" and assigned to the assignee of the present application. The outputs of all pinfall sensors PS are cabled to a common pinfall sensor electronics unit PSE from which the signals are transmitted at suitable timed

intervals to appropriate ones of player consoles PC₁, PC₂ and PC₃.

Each player console PC is located at the player end of a pair of bowling lanes and includes a cathode-ray-tube display device D, a keyboard KB and a logic unit L. The display device D is preferably a conventional television receiver which has been somewhat modified for use as a display device for alpha-numeric scoresheet information.

Each player console PC also includes a keyboard KB by means of which the following transactions can be introduced into the system: (a) Player Name Entry, (b) Handicap Entry, (c) Missing Player Entry, (d) Score Correction Entry, (e) Score Clear, (f) Lane Clear, and (g) Pinfall Entry. The keyboard KB consists of a push button matrix providing an output that is applied to a coder 12 (FIG. 2) in a logic unit L. The coder 12 has a number of output lines 13, and the pushing of a button results in a coded energization of appropriate ones of the output lines. The output lines are connected to the inputs of a corresponding number of stages of a transmit shift register TSR. The transmit shift register is constructed so that its contents can be shifted out in serial form through a switch 14 to a player console output line 15.

The logic unit L in player console PC also receives serially-presented pinfall information signals on lead 16 from the pinsensor electronics PSE. This serial signal is fed into the input of a pinfall buffer shift register PFB. Information stored in the buffer may be read out serially through line 17 and switch 14 to player console output line 15.

The output lines 15 in FIG. 1 from player console PC, are connected to a player console interface PCI in respective electronics modules MOD. The player console interface PCI in each electronics module is an interface between a player console PC and a lane pair memory LPM in the electronics module. Each lane pair memory LPM is a conventional known semiconductor random access memory consisting of 1024 words of eight bits each. The memory is made using eight semiconductor chips each having storage locations for 1024 bits. Each semiconductor chip includes an address decoder responsive to 10 input address bit lines ADDR (FIG. 2) and operative to select one of the 1024 bit storage locations on the chip. The same address is simultaneously applied to all eight chips to access 8 bit storage locations constituting one eight-bit memory word storage location. The eight data lines of the lane pair memory are designated DATA.

A player console interface PCI with the lane pair memory includes a serial-to-parallel converter SPC (FIG. 2) for the serial pinfall and other information received over line 15 from the player console. The parallel output lines 19 from the SPC are connected to the respective memory data lines DATA of the lane pair memory LPM. The player console interface also includes a word framing logic WFL which senses the start bit of a word received on lines 15, and transmits a write enable signal over line 21 to the memory LPM when an 8-bit word is accumulated in converter SPC. The information supplied from the serial-to-parallel converter SPC is read into a storage location in memory LPM determined by the address in a counter CTR in the timing unit T. The address is passed through gate 22 when enabled by a memory cycle signal B.

The lane pair memories LPM in the electronic modules MOD in FIG. 1 are all connected by means of a multiconductor bus B and a memory interface MI with a general purpose mini-computer or processor PROC in a central control unit CC. As shown in FIG. 2, the memory interface MI includes an address register AR, which is a serial-to-parallel converter, and to which addresses are supplied in serial form over line 23 from the processor. Pin address bits are applied in parallel from register AR through gate 24 and over pin conductors 25 to the 10 address input lines ADDR of lane pair memory LPM. A 10-bit address from the processor PROC can address any one of the 1024 word locations in the memory LPM. On the other hand, the remaining 6 bits in address register AR are applied to a decoder DEC, from which one output line 26 is applied through gate 28 to the chip enable input of one respective lane pair memory LPM.

The memory interface MI also includes an eight-bit data register MDR connected by eight parallel conductors 27 with the eight data lines DATA of the lane pair memory LPM. The data register MDR is a serial-to-parallel converter and a parallel-to-serial converter. Eight data bits applied from memory LPM over parallel lines 27 to data register DR are transferred serially over line 29 to the processor PROC. And, eight serial bits applied over line 31 to register MDR are transmitted over parallel lines 27 to the data lines DATA of memory LPM.

Each electronics module MOD in FIG. 1 also includes a character generator CG and a video mixer VM. Each character generator, as shown in FIG. 2, includes a character generator read-only memory CGM connected to receive eight-bit data words from memory LPM over lines 33. Each such data word is applied as an address to the read-only memory CGM. The digital information bits in the addressed location are applied in parallel over lines 35 to a video shift register, or parallel-to-serial converter VSR. The contents of the converter VSR is shifted out on serial output lead 37 as a digitally-generated video signal. That is, the signal on lead 37 is a pattern of pulses and spaces existing in time sequence such that it can be used to control the intensity of the electron beam in a cathode-ray tube and thus trace one line of a black-and-white line image (no gray scale) on the face of the tube. The signal on lead 37 is thus a video signal for tracing a part of an alphanumeric character corresponding to a conventional digital representation of the character supplied from the data output DATA of lane pair memory LPM to the address input of character generator read-only memory CGM.

The digitally-generated video signal on line 37 is applied to a video mixer VM, which also receives horizontal and vertical synchronizing signals, and signals for creating a crossed line score sheet pattern on the display, from the timing unit T over line 39. The video signal, the synchronized pulses, and the crossed line signal are mixed to produce an output video signal on lead 41 which is a standard television video signal suitable for application to the video circuit of a television receiver. The signal is applied over lead 41 to a display device D in the player console PC (FIG. 1), the display device D being a slightly modified television receiver. The video signal on line 37 is also applied over line 43 to a selector SEL in the central control unit CC.

Each one of the electronics modules MOD is needed for a corresponding bowling lane pair. The modules are constructed exactly alike, and any reasonable number of modules can be connected into the system, that is, an electronics module (and player console) can be added to the system for every bowling lane pair that is added to the bowling establishment, without requiring any changes in, or substitution of, the central control unit CC.

The central control unit CC (FIG. 1) includes a proprietor's control console PCC by which the proprietor manages the operation of the bowling establishment through its automatic scoring system. The proprietor's control console includes a thumb wheel by which the proprietor controls the digital video selector SEL to select the video signal from the electronics module corresponding to any desired bowling lane pair. The selected video signal is combined with horizontal and vertical synchronizing pulses in a video mixer VM' and is then applied over line 44 to a proprietor's display device D', which is the same as the display device D in the player consoles PC. The video signal from mixer VM' is also applied over line 45 to a printer PTR. The printer PTR includes a cathode-ray-tube display on the face of which appears the same score sheet information as appears on the display device D'. The printer also includes means to make a hard copy of the displayed score sheet on a piece of paper by any suitable method such as the xerographic method.

The proprietor's control console PCC includes a control panel and logic by which commands are sent over lines 46 between the console PCC and the computer processor PROC. For example, the proprietor can designate each bowling lane as having a status of "off", "league", "open", or "practice". The proprietor's console has switches to accomplish "score clear", "lane clear", and "print score" functions. And player's names for any desired lanes can be entered. All of these controls and others are accomplished by signals over lines 46 to the processor PROC.

A central timing unit T controls the timing of the entire system by supplying various timing signals, designated t , to all units of the system.

The central control unit CC includes a general purpose mini-computer PROC and read-only memory ROM, as shown in more detail in FIG. 3. The read-only memory ROM is a semiconductor memory containing computer instruction words 16-bits long. Instructions are read out of the memory under control of addressing circuits including a program counter PCTR, an extended program counter PCE and a program counter control CC. The instructions are read out in sequence, except when a jump to an out-of-sequence instruction is effected by conventional logic in the computer processor. Instructions are read out to a 16-bit instruction register IR. There are eight types of instructions: Unconditional jump, Jump and save, Logic function, Arithmetic function, Control and test, Load immediate, Add immediate, and And immediate.

Portions of an instruction in the instruction register IR are applied to an operation decoder OP, a destination decoder DD, and a source decoder SD, which provide output signals to control transfers from one place to another in the systems. Another "function" portion of an instruction in register IR is applied to an arithmetic unit AU together with the operation code, to control all functions performed on data present on busses A

and B. The functions include: Add with carry, Subtract with carry, Left shift with carry, Gray to Binary with carry, Add, Subtract, Left shift, and Gray to binary, Logical AND, Exclusive OR, Inclusive OR, Complement, Rotate right, Transfer and Compare. The result is supplied to bus C. Eight-bit-word general registers GR-0 to GR-7 are connected with the busses and can be used by the computer programmer for the temporary storage of any type of information as needed in the execution of the computer program by which bowling scores are automatically computed and displayed. Data words handled by the processor contain eight bits and are transferred on busses A, B, C in bit serial form. Timing signals are provided by an oscillator OSC and clock CLK which provide two-phase clock signals TBA and TBB used for the basic timing of the processor. A bit time generator BTG produces 12 timing pulses to control status level functions during execution of each instruction.

FIG. 4 shows one of the lane pair memories LPM included in the system of FIG. 1, and the memory interface MI included in the central control unit CC. The memory address register consists of an X address register XAR and a Y address register YAR. Eight address bits from register XAR and two address bits from register YAR are applied through an address gating unit G to a decoder in the memory LPM to select one eight-bit word location from the 1024 word locations in the memory LPM. Six bits from register YAR are applied to an address decoder AD to select one lane pair memory LPM from the plurality of up to 64 similar lane pair memories in the system. Eight-bit memory words are read to and from the memory via a memory data register MDR. Data words are transferred in bit serial form between the memory register MDR and the data busses connected to the computer processor PROC.

The memory control unit MC in FIG. 4 controls the cyclic operation of the lane pair memory LPM in synchronism with timing and control signals supplied thereto over leads 47. There are two alternating memory access cycles A and B during each bit time pulse from the bit timing generator BTG in FIG. 3. Memory cycles A can be used by the processor PROC shown in FIGS. 1, 2 and 3. During memory cycles B a digital word is read out from the memory to the respective character generator CG, shown in FIGS. 1 and 2, where it is converted into a video signal to refresh the score sheet display on the respective cathode ray tube display device D. During field retrace in the display device D, memory cycles B can be used to store information in the lane pair memory from the corresponding player console.

In the operation of the automatic scoring system, the proprietor acting through the proprietor's control console PCC energizes a particular lane pair for bowlers in a league, open, or practice mode. The player's names are then entered, from the keyboard KB at the player's console PC, to the lane pair memory LPM during memory cycles B of the memory. Each lane pair memory has storage space reserved for the names of players using the corresponding pair of lanes, and their scores for bowling "frames" 1 through 10. Once the lane pair is put in operation, the display D in the player console PC is automatically and periodically refreshed with the information, such as players' names, contained in the lane pair memory during the memory cycles B of the memory.

As pinfall information is introduced, automatically by the pinfall sensors PS or manually from the player's console PC, this information for a given player is supplied to a nondisplayed storage location reserved for information from a respective player console in the lane pair memory during a memory cycle B of the memory. During memory cycles A, the processor continuously scans these non-displayed memory locations, and when new pinfall information of a given player is found in one of these memory locations, the processor uses the information, together with the information located in displayed memory locations for the given player, to compute the score that should be displayed for that frame for the particular player. The score for the frame is then transferred to a prescribed location in the displayed portion of the lane pair memory LPM. All these memory accesses by the processor are done during memory cycles A of the memory. During memory cycles B of the memory, the entire score sheet information stored in the displayed portion of the memory, including the score for the frame just computed, is read out of the memory to the character generator CG where the digital information is translated to a video signal suitable for tracing the score sheet information on the face of a cathode-ray-tube display D.

In this way, the scores of a player in each successive frame of a game are computed and displayed. At the same time, the scores of all other players on the two lanes are computed and displayed as the balls are rolled. And, at the same time, the scores of all the players on all the other lane pairs are computed and displayed at the respective player consoles. The single, general-purpose computer processor PROC handles the computations for the many players and many frames in a time division multiplex fashion. The processor PROC accomplishes the computation of each frame score so rapidly that it has time to handle the scores for up to 12 bowlers bowling on each of up to 64 pairs of bowling lanes.

Provision is made for correcting an error in a player's score. An error may occur as the result of a human error when operating in the semi-automatic mode, and as the result of unusual pin action when operating in the automatic mode. For example, a pin may be shifted sideways by the ball to such an extent that it cannot be recognized as a standing pin by the pinfall sensor. An erroneous score in any frame is corrected by transferring the correct score for the frame from the player console to the message receiving area in the lane pair memory. The processor recognizes the error correcting message, and requests a hard copy print of the existing score sheet information. While the print is being made, new pinfall information resulting from continued bowling is accumulated in a queue in the lane pair memory. When the print is finished, the processor recomputes the correct scores in the frame in which the correction was inserted, and preceding frames if they are affected, and in succeeding frames. The corrected scores are stored by the processor in the appropriate displayed information storage region of the respective lane pair memory. Then the queued pinfall information is processed to compute scores for frames bowled after the error was corrected. Then the score sheet information displayed contains the fully-corrected up-to-date scores, the correction having been accomplished without any delay to the bowlers.

Provision is made for a "pacer" player to even up the number of players on two competing teams. The pacer's name is entered with a + sign in front of the name. The pacers' scores are displayed, but not included in the team score total. Provision is also made for a missing player. The player's average score is inserted in the tenth frame. These features of the system are accomplished by appropriate program routines stored in the read-only-memory ROM.

When a game on a lane pair is finished, a team captain pushes a score clear button on the player console. This causes the score clear information to be transferred from the player console to the lane pair memory. The processor recognizes the order, and checks to make sure the game is finished, and then causes a hard copy of the score sheet information to be made by the printer PTR. Then the scores for frames 1 through 10 are erased from the lane pair memory, and consequently from the displayed score sheet information. The pressing of a lane clear button on the player console causes a clearing of the player's names from the displayed score sheet.

When the players are relieved of the onerous score-keeping task, the bowling games proceed much more rapidly, and the increased revenue for the bowling establishment more than pays for the automatic scoring system.

What is claimed is:

1. A semiautomatic scoring system for a plurality of pairs of bowling lanes comprising:
 - a player console for each pair of bowling lanes, including a cathode-ray-tube display device, a keyboard and a logic unit,
 - an electronic module for each pair of bowling lanes, including a lane-pair memory and a character generator,
 - said keyboard in each player console being connected to supply player and pinfall information in the form of digital signals through said logic unit in the player console to the lane-pair memory in the respective electronic module,
 - said character generator in each electronic module being constructed to translate digital information received from the corresponding lane-pair memory into video signals and to supply the video signals to the display device in the respective player console, and
 - a central control unit for all bowling lanes including a proprietor's control console, a proprietor's cathode-ray-tube display device, a displayed-information printer unit, a lane-pair video signal selector to connect the video signal from the char-

acter generator associated with any desired one of said bowling lane pairs to said proprietor's display device and said printer unit, a general purpose mini-computer processor connected through a memory interface with all of said lane-pair memories so that they serve as the main memory for said processor, and a read-only memory containing a computer program for controlling the operation of the processor in the computing and display of scores in all bowling lanes.

2. A fully automatic scoring system for a plurality of pairs of bowling lanes, comprising:

a player console for each pair of bowling lanes, including a cathode-ray-tube display device, a keyboard and a logic unit,

an electronic module for each pair of bowling lanes, including a lane-pair memory and a character generator,

said keyboard in each player console being connected to supply player and score correcting information in the form of digital signals through said logic unit in the player console to the lane-pair memory in the respective electronic module,

a separate, automatic pinfall sensor for each of said bowling lanes connected to supply pinfall information in electrical form through the logic unit of the corresponding player console to the lane-pair memory in the electronic module associated with that player console,

said character generator in each electronic module being constructed to translate digital information received from the corresponding lane-pair memory into video signals and to supply the video signals to the display device in the respective player console, and

a central control unit for all bowling lanes including a proprietor's control console, a proprietor's cathode-ray-tube display device, a displayed-information printer unit, a lane-pair video signal selector to connect the video signal from the character generator associated with any desired one of said bowling lane pairs to said proprietor's display device and said printer unit, a general purpose mini-computer processor connected through a memory interface with all of said lane-pair memories so that they serve as the main memory for said processor, and a read-only memory containing a computer program for controlling the operation of said processor in the computing and display of scores in all bowling lanes.

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