(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
17 June 2004 (17.06.2004)

PCT

(10) International Publication Number
WO 2004/051491 A1

(51) International Patent Classification[7]: G06F 13/38

(21) International Application Number:
PCT/FI2003/000908

(22) International Filing Date:
27 November 2003 (27.11.2003)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
20022113 29 November 2002 (29.11.2002) FI

(71) Applicant *(for all designated States except US)*: **NOKIA CORPORATION** [FI/FI]; Keilalahdentie 4, FIN-02150 Espoo (FI).

(72) Inventors; and
(75) Inventors/Applicants *(for US only)*: **MYLLY, Kimmo** [FI/FI]; Niemenkuja 8 as 1, FIN-39160 Julkujärvi (FI). **FLOMAN, Matti** [FI/FI]; Suoramantie 25, FIN-36220 Kangasala (FI).

(74) Agent: **TAMPEREEN PATENTTITOIMISTO OY**; Hermiankatu 12 B, FIN-33720 Tampere (FI).

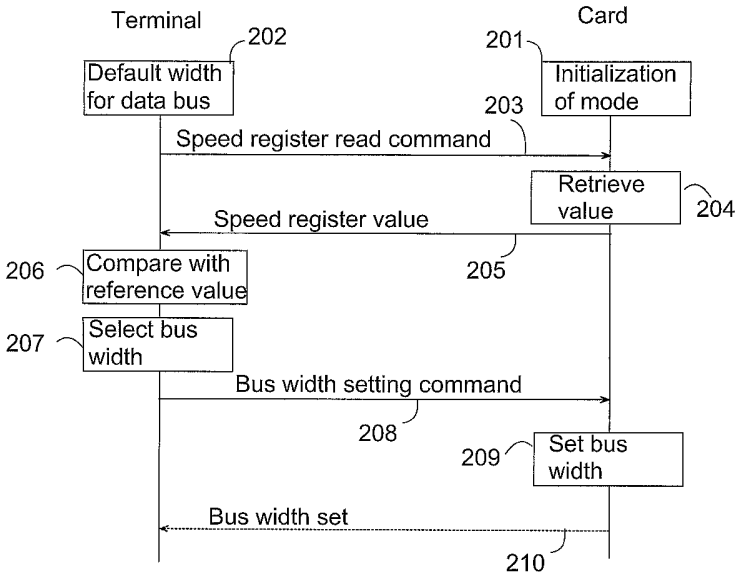
(81) Designated States *(national)*: AE, AG, AL, AM, AT (utility model), AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ (utility model), CZ, DE (utility model), DE, DK (utility model), DK, DM, DZ, EC, EE (utility model), EE, EG, ES, FI (utility model), FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NI, NO, NZ, OM, PG, PH, PL, PT (utility model), PT, RO, RU, SC, SD, SE, SG, SK (utility model), SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States *(regional)*: ARIPO patent (BW, GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*

[Continued on next page]

(54) **Title:** A METHOD AND A SYSTEM FOR DETECTING BUS WIDTH, AN ELECTRONIC DEVICE, AND A PERIPHERAL DEVICE



(57) **Abstract:** The present invention relates to a method for detecting the bus width of a peripheral device (12) connected to an electronic device (1). At least one bus width from a defined set of bus widths is available in the peripheral device (12). In the method, for detecting the bus widths available for the peripheral device (12), one or more indicators (17, DAT3) formed in the peripheral device (12) are used, which indirectly indicate which one or ones of said set of bus widths are available in the peripheral device (12). The invention also relates to a system, in which the method is applied, as well as an electronic device (1) and a peripheral device (12).

WO 2004/051491 A1

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

A method and a system for detecting bus width, an electronic device, and a peripheral device

The present invention relates to a method for detecting the bus width of a peripheral device connected to an electronic device, which peripheral device has at least one bus width available from a defined set of bus widths. The invention also relates to a system comprising an electronic device, an auxiliary device which can be connected to the electronic device and in which at least one bus width from a defined set of bus widths is arranged to be used, and which system comprises a bus width detector for detecting at least one bus width available for used in the peripheral device connected to the electronic device. The invention also relates to an electronic device provided with a bus width detector for detecting the bus width of a peripheral device connected to the electronic device, in which peripheral device at least one bus width is arranged to be used from a defined set of bus widths. The invention also relates to a peripheral device which can be connected to an electronic device provided with a bus width detector for detecting the bus width of the peripheral device connected to the electronic device, and in which peripheral device at least one bus width is arranged to be used from a defined set of bus widths.

Electronic devices are known, to which it is possible to connect various peripheral devices, such as cards (interface cards, expansion cards), by which it is possible to change the facilities of the electronic device. For example, such a card can be used to provide a memory expansion for an electronic device, such as a computer, a wireless communication device, a personal digital assistant, *etc.* The electronic device is thus equipped with a peripheral device connection, such as a card connection, in which the peripheral device is placed. Via the peripheral device connection, it is possible to supply the necessary operating voltages, control and data signals to the card. In a corresponding manner, information can be transmitted from the card to the electronic device via this peripheral device connection. The peripheral device connection typically comprises a control bus, an address bus and/or a data bus. The

control bus is used for the transmission of control information between the electronic device and the card. The address bus is used for the transmission of addresses to the card. The data bus, in turn, is intended for the transmission of information between the electronic device and the card. However, arrangements have been developed, in which one or several of said buses are combined at least partly. For example, some of the address data can be transmitted via the control bus. An example of such a card is the memory card complying with the MultiMediaCard™ specifications. It is also possible that some of the address data can be transmitted via the data bus.

A problem in the systems of prior art is, for example, the fact that the same bus widths are not necessarily used in all cards, wherein the electronic device should, in each case, be capable of determining the bus width of the card connected to the electronic device, for example the width of the data bus. If the bus width is assumed or detected to be incorrect in the electronic device, this will cause error situations and the card can probably not be used at all. For example, the memory card complying with so-called SD Memory Card specifications (v. 1.01) comprises a data bus, in which it is possible to select either a 1-bit data bus or a 4-bit data bus. To maintain compatibility of such cards complying with newer specifications with the earlier versions, the card initialization steps are taken by using the data bus width of 1 bit. Thus, when starting the card, the card and the device to which the card is connected communicate on the 1-bit data bus. After the electronic device has determined the bus widths supported by the card, the electronic device can control the card to use another bus width which can be selected, for example a 4-bit bus. If the card or the electronic device does not support other bus widths than the 1-bit data bus, the operation is continued by using the 1-bit data bus width. The bus widths can be determined, for example, in such a way that the electronic device transmits a card initialization command complying with the SD specifications (ACMD 41). If the card responds to this command, it can be determined that the card is a card complying with said specifications. In other cases, it is possible to transmit, for example, an initialization command complying with the MultiMediaCard™ specifications

(CMD 1), and if the card responds to this command, it can be determined that the card is a card complying with the MultiMediaCard™ specifications.

International patent application WO 02/15020 discloses an arrangement, in which two or more memory cards can be connected to an electronic device. Thus, information about the data bus width supported by the card is stored in each memory card. The electronic device can thus read this information and select the data bus width to be one supported by the card in question. One drawback in such an arrangement is that the storage of the bus width data requires memory space (registers) on the card.

It is an aim of the present invention to provide an improved method and a system, in which the determination of the bus widths supported by the card does not require that the bus width data is stored on the card. The invention is based on the idea that for determining the bus width, another indication formed on the card is used, on the basis of which the bus width can be determined. One advantageous example of such an indication is the information, stored on the card, about the standard and/or standard version supported by the card. To put it more precisely, the method according to the present invention is primarily characterized in that for detecting the bus widths available on the card, one or more indicators formed on the card are used, which indirectly indicate which one or ones of said set of bus widths are available on the card. The system according to the present invention is primarily characterized in that the card is provided with one or more indicators which are arranged to indirectly indicate, which one or ones of said set of bus widths are available on the card. The electronic device according to the present invention is primarily characterized in that the detector also comprises means for determining the value of one or more indicators formed on the card, which indicator is arranged to indirectly indicate which one or ones of said set of bus widths are available on the card. The card according to the present invention is primarily characterized in that the card is provided with one or more indicators which are

arranged to indirectly indicate, which one or ones of said set of bus widths are available on the card.

Considerable advantages are achieved by the present invention. By means of the arrangement according to the invention, the bus widths supported by the card can be determined in the electronic device without the need to store this information as such on the card, wherein the register capacity of the card is saved for another purpose. Furthermore, the detection is also faster than the use of different initialization commands in the detection of the bus width.

In the following, the invention will be described in more detail with reference to the appended drawings, in which

Fig. 1 shows an electronic device and a card according to a first advantageous embodiment of the invention in a reduced block chart,

Fig. 2 illustrates the signalling between the electronic device and the card in connection with the method according to the first advantageous embodiment of the invention,

Fig. 3 shows an electronic device and a card according to a second advantageous embodiment of the invention in a reduced block chart, and

Fig. 4 illustrates the signalling between the electronic device and the card in connection with the method according to the second advantageous embodiment of the invention.

In the following description of an advantageous embodiment of the invention, the electronic device will be exemplified with a wireless terminal 1, but it will be obvious that the invention is not limited to be used in such terminals only. Furthermore, the peripheral device will be exemplified with a card-like peripheral device, wherein the peripheral device connection of the peripheral device 1 will be called a card con-

nection below. However, the invention is not limited solely to card-like peripheral devices, but the present invention can also be applied in connection with other peripheral devices in which one or more buses are used for connecting it to the electronic device 1. The terminal 1 comprises a processor 2, a memory 3, which may also comprise several different memory blocks, such as a read only memory (ROM) and a random access memory (RAM). Furthermore, a part of the memory can be a non-volatile memory, such as an EEPROM memory, in a way known as such. Furthermore, the terminal preferably comprises a display 4, a keypad 5, and audio means, such as an earpiece and/or a speaker 6 and a microphone 7. Preferably, the terminal 1 also comprises communication means, such as a transmitter 9 and a receiver 8, for data transmission between the terminal 1 and a communication network 10. These communication means 8, 9 are preferably intended for wireless communication, wherein the communication network 10 comprises a wireless communication network, such as a mobile communication network, a wireless local area network, or the like. The terminal also comprises a card connection 11 for connecting one or more cards 12 to the terminal 1.

In the card connection 11, there is preferably a card controller 13 for controlling the functions necessary for using the card 12 connected to the card connection. Furthermore, the card connection is provided with the necessary buses 14a, 14b, by means of which *e.g.* commands and data can be transferred between the card 12 and the terminal 1. If more than one card can be simultaneously connected to the card connection 11, the card connection 11 is provided with several connectors (not shown), to which the buses 14a, 14b are coupled.

In this advantageous embodiment, the card 12 is implemented in such a way that several widths of the data bus 14a can be used in connection with it. In this context, the bus widths of 1, 4 and 8 bits are used as non-restrictive examples of the bus widths. However, it will be obvious that the invention is not limited solely to the bus widths mentioned here. Furthermore, it should be mentioned in this context that the invention can also be applied in connection with other buses than the data bus.

For example, in connection with cards provided with an address bus, various alternative widths can be set for the address bus, if necessary, of which one is selected for use each time. Also, the control bus 14b can, in some cases, be implemented to have a selectable width according to the invention.

In various applications, the card 12 to be connected to the terminal 1 may be very different, and the present invention is not limited to any specific card. Some non-restrictive examples to be mentioned of such cards 13 include memory cards, such as a memory card complying with the specifications of a MultiMediaCard or a memory card complying with the specifications of an SD Memory Card, communication cards, such as cards comprising mobile communication functions, *etc.* In the use of the various card types, the terminal card connection 11 may vary, but a person skilled in the art will be able to apply the invention in also other types of cards and card connections on the basis of the following example applications. In the system according to an advantageous embodiment of the invention, shown in Fig. 1, the card is a memory card complying with the MultiMediaCard specifications, and the data transfer between the card 12 and the card controller 13 of the terminal 1 takes place in serial format according to the MultiMediaCard specifications. In this case, the card connection 11 is preferably provided with at least a data bus 14a and a control bus 14b, as well as one or more ground lines 14c (Gnd) set to the zero potential, and one or more operating voltage lines 14d (Vcc). The control bus 14b preferably comprises a command line CMD, a clock line CLK, and a chip select line CS. Pull-up resistances R are preferably coupled to the lines of the data bus 14a, of which only one resistance is shown in Fig. 1 for clarity.

Figure 1 also shows the internal structure of one such card 12 in a reduced block chart. The card 12 comprises a bus connection block 15, via which the buses 14a, 14b are connected to the card 12. The card is preferably also provided with a control unit 16 for controlling the functions of the card 12. Preferably, the card 12 also comprises internal registers 17 for storing some data. Since the card 12 used here as an

example is a memory card, the card 12 is also provided with a memory 18 which can be a read only memory and/or a random access memory. The memory 18 may comprise one or more memory types, such as a dynamic memory (DRAM), a static memory (SRAM), or a non-volatile memory (*e.g.* EEPROM, Flash). The memory 18 may also be implemented wholly or partly as a magnetic and/or optic memory, of which non-restrictive examples include a fixed disk, a CD-ROM, and a digital versatile disk. Furthermore, the card 12 preferably comprises a clock circuit for generating clock signals required in the operation of the different functional blocks of the card 12 in a way known as such.

In the method according to a first advantageous embodiment of the invention, the bus width of the card is preferably detected in the following way. The procedure of the method is also shown as a signalling chart in Fig. 2. The card 12 comprises some registers 17 containing stored information about the properties of the card 12. One such register is a speed register SP containing stored information about the maximum clock frequency supported by the card. After the operating voltages have been turned on, the card 12 performs initialization of the operating mode (block 201 in Fig. 2), after which the card 12 is in a given mode. At this stage, the width of the data bus 14a is set in the terminal 1 to a default value, which in this advantageous embodiment is the 1-bit data bus (block 202). After this, the controller 13 transmits a command to read the speed register SP on the command line CMD to the card (arrow 203). The card 12 receives the command via the bus connection 15, from which the command is transmitted to the controller 16 on the card. The controller 16 interprets the command and retrieves the value contained in the speed register SP (block 204) and transmits it via the bus connection 15 to the terminal 1 (arrow 205). In the terminal 1, the controller 13 interprets the received data and compares it with determined reference values (block 206). Let us assume here that the alternatives are 20 MHz, 25 MHz and 50 MHz. Furthermore, let us assume that if the maximum speed complies with the first alternative (20 MHz), the data bus width of the card is 1 bit. If the maximum speed complies with the second alternative (25 MHz) or the third alternative (50 MHz), the data bus width can be set to either 1, 4 or 8 bits on the

card 12. Thus, if the speed register value is the first alternative, the operation can, in this embodiment, be continued without changing the bus width, because the default value is the 1-bit bus. However, if the speed register value is the second or the third alternative, the bus width can be selected to one of the alternatives 1, 4 or 8 bits (block 207). Thus, when faster data transmission is desired, the bus with of 4 bits or 8 bits is selected for the data bus. To implement this, the controller 13 transmits a bus width set command (*e.g.* Switch) to the card 12, whereby the selected bus width is set as the new bus width, that is, 4 or 8 bits in this example (arrow 208). For each bus width, it is possible to form a separate command, or the bus width set command is provided with information about the bus width to be set on the card. On the card, the received command is examined and the bus width is set to comply with the bus width indicated in the command (block 209). After the bus width has been changed to the desired width, the card preferably indicates this in a suitable manner, for example by transmitting an acknowledgement command or the like (arrow 210), or the terminal 1 assumes that the bus width has been set after a given delay, wherein the card 12 does not need to separately inform about the setting of the bus width.

After the bus width has been set, the selected bus width can also be used in the terminal. For example, if the width of the data bus 14a has been changed to 4 bits, information can be transmitted in arrays of four bits between the terminal 1 and the card 12. After the change of the bus width, the card 12 and/or the terminal 1 may need to make internal changes in the data transmitted on the data bus 14a, such as to convert 4-bit data into 1-bit or 8-bit data for further processing. However, this is prior art known by anyone skilled in the art, wherein it is not necessary to describe it in more detail in this context. It should also be mentioned that in some applications, it is not necessary to write data on all the lines of the data bus simultaneously, but the writing on the different lines may take place within given timing tolerances, for example in sequential order.

The above-mentioned values of the speed register, 20 MHz, 25 MHz and 50 MHz, are only some examples. For example, an ordinary card complying with the MultiMediaCard™ specifications supports only one bus width (1 bit), and the maximum clock frequency is 20 MHz. There are also faster cards under development (HSMMC, High Speed Multi-MediaCard™), in which the maximum clock frequency may be 25 MHz or 50 MHz. In both of these cases, the data bus width may be 1, 4 or 8 bits.

In connection with the first advantageous embodiment of the invention, it is also possible to use another register than said speed register to determine the bus widths supported by the card 12. For example, information about the card version may be stored on the card 12, wherein the terminal 1 comprises information about the supported bus widths corresponding to the different versions. In this alternative, the terminal 1 reads the value of the register containing such version information from the card 12. In a card complying with the Multi-MediaCard™ specifications, the version may be, at the date of filing of the present application, for example 3.1 or 3.2 (or smaller). In cards 12 supporting fast data transmission (and bus widths greater than one bit), the version data is preferably greater than said 3.2. In general, if there are various bus width alternatives for the card, the version data stored on the card can be used to find out the bus width supported by the card. Thus, the terminal 1 comprises stored information about these versions and the bus widths supported by each version. However, also in this alternative, information about the bus width does not need to be stored on the card.

Yet another alternative for the above-presented registers is that information about the card type is stored on the card 12. Such type data may be, for example, information about whether it is a fast card or a slow card. A slow card (*e.g.* maximum clock frequency 20 MHz) will only support one bus width. In a corresponding manner, a fast card (maximum clock frequency *e.g.* greater than 20 MHz) will support several bus widths. Other type data may include information about the operating voltage (low/high voltage) or information about the physical

size of the card (full-size/half card). In this embodiment, the necessary quantity of bits of *e.g.* the CSD register can be used in the storage of the type data.

If necessary, the above-presented different alternatives can be combined, if the data of one register does not identify the bus width supported by the card 12 with sufficient certainty. In this case, the terminal 1 comprises information about the compliance of the different combinations and bus widths.

Figure 3 shows the coupling of the electronic device 1 according to another advantageous embodiment of the invention and a card 12 in a reduced manner. In a corresponding manner, Fig. 4 shows an advantageous example of the signalling to be used in the method according to this embodiment in connection with the determination of the bus width. In this embodiment, the card 12 indicates the bus width supported by it via one or several lines. In this non-restrictive example, a fourth data bus DAT3 is used, but also other lines can be used. Let us assume that either a default bus width or another bus width can be selected. Thus, in the method according to this embodiment, the bus width of the card is detected preferably in the following way. At the boot step, in connection with the initialization of a mode, or substantially after the same, the card 12 sets the state of the fourth data bus DAT3 in a first logical value, for example in the 0 state (401), if the card 12 supports also other bus widths than the default bus width. This can be provided *e.g.* in such a way that the controller 16 closes the switch 19, wherein the fourth data bus DAT3 is coupled to the ground potential. The state of the fourth data bus is thus in the logical 0 state. The terminal 1 reads the state of this fourth data bus DAT3 (402), and if it is in said logical 0 state, the data bus width can be set in the terminal 1 to another value than the default bus width (403). In a corresponding manner, if the card 12 does not set the state of the fourth data bus DAT3 to this first logical value, it is assumed that the card 12 only supports the default bus width. The pull-up resistance R3 of the data line DAT3 is used to provide that if such function of indicating the support bus widths is not implemented on the card 12, the state of the data line

DAT3 in the terminal 1 is in the logical 1 state, which is consequently interpreted in this case as the state corresponding to the default bus width.

After the terminal 1 has received information about the bus widths supported by the card 12, a command to set the bus width is transmitted to the card (404), if several different bus widths are available in the card 12. After the card 12 has received this command, the controller 16 of the card 12 opens the switch 19, after which the fourth data bus is available for data transmission (405).

Consequently, the above-described example comprises two alternatives for the bus widths supported by the card. If there are more alternatives, several lines can be used, such as a second and a third data line, wherein the combination of the states of these lines indicates the bus widths supported by the card 12.

Although only the 1-bit bus or the set of three alternatives (1/4/8 bits) was presented above as the bus width alternatives supported by the card 12, the invention can also be applied in the case of other bus widths and several different alternatives.

The above-mentioned functions for determining the bus width can be implemented primarily by software preferably in the controller 13, the processor 2, or both. However, it will be obvious that also other implementation alternatives are possible to apply the above-mentioned methods in the electronic device 1.

The present invention is not limited solely to the above-presented embodiments, but it can be modified within the scope of the appended claims.

Claims:

1. A method for detecting the bus width of a peripheral device (12) connected to an electronic device (1), wherein at least one bus width from a determined set of bus widths is available in the peripheral device (12), **characterized** in that for detecting the bus widths available in the peripheral device (12), one or more indicators (17, DAT3) formed in the peripheral device (12) are used, which indirectly indicate which one or ones of said set of bus widths are available in the peripheral device (12).

2. The method according to claim 1, **characterized** in that reference data is stored in the electronic device (1) about at least one bus width available in the peripheral device (12) and corresponding to said indicator value.

3. The method according to claim 2, **characterized** in that said indicator used is information stored in the peripheral device (12) and indicating indirectly, which one or ones of said set of bus widths are available in the peripheral device (12).

4. The method according to claim 3, **characterized** in that said data stored in the peripheral device (12) is information about the maximum clock frequency available in the peripheral device (12).

5. The method according to claim 3 or 4, **characterized** in that at least a fast peripheral device and a slow peripheral device are defined, wherein said information stored in the peripheral device (12) is information about whether the peripheral device (12) is fast or slow.

6. The method according to claim 3, **characterized** in that said data stored in the peripheral device (12) is information about the version of the peripheral device (12).

7. The method according to any of the claims 2 to 6, **characterized** in that at least the following steps are taken in the method:

- a request step (203), in which a request is transmitted from the electronic device to the peripheral device (12) to transmit the value of said indicator to the electronic device (1),
- a reply step (204, 205), in which said indicator value is transmitted from the peripheral device (12) to the electronic device (1),
- an identification step (206), in which said indicator value is compared with at least one reference value stored in the electronic device (1),
- a selection step (207) for selecting one bus width available in the peripheral device, and
- a setting step (208, 209) for setting the selected bus width for the peripheral device (12).

8. The method according to claim 1, **characterized** in that at least one connection line (14a–14d) is formed between the electronic device and the peripheral device, and that said indicator used is at least one said connection line (DAT3).

9. The method according to claim 8, **characterized** in that at least the following steps are taken in the method:

- an initialization step (401), in which the value of said at least one connection line (DAT3) is set to correspond indirectly to the bus widths available in the peripheral device (12),
- a detection step (402), in which the electronic device (1) examines the state of said at least one connection line (DAT3) and compares the state of said connection line (DAT3) with at least one reference value stored in the electronic device (1),
- a selection step (403) for selecting one bus width available in the peripheral device, and
- a setting step (404) for setting the selected bus width for the peripheral device (12).

10. A system comprising an electronic device (1), a peripheral device (12) which can be connected to the electronic device (1) and in which at least one bus width is arranged to be used from a defined set of bus widths, and which system comprises a bus width detector (13) for

detecting at least one bus width available in the peripheral device (12) connected to the electronic device (1), **characterized** in that the peripheral device (12) is provided with one or more indicators (17, DAT3), which are indirectly arranged to indicate which one or ones from said set of bus widths are available in the peripheral device (12).

11. An electronic device (1) comprising a bus width detector (11) for detecting the bus width of a peripheral device (12) connected to the electronic device (1), in which peripheral device (12) at least one bus width is arranged to be used from a defined set of bus widths, **characterized** in that the detector also comprises means (CMD, DAT3) for determining the value of one or more indicators (17, DAT3) formed in the peripheral device (12), which indicator (17, DAT3) is arranged to indirectly indicate which one or ones of said set of bus widths are available in the peripheral device (12).

12. The electronic device according to claim 11, **characterized** in that reference data is stored in the electronic device (1) about at least one bus widths available in the peripheral device (12) and corresponding to said indicator value.

13. The electronic device (1) according to claim 12, **characterized** in that said indicator arranged to be used is information stored in the peripheral device (12) and indicating indirectly, which one or ones of said set of bus widths are available in the peripheral device (12).

14. The electronic device (1) according to claim 13, **characterized** in that at least one connection line (14a–14d) is formed between the electronic device and the peripheral device, and that said indicator arranged to be used is at least one said connection line (DAT3).

15. The electronic device (1) according to claim 14, **characterized** in that said detector comprises means for examining the value of said connection line (DAT3).

16. A peripheral device (12) which can be connected to an electronic device (1) comprising a bus width detector (11) for detecting the bus width of the peripheral device (12) connected to the electronic device, and in which peripheral device (12) at least one bus width from a defined set of bus widths is arranged to be used, **characterized** in that the peripheral device (12) is provided with one or more indicators (17, DAT3) which are arranged to indirectly indicate which one or ones of said set of bus widths are available in the peripheral device (12).

17. The peripheral device (12) according to claim 16, **characterized** in that information about the maximum clock frequency available in the peripheral device (12) is stored in the peripheral device (12).

18. The peripheral device (12) according to claim 16 or 17, **characterized** in that at least a fast peripheral device and a slow peripheral device have been defined, wherein information about whether the peripheral device (12) is fast or slow is stored in the peripheral device (12).

19. The peripheral device (12) according to claim 16, 17 or 18, **characterized** in that information about version of the peripheral device (12) is stored in the peripheral device (12).

20. The peripheral device (12) according to claim 16, **characterized** in that it comprises at least one connection line (14a–14d), and means (16, 19) for setting said connection line in a value which indirectly corresponds to the bus widths available in the peripheral device (12).

21. The peripheral device (12) according to any of the claims 16 to 20, **characterized** in that it is a memory card.

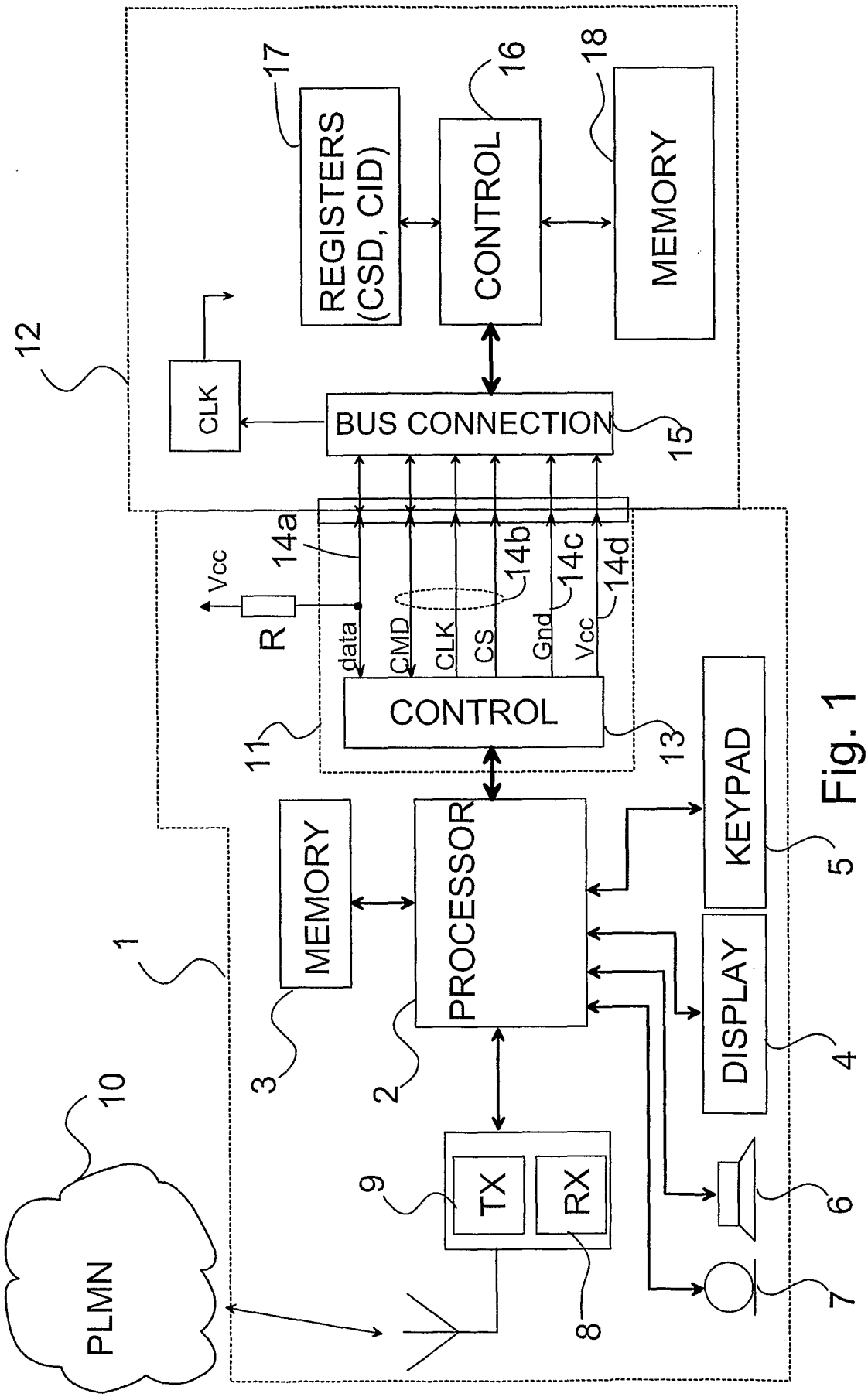

PLMN
10
1
MEMORY
3
PROCESSOR
2
KEYPAD
5
DISPLAY
4
TX
RX
9
8
6
7
12
CLK
BUS CONNECTION
15
REGISTERS (CSD, CID)
17
CONTROL
16
MEMORY
18
Vcc
R
14a
data
CMD
CLK
CS
Gnd
Vcc
14b
14c
14d
CONTROL
11
13

Fig. 1

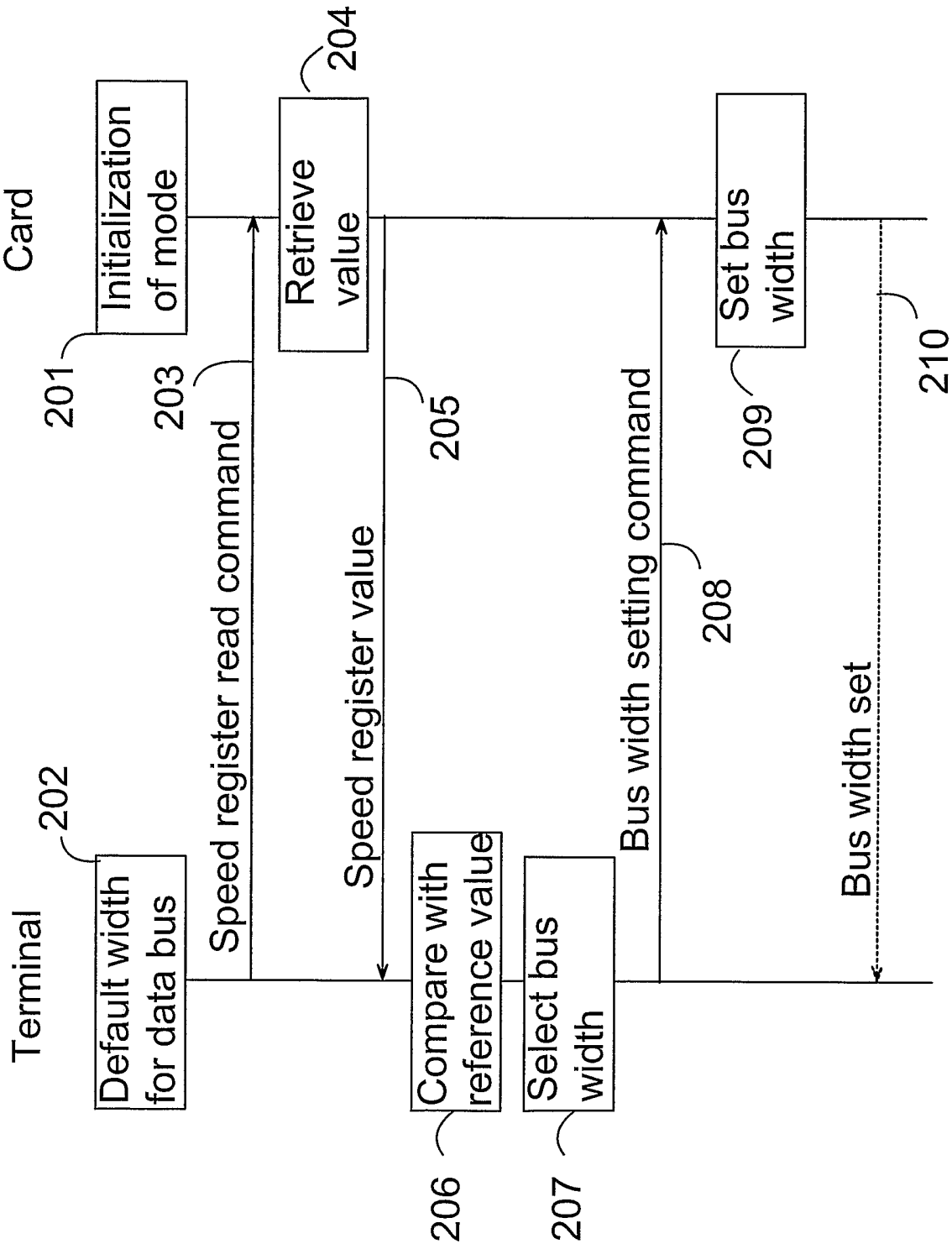

Terminal
Card
Default width for data bus
202
Initialization of mode
201
Speed register read command
203
Retrieve value
204
Speed register value
205
Compare with reference value
206
Select bus width
207
Bus width setting command
208
Set bus width
209
Bus width set
210

Fig. 2

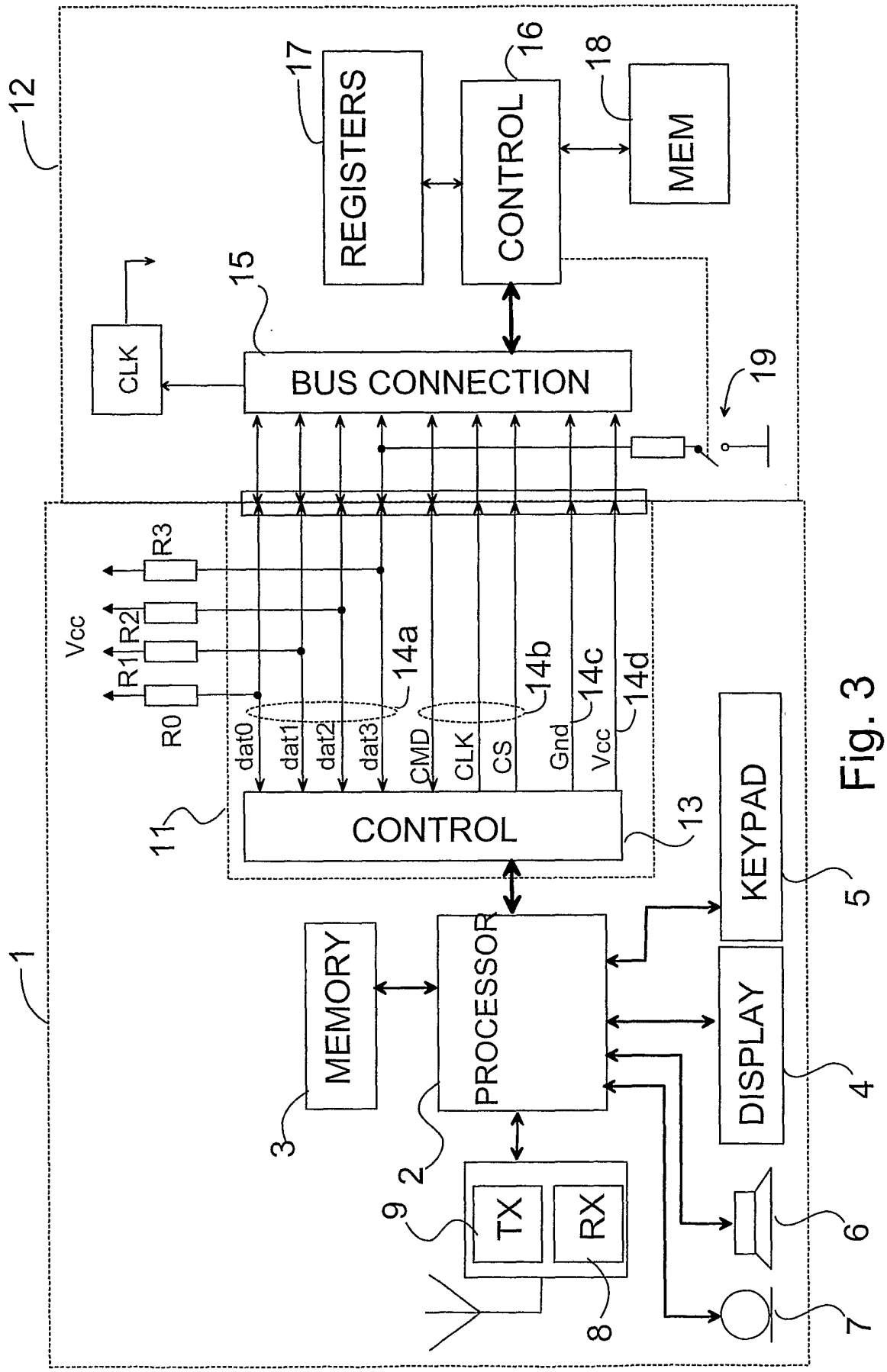

12
17
REGISTERS
16
CONTROL
18
MEM
15
CLK
BUS CONNECTION
19
R3
R2
R1
R0
Vcc
14a
14b
14c
14d
dat0
dat1
dat2
dat3
CMD
CLK
CS
Gnd
Vcc
11
CONTROL
13
KEYPAD
5
1
MEMORY
PROCESSOR
DISPLAY
4
3
2
9
TX
RX
6
8
7

Fig. 3

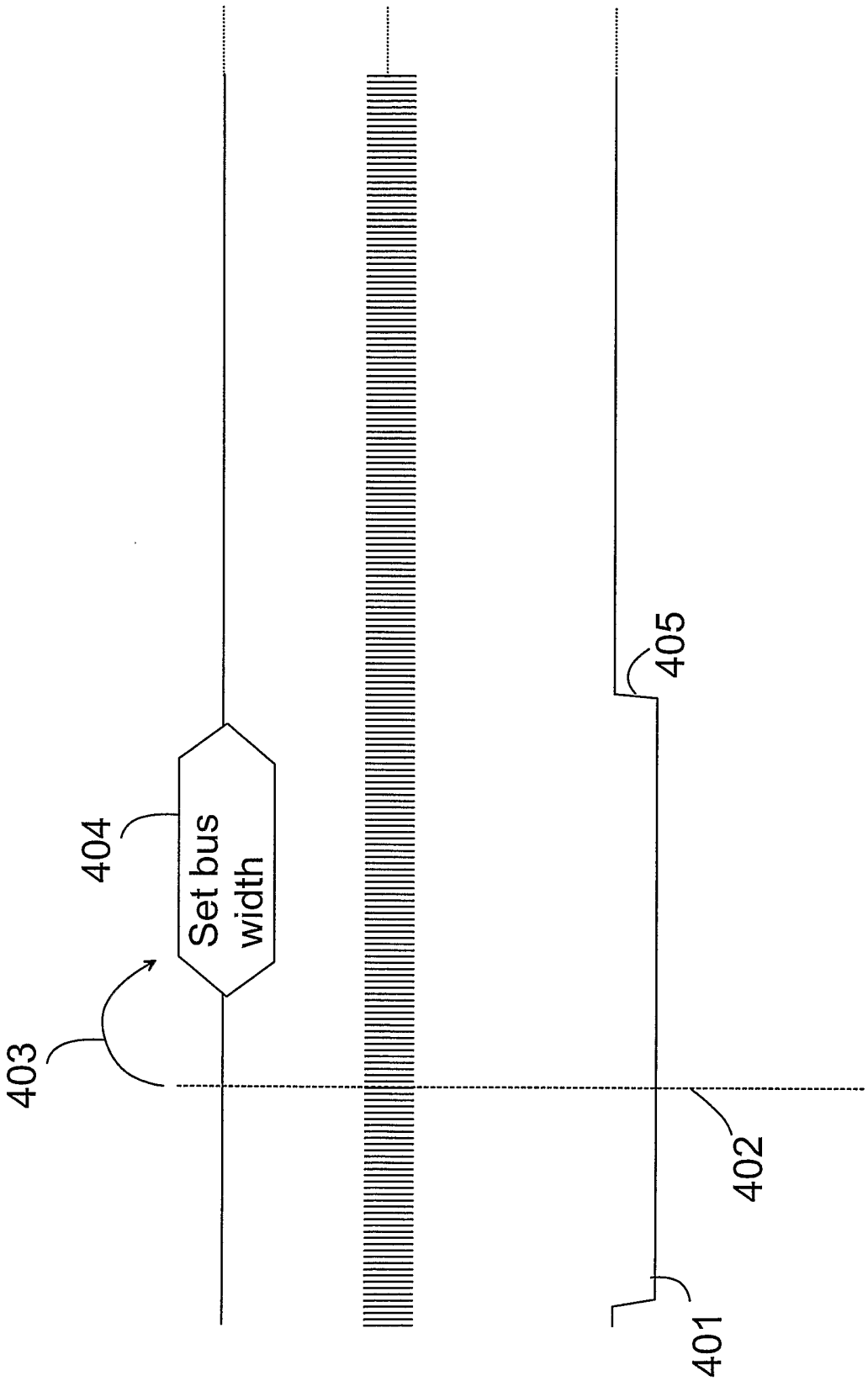


Fig. 4

INTERNATIONAL SEARCH REPORT

International application No.
PCT/FI 2003/000908

A. CLASSIFICATION OF SUBJECT MATTER

IPC7: G06F 13/38
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC7: G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

SE,DK,FI,NO classes as above

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-INTERNAL, WPI DATA, PAJ, NPL

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	DATABASE WPI Week 199917 Derwent Publications Ltd, London, GB; Class G06F 12/04 & JP 11 045206 A (CASIO COMPUTER CO LTD), 16 February 1999 (1999-02-16) abstract ---	1-21
X	US 5553244 A (NORCROSS, T M ET AL), 3 Sept 1996 (03.09.1996), column 1, line 27 - line 41; column 4, line 3 - line 18; column 7, line 49 - line 56, abstract ---	1-21
X	EP 1132824 A2 (KK TOSHIBA), 12 Sept 2001 (12.09.2001), abstract, [0045]-[0050] ---	1-21

[X] Further documents are listed in the continuation of Box C. [X] See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance: the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance: the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
11 February 2004	17 -02- 2004
Name and mailing address of the ISA/ Swedish Patent Office Box 5055, S-102 42 STOCKHOLM Facsimile No. +46 8 666 02 86	Authorized officer Nina Ödling /LR Telephone No. +46 8 782 25 00

INTERNATIONAL SEARCH REPORT

International application No.
PCT/FI 2003/000908

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
P,X	DATABASE WPI Week 200361 Derwent Publications LTD, London, GB; Class G06F 12/04, AN 2003-642257 &JP 2003-242 101 A (MINOLTA CAMERA KK) 29 August 2003 (2003-08-29) abstract --	1-21
A	WO 0215020 A2 (SANDISK CORP), 21 February 2002 (21.02.2002), abstract --	1-21
A	WO 9319424 A1 (SEIKO EPSON CORP), 30 Sept 1993 (30.09.1993), claim 1, abstract --	1-21
A	EP 0624846 A2 (SONY CORP), 17 November 1994 (17.11.1994), abstract -- --------	1-21

US	5553244	A	03/09/1996	EP	0597601	A	18/05/1994
				JP	7073101	A	17/03/1995
EP	1132824	A2	12/09/2001	JP	2001256174	A	21/09/2001
				US	2001021956	A	13/09/2001
WO	0215020	A2	21/02/2002	AU	8649501	A	25/02/2002
				CN	1455897	T	12/11/2003
				DE	1309919	T	27/11/2003
				EP	1309919	A	14/05/2003
WO	9319424	A1	30/09/1993	JP	7504773	T	25/05/1995
				US	5594877	A	14/01/1997
				US	5887148	A	23/03/1999
				US	6047348	A	04/04/2000
EP	0624846	A2	17/11/1994	DE	69432063	D,T	30/10/2003
				EP	1197871	A	17/04/2002
				JP	6324990	A	25/11/1994
				TW	535941	Y	00/00/0000
				US	5682555	A	28/10/1997
				US	5935428	A	10/08/1999