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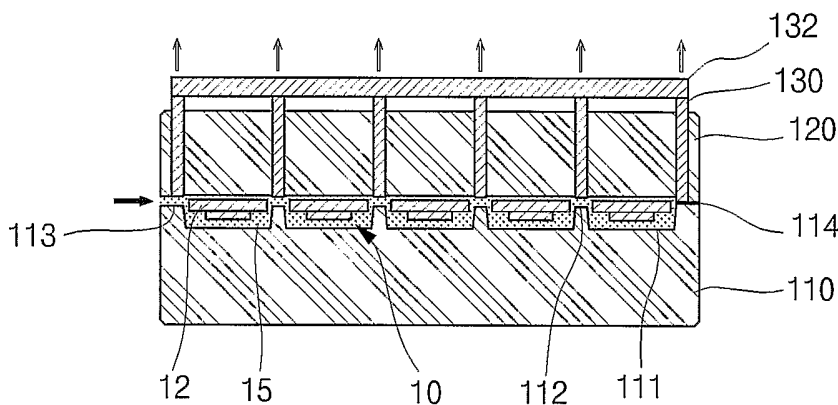
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(54) Title: MOLD FOR MANUFACTURING SEMICONDUCTOR DEVICE AND SEMICONDUCTOR DEVICE MANUFACTURED USING THE SAME



(57) Abstract: Disclosed is a mold for manufacturing semiconductor devices and a semiconductor manufactured by using the mold. The mold includes: a first mold having plural cavities with a predetermined depth, the plural cavities being arranged in one or more rows in such a manner as to be spaced from each other in each row, so that plural semiconductor devices are positioned in one or more rows, the plural cavities in each row being communicated with each other through through-gates, which are shallower than the cavities; a second mold which comes into close contact with the first mold and allows encapsulant to sequentially flow into all the cavities through the through-gates in such a manner as to surround the semiconductor devices positioned within the cavities; and plural gate lock blocks installed through the second mold at the areas corresponding to the through-gates of the first mold. The gate lock blocks open the through-gates during an encapsulating process and close the through-gates or reduce the open spaces of the through-gates after the encapsulating process is completed.

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Description

MOLD FOR MANUFACTURING SEMICONDUCTOR DEVICE AND SEMICONDUCTOR DEVICE MANUFACTURED USING THE SAME

Technical Field

- [1] The present invention relates to a mold for manufacturing semiconductor devices and a semiconductor device manufactured using the same. In particular, the present invention relates to a mold for manufacturing a semiconductor device, which is capable of saving the quantity of encapsulant to be used for manufacturing semiconductor device, suppressing the occurrence of voids in the encapsulant and the non-filling of the encapsulant, and preventing various defects from being caused in a trimming or sawing process, and a semiconductor device manufactured using such a mold.

[2]

Background Art

- [3] In general, a semiconductor device adapted to be capable of being mounted on a mother board or a main board includes a lead frame (or a circuit board), a semiconductor die mounted on the lead frame, plural conductive wires (or solder) for electrically interconnecting the lead frame and the semiconductor die, and an encapsulation part which is formed by encapsulant for encapsulating the lead frame, the semiconductor die, the conductive wires, etc. so as to protect them from the external environment.
- [4] In addition, such a semiconductor device is manufactured through a method including: a die-bonding process for mounting plural semiconductor dies on an array of plural lead frames; a wire-bonding process for electrically interconnecting the semiconductor dies and the lead frames, respectively; an encapsulating process for encapsulating the lead frames, the semiconductor dies, and the wires with encapsulant; and a trimming or sawing process for separating each semiconductor device from the lead frame array as a unit chip. That is, if only one semiconductor device is manufactured in each process, the yield is too low. Therefore, a large number of semiconductor devices are simultaneously manufactured by using an array of lead frames arranged in a form of strips.
- [5] FIG. 1 is a top plan view showing a number of semiconductor devices in a state of being encapsulated by a conventional mold for manufacturing semiconductor devices, and FIG. 2 is an enlarged top plan view showing a part of FIG. 1a.
- [6] As shown in the drawings, an array of plural lead frames 12' are provided in a strip

form, and each lead frame is formed with an encapsulation part 15' in a predetermined shape. Typically, one lead frame 12' and one encapsulation part 15' may be defined as a semiconductor device 10'.

- [7] Plural encapsulation parts 15' which are spaced from each other, may be arranged in two rows (or in more than two rows), and a small runner encapsulant 23' extends between the two rows of the encapsulation parts 15' wherein the small runner encapsulant part 23' which corresponds to a smaller of a mold. That is, the small runner encapsulant part 23' is formed as the encapsulant is cured in the small runner of a mold. In addition, each of the encapsulation parts 15' is connected to the small runner encapsulant part 23' via a gate encapsulant part 24' which is formed as the encapsulant is cured in a gate of a mold, wherein the gate encapsulant part 24' is perpendicular to a corresponding encapsulation part 15'. The encapsulation parts 15' are formed by cavities, which are provided in the mold, the cavities, the gates, and the small runner are connected with each other. In the drawings, reference numeral 21' denotes a ram pot encapsulant part, which corresponds to a ram pot of the mold, and 22' denotes a large runner encapsulant part, which corresponds to a large runner of the mold. In FIG. 1, arrows indicate the flow directions of encapsulant, wherein the encapsulant arrives at each of the gates and cavities through the ram pot, the large runner and the small runners.
- [8] After the encapsulating process, the encapsulation parts (that is, the semiconductor devices) are separated as unit chips through the trimming or sawing process. In addition, in such a trimming or sawing process, the gate encapsulant parts 24' as well as the lead frames are cut by a punch or a sawing blade. Therefore, each of the finished semiconductor devices has a gate encapsulant part cutting trace (or an encapsulant part trace), which remains on each of the encapsulation parts 15'.
- [9] Meanwhile, according to the prior art, it is necessary to remove all the small runner encapsulant parts and the gate encapsulant parts as well as the ram pot encapsulant part and the large runner encapsulant part after an encapsulating process. Consequently, there is a problem in that the encapsulant is excessively used. Once cured, the encapsulant cannot be melt for reuse, because such encapsulant is typically formed from a thermosetting resin. Therefore, all the above-mentioned encapsulant parts have been wasted in the prior art.
- [10] In addition, in the prior art, because the small runners are oriented perpendicular to the gates, violent swirling of the encapsulant is occurred within the cavities, by which the encapsulating process is eventually executed. As a result, the encapsulation parts may be formed in a state in which the cavities in the mold are not insufficiently filled with encapsulant or a number of voids may be formed in the encapsulant. Furthermore, such voids subsequently absorb moisture or the like, whereby the moisture may be

vaporized and cause the encapsulation part to be fractured when such a semiconductor device is laid under a high temperature condition.

[11] In addition, the prior art has a problem in that a life span of a punch or a sawing blade which is used in a trimming or sawing process is reduced and the encapsulation part enclosing the semiconductor dies may also be fractured in the trimming or sawing process because the punch or sawing blade should remove the gate encapsulant parts as well as the lead frames.

[12]

[13] **Disclosure of the Invention**

[14] Accordingly, the present invention has been made to solve the above-mentioned problems occurring in the prior art, and an object of the present invention is to provide a mold for manufacturing semiconductor devices, which can reduce the quantity of encapsulant to be used in manufacturing semiconductor devices, suppress the occurrence of voids in the encapsulation parts of the semiconductor devices and non-filling of encapsulant, and prevent various defects from being formed during a sawing or trimming process, and a semiconductor device manufactured by using the mold.

[15] In order to accomplish these objects, there is provided a mold for manufacturing semiconductor devices including a first mold having plural cavities with a predetermined depth, the plural cavities being arranged in one or more rows in such a manner as to be spaced from each other in each row, so that plural semiconductor devices are positioned in one or more rows, the plural cavities in each row being communicated with each other through through-gates, which are shallower than the cavities; and a second mold which comes into close contact with the first mold and allows encapsulant to sequentially flow into all the cavities through the through-gates in such a manner as to surround the semiconductor devices positioned within the cavities.

[16] The width of the through-gates formed in the first mold may be equal to or narrower than that of the cavities.

[17] Each of the through-gates may be communicated with an end portion or a central portion of a side of a corresponding cavity.

[18] In order to accomplish these objects, there is provided another mold for manufacturing semiconductor devices including a first mold having plural cavities with a predetermined depth, the plural cavities being arranged in one or more rows in such a manner as to be spaced from each other in each row, so that plural semiconductor devices are positioned in one or more rows, the plural cavities in each row being communicated with each other through through-gates, which are shallower than the cavities; a second mold which comes into close contact with the first mold and allows encapsulant to sequentially flow into all the cavities through the through-gates in such

a manner as to surround the semiconductor devices positioned within the cavities; and plural gate lock blocks installed through the second mold at the areas corresponding to the through-gates of the first mold, wherein the gate lock blocks open the through-gates during an encapsulating process and close the through-gates or reduce the open spaces of the through-gates after the encapsulating process is completed.

[19] The width of the gate lock blocks may be same as that of the through-gates, and the width of the through-gates is equal to or smaller than that of the cavities.

[20] Each of the through-gates may be communicated with an end portion or a central portion of a side of a corresponding cavity.

[21] The mold may further include a block moving member on the gate lock blocks so as to linearly reciprocate the gate lock blocks.

[22] The block moving member may be any one selected from a pneumatic cylinder, a hydraulic cylinder, and a motor.

[23] In order to accomplish these objects, there is provided another mold for manufacturing semiconductor devices including a first mold having a cavity with a predetermined depth, at least one gate of a predetermined depth being communicated with the cavity; a second mold which comes into close contact with the first mold and allows encapsulant to sequentially flow into the cavity through the gate of the first mold in such a manner as to surround all the semiconductor devices positioned within the cavity; and a split block installed through the first mold to the cavity so as to allow each of the semiconductor devices to be formed with a separate encapsulation part, wherein the split block completely opens the cavity so that encapsulant can smoothly flows during an encapsulating process, and comes into contact with or approaches each of the semiconductor devices so that the encapsulation parts of respective semiconductor devices could be separated from each other.

[24] The split block may include plural crosswise and longitudinal partitions which are crossed with each other.

[25] One encapsulation part may be formed in one area surrounded by two crosswise partitions and two longitudinal partitions.

[26] The mold may further include a block moving member installed on the split block so as to linearly reciprocate the split block.

[27] The block moving member may be any one selected from a pneumatic cylinder, a hydraulic cylinder, and a motor.

[28] In order to accomplish these objects, there is provided a semiconductor device including a semiconductor die; a lead frame, the semiconductor die being mounted on the lead frame and electrically connected with the lead frame; and an encapsulation part formed by encapsulating the semiconductor die and the lead frame with encapsulant, wherein the encapsulation part is formed, on its surface, with at least one en-

capsulant cutting trace corresponding to an inlet or an outlet of the encapsulant during an encapsulating process.

[29] The encapsulation part may include a first surface, which is flat and has a predetermined area, a second surface, which is positioned opposite to the first surface, and four third surfaces, which are arranged in a rectangular shape along and between the edges of the first and second surfaces, the third surfaces being narrower than either the first surface or the third surface.

[30] The encapsulant cutting traces may be symmetrically formed on two third surfaces, which are positioned opposite and parallel to each other, among the four third surfaces.

[31] The encapsulant cutting traces may be asymmetrically formed on two third surfaces, which are positioned opposite and parallel to each other, among the four third surfaces.

[32] The lead frame may be projected outwardly from any one of the four third surfaces by a predetermined length.

[33] The encapsulant cutting traces may be symmetrically formed on the two third surfaces which are positioned opposite and parallel to each other and perpendicular to the third surface, from which the lead frame is projected.

[34] The encapsulant cutting traces may be asymmetrically formed on the two third surfaces which are positioned opposite and parallel to each other and perpendicular to the third surface, from which the lead frame is projected.

[35] Each of the encapsulant cutting traces may be projected from a corresponding third surface of the encapsulation part by a predetermined length, recessed in the corresponding third surface by a predetermined depth, or flush with the corresponding third surface.

[36] The encapsulant cutting traces may be same with or smaller than the third surfaces in width.

[37]

Brief Description of the Drawings

[38] The above and other objects, features and advantages of the present invention will be more apparent from the following detailed description taken in conjunction with the accompanying drawings, in which:

[39] FIG. 1 is a top plan view showing an array of semiconductor devices, which are encapsulated by a conventional mold for manufacturing semiconductor devices, and FIG. 2 is an enlarged top plan view of a part of FIG. 1;

[40] FIG. 3 is a top plan view showing an array of semiconductor devices in a state of being encapsulated in a mold for producing semiconductor devices according to the present invention, and FIG. 4 is an enlarged top plan view showing a part of FIG. 3;

- [41] FIGs. 5 and 6 are cross-sectional and longitudinal sectional views showing an array of semiconductor devices in a state of being encapsulated in a mold according to an embodiment of the present invention, and FIG. 7 is a top plan view showing semiconductor devices seated in the mold;
- [42] FIGs. 8, 9 and 10 are cross-sectional, longitudinal sectional, and top plan views showing encapsulation parts in a mold according to another embodiment of the present invention before gate lock blocks are operated, respectively, and FIGs. 11, 12 and 13 are cross-sectional, longitudinal sectional and top plan views showing the encapsulation parts in the mold after the gate lock blocks are operated, respectively;
- [43] FIGs. 14, 15 and 16 are cross-sectional, longitudinal sectional, and top plan views showing the condition of encapsulation parts in a mold according to another embodiment of the present invention before gate lock blocks are operated, respectively, and FIGs. 17, 18 and 19 are cross-sectional, longitudinal sectional, and top plan views showing the condition of encapsulation parts in the mold after the gate lock blocks are operated, respectively;
- [44] FIGs. 20, 21 and 22 are cross-sectional, longitudinal sectional, and top plan views showing the condition of encapsulation parts in a mold according to another embodiment of the present invention before gate lock blocks are operated, respectively, and FIGs. 23, 24 and 25 are cross-sectional, longitudinal sectional, and top plan views showing the condition of encapsulation parts in the mold after operating gate lock blocks are operated, respectively;
- [45] FIGs. 26 and 27 are top plan and cross-sectional views showing the condition of encapsulation parts in a mold according to another embodiment of the present invention before the gate lock blocks of the inventive mold are operated, respectively, and FIGs. 28 and 29 are top plan and cross-sectional views showing the condition of encapsulation parts after the gate lock blocks are operated, respectively;
- [46] FIGs. 30, 31 and 32 are cross-sectional, longitudinal sectional, and top plan views showing the condition of encapsulation parts in a mold according to another embodiment of the present invention before the gate lock blocks of the inventive mold are operated, respectively, and FIGs. 33, 34 and 35 are cross-sectional, longitudinal sectional, and top plan views showing the condition of encapsulation parts after the gate lock blocks are operated, respectively;
- [47] FIG. 36 is a perspective view showing a semiconductor device according to an embodiment of the present invention, which is separated from a lead frame strip;
- [48] FIG. 37 is a top plan view showing the semiconductor device before an encapsulation part is formed, and FIGs. 38 and 39 are cross-sectional views showing the semiconductor device with the encapsulation part;
- [49] FIGs. 40 and 41 are top plan and side views showing various positions where en-

capsulant cutting traces may be formed on an encapsulation part of the inventive semiconductor device;

[50] FIGs. 42 and FIG. 43 show, in enlarged scale, gate lock blocks before and after they are operated, respectively;

[51] FIG. 44 is a perspective view showing a semiconductor device according to an embodiment of the present invention;

[52] FIG. 45 is a perspective view showing a semiconductor device according to another embodiment of the present invention; and

[53] FIG. 46 is a perspective view showing a semiconductor device according to another embodiment of the present invention.

[54]

Best Mode for Carrying Out the Invention

[55] Hereinafter, a preferred embodiment of the present invention will be described with reference to the accompanying drawings. In the following description and drawings, the same reference numerals are used to designate the same or similar components, so that repeated description on the same or similar components will be omitted.

[56] FIG. 3 is a top plan view showing an array of semiconductor devices in a state of being encapsulated in a mold for producing semiconductor devices according to the present invention, and FIG. 4 is an enlarged top plan view showing a part of FIG. 3.

[57] As shown, plural lead frames 12 (or circuit boards) are positioned in a strip form, and each of the lead frames 12 is formed with an encapsulation part 15 with the plural encapsulation parts 15 being spaced from each other. Here, one lead frame 12 and one encapsulation part 15 for encapsulating the lead frame 12 may be defined as a semiconductor device 10.

[58] More particularly, the plural encapsulation parts 15 are spaced from each other and arranged in two rows (they may be arranged in more than two rows). There may be provided a through-gate encapsulant part 24 between two adjacent arranged encapsulation parts 15, wherein the through-gate encapsulant parts 24 correspond to through-gates in a mold. The first encapsulation part 14, into which an encapsulant is firstly introduced, is formed with a gate encapsulant part 23, which is connected with a runner encapsulant part 22. In addition, the runner encapsulant part 22 is connected with a ram pot encapsulant part 21. Of course, the ram pot encapsulant part 21 is formed in correspondence with a ram pot in a mold, the runner encapsulant part 22 is formed in correspondence with a runner in the mold 22, and the through-gate encapsulant part 24 is formed in correspondence with a through-gate in the mold. In addition, the encapsulation parts 15 of the semiconductor devices 10 are formed in correspondence with cavities provided in the mold. In FIG. 3, arrows indicate the flow directions of the

encapsulant. According to the present invention, it can be appreciated that the encapsulant flows into a cavity through a ram part, a runner, a gate and a through-gate. According to the present invention, every other cavity is filled with the encapsulant, which is introduced into the cavity through a predetermined cavity unlike the prior art. That is, one through-gate, which serves as an inlet, and another through-gate, which serves as an outlet are formed with reference to one cavity, and all the cavities are interconnected with each other through such through-gates.

[59] The lead frames 12 encapsulated in this manner and hence the encapsulation parts thereof are separated from each other through the trimming or sawing process (That is, the semiconductor devices 10 are separated from each other as unit chips). As will be described later, if a mold with a gate lock block is employed, only the lead frames 12 are trimmed or sawed in the trimming or sawing process, whereby a life span of a punch for a trimming apparatus or a sawing blade for a sawing apparatus can be substantially increased.

[60] Now, various configurations of molds for obtaining encapsulation parts 15 are described in more detail. Here, for the convenience, the encapsulant and encapsulation parts are all denoted by reference numeral 15.

[61] FIGs. 5 and 6 are cross-sectional and longitudinal sectional views showing an array of semiconductor devices in a state of being encapsulated in a mold according to an embodiment of the present invention, and FIG. 7 is a top plan view showing semiconductor devices seated in the mold.

[62] As shown in FIGs. 5 to 7, the inventive mold includes a first mold 110 and a second mold 120, which is engaged with the first mold 110. The first mold 110 includes plural cavities 111 which are spaced from each other and arranged in rows, wherein the cavities have a predetermined depth so that semiconductor devices can be positioned within the cavities, respectively. The cavities 111 are communicated with each other via through-gates 112, which is shallower than the cavities 111. The second mold 120 comes into close contact with the top of the first mold 110, so that an encapsulant can flow into all the cavities, within which the semiconductor devices 10 are positioned, via the through-gates 112, which are provided in the first mold 110.

[63] Here, the cavities 111 formed in the first mold 110 may be formed substantially in a rectangular shape. In addition, as the through-gates 112 formed in the first mold 110 are shallower than the cavities 111, the through-gates 112 will affect the appearance of the encapsulation parts 15 to be formed later to a minimum. The through-gates 112 formed in the first mold 110 may be narrower than the cavities 111. Although not shown in the drawings, it is natural that the width of the through-gates 112 may be same as that of the cavities 111. In addition, each of the through-gates 112 is communicated with an end of a side of a corresponding cavity 111. Although not shown in

the drawings, it is natural that a through-gate 112 may be communicated with a center of a side of the corresponding cavity 111.

[64] In FIG. 5, thick arrow indicates the flow direction of the encapsulant 15. As shown, the encapsulant 15 fills the first cavity through the first through-gate 112, and then fills the second cavity 112 through the second through-gate 112. Therefore, the flowing path of the encapsulant 15 is not sharply curved from the runner 114 to the gate 113, the swirling of the encapsulant 14 scarcely occurs. Therefore, a finished encapsulation part contains little voids or non-filling areas. In FIG. 5, reference numeral 114 denotes an air vent for discharging air within the cavities to the outside of the mold.

[65] After completing the encapsulating process, a small amount of through-gate encapsulant parts 24 are only formed in the through-gates 112, whereby a massive runner encapsulant part is not formed unlike the prior art. Therefore, it is possible to reduce the quantity of encapsulant 15 to be used.

[66] FIGs. 8, 9, and 10 are cross-sectional, longitudinal sectional, and top plan views showing the condition of encapsulation parts in a mold according to another embodiment of the present invention before gate lock blocks are operated, respectively, and FIGs. 11, 12, and 13 are cross-sectional, longitudinal sectional, and top plan views showing the condition of encapsulation parts in the mold after gate lock blocks are operated, respectively.

[67] As shown in FIGs. 8 to 10, the inventive mold includes a first mold 110, a second mold 120, and plural gate lock blocks.

[68] The first mold 110 has plural cavities 111, each of which has such a depth that a semiconductor device can be positioned within a cavity, wherein the cavities 111 are spaced from each other and arranged in rows. Each of the cavities 111 is communicated with a through-gate of a predetermined depth. At the first through-gate 112, into which the encapsulant 15 is firstly introduced, a gate 113, the length of which is very short, is formed, and the last cavity 111 (the cavity 111 of the right end in the drawing) is formed with an air vent 114 for discharging the air in the cavities to the outside of the mold.

[69] In addition, the second mold 120 comes into close contact with the first mold 110, so that the sealant can be easily introduced into all the cavities 111, within which the semiconductor devices 10 are positioned, through the through-gates 112 formed in the first mold 110.

[70] The gate lock blocks 130 are positioned through the second mold 120 in such a manner as to correspond with the through-gates 112 of the first mold 110. In addition, the top ends of gate locks block 130 are provided with a block moving member 132 so as to vertically move the gate lock blocks 130. Such a block moving member 132 may be any one selected from a pneumatic cylinder, a hydraulic cylinder, a motor and the

like. However, the present invention is not limited to the type of the block moving member 132.

[71] The gate lock blocks 130 fully open the through-gates 112 during the encapsulating process as shown in FIGs. 8 to 11. Therefore, the encapsulant 14 easily flows into the first cavity 111 through the first through-gate 112, and then into the second cavity 111 through the second through-gate 112. Of course, the encapsulant 15 continuously flows through the remaining through-gates 112 and cavities 111, whereby all the cavities 111 are filled with the encapsulant 15.

[72] Meanwhile, the cavities 111 formed in the first mold 110 are preferably but not exclusively formed substantially in a rectangular shape. In addition, the through-gates 112 formed in the first mold 110 are shallower than the cavities 111. Moreover, the through-gates 112 formed in the first mold 110 may be equal to or smaller than the cavities 111 and equal to the gate lock blocks 130 in width. Therefore, the gate lock blocks 130 may completely close the through-gates 112 or substantially reduce the open space of the through-gates 112. Furthermore, each of the through-gates 112 may be communicated preferably but not exclusively with an end or a center of a side of a corresponding cavity 111.

[73] As shown in FIGs. 11 to 13, after all the cavities 111 are filled with the encapsulant 15, the gate lock blocks 130 are operated. That is, as the gate lock blocks 130 are lowered by a predetermined distance by the moving members 132, all the through-gates 112 are completely closed or the open space thereof is substantially reduced. Therefore, the through-gate encapsulant parts, which correspond to the through-gates 112, are not formed. Of course, the gate lock blocks 130 should be operated before the encapsulant 15 is cured.

[74] In this manner, no through-gate encapsulant part is formed on the areas of the semiconductor 10 devices which correspond to the through-gates 112. Even if through-gate encapsulant parts are formed, the thickness thereof is very thin unlike the prior art. That is, the encapsulation parts are substantially formed in the areas which correspond to the cavities 111. Therefore, the quantity of encapsulant 15 to be used can be minimized. In addition, because the encapsulant 15 is introduced into each of the cavities 111 through the through-gates 112 each formed between adjacent two cavities 111, the swirling of the encapsulant 15 can be minimized. Therefore, voids are scarcely formed in the encapsulation parts 15 and the non-filling of encapsulant is not caused after the encapsulating process is completed. Furthermore, in the trimming or sawing process of the semiconductor devices after the encapsulating process, a trim punch or a sawing blade only trims or saws the lead frames 12 (or circuit boards). That is, the trim punch or the sawing blade is scarcely fractured by encapsulation or encapsulant parts. Therefore, according to the present invention, the life span of the trim punch or the

sawing blade can be increased. Of course, because the read lead frames 12 (or circuit boards) are only trimmed or sawed in the trimming or sawing process, the appearance of the encapsulation parts is scarcely damaged.

[75] FIGs. 14, 15, and 16 are cross-sectional, longitudinal sectional, and top plan views showing the condition of encapsulation parts in a mold according to another embodiment of the present invention before gate lock blocks are operated, respectively, FIGs. 17, 18 and 19 are cross-sectional, longitudinal sectional, and top plan views showing the condition of encapsulation parts in the mold after the gate lock blocks are operated, respectively. The mold shown in FIGs. 14 to 16 is similar to that described above with reference to FIGs. 8 to 13 in configuration, only the different parts are described below.

[76] As shown in FIGs. 14 to 16, the mold according to another embodiment of the present invention also includes a first mold 110, a second mold 120 and plural gate lock blocks 130. Of course, the first mold 110 is formed with plural cavities 111, within which semiconductor devices 10 are positioned, respectively, in two rows (or in more than two rows), and the cavities in each row are communicated with each other via the through-gates 112. Here, the two rows of through-gates 112 are located as near as possible and extend parallel to each other. In addition, in the encapsulating process, the gate lock blocks 130 engaged with the second mold 120 open the through-gates 112, respectively.

[77] Meanwhile, as shown in FIGs. 17 to 19, the gate lock blocks 130 are operated after the encapsulating process is completed, whereby all the through-gates 112 are completely closed or the open space thereof can be substantially reduced. Therefore, through-gate encapsulant parts are scarcely formed in the areas corresponding to the through-gates 112. Of course, the gate lock blocks 130 should be operated before the encapsulant 15 is cured.

[78] FIGs. 20, 21, and 22 are cross-sectional, longitudinal sectional, and top plan views showing the condition of encapsulation parts in a mold according to another embodiment of the present invention before the gate lock blocks are operated, respectively, FIGs. 23, 24 and 25 are cross-sectional, longitudinal sectional, and top plan views showing the condition of encapsulation parts in the mold after the gate lock blocks are operated, respectively. The mold shown in FIGs. 20 to 25 is similar to that described above with reference to FIGs. 8 to 13 in configuration, only the different parts are described below.

[79] As shown in FIGs. 20 to 22, the mold according to another embodiment of the present invention also includes a first mold 110, a second mold 120 and plural gate lock blocks 130. Of course, the first mold 110 is formed with plural cavities 111, within which semiconductor devices 10 are positioned, respectively, in two rows (or in

more than two rows), and the cavities 111 in each row are communicated with each other via through-gates 112. Here, the two rows of through-gates 112 are located as remote as possible and extend parallel to each other. In addition, in the encapsulating process, the lock blocks 130 engaged with the second mold 120 open the through-gates 112, respectively.

[80] Meanwhile, as shown in FIGs. 23 to 25, the gate lock blocks 130 are operated after the encapsulating process is completed, whereby all the through-gates 112 can be completely closed or the open space thereof can be substantially reduced. Therefore, through-gate encapsulant parts are scarcely formed in the areas corresponding to the through-gates 112. Of course, the gate lock blocks 130 should be operated before the encapsulant 15 is cured.

[81] FIGs. 26 and 27 are top plan and cross-sectional views showing the condition of encapsulation parts in a mold according to another embodiment of the present invention before the gate lock blocks of the inventive mold are operated, respectively, and FIGs. 28 and 29 are top plan and cross-sectional views showing the condition of encapsulation parts after the gate lock blocks are operated, respectively.

[82] As shown in FIGs. 26 and 27, a ram pot 115 is formed at a side portion of the first mold 110, into which the encapsulant is introduced, wherein the ram pot 115 is connected with four runners 114, each being formed in a predetermined length and depth. At the ends of the runners 114, plural cavities 111, which are formed in a predetermined depth, are arranged in four rows with a predetermined space. Here, the cavities 111 in each row are communicated with each other through through-gates 112, the width of which is same as that of the cavities 111. Of course, there are also provided gate lock blocks 130 for completely closing the through-gates 112 or reducing the open space thereof, wherein the width of the gate lock blocks 130 is same as that of the through-gate 112. In this manner, the encapsulant 15 fed from the ram pot 115 is sequentially introduced into the first to last cavities 111 in each row, through corresponding runner 114 and gate 113 and first to last through-gates 112, whereby all the cavities 111 are filled with the encapsulant 115. In this encapsulating process, the gate lock blocks 130 engaged with the second mold 12 are not operated, so that all the through-gates 112 are opened.

[83] Meanwhile, as shown in FIGs. 28 and 29, after the encapsulating process is completed, the gate lock blocks 130 are lowered, thereby completely closing or substantially reducing the open space of all the through-gates 112, each being provided between two adjacent cavities 111. Therefore, through-gate encapsulant parts are not substantially formed at the areas corresponding to the through-gates 112. Of course, the gate lock blocks 130 are operated before the encapsulant 15 is cured.

[84] FIGs. 30, 31 and 32 are cross-sectional, longitudinal sectional, and top plan views

showing the condition of encapsulation parts in a mold according to another embodiment of the present invention before the gate lock blocks of the inventive mold are operated, respectively, and FIGs. 33, 34 and 35 are cross-sectional, longitudinal sectional, and top plan views showing the condition of encapsulation parts after the gate lock blocks are operated, respectively.

- [85] AS shown, the mold according to another embodiment of the present invention includes a first mold 110, a second mold 120, and a split block 130.
- [86] The first mold 110 is formed with a cavity 111, which has a predetermined depth and area, so that plural semiconductor devices 10 can be positioned in the cavity at once, and one or more gates 113 of a predetermined depth are communicated with the cavity 111. Each gate 113 is communicated with a runner 114 of a predetermined depth, which is in turn communicated with a ram pot 115.
- [87] Upon coming into close contact with the first mold 110, the second mold 120 allows encapsulant 15 to flow into the cavity 111 so as to surround all the semiconductor devices, which are positioned in the cavity 111, through the gates 113 of the first mold 110.
- [88] The split block 130 is installed through the first mold 110 and extends to the cavity 111, so that a separated encapsulation part 115 is formed over each of the semiconductor devices 10 within the cavity 111. Such a split block 130 includes plural crosswise partitions 134 and longitudinal partitions 136, which are crossed with each other. In other words, the crosswise partitions 134 and longitudinal partitions 136 are arranged in a grid form in the split block 130. By each rectangular area surrounded by the crosswise and longitudinal partitions 134 and 136, one encapsulation part 15 (i.e., one semiconductor device) is formed. In addition, a block moving member 132 is further provided so as to vertically reciprocate the split block 130. The block moving member 132 may be selected preferably but not exclusively from a pneumatic cylinder, a hydraulic cylinder, a motor, and the like.
- [89] As shown in FIGs. 30 to 32, the split block 130 is not moved toward the inside of the cavity 111 while the encapsulant 15 is being introduced into the cavity 111 through the ram pot 115, the runners 114, and the gates 113. That is, in order to ensure that the encapsulant 15 arrives at all the semiconductor devices 10 within the cavity 111, the split block 130 remains in a state of being raised from the semiconductor devices 10 by a predetermined distance. As such, the cavity 111 is completely opened.
- [90] However, after the encapsulating process is completed, as shown in FIGs. 33 to 35, the split block 130 is lowered by a predetermined distance as the block moving member 132 is driven, so that the split block 130 comes into contact with or is positioned adjacent the surfaces of the semiconductor devices 10. Specifically, the split block 130 completely closes the cavity 111 or substantially reduces the open space of

the cavity 111, so that the encapsulation parts formed over the semiconductor devices are completely separated from each other. In other words, as the split block 130 is lowered, one encapsulation part 15 is formed on each semiconductor device 10.

Between adjacent semiconductor devices 10, no encapsulant part is formed, or even if formed, the thickness of such an encapsulant part is very thin unlike the prior art.

[91] Therefore, in the trimming or sawing process, which is performed after the encapsulation process is completed, a sawing blade or a trimming punch comes into contact with the lead frames 12 (or circuit boards) without coming into contact with an encapsulant part (or even if the sawing blade or the trimming punch comes into contact with an encapsulant part, the encapsulant part is very thin), whereby the life span of the sawing blade or the trimming punch can be increased. In addition, by making the runners 114 and the gates 113 as short as possible, the quantity of the encapsulant 15 to be used can be minimized.

[92] FIG. 36 is a perspective view showing a semiconductor device according to an embodiment of the present invention, which is separated from a lead frame strip. In addition, FIGs. 37 is a top plan view showing the semiconductor device before an encapsulation part is formed, and FIGs. 38 and 39 are cross-sectional views showing the semiconductor device with the encapsulation part.

[93] As shown, the inventive semiconductor device 10 includes a semiconductor die 11, a lead frame 12, on which the semiconductor die 11 is mounted, the semiconductor die 11 being electrically connected with the lead frame, and an encapsulation part 15 formed by encapsulating the semiconductor die 11 and the lead frame 12 with an encapsulant. In addition, the inventive semiconductor device 10 is formed with at least two encapsulant cutting traces 16, which are formed on the lateral sides of the encapsulation part 15 due to the inlet and outlet of a through-gate.

[94] More particularly, the encapsulation part 15 includes a first surface 15a, which is substantially flat and has a predetermined area, a second surface 15b, which is positioned opposite to the first surface 15a, and four third surfaces which extend along and between the four edges of the first and second surfaces 15a and 15b, thereby being arranged in a rectangular form. The lead frame 12 is projected through one of the four third surfaces 15c, so that the lead frame 12 can be easily connected to an external apparatus.

[95] Meanwhile, the two encapsulant cutting traces 16 may be formed on symmetrically arranged areas of two third surfaces 15c, which are parallel to each other, among the four third surfaces 15c. In other words, the two encapsulant cutting traces 15 may be symmetrically formed on the two opposite third surfaces 15c, which are parallel to each other but perpendicular to the third surface 15c, through which the lead frame 12 is projected. In addition, each of the encapsulant cutting traces 16 may take a form of a

protrusion projected from the encapsulation part by a predetermined length. Of course, the encapsulant cutting trace 16 formed on one third surface 15c may be a trace of the inlet of a through-gate, and the encapsulant cutting trace 16 formed on another third surface 15c may be a trace of the outlet of the through-gate. In the drawings, reference numeral 13 denotes a conductive wire for electrically interconnecting the semiconductor die 11 and the lead frame 12, and reference numeral 14 denotes an Ag paste or solder paste for interconnecting the semiconductor die 11 and the lead frame 12.

[96] Here, the above-mentioned two encapsulant cutting traces 16 may be formed because through-gates are oppositely formed with reference to a cavity in a mold. That is, through-gate encapsulant parts are formed after the encapsulating process is completed, and cut in a cutting process, whereby the encapsulation cutting parts defined herein are formed. Although the encapsulant cutting traces 16 are drawn in a shape projected too much from the encapsulation part 15, the length of each encapsulation part does not exceed several nanometers. Of course, the encapsulant cutting traces 16 may be flush with the corresponding third surfaces 15c of the encapsulation part 15 without being projected from the third surfaces 15c. In addition, the encapsulant cutting traces 16 may be also formed through the sawing process or the punching process.

[97] FIGs. 40 and 41 are top plan and side views showing various positions where encapsulant cutting traces may be formed on an encapsulation part of the inventive semiconductor device.

[98] As shown in FIG. 40, the inventive semiconductor device 10 has encapsulant cutting traces 16 each formed in a protrusion shape (or merely in a trace form without being projected) wherein the encapsulant cutting traces 16 may be formed on positions of a-a , a-b , a-c , b-a , b-b , b-c , c-a , c-b or c-c on the encapsulation part of the semiconductor device 10. That is, the encapsulant cutting traces 16 may be symmetrically or asymmetrically formed on two oppositely positioned third surfaces 15c. In addition, the encapsulant cutting traces 16 may be formed on at least two positions among the positions a, b and c, and on at least two positions among the positions a , b and c .

[99] As shown in FIG. 41, the encapsulant cutting traces 16 may be formed on d, e, f, g or h position beyond the a position, and the present invention is not limited by the positions and number of the encapsulant cutting traces 16 formed on one of the third surfaces 15c.

[100] In addition, although the encapsulant cutting traces 16 are shown as a rectangular shape in FIG. 40, the present invention is not limited to this. That is, the encapsulant cutting traces 16 may take various forms such as a trapezoidal shape, a circular shape, a semi-circular shape, or the like. Of course, the shapes of the encapsulant cutting traces 16 are solely dependent from the cross-sectional shape of through-gates formed

on opposite sides of a cavity.

[101] FIG. 42 shows, in enlarged scale, gate lock blocks before they are operated, and FIG. 43 shows, in enlarged scale, the gate lock blocks after they are operated.

[102] As shown in FIG. 42, at the areas corresponding to through-gates of a mold, through-gate encapsulant parts 24 may be formed, which are connected to an encapsulation part 15, during the encapsulating process, and they are removed by gate lock blocks 130 prior to being cured. However, one or more positional errors may be caused in connection with such gate lock blocks 130. That is, a positional error in engagement between the gate lock blocks 130 and the second mold 120, a positional error between a lock block 130 and a cavity 111, a positional error between a gate lock block 130 and a through-gate 112, etc. may be caused. Therefore, it is also possible that one surface (third surface) is formed with an encapsulant cutting trace 16 in a form of a protrusion as shown in FIG. 44 but the other surface (third surface) in the opposite side is formed with an encapsulant cutting trace 16 in a form of a recess.

[103] Therefore, the inventive semiconductor device 10 may be formed with an encapsulant cutting trace 16 in a form of a protrusion on one third surface 15c of the encapsulation part 15 and an encapsulant cutting trace 16 in a form of a recess on the other third surface 15c in the opposite side of the encapsulation part 15. If a positional error does not substantially exist, it is of course that the encapsulant cutting traces 16 are substantially flush with the third surfaces 15c of the encapsulation part 15. However, the encapsulant cutting traces 16 formed by these gate lock blocks 130 are sufficiently visually recognizable.

[104] FIG. 44 is a perspective view showing a semiconductor device according to an embodiment of the present invention.

[105] As described above, if a positional error is produced in connection with the gate lock blocks 130, one third surface 13c of the semiconductor device 10 may be formed with an encapsulant cutting trace 16 in a form of a protrusion, and the other third surface 15c in the opposite side may be formed with an encapsulant cutting trace 16 in a form of a recess. Therefore, the inventive semiconductor device 10 may have encapsulant cutting traces 15c in the forms of a protrusion and a recess on the third surfaces 15c, which are the opposite lateral sides of the encapsulation part 15.

[106] FIG. 45 is a perspective view showing a semiconductor device according to another embodiment of the present invention.

[107] As described above, if a positional error is produced in connection with the gate lock blocks 130, one third surface 13c of the semiconductor device 10 may be formed with an encapsulant cutting trace 16 in a form of a recess. Of course, the other third surface 15c in the opposite side may be also formed with an encapsulant cutting trace 16 in a form of a recess. In addition, although not shown in the drawing, both of the

encapsulant cutting traces 16 may be formed in a shape of protrusion on the two opposite third surfaces 15c of the encapsulation part 15. Moreover, one encapsulant cutting trace 16 formed on one third surface 15c may be in a form of a protrusion and the other encapsulant cutting trace 16 formed on the other third surface 15c in the opposite side may be in a form of a recess. Finally, both of the encapsulant cutting traces 16 formed on the opposite third surfaces 15c may be flush with the third surfaces 15c. In addition, the encapsulant cutting traces 16 may be equal to or slightly smaller than corresponding third surfaces in length. However, the invention is not limited by the length of the encapsulant cutting trace 16.

[108] FIG. 46 is a perspective view showing a semiconductor device according to another embodiment of the present invention.

[109] As shown in FIG. 46, a large-scale semiconductor device 10 may be formed with encapsulant cutting traces 16 on only one of third surfaces 15c. That is, because a large-scale semiconductor device 10 is not manufactured through a method, which forms plural encapsulation parts 15 on one lead frame strip, it is difficult to form an encapsulation part 15 in a through-gate type. However, in such a case, the inventive gate lock blocks 130 can be sufficiently employed. That is, by providing gate lock blocks 130 at the areas corresponding to the gates connected to a cavity 111, a finished semiconductor device may be formed with encapsulant cutting traces only at one side of the encapsulation part. Of course, such encapsulant cutting traces 16 may be projected, recessed or flush with the corresponding lateral surface of the encapsulation part 15. In manufacturing such a large-scale semiconductor device 10, if such gate lock blocks 130 are employed, no gate encapsulant part is formed at the areas corresponding to the gates of a mold or even if formed, such a gate encapsulant part is very thin, whereby it is also possible to reduce the quantity of encapsulant to be used.

[110]

Industrial Applicability

[111] As described above, according to the present invention, cavities in a mold for manufacturing semiconductor devices are communicated with each other through through-gates, each of which extends between two adjacent cavities, rather than being communicated with each other through a single runner and gates, which extend from the single runner, as in the prior art, whereby the quantity of encapsulant to be used in manufacturing semiconductor devices can be substantially reduced. This is because the gate encapsulant parts, which are formed in the through-gates of the mold and wasted after an encapsulating process, are formed from a small amount of encapsulant.

[112] In addition, according to the present invention, encapsulant is introduced into each of cavities through a straightly arranged through-gate rather than through a gate which

substantially extends perpendicularly from a runner as in the prior art, whereby the swirling of the encapsulant can be suppressed. Therefore, voids are scarcely produced in encapsulation parts formed within the cavities. Furthermore, it is very seldom that the cavities are insufficiently filled with encapsulant.

[113] The present invention provides gate lock blocks for opening through-gates during an encapsulating process and closing the through-gates after the encapsulating process is completed, whereby it is sufficient if lead frames (or circuit boards) are only trimmed by a punch during a trimming process. That is, it is not necessary to trim encapsulant or encapsulation parts along with lead frames with a punch. Therefore, the life span of such a punch can be increased. In addition, because no gate encapsulant part exists (even if existing, the thickness of such a gate encapsulant part is very thin as compared with those of the prior art), the fracture of encapsulation parts, which has been caused when cutting gate encapsulant parts in the prior art, is not caused.

[114] According to the present invention, the encapsulation parts of semiconductor devices are formed through a through-gate type or gate-block type method. Therefore, after the encapsulating process is completed, opposite lateral surfaces (or one lateral surface) of an encapsulation part are formed with encapsulant cutting traces, which are the traces of the inlet and outlet of the encapsulant are naturally formed during the encapsulation cutting process, which is performed after the encapsulating process is completed. Therefore, if encapsulant cutting traces as mentioned above are seen in a semiconductor device, it can be inferred that the semiconductor device is manufactured by using the inventive method.

[115] According to the present invention, a split block is provided which enables encapsulant to easily flow between and over semiconductor devices during the encapsulating process and which allows the encapsulation parts for individual semiconductor devices to be smoothly separated from each other. As a result, it is possible to form a single large cavity instead of plural cavities in a mold. If plural semiconductor dies are manufactured using such a single large cavity, it may be necessary to saw encapsulation parts and lead frames (or circuit boards) in unison in the sawing process. However, according to the present invention, the encapsulation parts are separated from each other by the split block in advance, any one of a sawing process using a sawing blade and a trimming process using a punch can be selected and employed. Of course, substantially no impact is applied to the encapsulation parts while they are sawed or trimmed, except lead frames (or circuit boards), the fracture of encapsulation parts can be greatly reduced.

[116] Although a preferred embodiment of the present invention has been described for illustrative purposes, those skilled in the art will appreciate that various modifications, additions and substitutions are possible, without departing from the scope and spirit of

the invention as disclosed in the accompanying claims.

[117]

Claims

- [1] A mold for manufacturing semiconductor devices comprising:
a first mold having plural cavities with a predetermined depth, the plural cavities being arranged in one or more rows in such a manner as to be spaced from each other in each row, so that plural semiconductor devices are positioned in one or more rows, the plural cavities in each row being communicated with each other through through-gates, which are shallower than the cavities; and
a second mold which comes into close contact with the first mold and allows encapsulant to sequentially flow into all the cavities through the through-gates in such a manner as to surround the semiconductor devices positioned within the cavities.
- [2] A mold as claimed in claim 1, wherein the width of the through-gates formed in the first mold is equal to or narrower than that of the cavities.
- [3] A mold as claimed in claim 1, wherein each of the through-gates is communicated with an end portion or a central portion of a side of a corresponding cavity.
- [4] A mold for manufacturing semiconductor devices comprising:
a first mold having plural cavities with a predetermined depth, the plural cavities being arranged in one or more rows in such a manner as to be spaced from each other in each row, so that plural semiconductor devices are positioned in one or more rows, the plural cavities in each row being communicated with each other through through-gates, which are shallower than the cavities;
a second mold which comes into close contact with the first mold and allows encapsulant to sequentially flow into all the cavities through the through-gates in such a manner as to surround the semiconductor devices positioned within the cavities; and
plural gate lock blocks installed through the second mold at the areas corresponding to the through-gates of the first mold, wherein the gate lock blocks open the through-gates during an encapsulating process and close the through-gates or reduce the open spaces of the through-gates after the encapsulating process is completed.
- [5] A mold as claimed in claim 4, wherein the width of the gate lock blocks is same as that of the through-gates, and the width of the through-gates is equal to or smaller than that of the cavities.
- [6] A mold as claimed in claim 4, wherein each of the through-gates is communicated with an end portion or a central portion of a side of a corresponding cavity.

- [7] A mold as claimed in claim 4, further comprising a block moving member on the gate lock blocks so as to linearly reciprocate the gate lock blocks.
- [8] A mold as claimed in claim 7, wherein the block moving member is any one selected from a pneumatic cylinder, a hydraulic cylinder, and a motor.
- [9] A mold for manufacturing semiconductor devices comprising:
a first mold having a cavity with a predetermined depth, at least one gate of a predetermined depth being communicated with the cavity;
a second mold which comes into close contact with the first mold and allows encapsulant to sequentially flow into the cavity through the gate of the first mold in such a manner as to surround all the semiconductor devices positioned within the cavity; and
a split block installed through the first mold to the cavity so as to allow each of the semiconductor devices to be formed with a separate encapsulation part, wherein the split block completely opens the cavity so that encapsulant can smoothly flow during an encapsulating process, and comes into contact with or approaches each of the semiconductor devices so that the encapsulation parts of respective semiconductor devices could be separated from each other.
- [10] A mold as claimed in claim 9, wherein the split block comprises plural crosswise and longitudinal partitions which are crossed with each other.
- [11] A mold as claimed in claim 10, wherein one encapsulation part is formed in one area surrounded by two crosswise partitions and two longitudinal partitions.
- [12] A mold as claimed in claim 9, further comprising a block moving member installed on the split block so as to linearly reciprocate the split block.
- [13] A mold as claimed in claim 12, wherein the block moving member is any one selected from a pneumatic cylinder, a hydraulic cylinder, and a motor.
- [14] A semiconductor device comprising:
a semiconductor die;
a lead frame, the semiconductor die being mounted on the lead frame and electrically connected with the lead frame; and
an encapsulation part formed by encapsulating the semiconductor die and the lead frame with encapsulant, wherein the encapsulation part is formed, on its surface, with at least one encapsulant cutting trace corresponding to an inlet or an outlet of the encapsulant during an encapsulating process.
- [15] A semiconductor device as claimed in claim 14, wherein the encapsulation part comprises a first surface, which is flat and has a predetermined area, a second surface, which is positioned opposite to the first surface, and four third surfaces, which are arranged in a rectangular shape along and between the edges of the first and second surfaces, the third surfaces being narrower than either the first

surface or the third surface.

- [16] A semiconductor device as claimed in claim 15, wherein the encapsulant cutting traces are symmetrically formed on two third surfaces, which are positioned opposite and parallel to each other, among the four third surfaces.
- [17] A semiconductor device as claimed in claim 15, wherein the encapsulant cutting traces are asymmetrically formed on two third surfaces, which are positioned opposite and parallel to each other, among the four third surfaces.
- [18] A semiconductor device as claimed in claim 15, wherein the lead frame is projected outwardly from any one of the four third surfaces by a predetermined length.
- [19] A semiconductor device as claimed in claim 18, wherein the encapsulant cutting traces are symmetrically formed on the two third surfaces which are positioned opposite and parallel to each other and perpendicular to the third surface, from which the lead frame is projected.
- [20] A semiconductor device as claimed in claim 18, wherein the encapsulant cutting traces are asymmetrically formed on the two third surfaces which are positioned opposite and parallel to each other and perpendicular to the third surface, from which the lead frame is projected.
- [21] A semiconductor device as claimed in claim 14, wherein each of the encapsulant cutting traces is projected from a corresponding third surface of the encapsulation part by a predetermined length, recessed in the corresponding third surface by a predetermined depth, or flush with the corresponding third surface.
- [22] A semiconductor device as claimed in claim 15, wherein the encapsulant cutting traces are same with or smaller than the third surfaces in width.

Fig. 1

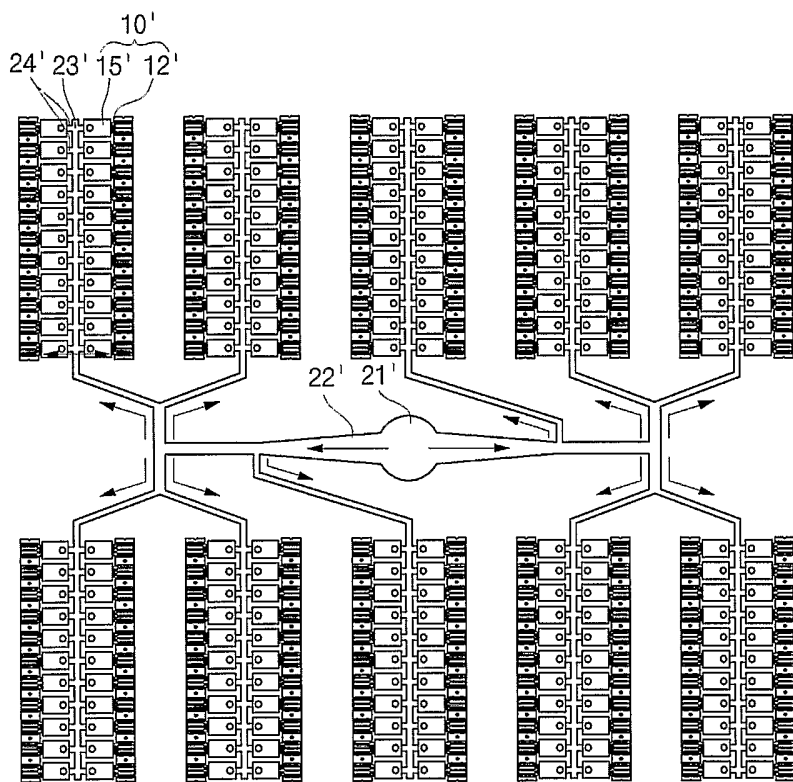


Fig. 2

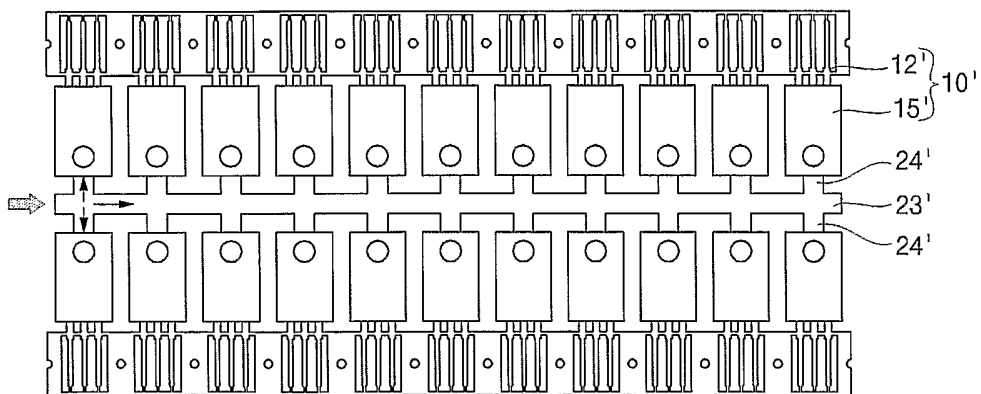


Fig. 3

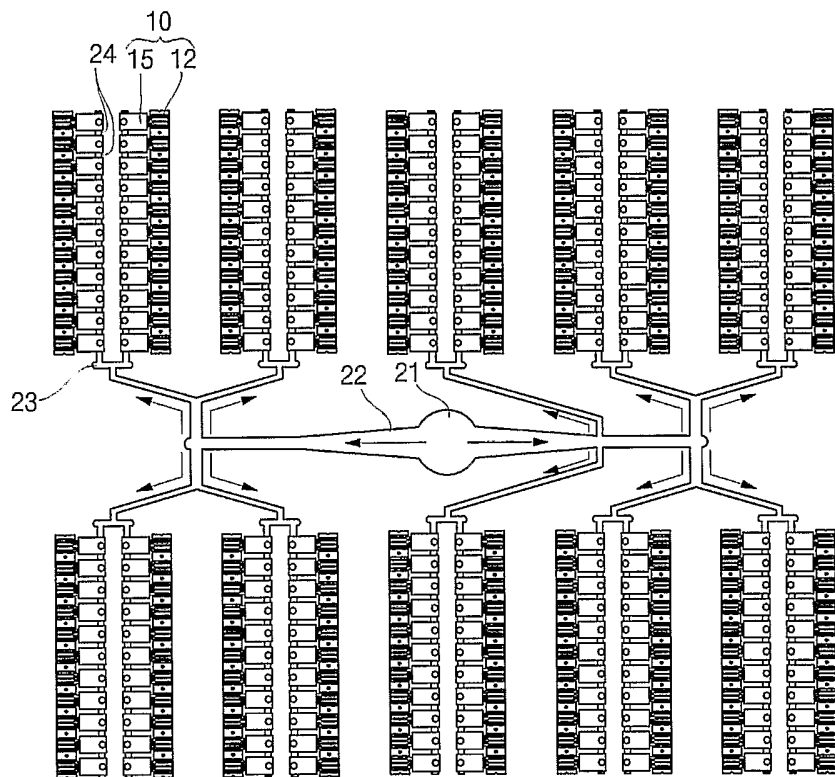


Fig. 4

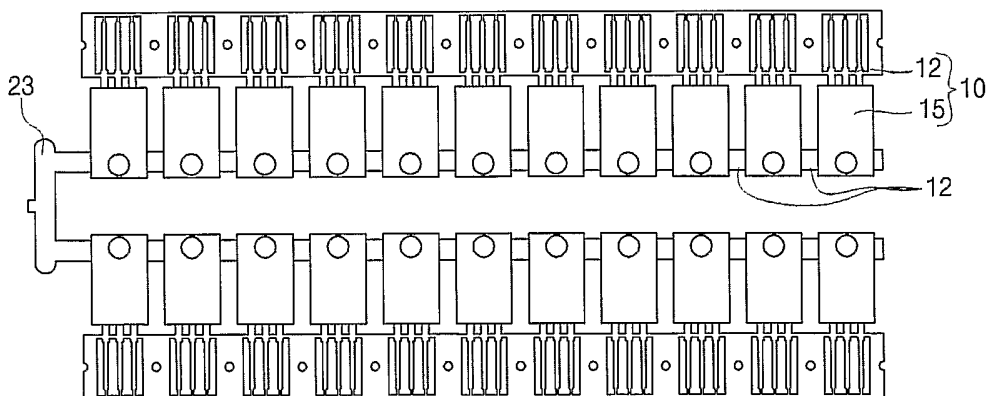


Fig. 5

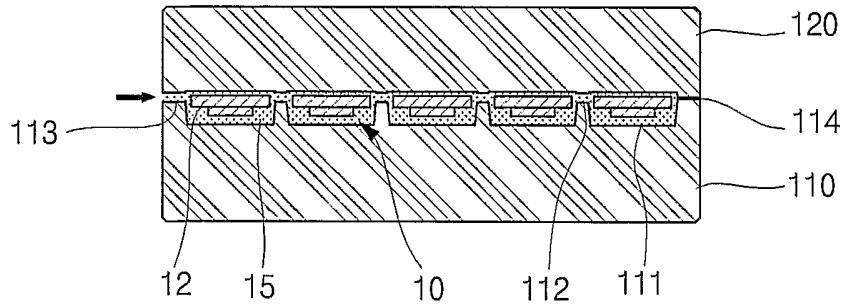


Fig. 6

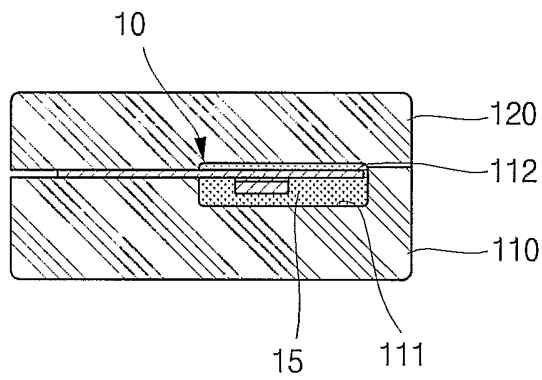


Fig. 7

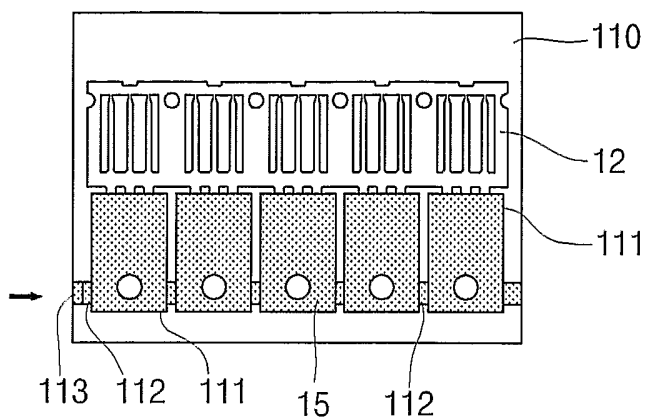


Fig. 8

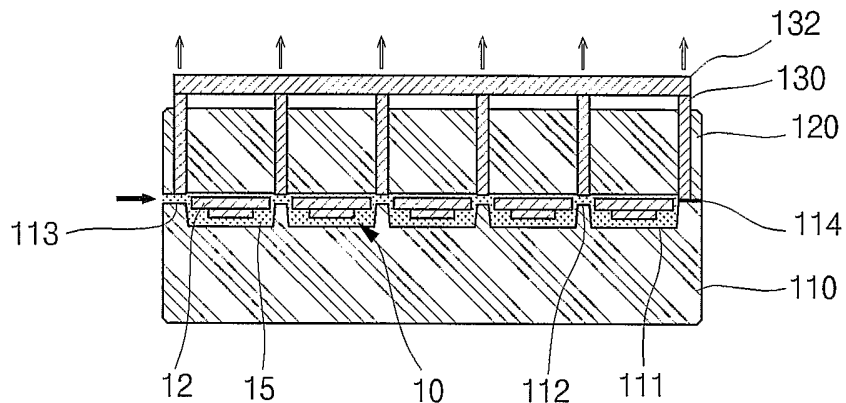


Fig. 9

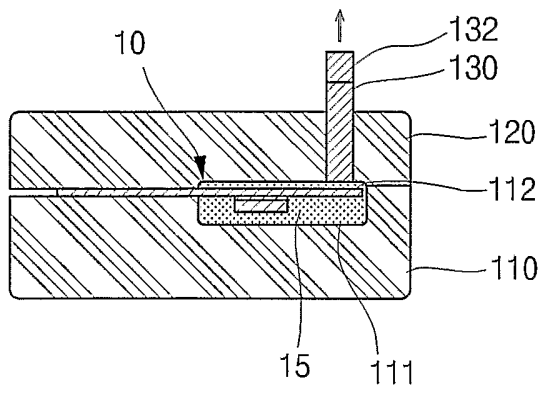


Fig. 10

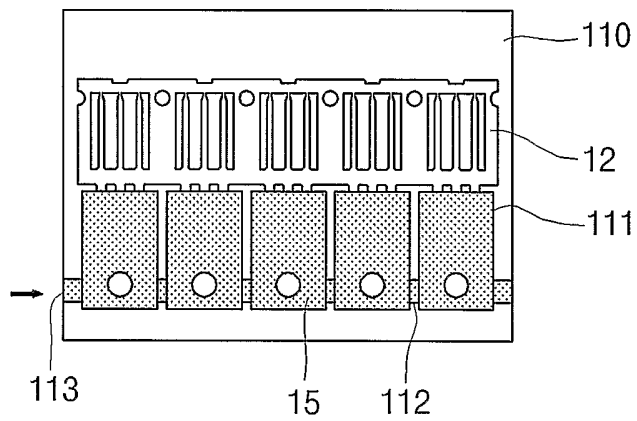


Fig. 11

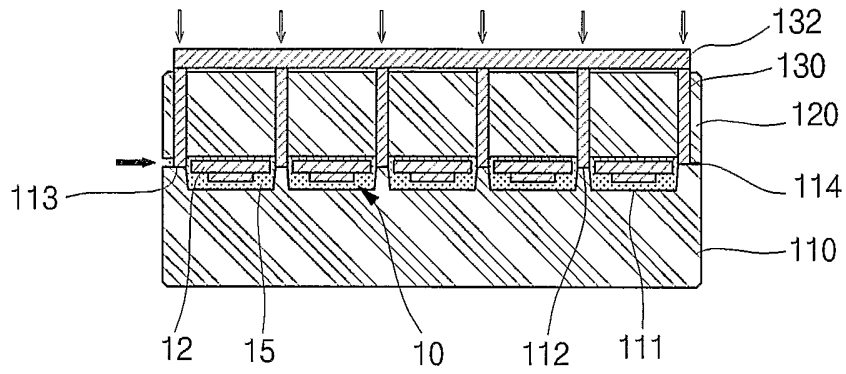


Fig. 12

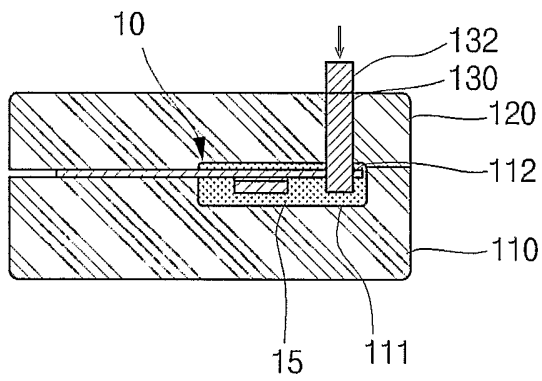


Fig. 13

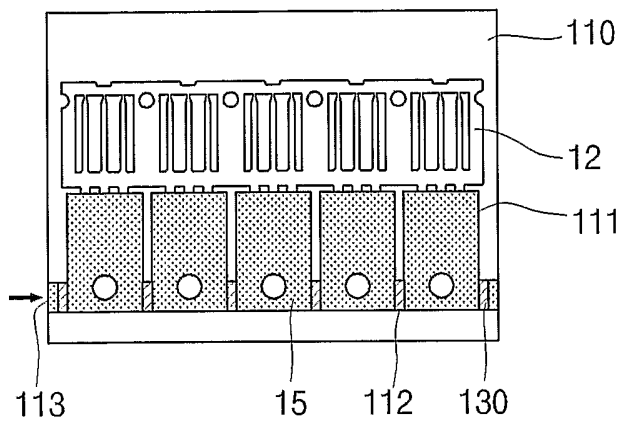


Fig. 14

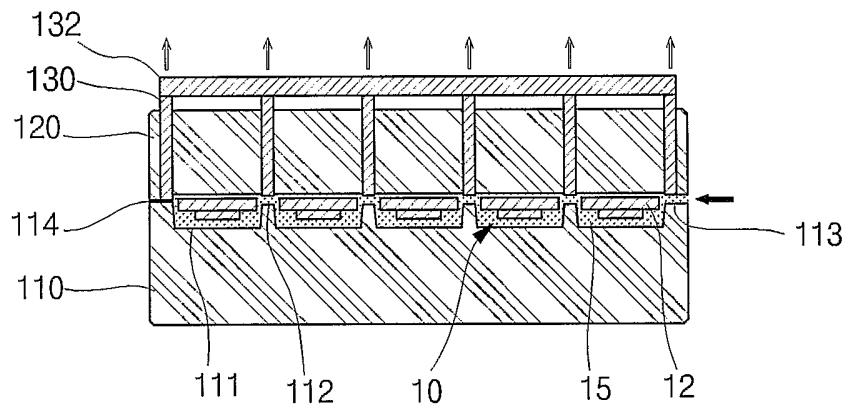


Fig. 15

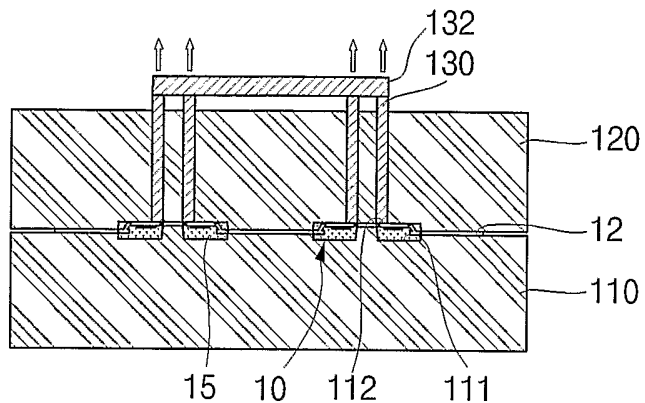


Fig. 16

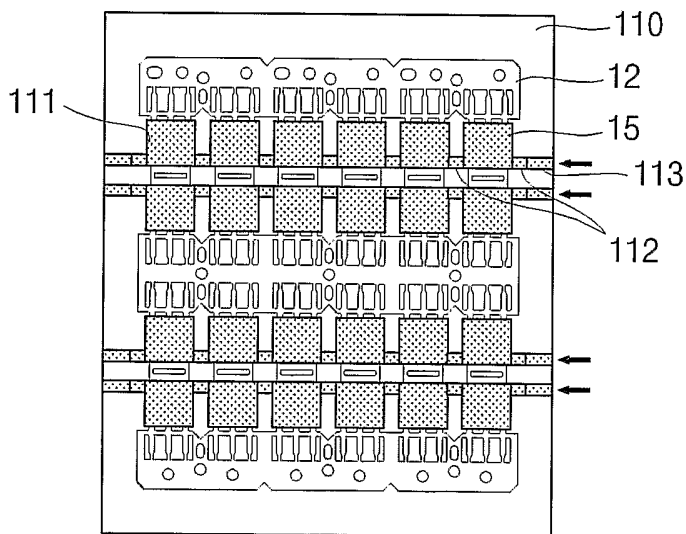


Fig. 17

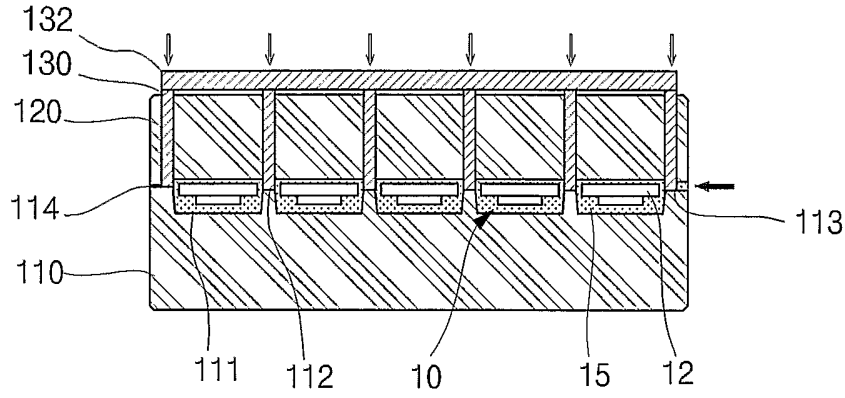


Fig. 18

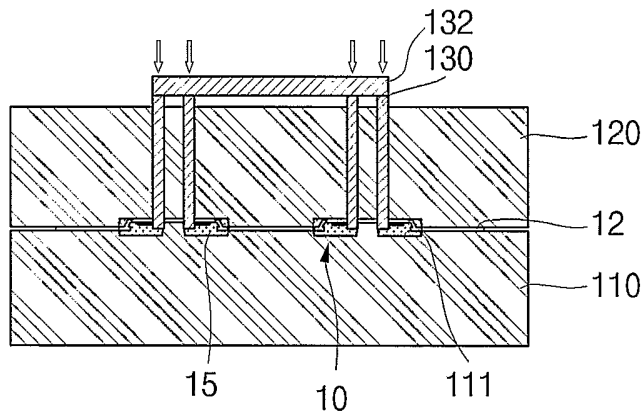


Fig. 19

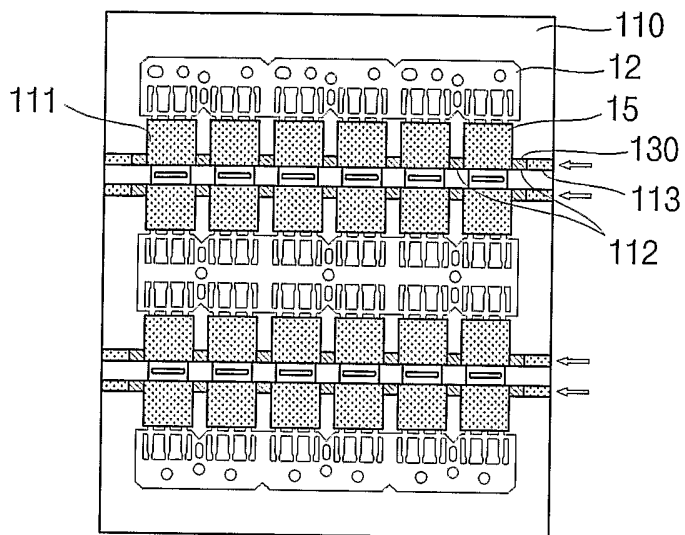


Fig. 20

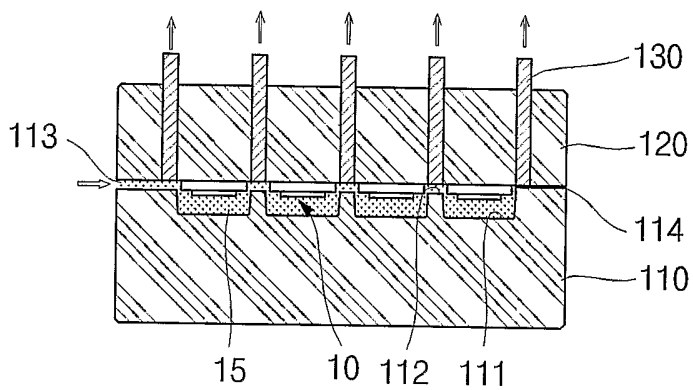


Fig. 21

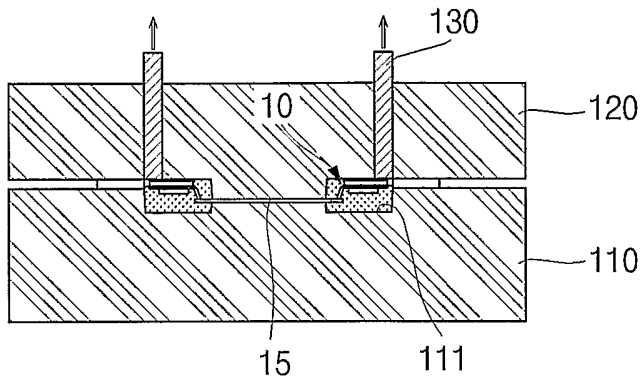


Fig. 22

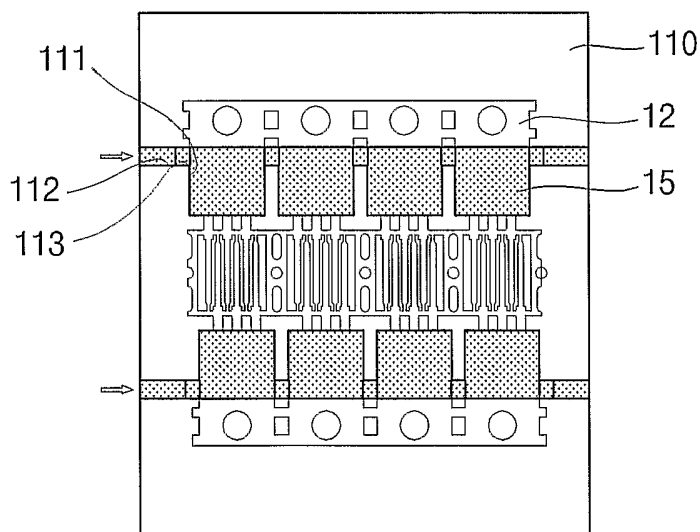


Fig. 23

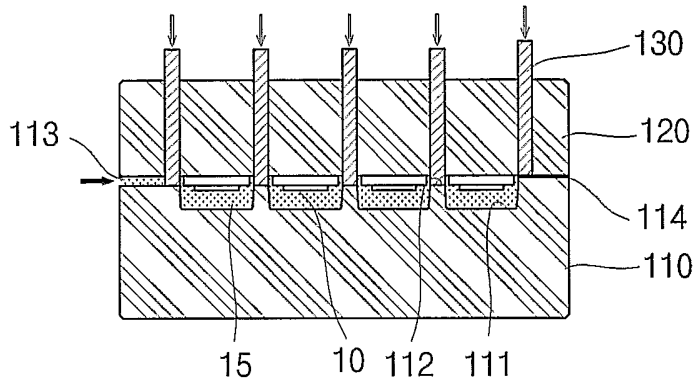


Fig. 24

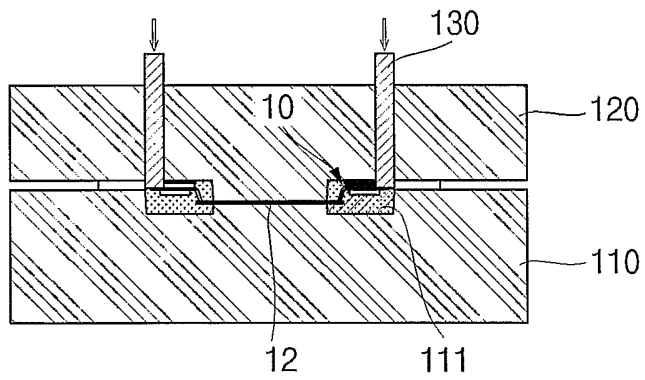


Fig. 25

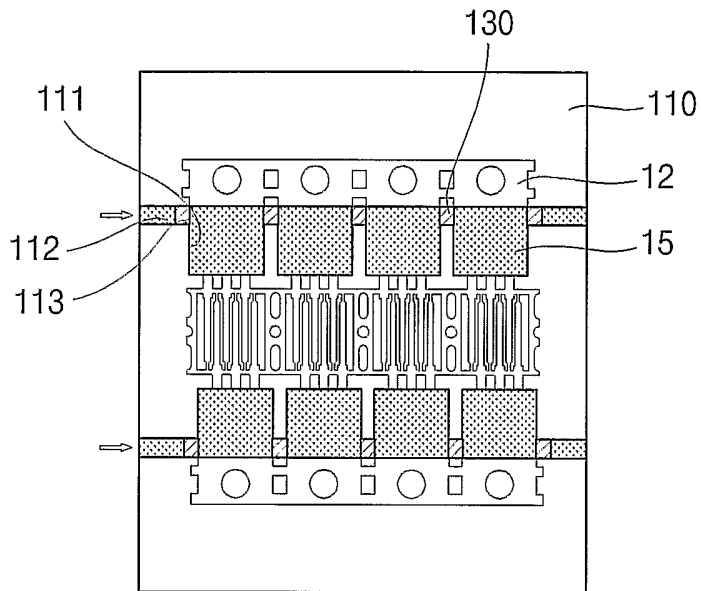


Fig. 26

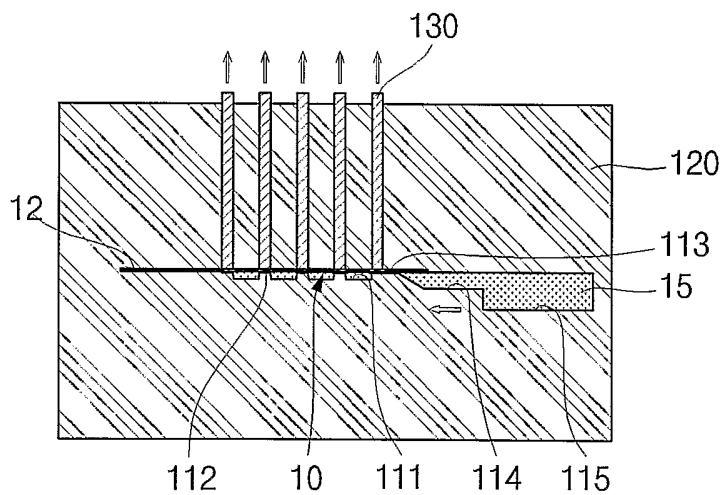


Fig. 27

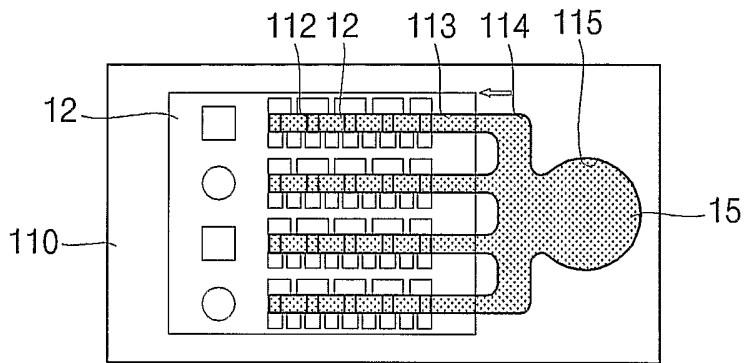


Fig. 28

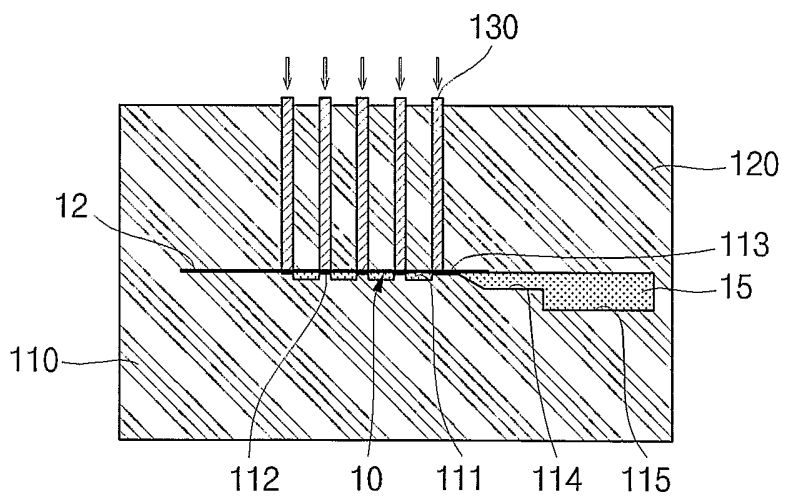


Fig. 29

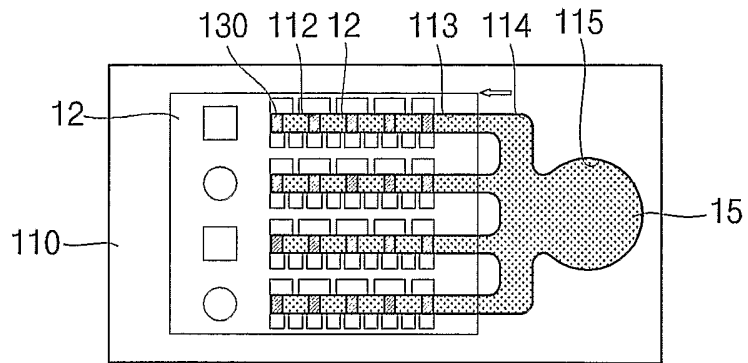


Fig. 30

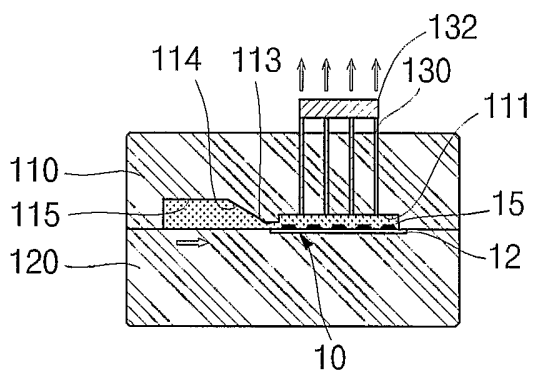


Fig. 31

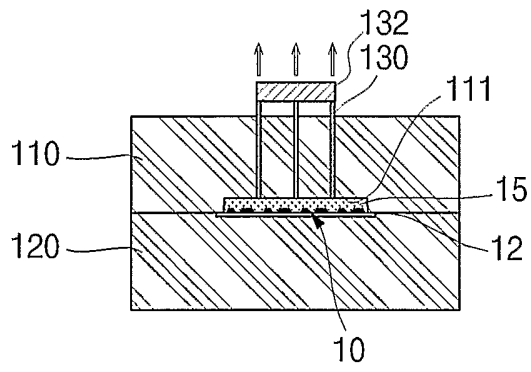


Fig. 32

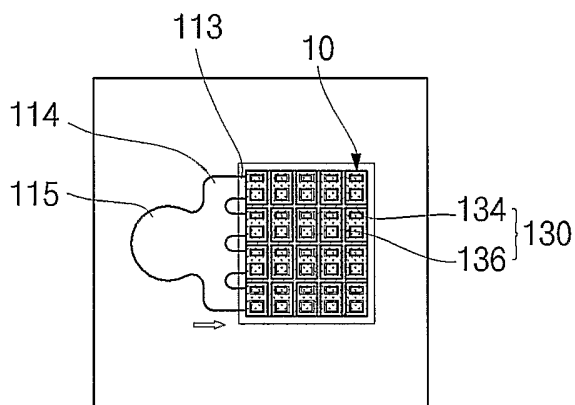


Fig. 33

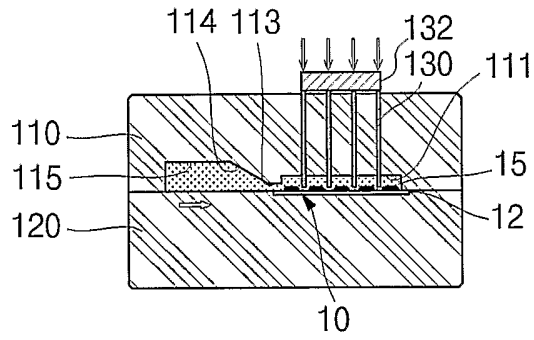


Fig. 34

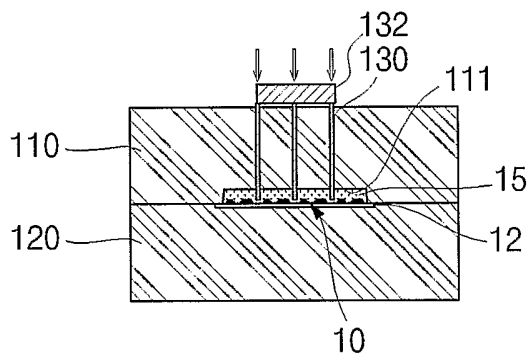


Fig. 35

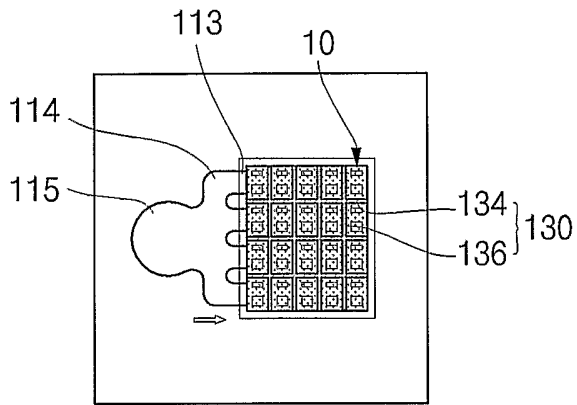


Fig. 36

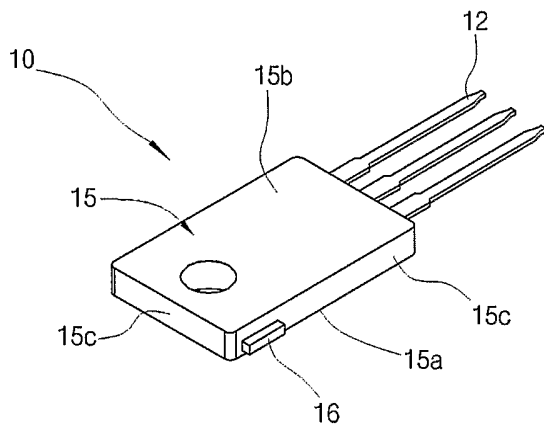


Fig. 37

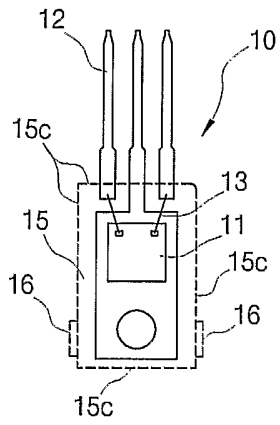


Fig. 38

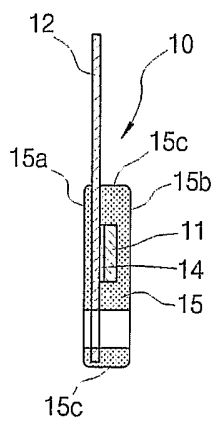


Fig. 39

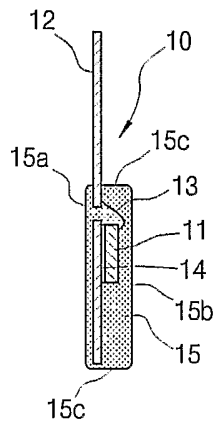


Fig. 40

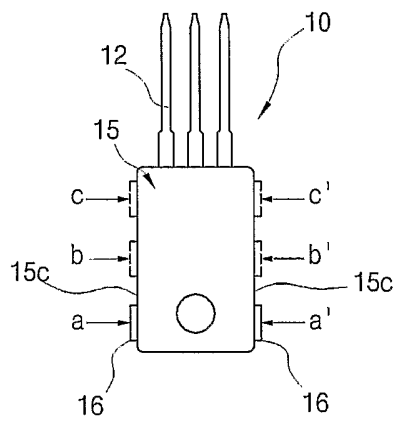


Fig. 41

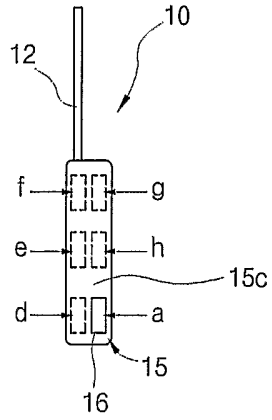


Fig. 42

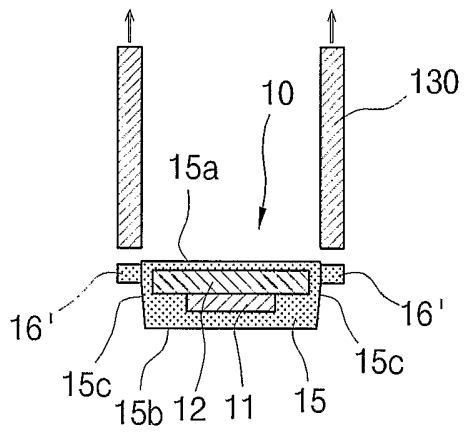


Fig. 43

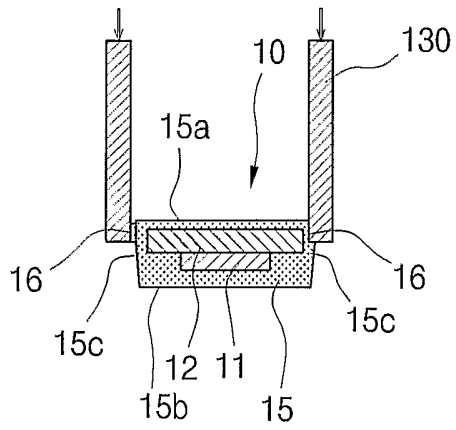


Fig. 44

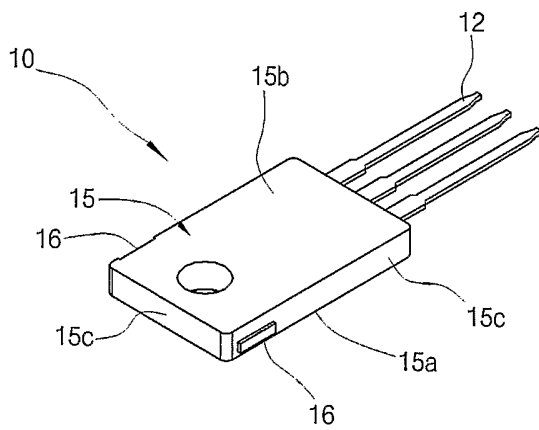


Fig. 45

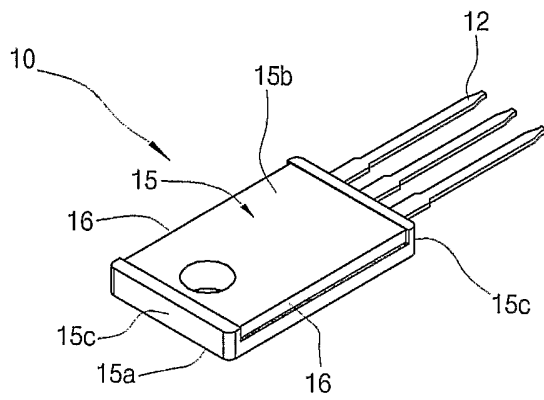
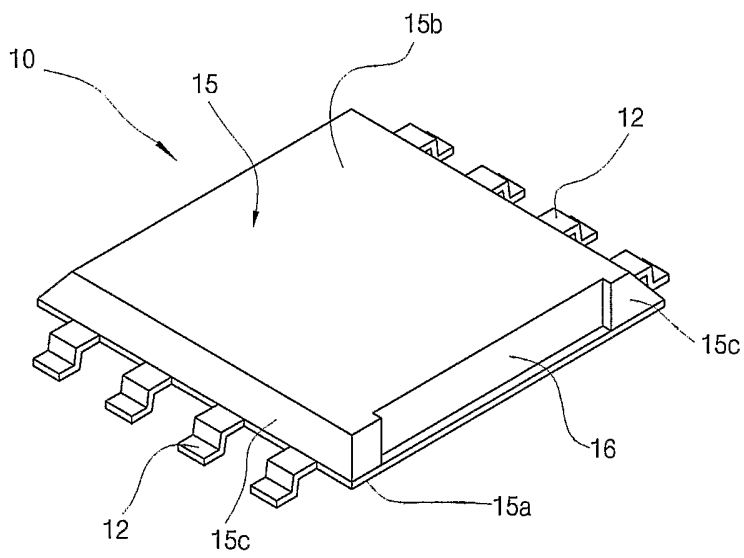


Fig. 46



INTERNATIONAL SEARCH REPORT

International application No.
PCT/KR2006/001937**A. CLASSIFICATION OF SUBJECT MATTER****H01L 23/50(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 8 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Japanese Utility models since 1975

Korean Patents and applications for inventions since 1975

Korean Utility models and applications since 1975

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

e-KIPASS : "mold", "lead frame", "cavity", "gate", "semiconductor"

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	JP 2000-031180 A (HITACHI LTD) 28 JAN 2000 & PAJ 2000031180 See the paragraph [12] - [24] Figure 1,7,11	1-3
A	See the entire document	4-22
X	JP 1983-217313 A (NEC HOME ELECTRONICS LTD) 17 DEC 1983 & PAJ 58217313 See claim and figure 3,7,8	1-3
A	See the abstract and figures	4-22
X	JP 1982-203532 A (TOSHIBA CHEM CORP) 13 DEC 1982 & PAJ 57203532 See claims and figure 2,3	1-3
A	See the abstract and figures	4-22

 Further documents are listed in the continuation of Box C. See patent family annex.

* Special categories of cited documents:

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"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

17 OCTOBER 2006 (17.10.2006)

Date of mailing of the international search report

18 OCTOBER 2006 (18.10.2006)

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Telephone No. 82-42-481-5747



INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/KR2006/001937

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
JP12031180	28.01.2000	JP12031180 JP2000031180A2 JP3149409B2	28.01.2000 28.01.2000 26.03.2001
JP58217313	17.12.1983	JP2037856B4 JP58217313	28.08.1990 17.12.1983
JP57203532	13.12.1982	JP1024612B4 JP57203532A2 JP57203532	12.05.1989 13.12.1982 13.12.1982