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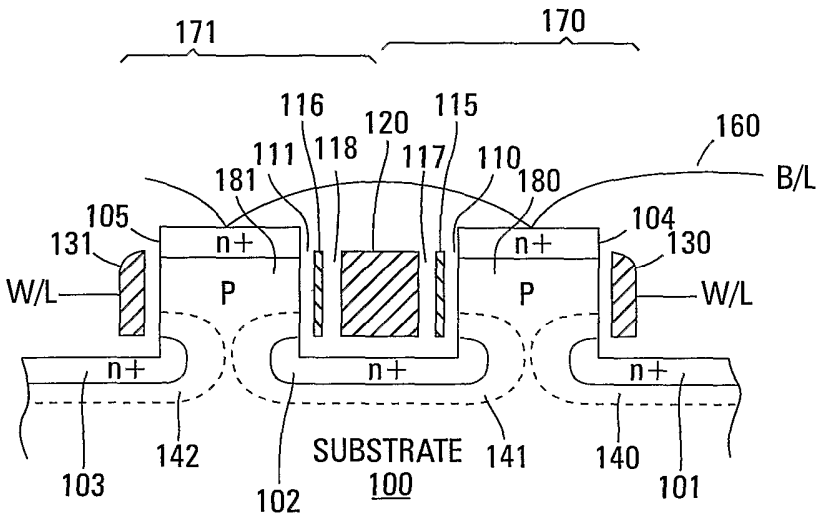
(54) **Title:** INTEGRATED DRAM-NVRAM MULTI-LEVEL MEMORY



(57) **Abstract:** An integrated DRAM-NVRAM (170, 171), multi-level memory cell is comprised of a vertical DRAM device with a shared vertical gate (120) floating plate (115, 116) device. The floating plate device (115, 116) provides enhanced charge storage for the DRAM part (104, 130, 101, 105, 131) of the cell through the shared floating body in a pillar between the two functions. The memory cell is formed in a substrate (100) with trenches that form pillars. A vertical wordline/gate (131, 130) on one side of a pillar is used to control the DRAM part (104, 130, 101, 105, 131, 103) of the cell. A vertical trapping layer (115, 116) on the other side of the pillar stores one or more charges as part of the floating plate device and to enhance the DRAM function through the floating body between the DRAM and floating plate device. A vertical NVRAM wordline/control gate (120) is formed alongside the trapping layer and is shared with an adjacent floating plate device (115, 116).

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INTEGRATED DRAM-NVRAM MULTI-LEVEL MEMORY

TECHNICAL FIELD OF THE INVENTION

The present invention relates generally to memory devices and in particular the present invention relates to DRAM and NVRAM architectures.

BACKGROUND OF THE INVENTION

Memory devices are typically provided as internal, semiconductor, integrated circuits in computers or other electronic devices. There are many different types of memory including random-access memory (RAM), read only memory (ROM), flash memory, dynamic random access memory (DRAM), and synchronous dynamic random access memory (SDRAM).

Conventional DRAM cells are comprised of a switching transistor and an integrated storage capacitor tied to the storage node of the transistor. Charge storage is enhanced by providing appropriate storage capacity in the form of a stacked capacitor or a trench capacitor in parallel with the depletion capacitance of the floating storage node. DRAM cells are volatile and therefore lose data when the power is removed.

DRAMs use one or more arrays of memory cells arranged in rows and columns. Each of the rows of memory cells is activated by a corresponding row line that is selected from a row address. A pair of complementary digit lines are provided for each column of the array and a sense amplifier coupled to the digit lines for each column is enabled responsive to a respective column address. The sense amplifier senses a small voltage differential between the digit lines and amplifies such voltage differential.

Due to finite charge leakage across the depletion layer, the capacitor has to be recharged frequently to ensure data integrity. This is referred to in the art as refreshing and can be accomplished by periodically coupling the memory cells in the row to one of the digit lines after enabling the sense amplifiers. The sense amplifiers then restore the voltage level on the memory cell capacitor to a voltage level corresponding to the stored data bit. The permissible time between refresh cycles without losing data depends on various factors such as rate of charge dissipation in the memory capacitor. \

As computers become smaller and their performance increases, the computer components should also go through a corresponding size reduction and performance increase. To accomplish this, the capacitors and transistors of DRAM cells can be reduced in size. This has the effect of increased speed and memory density with decreased power requirements.

However, a problem with decreased capacitor size is that sensing a conventional DRAM cell requires a minimum value of capacitance per cell. As the capacitor gets smaller, the capacitance is reduced. This has become a scalability challenge for DRAM.

For the reasons stated above, and for other reasons stated below which will become apparent to those skilled in the art upon reading and understanding the present specification, there is a need in the art for a more scalable DRAM cell.

SUMMARY

The above-mentioned problems with DRAMs and other problems are addressed by the present invention and will be understood by reading and studying the following specification.

The present invention encompasses an integrated DRAM-NVRAM memory cell. The cell comprises a dynamic random access memory function and a non-volatile random access memory function that is coupled to the dynamic random access memory function. The data storage by the dynamic random access memory function is enhanced by the non-volatile random access memory device that provides a non-volatile state retention in the DRAM. The non-volatile random access memory can store multiple bits of data.

Further embodiments of the invention include methods and apparatus of varying scope.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 shows a cross-sectional view of one embodiment of a DRAM-NVRAM multi-level memory cell of the present invention.

Figure 2 shows an electrical equivalent circuit diagram of the embodiment of Figure 1.

Figure 3 shows a cross-sectional view of an alternate embodiment of the DRAM-NVRAM multi-level memory cell of the present invention.

Figure 4 shows a block diagram of an electronic system that incorporates the non-planar, stepped NROM array of the present invention.

DETAILED DESCRIPTION

In the following detailed description of the invention, reference is made to the accompanying drawings that form a part hereof and in which is shown, by way of illustration, specific embodiments in which the invention may be practiced. In the drawings, like numerals describe substantially similar components throughout the several views. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention. Other embodiments may be utilized and structural, logical, and electrical changes may be made without departing from the scope of the present invention. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined only by the appended claims and equivalents thereof. The terms wafer or substrate used in the following description include any base semiconductor structure. Both are to be understood as including silicon-on-sapphire (SOS) technology, silicon-on-insulator (SOI) technology, thin film transistor (TFT) technology, doped and undoped semiconductors, epitaxial layers of a silicon supported by a base semiconductor structure, as well as other semiconductor structures well known to one skilled in the art. Furthermore, when reference is made to a wafer or substrate in the following description, previous process steps may have been utilized to form regions/junctions in the base semiconductor structure, and terms wafer or substrate include the underlying layers containing such regions/junctions.

Figure 1 illustrates a cross-sectional view of one embodiment of DRAM-NVRAM multi-level memory cells of the present invention. The cells are fabricated in trenches in a bulk silicon substrate 100. Pillars are formed between the trenches. In one embodiment, the substrate is comprised of p-type silicon. In alternate embodiments, the substrate is comprised of n-type material.

For purposes of clarity, Figure 1 illustrates only two of the DRAM-NVRAM memory cells 170 and 171 that comprise an array of memory cells. It is well known in the art that a typical memory array could have millions of cells.

Each DRAM-NVRAM cell 170 and 171 is comprised of a DRAM transistor and a NVRAM transistor. Each DRAM transistor is comprised of a drain region 104 and 105 and a source region 101 and 103. These regions 101, 103 – 105, in one embodiment, are doped n+ regions in the trenches and pillars of the substrate 100.

Vertical gates 130 and 131 are formed along the sidewalls of the trenches such that they are substantially between each transistor's active regions 101 and 104 or 103 and 105 with respective floating bodies 180 and 181. The vertical gates 130 and 131 are separated from the pillars by a dielectric material. The gates 130 and 131 are coupled to wordlines of the memory array.

Each NVRAM transistor is comprised of a drain region 104 and 105 that is formed in the tops of the pillars and shared with its respective DRAM transistor. A source region 102 is formed at the bottom of the trench and is shared between the two NVRAM transistors.

A vertical channel region exists between each pair of source/drain regions 101, 104 or 103, 105 for the gated transistors or 102, 104 or 102, 105 for the NV transistors gated by the shared control gate 120. For example, during operation, a channel forms in the floating body channel region between one drain 104, 101 or 105, 103.

Each NVRAM transistor is comprised of a floating plate 115 and 116 in which one or more charges are trapped and stored. The floating plates 115 and 116 are isolated from the channel regions by tunneling dielectrics 110 and 111 and from the shared control gate 120 by a charge blocking layer (i.e., intergate dielectric) 117 and 118 that prevents a trapped charge from leaking to the control gate. Each tunneling dielectric/floating plate/charge blocking layer makes up an insulator stack for each NVRAM transistor and, in one embodiment, is approximately 15 nm thick. The materials of construction are not critical to the present invention, but commonly include doped polysilicon for the gate/plate materials, and silicon oxides, nitrides or oxynitrides for the dielectric materials.

A data/bitline 160 couples each of the drain regions 104 and 105 in the tops of the pillars. Additionally, the source regions 101 – 103 are coupled to a source line of the memory array. As is shown later with reference to Figure 2, the source lines 101 – 103 of the cells 170 and 171 may be coupled to ground potential with the substrate (p-type silicon) held at a

negative potential such that the source lines and associated junctions are constantly held reverse biased.

During operation of the transistors of the present invention, depletion regions 140 – 142 form around each of the source regions 101 –103 respectively. The touching of the depletion regions 140 and 141 or 141 and 142 isolates the active p-type pillar body above the depletion regions, thus creating a p-type floating body in each pillar.

Figure 2 illustrates an electrical equivalent circuit diagram of the embodiment of Figure 1. This figure shows the two DRAM-NVRAM cells 170 and 171 of Figure 1.

Each cell 170 and 171 is comprised of an NVRAM transistor 202 and 201 that shares a common control gate/wordline 120 that couples a row of cells in the memory array. Each cell 170 and 171 also has a field effect transistor (FET) 205 and 206. The gate 130 and 131 of each FET 205 and 206 is coupled to a respective DRAM wordline 232 and 233. The DRAM wordlines 232 and 233 couple the FETs in a common row of cells of the array. The memory array bitline 170 couples the drains of each transistor in a common column of cells.

Figure 3 illustrates a cross-sectional view of an alternate embodiment of the DRAM-NVRAM multi-level cell of the present invention. This embodiment uses a silicon-on-insulator (SOI) structure. SOI refers to placing a thin layer of silicon on an insulator such as silicon oxide or glass. The transistors would then be built on this thin layer of SOI. The SOI layer reduces the capacitance of the transistors so that they operate faster. The embodiment of Figure 3 shares the electrical equivalent schematic of Figure 2.

As in the embodiment of Figure 1, each cell is comprised of a DRAM transistor and a NVRAM transistor. The DRAM transistors are comprised of pillars that have drain 304 and 305 regions at the top. The source regions 302 and 303 are formed at the bottom of the pillars. The DRAM vertical gates 330 and 331 are formed over the channel regions and are coupled to their respective wordlines.

Each NVRAM transistor uses the same drain 304 and 305 and source regions 302 and 303 as their respective DRAM transistors. Each insulator stack is comprised of a tunnel dielectric 310 and 311, floating plate 315 and 316, and charge blocking oxide 317 and 318. The common control gate 320 is formed in the center of the trench and is coupled to the array NVRAM wordline.

The above structure is formed on the insulator layer 301 that is formed over the substrate 300. In one embodiment, the insulator layer 301 is an oxide and the substrate and the floating body are a p-type silicon.

In operation, the DRAM-NVRAM cell of the present invention provides multi-functionality as well as multi-level NVRAM storage. When the NVRAM control gate is grounded, the cell works like a DRAM. Even though the DRAM transistor of the present invention is a capacitor-less DRAM cell, it operates in the same manner as a DRAM cell except with an improved retention state compared to typical prior art DRAM cells.

When the DRAM device is in a high conductance state (i.e., a logic 0 is written), some of the excess hole charge in the floating body tunnels through the trapping layer and gets trapped. Consequently the device conductance is further increased, thus creating a "fat 0" where the DRAM device has an increased hole charge in comparison to typical prior art DRAM cells.

Conversely, when electrons are generated in the floating body to create the lower conductance state (i.e., a logic 1 is written), some of the excess electrons get trapped into the trapping layer with the resulting effect of still lower conductance. Hence, a "fat 1" is created. A transistor that stores a "fat 1" has an elevated threshold voltage and, therefore, less leakage current than a typical prior art device. Thus the effect of the trapping layer of the DRAM transistor of the present invention is to improve the logic separation and associated signal margin of the DRAM state and/or state retention.

For NVRAM operation, the NVRAM control gate is pulsed to a negative potential concurrent to pulling up both the bitline and the NVRAM wordline to V_{dd}. This drives the access device to saturation. A strong lateral field generated between the floating body and the control gate drives excess holes, generated in the body, to tunnel through the tunnel oxide and to be trapped. Due to this hole trapping, the adjacent body potential is raised to a positive potential where it is held permanently until the trapped state is discharged by trapping electrons. This is a non-volatile "zero" state. It can be sensed readily (i.e., a read 0) by turning the access device wordline up and sensing the current through the bitline.

To write a non-volatile "one" state, the control gate is pulsed positive concurrent to forward bias either the drain-body diode or the source-body diode. This injects excess electrons into the floating body. The trapping layer traps the excess electrons that cause a

permanent negative potential. As a result, the access device V_t is raised and the device does not conduct during a logical one read operation. The device remains in the non-volatile logical 1 state until the trapping layer electrons are neutralized by injecting holes during an erase operation.

For multi-level NVRAM operation, the above-described logical 0 and 1 states can be addressed or read either by the wordline of the access device (corresponding to a $V_{t\text{-}WL}$ of a logic"0" and a $V_{t\text{-}WL}$ of a logic"1" respectively) or by the control gate device (corresponding to a $V_{t\text{-}CG}$ of a logic "0" and a $V_{t\text{-}CG}$ of a logic "1" respectively). For the same degree of charge storage in the trapping layer, the control gate V_t's would be significantly different than those of the access device V_t's and, therefore, bi-level addressing could be achieved and the device achieves virtual dual-bit storage for the same written state.

Additional multi-level non-volatile storage could be achieved by directly storing increasing density of charges (i.e., electrons or holes) into the trapping layer by appropriate programming of the control gate conventionally with increasing programming voltages (positive or negative). This generates multiple high V_t states (i.e., multiple $V_{t\text{-}CG}$ logical ones). Addressing is performed using both the DRAM wordline and NVRAM control gate and establishing appropriate sensing schemes to separate all levels of storage states.

The DRAM-NVRAM cell of the present invention can also be converted into a PROM for use in a field programmable gate array (FPGA), an alterable switch, or a BIOS-storing application. The cell can be converted into a PROM by appropriate electron charge density or hole charge density stored into the trapping layer by programming via the NVRAM control gate.

The floating plate NVRAM transistor of the present invention requires a significantly lower field across the dielectric stack for programming via the control gate. This results in an increased endurance capability (e.g., $> 10 \times 10^{10}$ cycles) and scalability both in geometry and voltages. With appropriate selection and scaling of the gate insulator stack (i.e., tunnel insulator, trapping layer, charge blocking layer), the average programming field can be reduced to between 3×10^6 and 6×10^6 V/cm compared to a typical average field of 12×10^6 V/cm for a floating gate device.

The following table illustrates one embodiment of operational voltages for a gate insulator stack comprising a 4.5 nm tunnel insulator, a 6 nm Silicon-Silicon rich-Nitride

trapping dielectric, and a 6.5 nm SiO_2 charge blocking layer that requires a programming voltage below 9 V. This table is for purposes of illustration only as different embodiments of the present invention can use different operational voltages to enable the read or write operational modes.

OPERATION	V_{BL}	V_{WL}	V_{SL}	V_{CG}	V_{sub}
DRAM write "0"	2.5	2.5	Gnd	Gnd	-2.5
DRAM write "1"	Gnd	0.8	-2.5	Gnd	-2.5
DRAM read "0"	Float	0.8	Gnd	Gnd	-2.5
DRAM read "1"	Float	0.8	Gnd	Gnd	-2.5
NVRAM write "0"	2.5	2.5	Gnd	-2.5/-9	-2.5
NVRAM write "1"	Gnd	0.8	-2.5	2.5/9	-2.5
NVRAM read "A0"	Float	0.8	Gnd	Gnd	-2.5
NVRAM read "A1"	Float	0.8	Gnd	Gnd	-2.5
NVRAM read "B0"	Float	0.0	Gnd	1.2	-2.5
NVRAM read "B1"	Float	0.0	Gnd	1.2	-2.5

In this table, V_{BL} is the bitline voltage, V_{WL} is the DRAM wordline voltage, V_{SL} is the DRAM source line or region voltage, V_{CG} is the NVRAM control gate/wordline voltage, and V_{sub} is the negative substrate bias. The "Ax" and "Bx" of the above table describes the two states of a single bit (i.e., bit A or bit B). In the case of the NVRAM reading of "A1" and "B1", the bitline potentials are unchanged.

The above-described logic separation between "Ax" and "Bx" could be used for multi-level storage. The programming voltage, $V_{x\text{-}CG}$, could be altered to $V_{y\text{-}CG}$ to create a different logic level separation "Ax" and "Bx" for multi-level storage. Substantially similar approaches can be used for PROM writing of "1" and "0".

Figure 4 illustrates a functional block diagram of a memory device 400 that can incorporate the DRAM-NVRAM memory cells of the present invention. The memory device 400 is coupled to a processor 410. The processor 410 may be a microprocessor or some other type of controlling circuitry. The memory device 400 and the processor 410 form part of an electronic system 420. The memory device 400 has been simplified to focus on features of the memory that are helpful in understanding the present invention.

The memory device includes an array of memory cells 430 that can be comprised of the multi-level DRAM-NVRAM cells previously illustrated. The memory array 430 is arranged in banks of rows and columns. The gates of each row of memory cells is coupled with a wordline while the drain and source connections of the memory cells are coupled to bitlines.

An address buffer circuit 440 is provided to latch address signals provided on address input connections A0-Ax 442. Address signals are received and decoded by a row decoder 444 and a column decoder 446 to access the memory array 430. It will be appreciated by those skilled in the art, with the benefit of the present description, that the number of address input connections depends on the density and architecture of the memory array 430. That is, the number of addresses increases with both increased memory cell counts and increased bank and block counts.

The memory device 400 reads data in the memory array 430 by sensing voltage or current changes in the memory array columns using sense/buffer circuitry 450. The sense/buffer circuitry, in one embodiment, is coupled to read and latch a row of data from the memory array 430. Data input and output buffer circuitry 460 is included for bi-directional data communication over a plurality of data connections 462 with the controller 410. Write circuitry 455 is provided to write data to the memory array.

Control circuitry 470 decodes signals provided on control connections 472 from the processor 410. These signals are used to control the operations on the memory array 430, including data read, data write (program), and erase operations. The control circuitry 470 may be a state machine, a sequencer, or some other type of controller.

The memory device illustrated in Figure 4 has been simplified to facilitate a basic understanding of the features of the memory. A more detailed understanding of internal circuitry and functions of memories are known to those skilled in the art.

CONCLUSION

In summary, the embodiments of the integrated DRAM-NVRAM memory of the present invention provide the functions of DRAM storage that does not require stack or trench capacitors for data storage as well as non-volatile memory storage in a memory cell. The NVRAM transistor is capable of multi-level storage in order to increase memory density without additional transistors.

The DRAM-NVRAM cell functionally integrates DRAM and non-volatile memory while overcoming the limitations of both. For example, the DRAM function can use the trapping layer of the NVRAM transistor to enhance charge storage so that a refresh cycle is not required. Similarly, the NVRAM function uses a floating plate for charge storage that is more scalable than a typical floating gate device.

Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement that is calculated to achieve the same purpose may be substituted for the specific embodiments shown. Many adaptations of the invention will be apparent to those of ordinary skill in the art. Accordingly, this application is intended to cover any adaptations or variations of the invention. It is manifestly intended that this invention be limited only by the following claims and equivalents thereof.

What is claimed is:

1. A memory cell comprising:
a dynamic random access memory device for storing data; and
a non-volatile random access memory device coupled to the dynamic random access memory device such that the data storage by the dynamic random access memory device is enhanced.

2. The memory cell of claim 1 wherein the non-volatile random access memory device is comprised of a floating plate charge storage region.

3. The memory cell of claim 1 wherein the dynamic random access memory device is comprised of a floating body transistor.

4. The memory cell of claim 1 wherein the non-volatile random access memory device is a multi-level device capable of storing a plurality of data bits.

5. The memory cell of claim 4 wherein the plurality of data bits are addressed by a first voltage level of a set of read voltage levels applied to the memory cell.

6. The memory cell of claim 1 wherein the non-volatile random access memory device enhances the data storage by the dynamic random access memory device by providing non-volatile state retention.

7. The memory cell of claim 1 wherein the dynamic random access memory device is a capacitor-less DRAM cell and the non-volatile random access memory device is a floating plate transistor.

8. An integrated DRAM-NVRAM memory cell comprising:
a field effect transistor having a floating body portion; and
a floating plate transistor coupled to the field effect transistor through the floating body portion.

9. The memory cell of claim 8 and further including:
the field effect transistor having a drain region and a first source region located on opposite sides of the floating body; and
the floating plate transistor having a second source region and sharing the drain region with the field effect transistor, the first and second source regions each capable of generating a depletion region that are substantially close enough to create the floating body portion.

10. The memory cell of claim 8 wherein the field effect transistor and the floating plate transistor are vertical transistors that are fabricated in trenches and pillars formed into a substrate material.

11. The memory cell of claim 8 wherein the floating body portion stores data for a DRAM function of the cell.

12. The memory cell of claim 8 wherein the floating plate increases field effect transistor conductance by accepting excess hole charge from the floating body.

13. The memory cell of claim 8 wherein the floating plate decreases field effect transistor conductance by accepting excess electrons from the floating body.

14. The memory cell of claim 11 wherein the floating plate transistor enables the field effect transistor to store data without refresh.

15. An integrated DRAM-NVRAM memory cell comprising:
a substrate comprising a plurality of trenches that form a pillar between each pair of trenches;
a doped drain region in the top of each pillar;
a doped source region at the bottom of each of the plurality of trenches;
a vertical gate formed along a side wall of a first pillar;
a trapping layer formed along an opposite side wall of the first pillar; and
a vertical control gate formed over the trapping layer such that the vertical control gate is shared by an adjacent NVRAM transistor.

16. The memory cell of claim 15 wherein the doped drain regions are n+ regions and the substrate is a p-type conductivity.

17. The memory cell of claim 15 wherein, during operation of the memory cell, the source regions at the bottom of the first and the second trenches are capable of generating depletion regions that substantially meet under the first pillar to form a floating body in the first pillar.

18. The memory cell of claim 15 wherein the trapping layer is separated from the first pillar by a tunnel layer and the trapping layer is separated from the vertical control gate by a charge blocking layer.

19. The memory cell of claim 18 wherein the tunnel layer and the charge blocking layer are comprised of silicon dioxide.

20. The memory cell of claim 15 and further including a bitline coupling each of the drain regions in a column of memory cells.

21. The memory cell of claim 15 wherein the vertical gate is coupled to a DRAM wordline and the vertical control gate is coupled to a NVRAM wordline.

22. An electronic system comprising:
a processor for generating memory control signals; and
a DRAM-NVRAM integrated memory array coupled to the processor and operating in response to the memory control signals, the memory array having a plurality of memory cells, each cell comprising:
a dynamic random access memory device for storing data; and
a non-volatile random access memory device coupled to the dynamic random access memory device such that the data storage by the dynamic random access memory device is enhanced.

23. The system of claim 22 wherein the dynamic random access memory device and the non-volatile random access memory device share a floating body that stores a charge for the dynamic random access memory device.

24. A method for operation of an integrated DRAM-NVRAM cell, the cell comprising a DRAM gate, a NVRAM control gate, a DRAM source region, a NVRAM source region, a shared drain region, and a bitline coupled to the shared drain region, the method comprising:
applying a ground potential to the NVRAM control gate;
applying a positive bias voltage to the DRAM gate; and
applying the ground potential to the NVRAM source region wherein the DRAM is in one of a read or write operational mode in response to the positive bias voltage.

25. The method of claim 24 wherein the ground potential applied to the NVRAM control gate is shared by an adjacent NVRAM cell.

26. The method of claim 24 wherein the ground potential applied to the NVRAM control gate causes the integrated DRAM-NVRAM cell to operate as a DRAM function.

27. The method of claim 24 wherein the bitline is allowed to float.

28. The method of claim 24 wherein the bitline is biased at 2.5V.

29. The method of claim 24 and further including applying a negative substrate bias.

30. The method of claim 29 wherein the negative substrate bias is –2.5V.

31. A method for operation of an integrated DRAM-NVRAM cell, the cell comprising a DRAM gate, a NVRAM control gate, a DRAM source region, a NVRAM source region, a shared drain region, and a bitline coupled to the shared drain region, the method comprising:
applying a ground potential to the NVRAM control gate;

applying a positive bias voltage to the DRAM gate;

applying the ground potential to the bitline; and

applying a negative bias voltage to the NVRAM source region to write a logical one to a DRAM portion of the integrated DRAM-NVRAM cell.

32. The method of claim 31 wherein the positive bias voltage is 0.8V and the negative bias voltage is -2.5V.

33. The method of claim 32 and further including applying a 9.0V bias to the NVRAM control gate in order to program a NVRAM logical "0".

34. A method for operation of an integrated DRAM-NVRAM cell having a DRAM function and a NVRAM function, the cell comprising a DRAM gate, a NVRAM control gate, a DRAM source region, a NVRAM source region, a shared drain region, and a bitline coupled to the shared drain region, the method comprising:

applying a ground potential to the NVRAM source region;

applying a negative bias voltage to the NVRAM control gate;

applying a first positive bias voltage to the bitline; and

applying a second positive bias voltage to the DRAM gate in order to write a logical zero to the NVRAM function of the DRAM-NVRAM cell.

35. The method of claim 34 wherein the negative bias voltage is –2.5V and the first and second positive bias voltages are 2.5V.

36. The method of claim 35 and further including applying a –9.0V bias to the NVRAM control gate in order to program a NVRAM logical "1".

37. A method for operation of an integrated DRAM-NVRAM cell having a DRAM function and a NVRAM function, the cell comprising a DRAM gate, a NVRAM control gate, a DRAM source region, a NVRAM source region, a shared drain region, and a bitline coupled to the shared drain region, the method comprising:

applying a negative bias voltage to the DRAM source region;

applying a first positive bias voltage to the NVRAM control gate;

applying a ground potential to the bitline; and

applying a second positive bias voltage to the DRAM gate in order to write a logical one to the NVRAM function of the DRAM-NVRAM cell.

38. The method of claim 37 wherein the negative bias voltage is –2.5V, the first positive bias voltage is 2.5V, and the second positive bias voltage 0.8V.

39. A method for operation of an integrated DRAM-NVRAM cell having a DRAM function and a NVRAM function, the cell comprising a DRAM gate, a NVRAM control gate, a DRAM source region, a NVRAM source region, a shared drain region, and a bitline coupled to the shared drain region, the method comprising:

applying a ground potential to the NVRAM source region;

applying a first voltage to the NVRAM control gate; and

applying a second voltage to the DRAM gate in order to read one of a plurality of data bits from the NVRAM function in response to the first voltage and the second voltage.

40. The method of claim 39 wherein the bitline is floating.

41. The method of claim 39 wherein when the first voltage is 0V and the second voltage is 0.8V, a first bit of the plurality of bits is read.

42. The method of claim 39 wherein when the first voltage is 1.2V and the second voltage is 0V, a second bit of the plurality of bits is read.

43. The method of claim 39 wherein the DRAM function operates as an access device for the NVRAM function.

44. An integrated DRAM-NVRAM memory cell comprising:

a silicon-on-insulator substrate comprising a layer of insulating material;

a doped drain region in the top of each pillar;

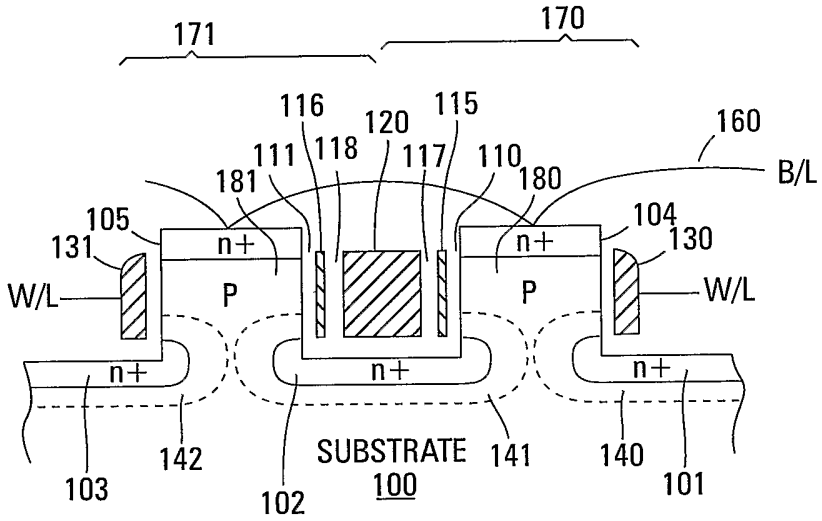
a doped source region at the bottom of each pillar;

a vertical gate formed along a side wall of a first pillar;

a trapping layer formed along an opposite side wall of the first pillar; and

a vertical control gate formed over the trapping layer such that the vertical control gate is shared by an adjacent NVRAM transistor.

45. The memory cell of claim 44 wherein the insulating material is an oxide.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170
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115
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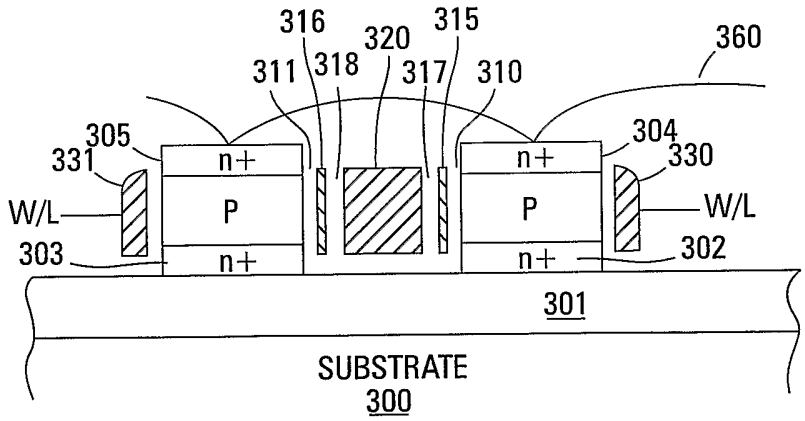
111
118
117
110
B/L
181
180
105
104
131
130
n+
n+
W/L
P
P
W/L
n+
n+
n+
142
SUBSTRATE
141
140
103
102
100
101

Fig. 1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320
315
360
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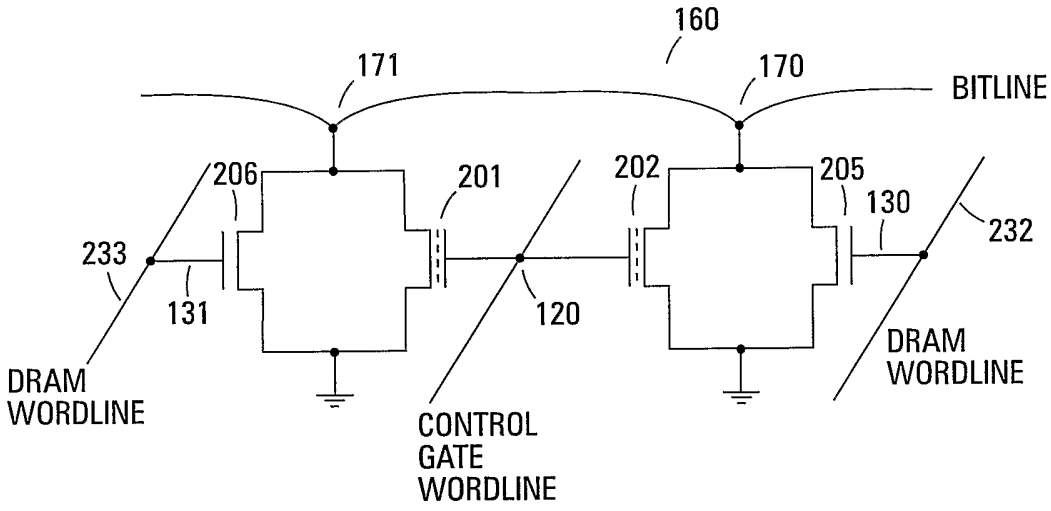
310
305
304
331
330
n+
n+
W/L
P
P
W/L
303
n+
n+
302
301
SUBSTRATE
300

Fig. 3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171
170
BITLINE
206
201
202
205
130
232
233
131
120
DRAM
WORDLINE
CONTROL
GATE
WORDLINE
DRAM
WORDLINE

Fig. 2

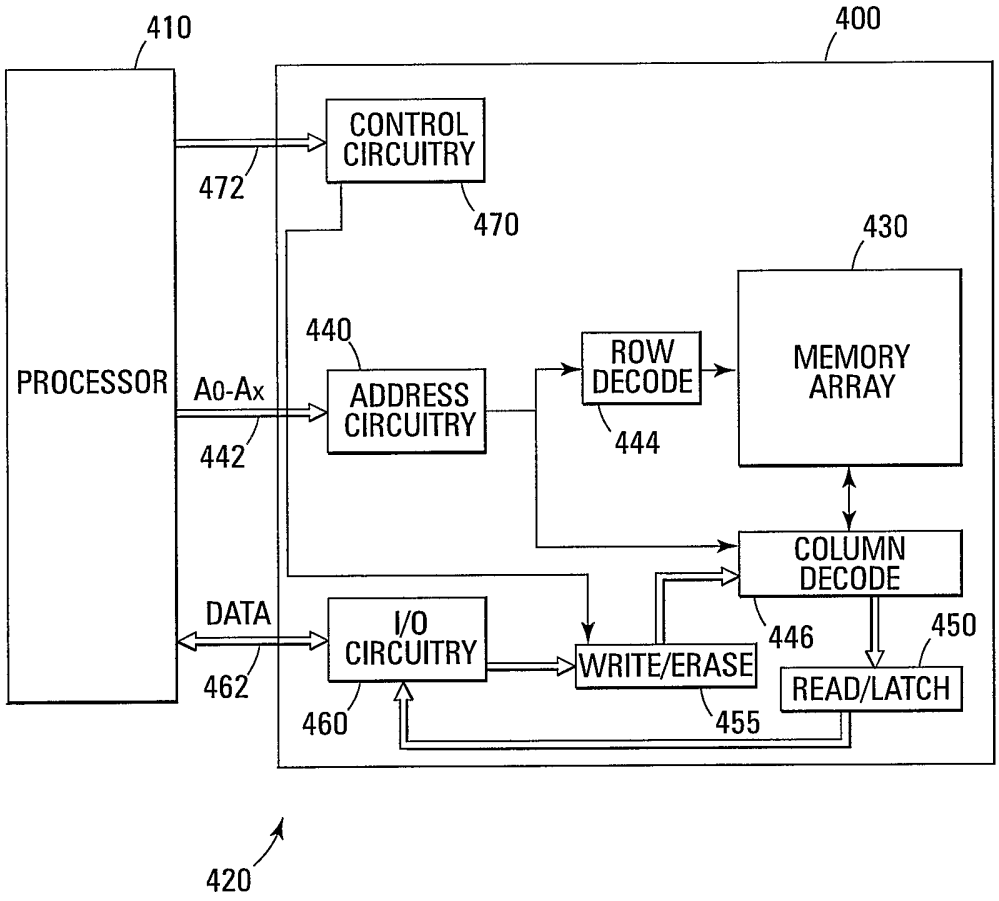
410
400
CONTROL CIRCUITRY
472
470
430
440
ROW DECODE
MEMORY ARRAY
PROCESSOR
A0-Ax
ADDRESS CIRCUITRY
444
442
COLUMN DECODE
DATA
I/O CIRCUITRY
446
450
WRITE/ERASE
READ/LATCH
462
460
455
420

Fig. 4

INTERNATIONAL SEARCH REPORT

International Application No
../US2005/029150

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G11C11/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 140 552 A (YAMAUCHI ET AL) 18 August 1992 (1992-08-18) abstract; figures 1-9 column 4, line 5 - column 5, line 5	1-14, 22-43
X	US 6 282 118 B1 (LUNG HSIANG-LAN ET AL) 28 August 2001 (2001-08-28) figures 1-5 column 2, line 60 - column 3, line 55	1-14, 22-43
X	EP 1 383 134 A (HEWLETT-PACKARD DEVELOPMENT COMPANY, L.P) 21 January 2004 (2004-01-21)	1,8
A	paragraph '0001! - paragraph '0014!	2-7,9-45

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
10 November 2005	18/11/2005

Name and mailing address of the ISA	Authorized officer
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INTERNATIONAL SEARCH REPORT

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

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