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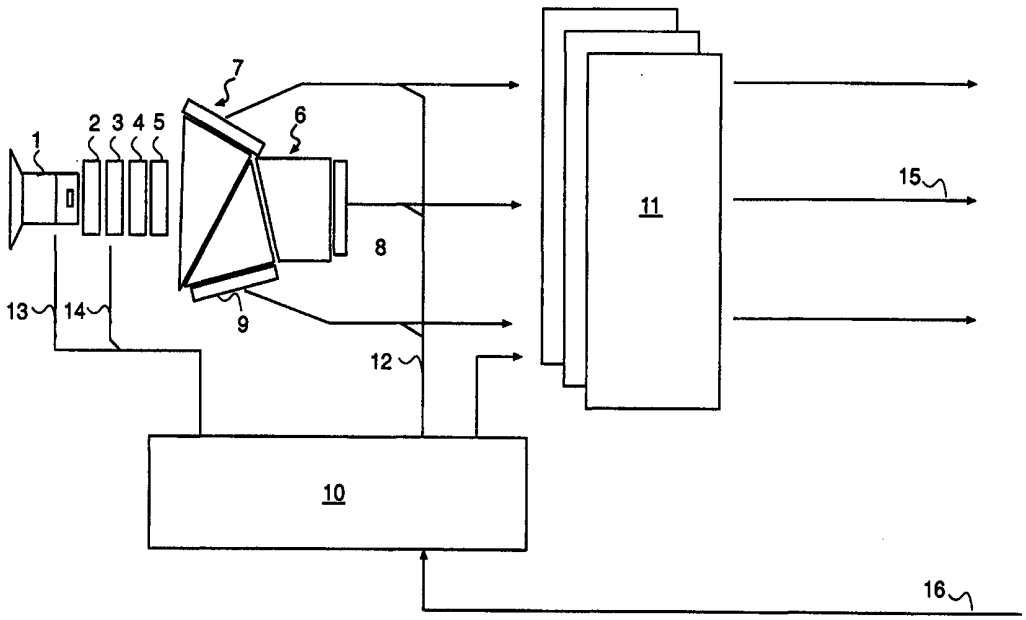

(57) Abstract

The present invention includes a television camera architecture that progressively scans the scene, providing a complete picture for each frame of video output. The camera produces high-definition digital format that may be converted into any of a number of industry accepted formats. The invention includes a flexible formatter that allows the user to specify the required format.

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HIGH DEFINITION TELEVISION CAMERA AND FORMATTER

Cross Reference to Related Applications

This application claims priority to U.S. Provisional Application Serial No. 60/076,281, entitled "HIGH DEFINITION TELEVISION CAMERA AND FORMATTER," filed on February 27, 1998.

Field of the Invention

This invention relates to television cameras and related equipment that capture images in high-definition form.

Background of the Invention

Electronic video cameras provide a method of converting scenes, objects, movie film, actors, etc., to electronic video signals that may be viewed, recorded, transformed, and transmitted to one or multiple receiver sites in a realistic manner. The unique architecture of the present invention provides an improved capability to capture and manipulate visual information so that it may be used by television stations to originate broadcast-quality (contribution quality) images in full motion and full color. The present invention includes a camera architecture that is capable of progressively scanning the scene, providing a complete picture for each frame of video output. Progressive scanning provides several advantages, such as: fewer motion artifacts associated with the scanning process, and a video output that is directly compatible with computer manipulation techniques.

The present invention increase the utility of the equipment associated with the production and distribution of high-definition television ("HDTV"). Such equipment may include, but is not limited to, high-definition cameras, tape recorders, switching units, special effect generators, and compression engines. The increase in utility resides in the ability of the equipment to accept and distribute an electrical signal representing a HDTV picture in any of a variety of industry-accepted formats and convert that signal to a common format. For example, in the case of a camera, the internal signal of the camera may be in a particular format, but the user might need another format. The present invention includes a programmable formatter that may convert a video signal to user specified format (or formats).

Object of the Invention

It is therefore an object of the present invention to provide an efficient image capture system that may be used as the initial input to a broadcast or post-production facility.

It is another object of the present invention to provide a formatter that utilizes application specific software to operate on the video signal.

It is a further object of the present invention to convert one HDTV signal into another with a common set of electronics.

It is a further object of the present invention to provide a flexible formatter for video signal conversion.

It is a further object of the present invention to increase the utility of the equipment associated with the production and distribution of HDTV.

It is yet another object of the present invention to provide a camera that progressively scans the scene.

Summary of the Invention

The present invention includes a high definition digital television camera comprising: an optical sensor that generates a digital output; a front-end electronics section that receives and processes the digital output from the optical sensor and produces a digital video signal; a back-end electronics section that receives and processes the digital video signal that is generated by the front-end electronics section and produces a format specified by the camera user, wherein the back-end electronics section includes a flexible formatter capable of converting the digital video signal to a plurality of different formats.

The flexible formatter may comprise one or more field programmable gate array(s). The field programmable gate array may convert the digital video signal from progressive to interlaced format. The flexible formatter may include a storage media for storing the digital video signal during conversion. The flexible formatter may further include a digital to analog converter for converting the digital video signal to analog format. The flexible formatter may further comprise a programming port for receiving control data that controls the formatter and determines the formats for the digital video signal.

Alternatively, the flexible formatter may comprise a general purpose video processor. The flexible formatter may further comprise a storage media for storing the digital video signal during

conversion. The flexible formatter may further comprise a read only memory device for storing program code that controls the video processor and controls the conversion of the digital video signal. In addition, the flexible formatter that includes a video processor may also further comprise a digital to analog converter for converting the digital video signal to analog format.

The camera's optical sensor may include an optical lens and optical filters. In addition, the optical sensor may include an optical prism assembly. The optical sensor may be controlled by control signals that are provided by an optical decoder.

The camera's front-end electronics section may include a logic circuit that corrects for defective pixels. In addition the front-end electronics section may include a logic circuit that corrects for shading of the video signal. The camera may include a digital accumulator that provides automatic gain control. The camera may also comprise programmable random-access memories for compensating for non-linearities in the optical sensors and for transforming the color of the sensor's digital output.

Brief Description of the Drawings

Figure 1 is a block diagram illustrating the optical and initial electrical portions of the invention.

Figure 2 is a block diagram showing the details of the front-end electronics.

Figure 3 is a block diagram showing details of the architecture for the back-end electronics of the camera and its relationship with the studio equipment.

Figure 4 shows the invention implemented using a field-programmable logic array.

Figure 5 shows an alternative method for the implementation of the invention using one or more processors.

Detailed Description of the Invention

Fig. 1 illustrates the optical and initial electrical portions of the invention. The front-end optics and electronics are used with all versions of cameras produced with this unique architecture. Light from the scene enters the lens **1** that is designed for high-quality video production. The lens has three servo-controlled settings: iris, focus, and zoom (effective focal length). Input commands from the operator or the camera control unit (CCU) can change these three settings. The control signals are received on the system control bus **16** and decoded by the optical decoder electronics **10**.

Signals from the optical decoder electronics **10** then control the three lens settings through line **13**. Behind the lens are provisions for two sets of filter wheels **2** and **3**, a quarter-waveplate **4**, and a low-pass spatial optical filter **5**. The filters in the first wheel **2** can be used for color correction, while those in the second wheel **3** are neutral density filters to reduce the light intensity to the photosensors in bright sunlight conditions. The quarter-wave plate and the spatial low-pass filter reduce video artifacts (moire patters) that would be generated under certain conditions by the tessilated structure of the photosensors. The present invention includes an optical prism assembly **6** that serves two purposes: it splits the incoming light into three beams directed at the photosensors **7**, **8**, and **9**, and it contains dichotic filters on its inner two surfaces to provide the correct spectral response of the photosensors. The dichotic filters are arranged such that red light from the scene impinges on photosensor **7**, blue light impinges on photosensor **9**, and green light passes through the two filters to impinge on photosensor **8**.

Photosensors **7**, **8**, and **9** are pixel arrays of CMOS devices with structures similar to memories, which may be addressed to scan over the device area by address lines **12**, also controlled by the decoded electronics **10**. In addition to scanning control, the control electronics also provide the photosensor chips with signals that control the black level, the gain of the sensor (its sensitivity to light), and the integration time of the sensor. As the optically active section of the CMOS devices are scanned, digitized signals are generated by the CMOS photosensors. The digital value produced at the output of each photosensor is proportional to the light intensity at each pixel. Thus, the three photosensors provide three digital outputs (nominally 10 to 12 bits each, for a total of 30 to 36 bits) that represent the color tristimulus video signals. The outputs of the sensors are directed to the front-end electronics section **11** that performs the basic signal processing necessary to provide a video signal of professional quality. Details of front-end electronics are given in Fig. 2.

The front-end electronics may be used in all versions of cameras designed with this unique architecture. The order of the signal path through the processing electronics may change slightly depending on the application of the camera (e.g., medical imaging, entertainment, movie films, etc.). The tristimulus signals **15** from the photosensors (shown in Fig. 1 as photosensors **7**, **8**, and **9**) are initially presented to the defective-pixel correction logic **201**. This logic block modifies the value of any pixel that is designated defective. Pixels are designated defective by tests performed at the time of manufacture of the camera, or during testing routines after the camera system is deployed. A non-volatile memory **202** contains the address of each defective pixel. The logic interpolates the defective pixel's value from the value of the pixel on either side of the defective one. In this manner,

a defective pixel assumes the luminance that is the average along the horizontal line of nearest neighboring pixels. Video from the defective pixel logic is presented to the shading correction logic **203**.

The shading correction ensures that the signal out of this block has a zero value when the light level into the camera is zero. It removes the 'offsets' or systematic errors that may impair the dynamic range of the video signal. The shading correction unit subtracts a constant, prestored value from each of the digital inputs presented to the shading correction unit. The prestored values are read into the correction unit over the system control bus **16**.

The automatic gain control ("AGC") signal generator **204** provides a digital output that is proportional to the illumination in the central portion of the video picture. The AGC functions as a simple digital accumulator which sums the outputs of the red, green, and blue channels over a set of pixels on a frame-by-frame basis. The digital AGC data is accumulated over time (an integration period) to provide a measure of the general illumination of a scene. The data from the output of the AGC is used by other sections of the camera, especially by the lens section to control the iris of the lens. In this manner, the video output of the camera stays relatively constant with changes in illumination. Furthermore, the weighting of the AGC output can be programmed to meet different demands. For example, the bottom of the frame can contribute more heavily than the top of the frame when scanning a scene where the ground illumination changes more rapidly than the sky illumination.

The non-linearity compensation **205** may be programmable random-access memory ("RAM"). The number of bits (nominally 10 or 12) is the same for input and output. The data in the RAM determine the transfer function between the digital input and the digital output for each of the three colors. The data in the RAM are provided by the system control bus and compensates for non-linearities that are inherent in the photosensors.

The color transformation matrix **206** permits the exchange of any color for any other color. Like the non-linearity compensation RAM, the color transformation matrix operates on equal number of bits for both input and output (typically 30 or 36). However, the color transformation RAM permits any two colors to affect a third color. In this manner, any color at its input (R', G', B') can be recapped to any other color (R", G", B").

The present invention allows for the introduction of non-linearities in the optical signal in order to improve picture quality. This introduction is accomplished by the gamma correction RAM. The gamma correction RAM **207** is similar in construction to the non-linearity compensation RAM.

The gamma correction RAM holds data that permit the operator to adjust the input and output black levels, the maximum gain of the gamma curve at black, and the overall gamma value. The transfer curve that defines the input versus output for the gamma correction is calculated using an exponential relationship involving the number of bits (typically 10 or 12), the black level, and the clamp level.

Lastly, the Finite Impulse Response ("FIR") filter **208** provides a method to keep out-of-band signals from being propagated to the output of the camera. The finite response filter is based on a multiply-accumulate function to prevent artifacts created by the digital processing from propagating further in the system. The response characteristic of the FIR filter is determined by coefficients loaded into the multiplier registers by the control bus.

Fig. 3 shows details of the architecture for the back-end electronics of the camera and its relationship with the studio equipment. The back-end electronics implements the optional features that provide for flexibility of use and minimize the risk of obsolescence for the camera equipment. The incoming video signal **301** is routed to the format converter **302**. The format converter consists of a large programmable-logic array and associated memory that can convert the camera's internal parallel format to other formats that are more compatible with the production, post-production, and transmission standards. From the format converter, the video signal can be recorded or transmitted via either of two down-links: wireless or fiber-optic cable.

For Electronic News Gathering ("ENG") applications, the camera is fitted with a digital data recorder **303** that can record the audio and video information. The use of a high-density, low-cost media such as magnetic or optical tape, disks, or solid state recording technology, provides a method to record and play back the audio and video information captured by the camera.

An alternative to the direct recording of video signals is the transmission of the signals through a radio frequency ("RF") wireless telemetry down-link **314** to a control room. A pair of short-range wireless transceivers **304**, **308** provide a digital link between the camera and -- if necessary -- the studio equipment and between the studio's camera control unit **307** and the camera. Because of the high data rate for the camera-to-studio transmission, the carrier frequency of the link is typically in the 2.4 GHZ band (or higher frequency) and typical operating power is on the order of .25 Watt to 1 Watt. the wireless link is intended for short-haul applications such as sports events, real-time news broadcasts, and studio applications where a cable is not desired. The wireless transceiver also provides for the studio camera control unit to up-link data from the studio camera control unit **307** to the camera.

The fiber-optic interface between the camera **305** and the control room **309** is intended for camera to control room communications in studios where cable may be accommodated. Digital fiber-optic connections offer a wide bandwidth for video down-link with high reliability of transmission. The fiber-optic link **359** also supports the transmission of the commands from the studio's camera control unit **307** on the up-link.

The local camera control unit **306** is attached to the camera and generates the signals that are carried on the system control bus **16** and preset the mode of operation of the hardware shown in Fig. 2. A similar and redundant unit may be located in the studio control room for remote operation of the camera, if desired. The camera control unit provides signals that conform to industry-standard serial bus much as the Inter IC or I^2C-Bus by Phillips. Data can be transferred at a rate of up to 100 kbits/s in the standard mode, or up to 400 kbits/s in the fast mode.

The present invention also includes a novel formatter **302** capable of implementing at least two approaches to the conversion process. In one approach, shown in Fig. 4, one or more field programmable logic devices may be used as logic gates and registers necessary for converting signals from one standard format to another. This programmable logic approach has the advantage of speed (short propagation time between input signal and output signal) and cost effectiveness. The disadvantage of the approach is that it requires specialized design tools to implement the designs. The design tools typically comprise software to configure the devices for particular applications. However, the design for converting from one standard format to another, need only be created once but may be implemented in many signal processors (e.g., HDTV cameras). A second approach, shown in Fig. 5, includes the use of a general-purpose video processor. Video processors are currently available from several manufactures, including Philips. Data may be read into a memory, processed by the general purpose processor, and then read out of memory. If processing speed is not sufficient to accomplish the conversion within one frame time of the picture, then multiple processors may be used to increase the processing bandwidth. This approach includes the use of software code for controlling the television signal conversion from one standard format to another.

Fig. 4 shows the Field Programmable Logic Array ("FPLA")-Based Flexible Formatter **302**. The digital video signal input is shown at **301** entering the FPLA **401**. The array may consist of a large number of interconnected gates, the interconnection of which can be programmed through data inputs **409** to create a logic network that implements the digital video format conversion. Some conversions, such as from progressive to interlaced signals, require a means to temporarily store the progressive video signal such that the conversion can be accomplished. This means is provided by

the video read/write memory **403**. The video memory is connected to the FPLA through data, address, and control lines **404**. For an analog output **407**, a digital to analog converter **405** may also be connected to the outputs of the FPLA via data and control lines **406**. For users who require a digital signal, a direct digital connection can be made to the outputs of the FPLA at **408**. The FPLA is programmed to convert from one particular format to another by the data provided at the FPLA programming port **409**. This input accepts the signals that program the interconnections of the gates.

Fig. 5 shows an alternative embodiment of the flexible formatter **302** of the present invention. The formatter disclosed in Fig. 5 is a processor-based flexible formatter capable of accomplishing the same conversion result as the FPLA based formatter. However it uses different components to make the conversion. The digital video input signal **301** is presented to the video processor or processors for storage in a video memory **403**, for operation by the software code stored in the program read-only memory **503**. The data, address, and control lines for the video memory and the program memory are shown as **404** and **504**, respectively. If the conversion is from a digital format to another digital format, the output **408** comes from a data port of the processor directly. If an analog signal **407** is required, the digital representation of the signal is converted to analog by the digital-to-analog converter **405** controlled by its interface **406**. The control of the conversion is accomplished by storing the conversion algorithm in the program read-only memory at port **503**.

The flexible formatter **302** of the present invention may convert the digital video signal **301** to any of a number of different user-specified formats. Typically, the digital video signal **301** will be in 1280 x 720 progressive format, but also may be in 720 x 480 progressive. The output signal **408** may be produced in a number of different formats including NTSC, PAL, 720 x 483 progressive, 720 x 480 progressive, 640 x 360 progressive, 360 x 256 progressive, 1920 x 1080 interlaced, 720 x 483 interlaced. The formatter **302** of the present invention may include a plurality of output ports so that multiple signals may be produced simultaneously. For example, the present invention includes a formatter that may produce an NTSC, interlaced and progressive format simultaneously in order to accommodate television broadcast facilities that do not transmit HDTV signals exclusively.

It will be apparent to those skilled in the art that various modifications and variations can be made in the construction and configuration of the present invention without departing from the scope or spirit of the invention. Various modifications and variations can be made in the construction of the front-end electronics without departing from the cope or spirit of the invention's use of a flexible formatter. For example, corrections for signal irregularities may not be necessary in all cases and

certain logic circuits may be eliminated. Thus, it is intended that the present invention cover the modifications and variations of the invention provided they come within the scope of the appended claims and their equivalent.

I CLAIM:

1. A high definition digital television camera comprising:

an optical sensor that generates a digital output;

a front-end electronics section that receives and processes the digital output from the optical sensor and produces a digital video signal;

a back-end electronics section that receives and processes the digital video signal that is generated by the front-end electronics section and produces a format specified by the camera user, wherein said back-end electronics section includes a flexible formatter capable of converting the digital video signal to a plurality of different formats.

2. The camera of claim 1, wherein said flexible formatter comprises a field programmable gate array.

3. The camera of claim 2, wherein said field programmable gate array converts the digital video signal from progressive to interlaced format.

4. The camera of claim 2, wherein said flexible formatter includes a storage media for storing the digital video signal during conversion.

5. The camera of claim 2, wherein said flexible formatter includes a digital to analog converter for converting the digital video signal to analog format.

6. The camera of claim 2, wherein said flexible formatter further comprises a programming port for receiving data, wherein said control data controls the operation of said formatter and determines the format for the digital video signal.

7. The camera of claim 1, wherein said flexible formatter comprises a general purpose video processor.

8. The camera of claim 7, wherein said flexible formatter further comprises a storage media for storing the digital video signal during conversion.

9. The camera of claim 8, wherein said flexible formatter further comprises a read only memory device for storing program code that controls the video processor and controls the conversion of the digital video signal.

10. The camera of claim 7, wherein said flexible formatter further comprises a digital to analog converter for converting the digital video signal to analog format.

11. The camera of claim 1, wherein said optical sensor further comprises an optical lens.

12. The camera of claim 1, wherein said optical sensor further comprises optical filters.

13. The camera of claim 1, wherein said optical sensor further comprises an optical prism assembly.

14. The camera of claim 1, wherein said optical sensor is controlled by control signals that are converted by an optical decoder into an optical control signal.

15. The camera of claim 1, wherein said front-end electronics section further comprises defective pixel correction logic.

16. The camera of claim 1, wherein said front-end electronics section further comprises shading correction logic.

17. The camera of claim 1, wherein said front-end electronics section further comprises a digital accumulator that provides automatic gain control.

18. The camera of claim 1, wherein said front-end electronics includes programmable random-access memory for compensating for non-linearities in the optical sensors.

19. The camera of claim 1, wherein said front-end electronics includes programmable random-access memory for transforming the color of the digital output.

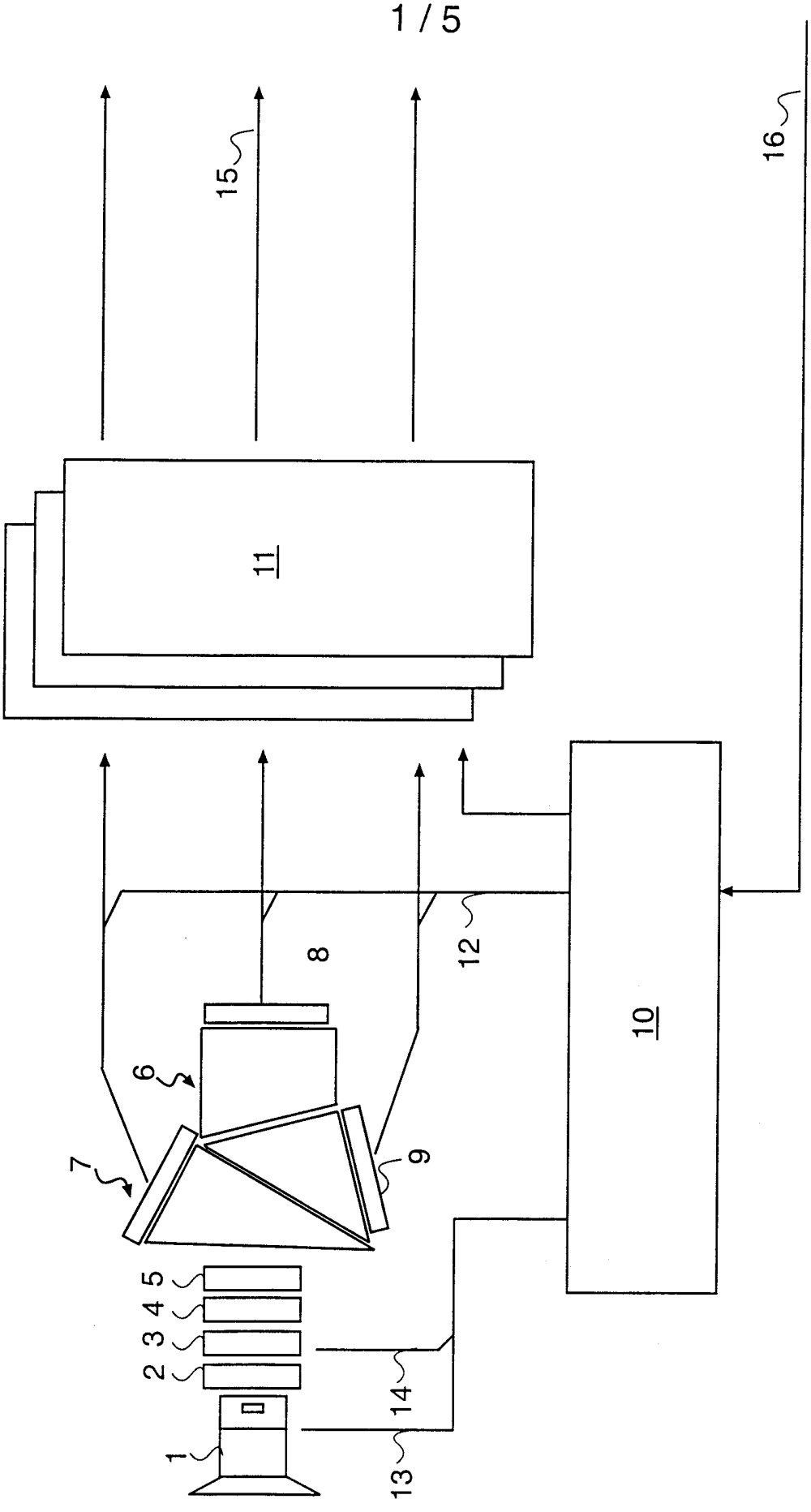

FIG. 1

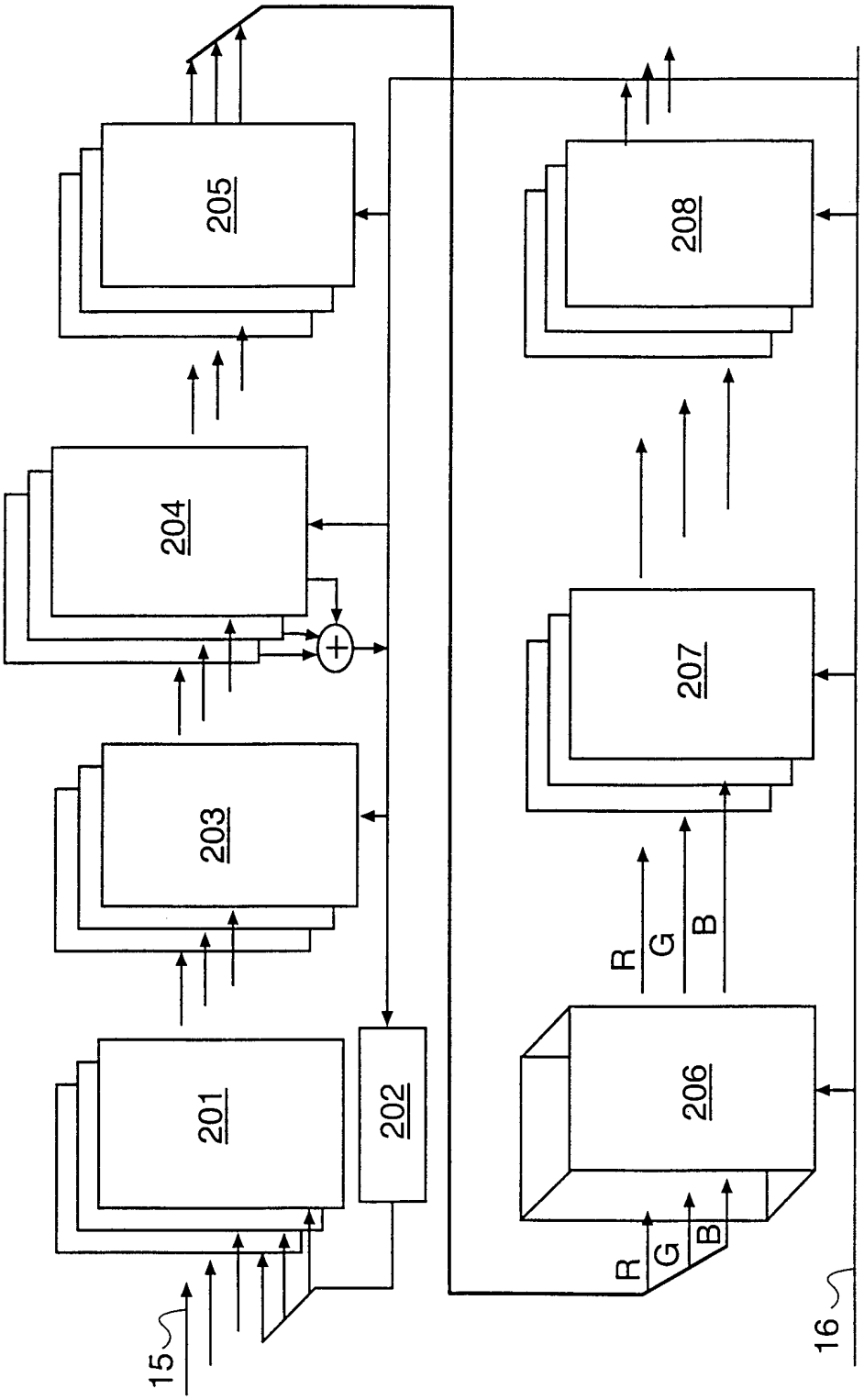

FIG. 2

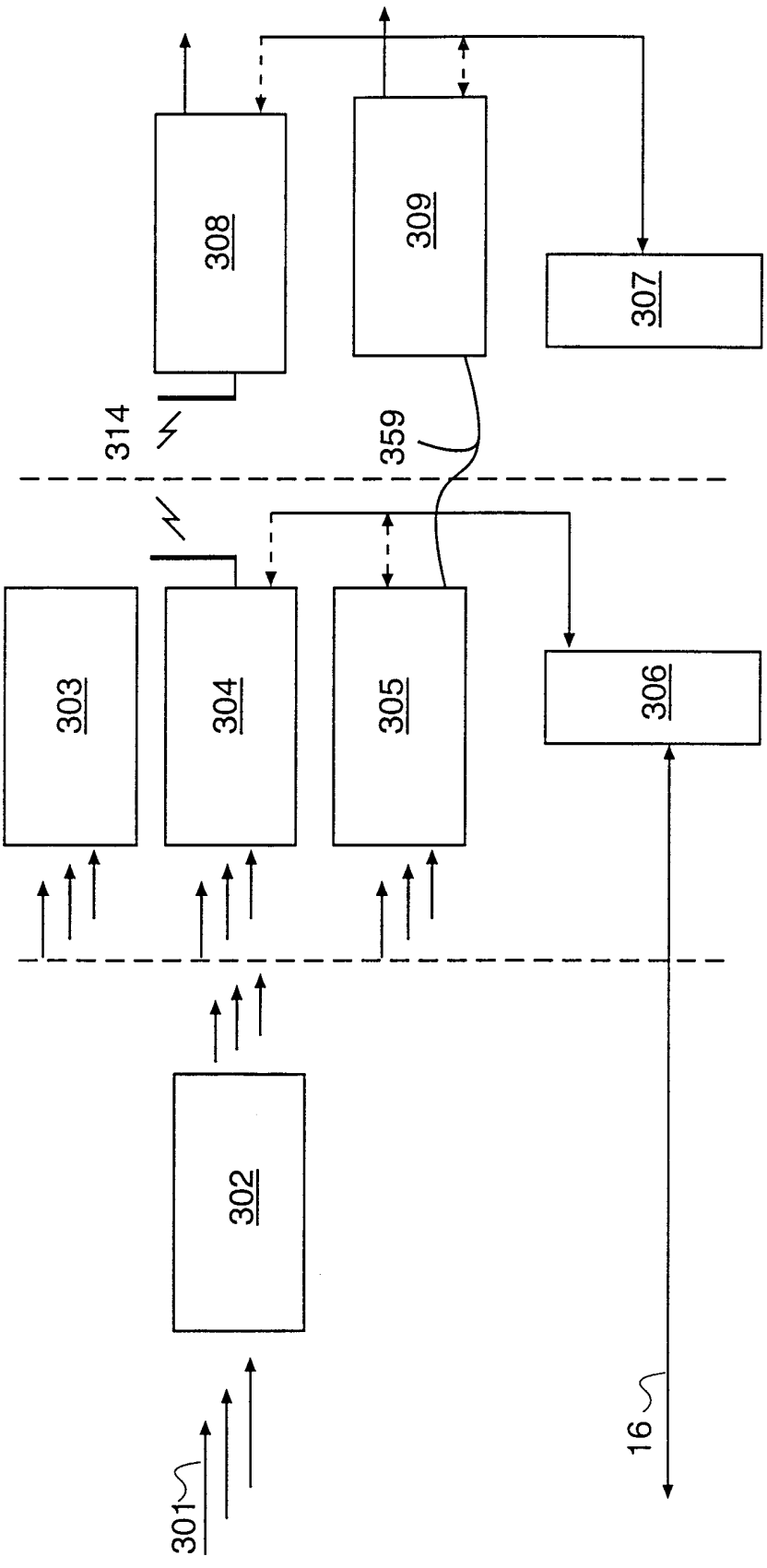

FIG. 3

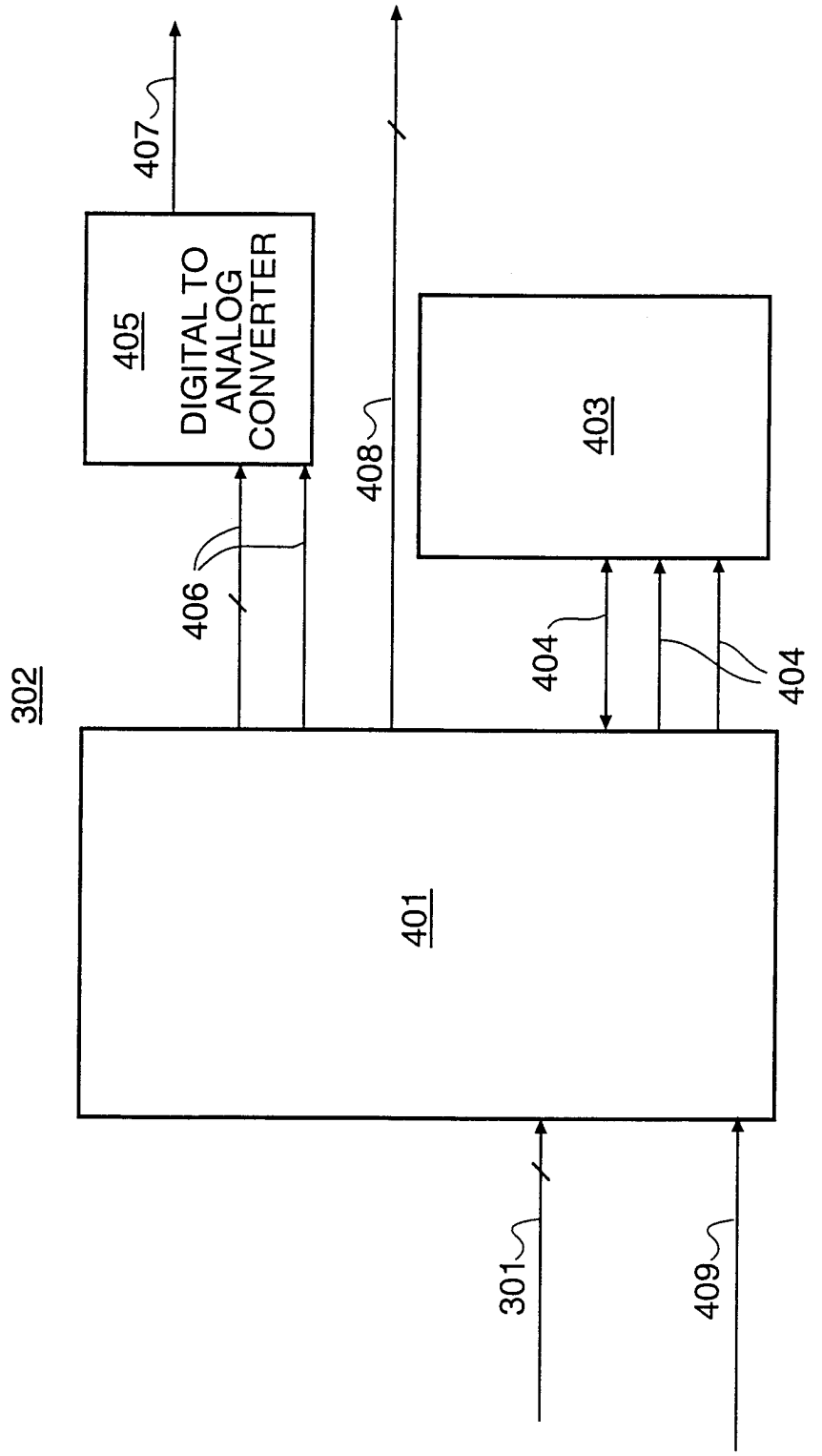
407
405
DIGITAL TO ANALOG CONVERTER
408
403
406
404
404
302
401
301
409

FIG. 4

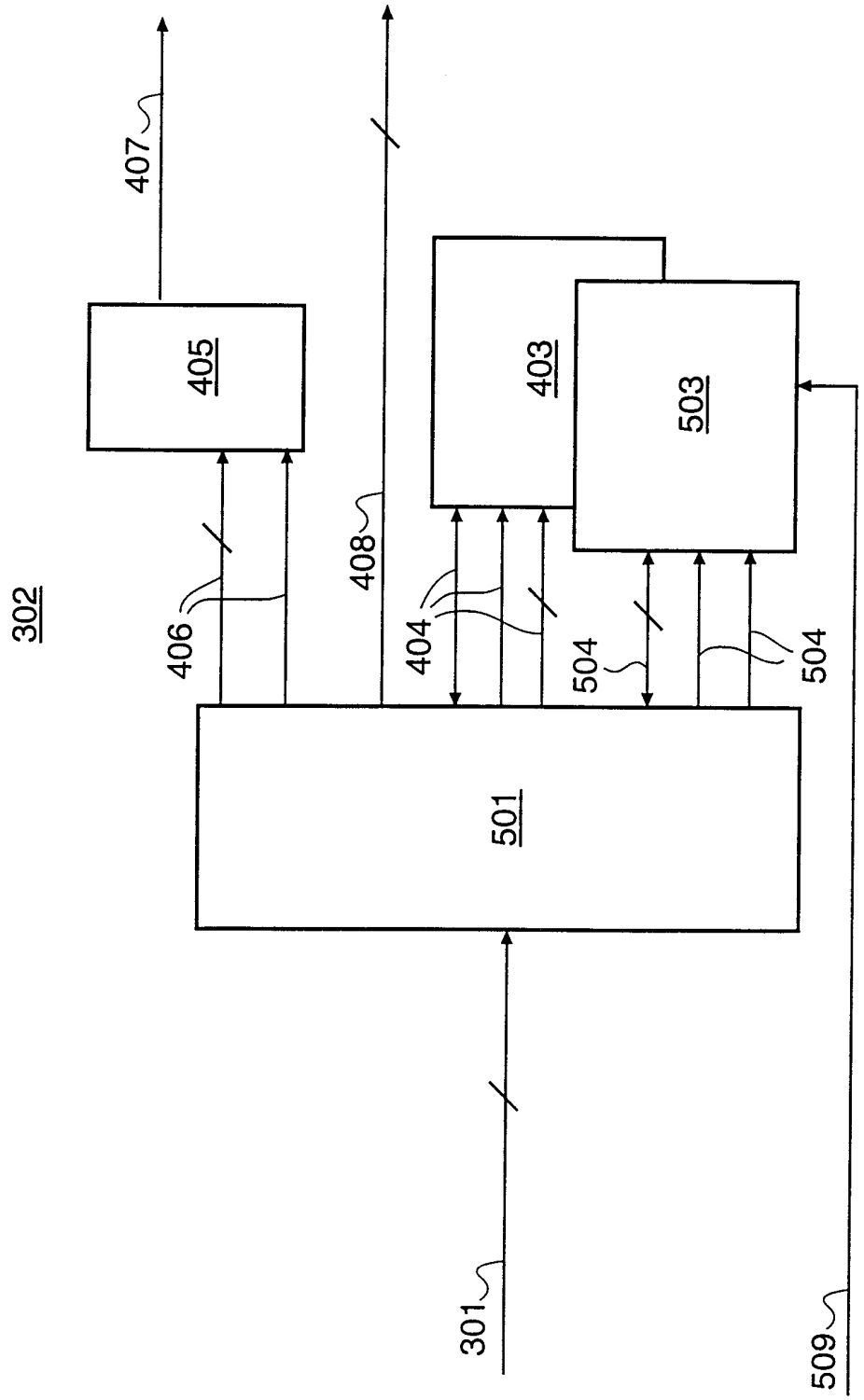

FIG. 5