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(12) **United States Patent**
Hwang et al.

(10) **Patent No.: US 6,265,318 B1**
(45) **Date of Patent: *Jul. 24, 2001**

(54) **IRIDIUM ETCHANT METHODS FOR ANISOTROPIC PROFILE**

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(73) Assignee: **Applied Materials, Inc.**, Santa Clara, CA (US)

(*) Notice: This patent issued on a continued prosecution application filed under 37 CFR 1.53(d), and is subject to the twenty year patent term provisions of 35 U.S.C. 154(a)(2).

Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 27 days.

(21) Appl. No.: **09/251,633**

(22) Filed: **Feb. 17, 1999**

Related U.S. Application Data

(63) Continuation-in-part of application No. 09/006,092, filed on Jan. 13, 1998.

(51) **Int. Cl.**[7] **H01L 21/00**

(52) **U.S. Cl.** **438/720**; 216/67; 216/75; 438/742

(58) **Field of Search** 438/710, 712, 438/720, 738, 742, 650, 686; 216/41, 67, 75

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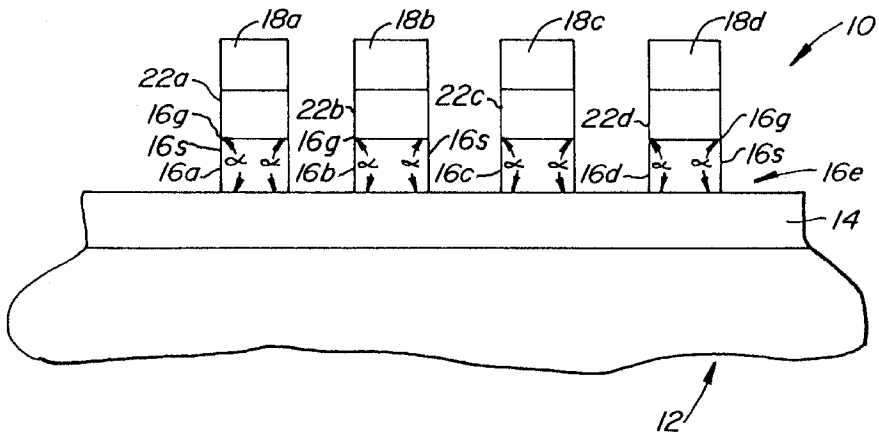
(74) *Attorney, Agent, or Firm*—Shirley L. Church

(57) **ABSTRACT**

A method of etching an electrode layer (e.g., a platinum electrode layer or an iridium electrode layer) disposed on a substrate to produce a semiconductor device including a plurality of electrodes separated by a distance equal to or less than about 0.3 μm and having a profile equal to or greater than about 85°. The method comprises heating the substrate to a temperature greater than about 150° C., and etching the electrode layer by employing a high density inductively coupled plasma of an etchant gas comprising oxygen and/or chlorine, argon and a gas selected from the group consisting of BCl_3, HBr, HCl and mixtures thereof. A semiconductor device having a substrate and a plurality of electrodes supported by the substrate. The electrodes have a dimension (e.g., a width) which include a value equal to or less than about 0.3 μm and a profile equal to or greater than about 85°.

140 Claims, 17 Drawing Sheets



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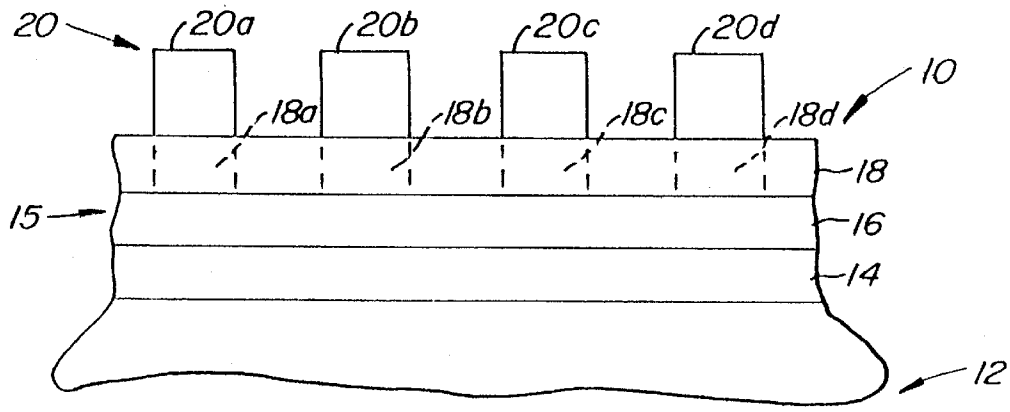


FIG. 1.

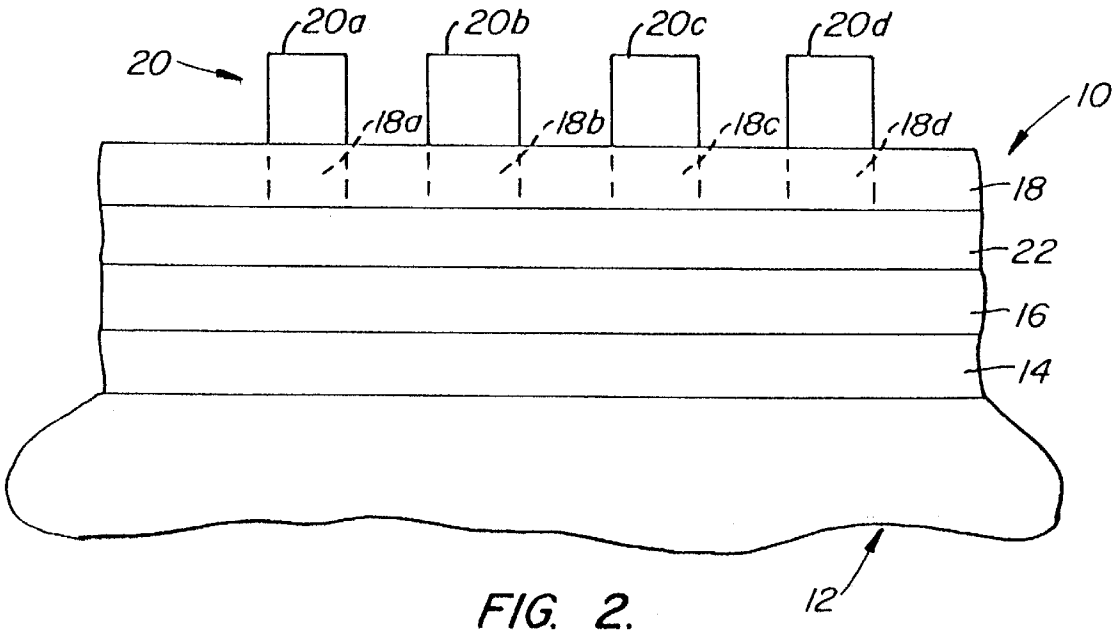
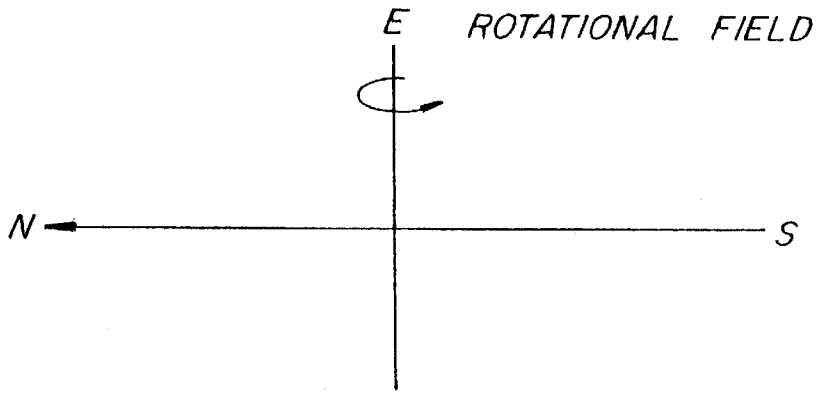


FIG. 2.



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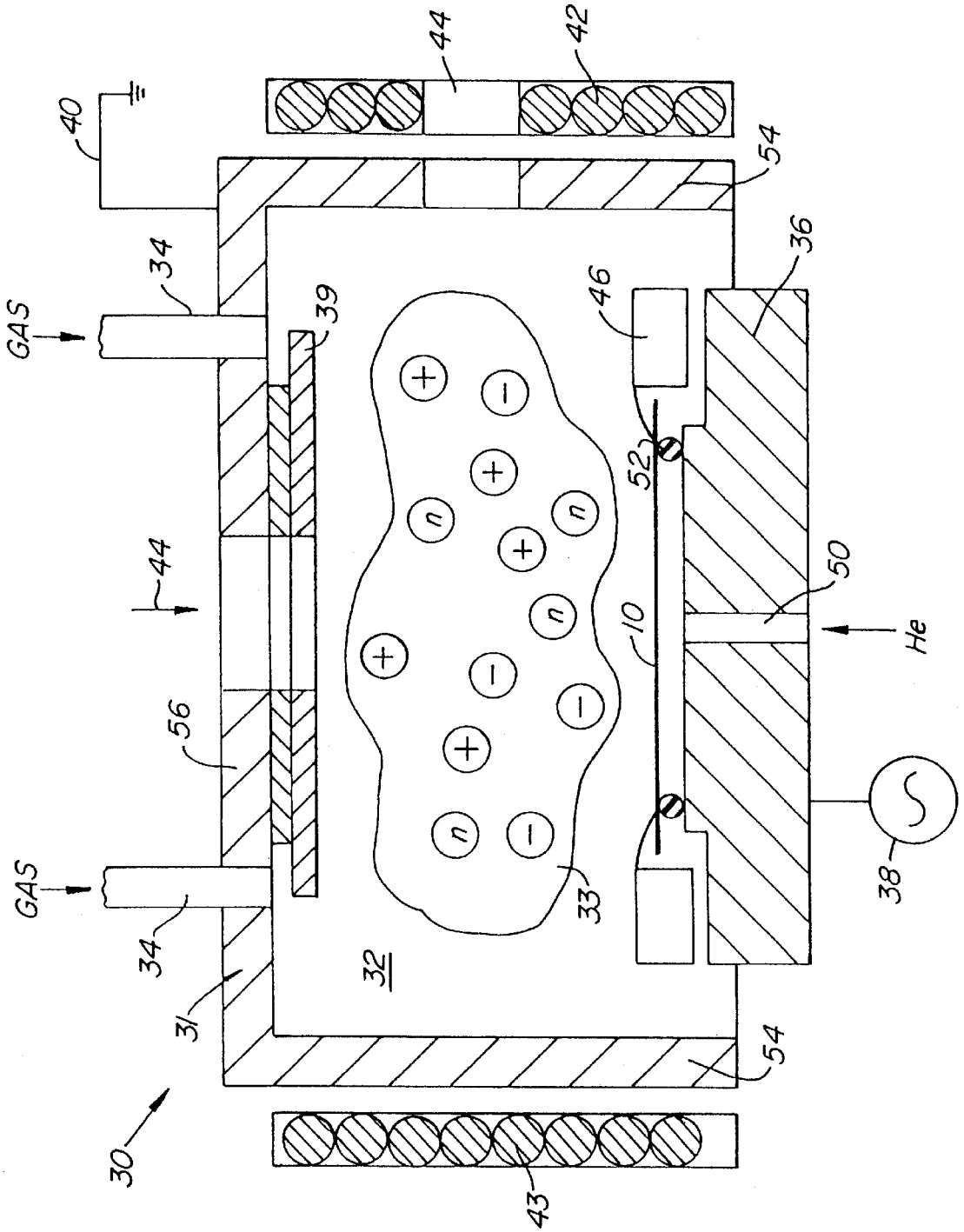
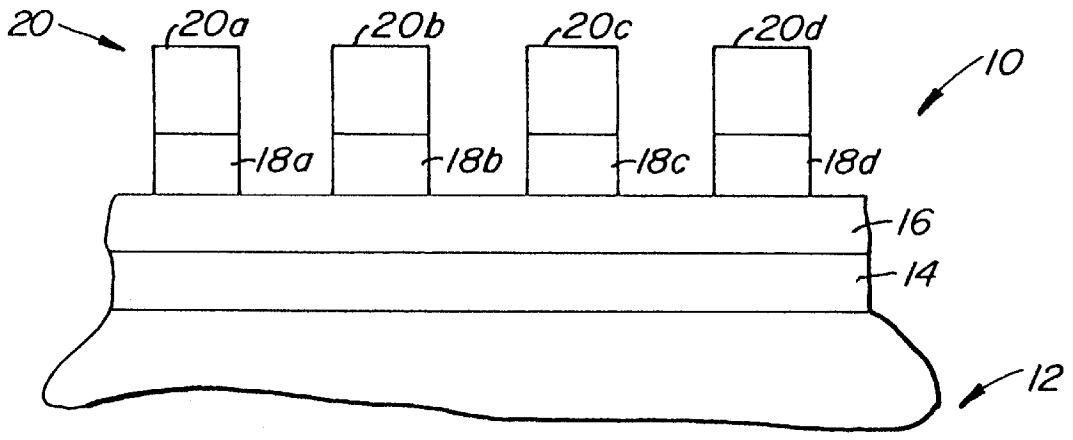


PRIOR ART

FIG. 3.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20a
20b
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20d
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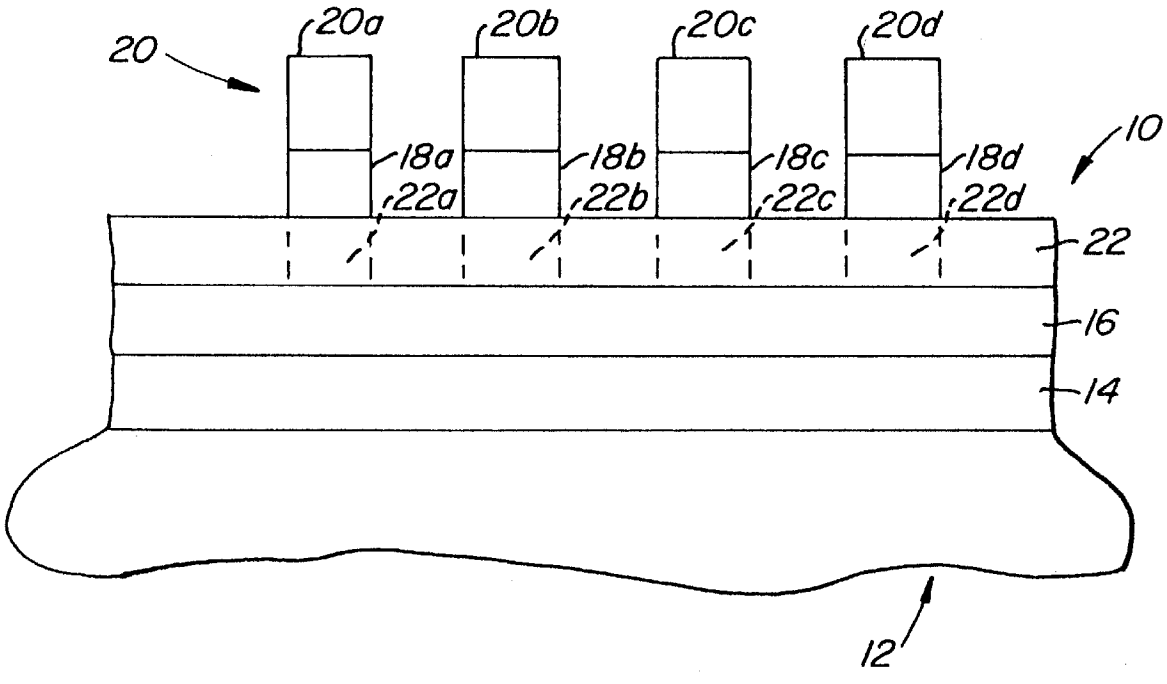
18a
18b
18c
18d
16
14
12

FIG. 5.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20a
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20c
20d
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18a
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FIG. 6.

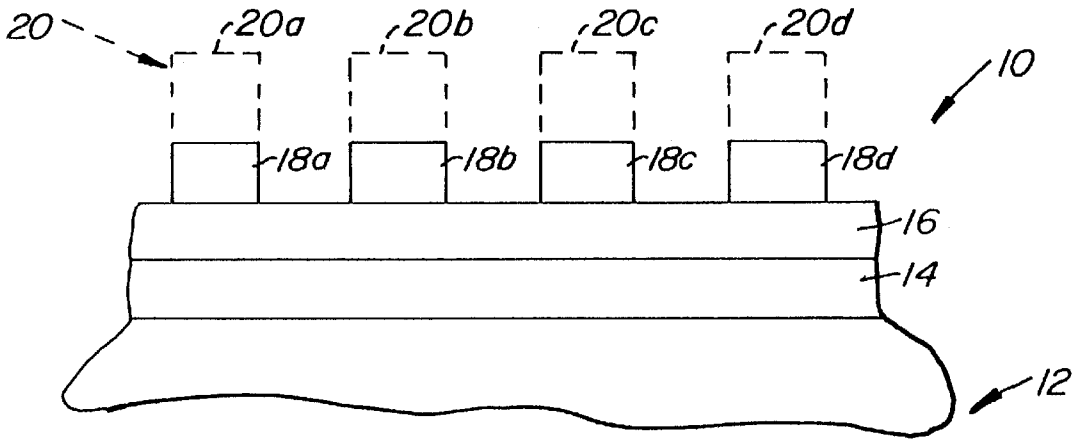
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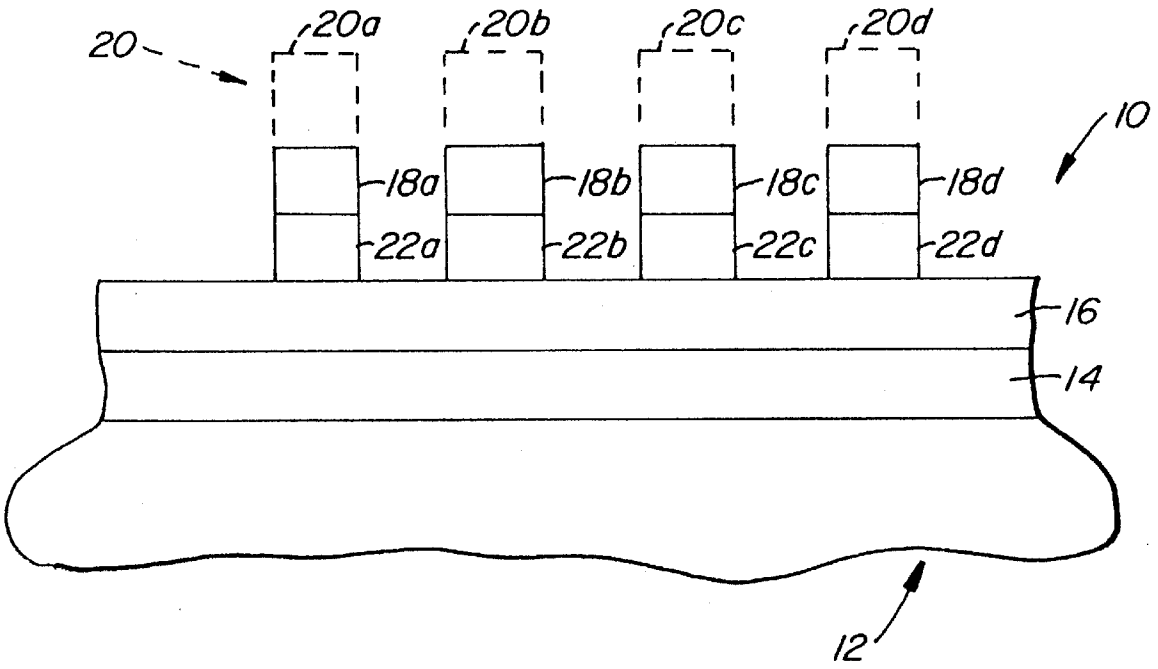
FIG. 7.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20a
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18a
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18c
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22a
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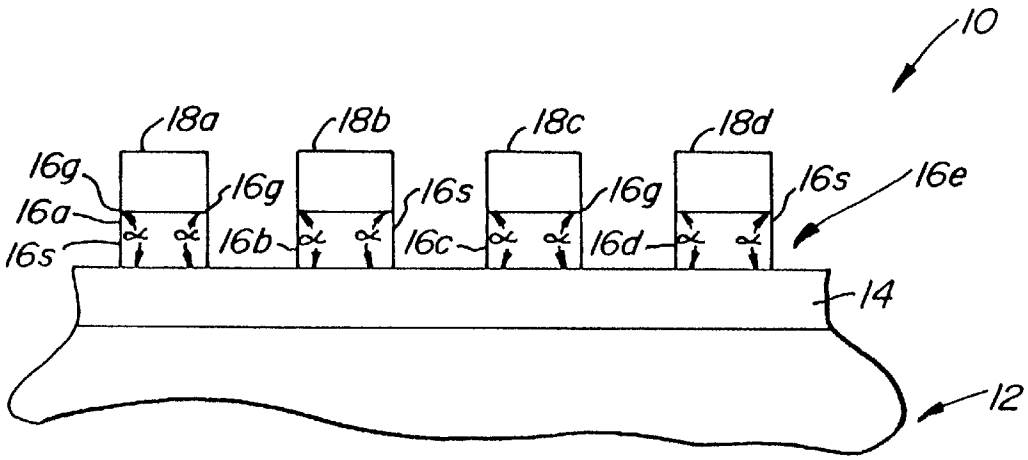
22d
16
14
12

FIG. 8.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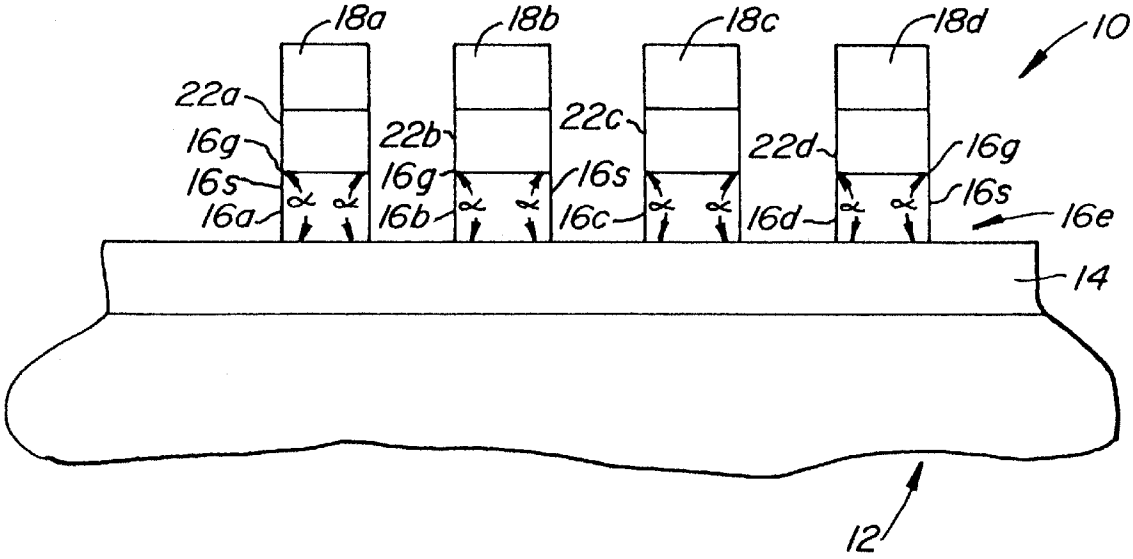
18a
18b
18c
18d
16g
16a
16s
16g
16b
16s
16c
16g
16d
16s
16e
14
12

FIG. 9.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18c
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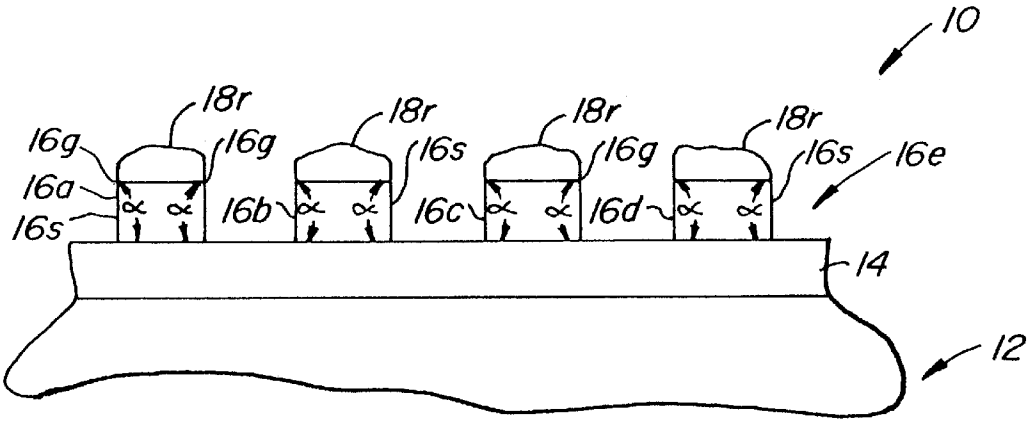
10
22a
16g
16s
16a
22b
16g
16b
16s
16c
22c
22d
16d
16g
16s
16e
14
12

FIG. 10.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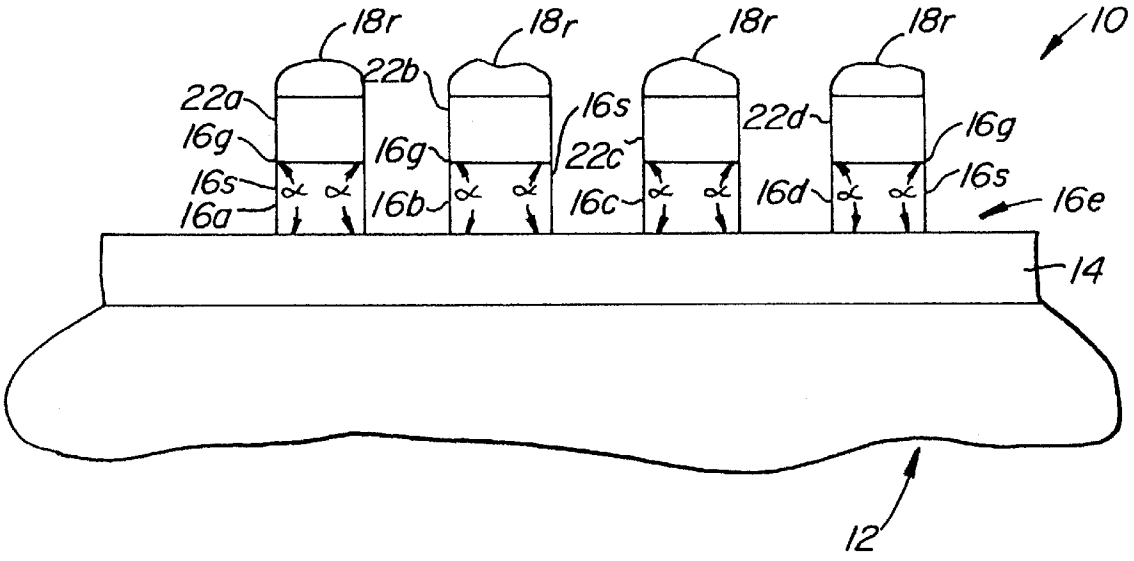
18r
18r
18r
18r
16g
16g
16s
16g
16s
16e
16a
16s
16b
16c
16d
14
12

FIG. 11.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18r
18r
18r
10
22a
22b
16s
22d
16g
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22c
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16s
16e
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16c
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14
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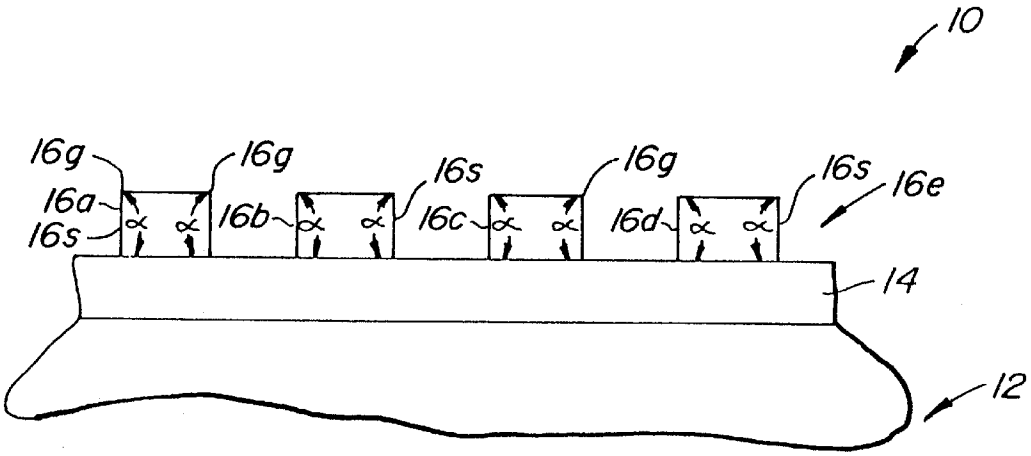
FIG. 12.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16g
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16c
16d
14
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FIG. 13.

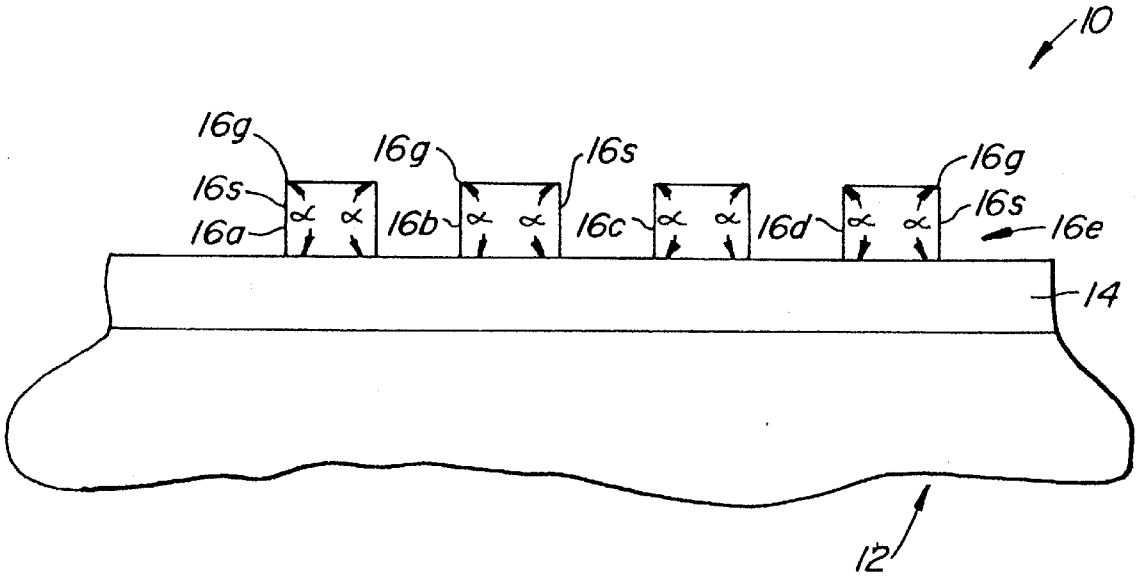
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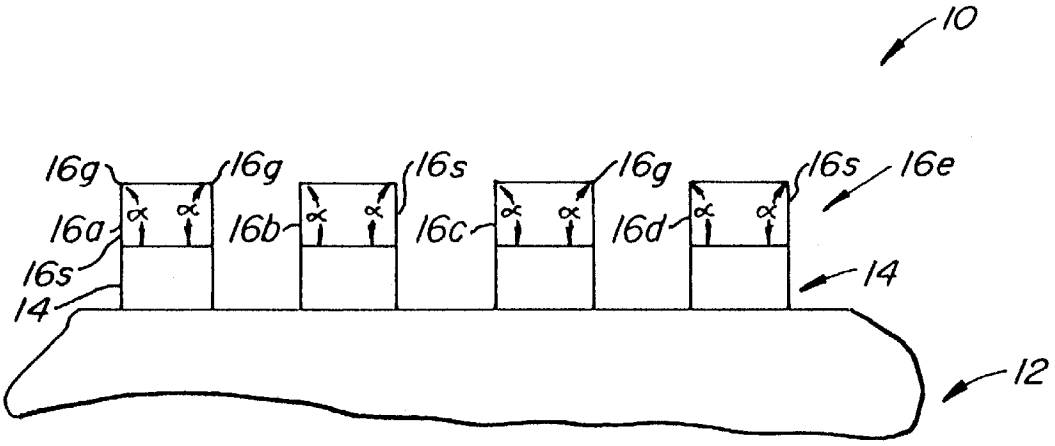
FIG. 14.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16s
16e
16a
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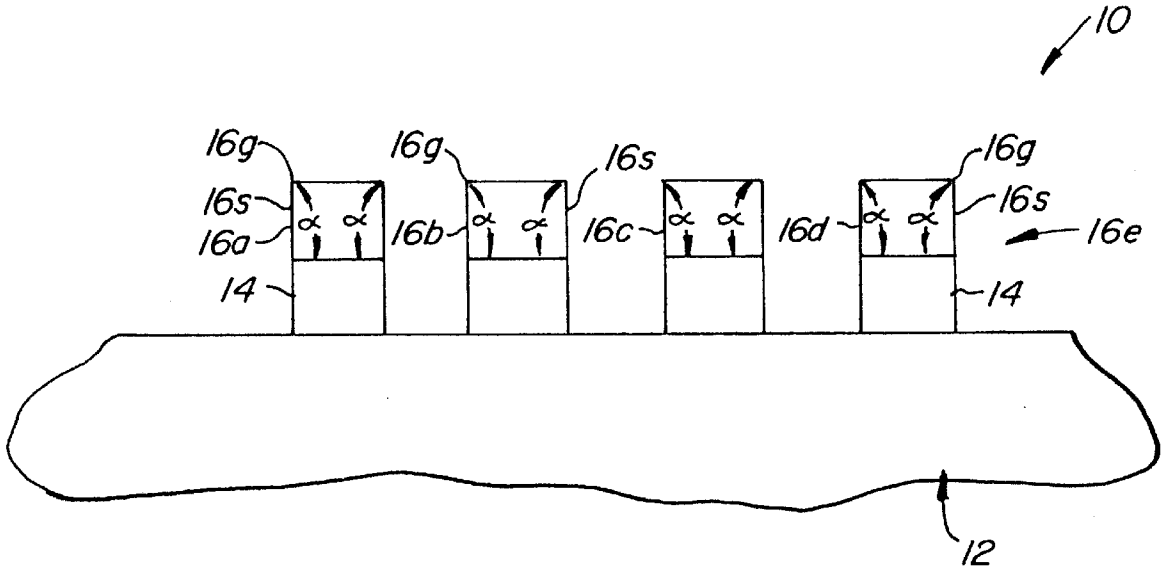
16c
16d
16s
14
14
12

FIG. 15.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16g
16s
16s
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16e
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14
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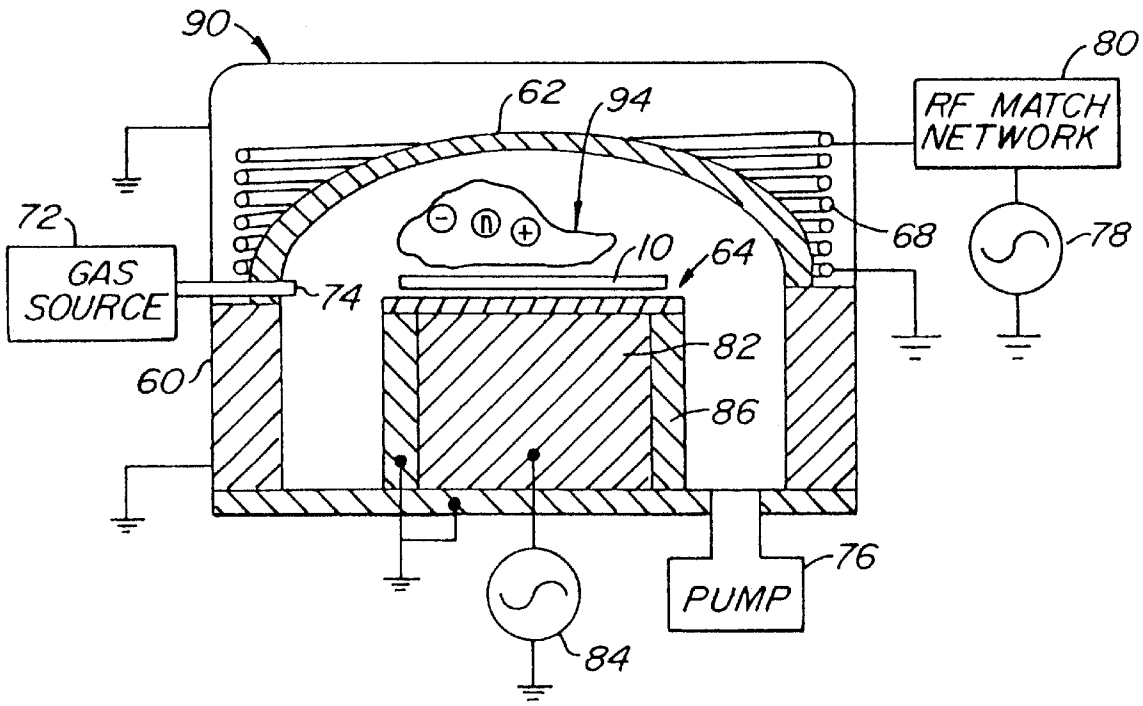
FIG. 16.


90
80
62
94
RF MATCH NETWORK
72
GAS SOURCE
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86
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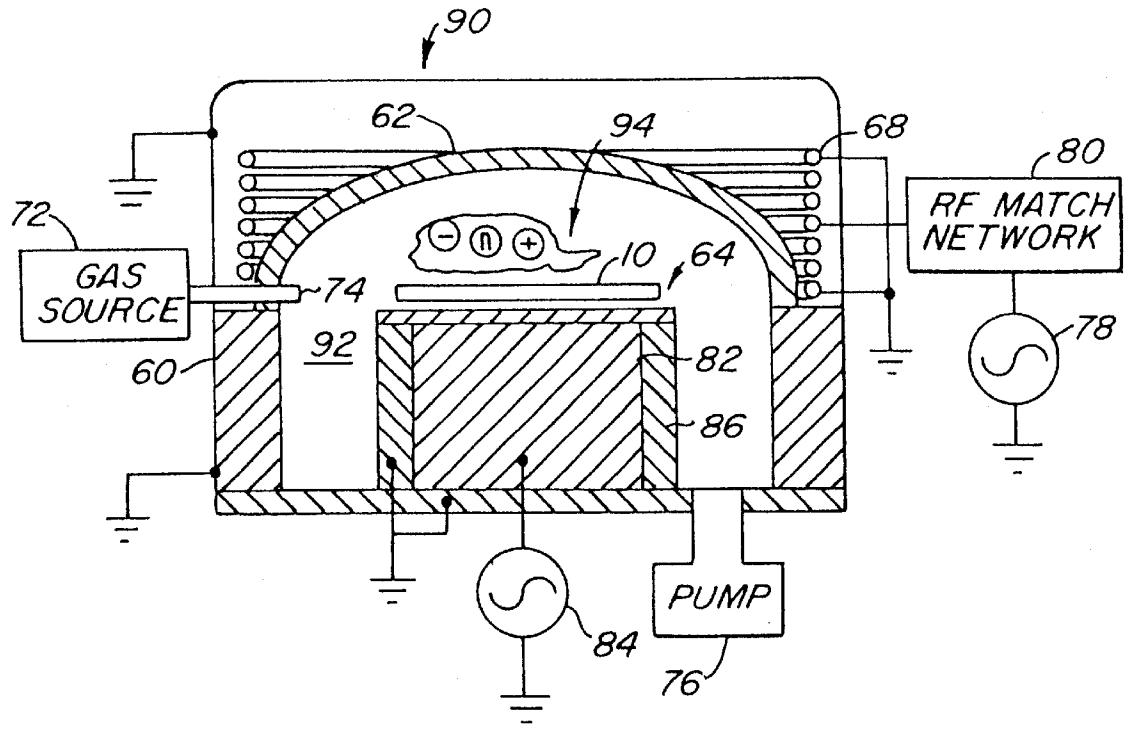
PUMP
84

FIG. 17.


90
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RF MATCH NETWORK
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GAS SOURCE
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PUMP
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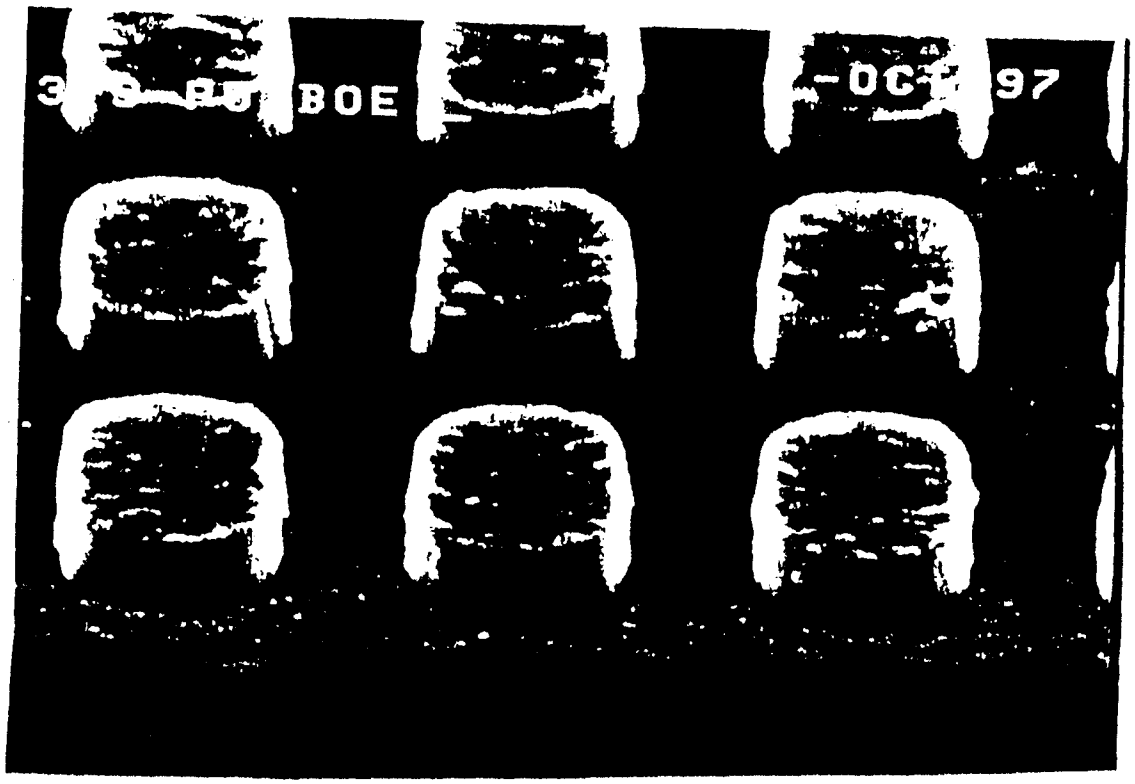
FIG. 18.

FIG. 19.



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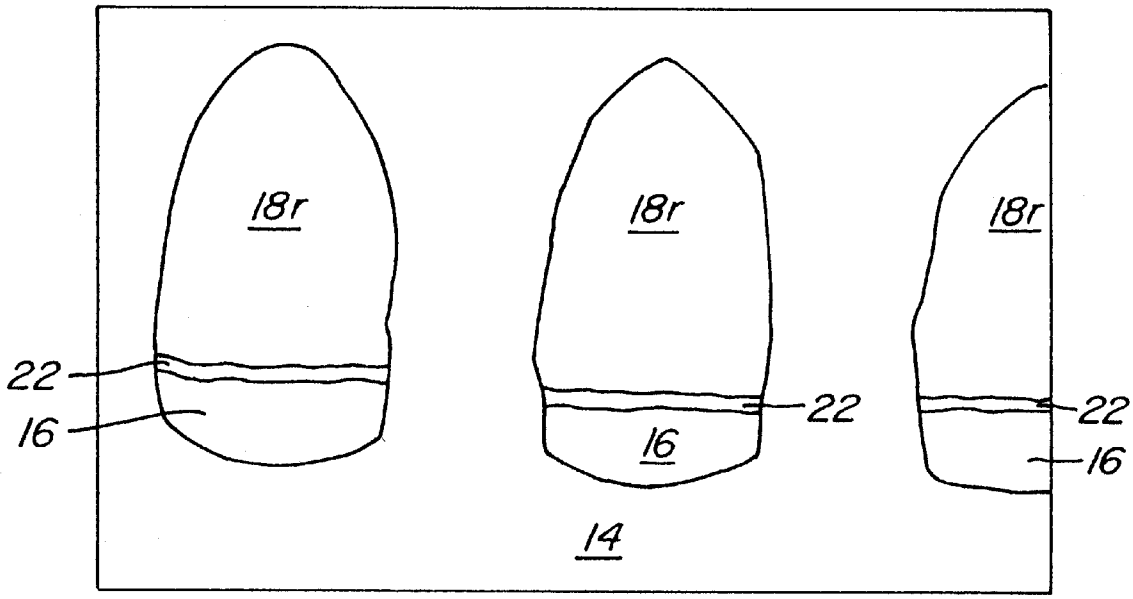
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FIG. 21.

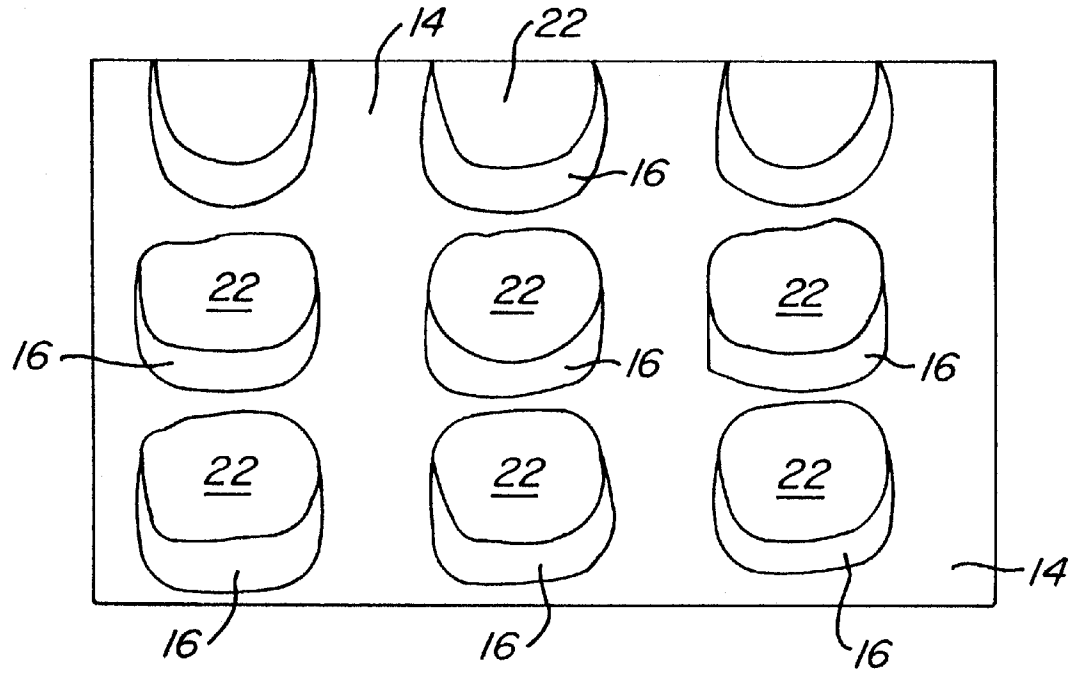
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FIG. 22.

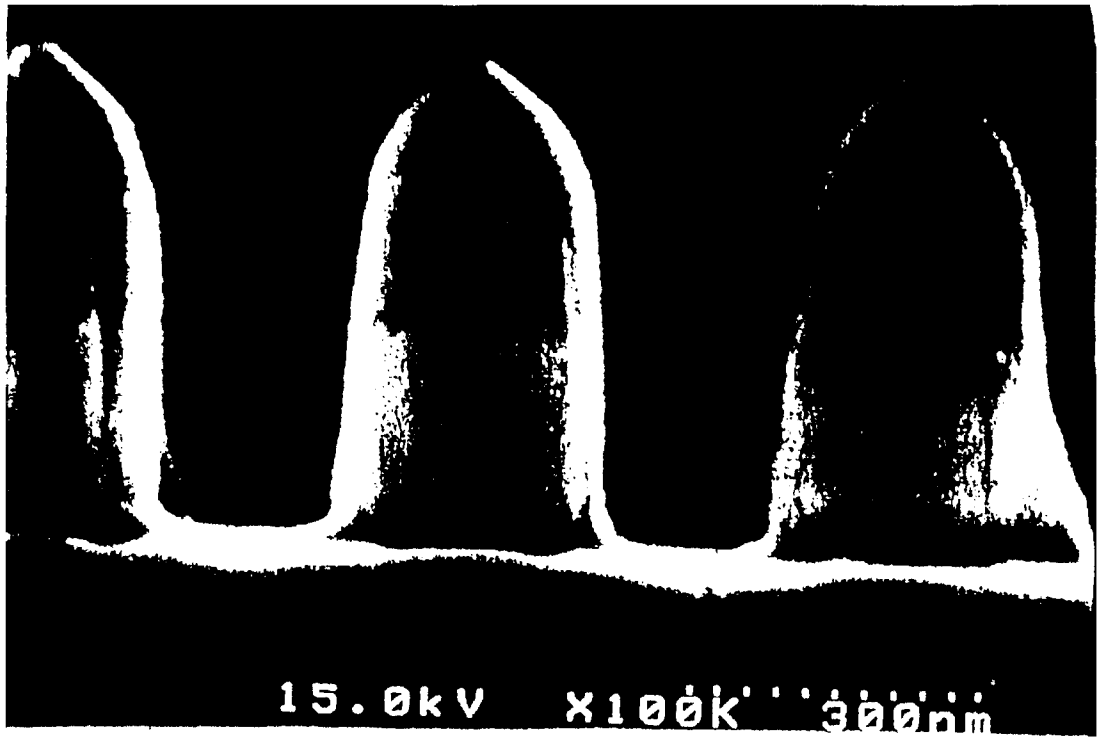
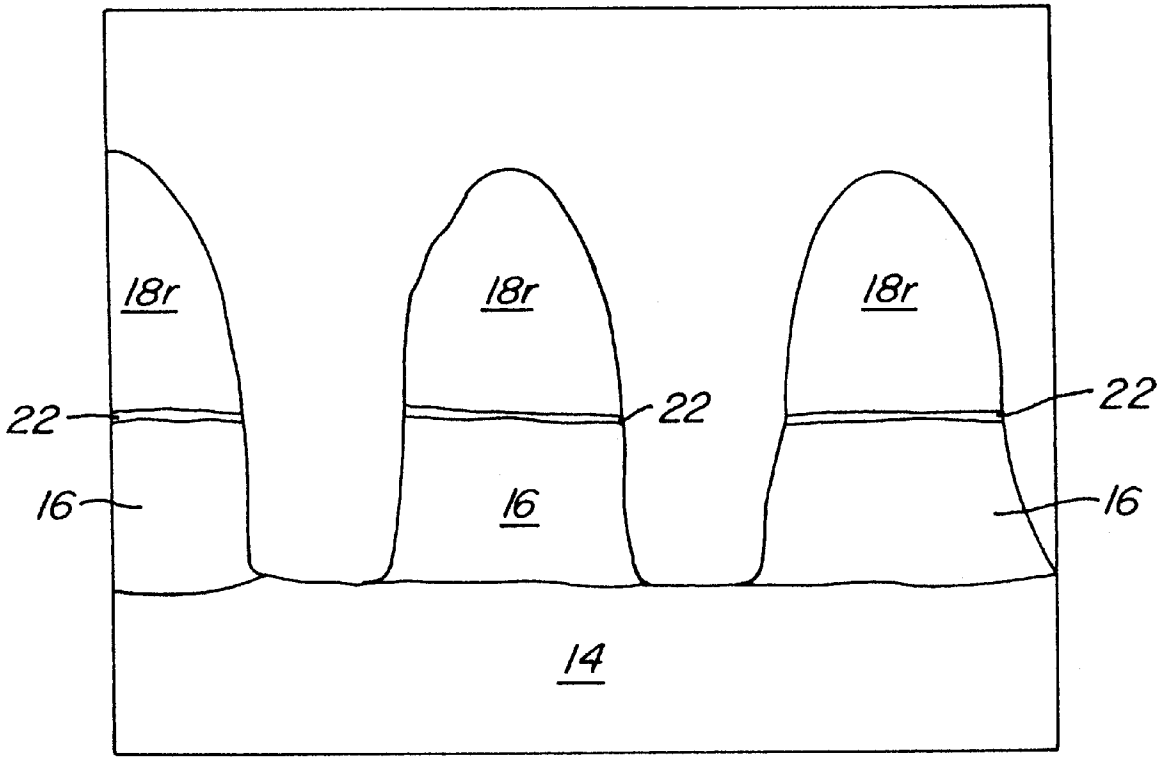


FIG. 23.



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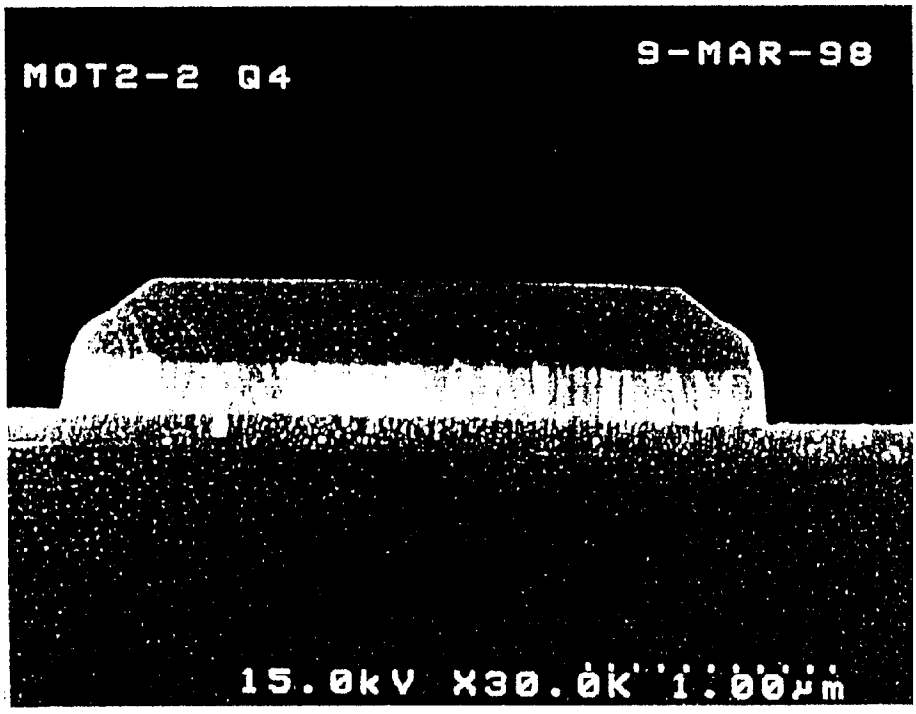
MOT2-2 Q4
9-MAR-98
15.0kV X30.0K 1.00µm

FIG. 25.

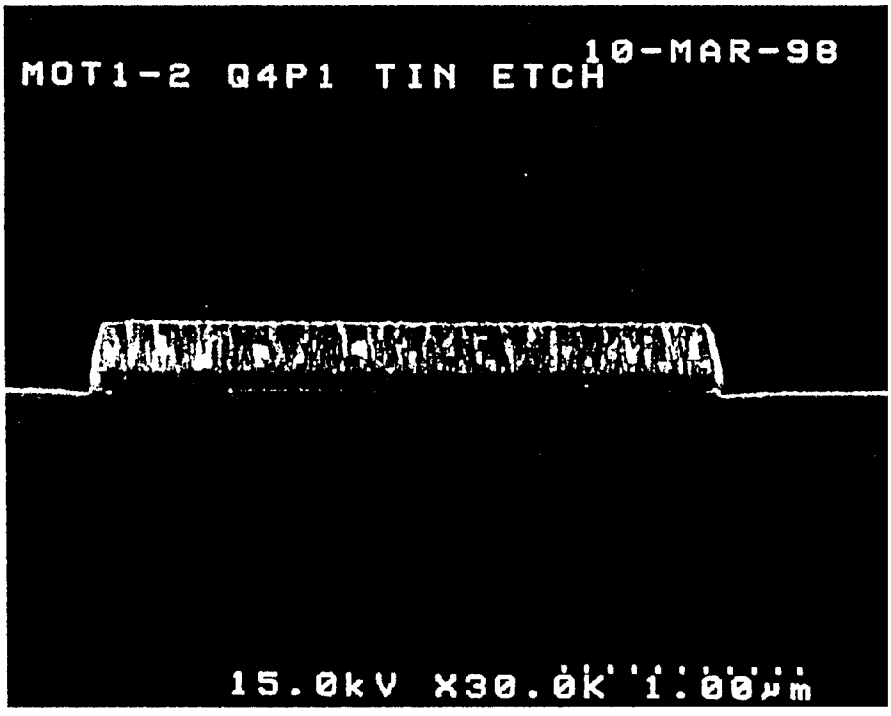
MOT1-2 Q4P1 TIN ETCH
10-MAR-98
15.0kV X30.0K 1.00µm

FIG. 27.

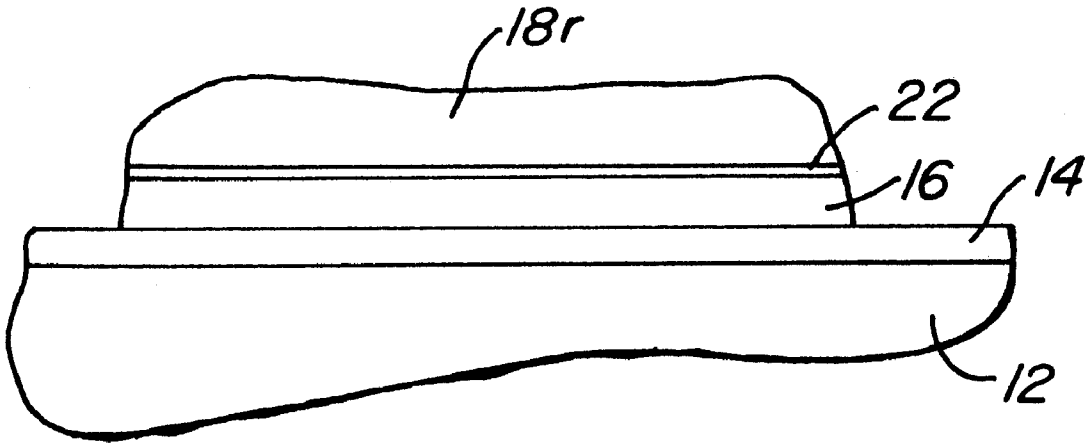

FIG. 26.

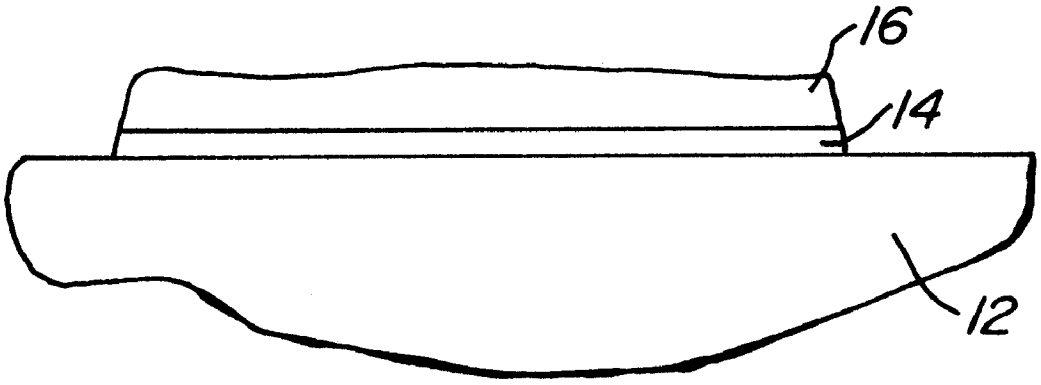

FIG. 28.

IRIDIUM ETCHANT METHODS FOR ANISOTROPIC PROFILE

This is a continuation-in-part patent application of the copending patent application entitled "Etching Methods for Anisotropic Platinum Profile," Ser. No. 09/006,092, filed Jan. 13, 1998.

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to plasma etching of platinum and iridium. More specifically, this invention provides a method for plasma etching of platinum and iridium for producing semiconductor integrated circuits containing platinum and iridium electrodes.

2. Description of the Prior Art

The implementation of digital information storage and retrieval is a common application of modern digital electronics. Memory size and access time serve as a measure of progress in computer technology. Quite often storage capacitors are employed as memory array elements. As the state of the art has advanced, small-feature-size high density dynamic random access memory (DRAM) devices require storage capacitors of larger capacitance having high dielectric constant materials. The high dielectric constant materials or ferroelectric materials are made primarily of sintered metal oxide and contain a substantial amount of very reactive oxygen. In the formation of capacitors with such ferroelectric materials or films, the electrodes must be composed of materials with least reactivity to prevent oxidation of the electrodes which would decrease the capacitance of storage capacitors. Therefore, precious metals, such as platinum (Pt), palladium (Pd), iridium (Ir), etc., are preferred metals used in the manufacture of capacitors for high density DRAM.

Among the possible precious metals for capacitor electrodes, platinum and iridium have emerged as an attractive candidates because they are inert to oxidation and are known to have a leakage current ($<10^{-9}$ amps/cm^2) lower than other electrodes such as RuO_2 and Pd. Platinum and iridium also are good conductors.

In the prior art, platinum and iridium etching have been conducted by means of isotropic etching, such as wet etching with aqua regia, or by anisotropic etching, such as ion milling with Ar gas or by other means. Because of the nature of isotropic etching, using wet etching with aqua regia causes deteriorated processing accuracy. The grade of precision in isotropic etching is not high enough for fine pattern processing. Therefore, it is difficult to perform submicron patterning of platinum and iridium electrodes due to their isotropic property. Furthermore, a problem with ion milling (i.e. anisotropic etching) occurs because the etching speed on platinum and iridium, which is to form the electrode, is too slow for mass production.

In order to increase processing accuracy in etching platinum and iridium, research and development has been quite active, particularly in the area of etching platinum and iridium by means of a dry etching process where etchant gases (e.g., Cl_2, HBr, O_2, etc.) are used. The following prior art is representative of the state of art with respect to etching platinum with a plasma of etching gases.

U.S. Pat. No. 5,492,855 to Matsumoto et al. discloses a semiconductor device manufacturing method, wherein an insulation layer, a bottom electrode Pt layer, a dielectric film and a top electrode Pt layer are provided on top of a substrate having already-completed circuit elements and wiring, and then, a capacitor is formed by selectively dry etching the bottom electrode Pt layer after selectively dry etching the top electrode Pt layer and the dielectric film. The manufacturing method uses a gas containing an S component as etching gas for Pt etching, or an etching gas containing S component as an additive gas; and also it implants S into the Pt layer before the Pt dry etching process by means of ion implantation to compose a S and Pt compound, and then dry etches the Pt compound thus composed.

U.S. Pat. No. 5,527,729 to Matsumoto et al. discloses process steps to form on a substrate in which circuit elements and wirings, etc., are already shaped, an insulation layer, a first metal layer, a dielectric film and a second metal layer. A top electrode and a capacitance film are formed by dry etching the second metal layer and the dielectric film. A bottom electrode is formed by dry etching the first metal layer. The etching gas for dry etching the second metal layer is a mixed gas containing hydrogen halide (e.g. HBr) and oxygen, having a ratio of oxygen against the total of hydrogen halide and oxygen set at about 10%–35%. The etching gas is also taught as a gas containing hydrocarbon, such as chloroform. Matsumoto et al. employs a silicon oxide layer as the insulation layer on the substrate, and a platinum layer or palladium layer as the first and second metal layers. Dry etching of the second metal layer and dielectric film is conducted in a low pressure region not higher than about 5 Pa, where the etching speed is high. Matsumoto et al. further teaches that where a mixed gas of hydrogen halide and oxygen is used as the etching gas, the etching speed on the silicon oxide layer can be made sufficiently low relative to that on the second metal layer made of a platinum layer or a palladium layer; in this way, the excessive etching of the silicon oxide layer underlying the first metal layer is avoided, and damage to the circuit elements and wiring, etc. underneath the silicon oxide layer can be prevented. Furthermore according to Matsumoto et al, the ratio of etching speed of the platinum and dielectric material to the resist can be increased by lowering the etching speed on the resist. Therefore, etching of the platinum and dielectric material may be conducted by using a mask of normal lay-thickness resist (generally speaking, about 1.2 μm to about 2.0 μm thick), instead of using a conventional thick-layer resist (about 3 μm and thicker).

Chou et al. in an article entitled "Platinum Metal Etching in a Microwave Oxygen Plasma", J. Appl. Phys. 68 (5), Sep. 1, 1990, pages 2415–2423, discloses a study to understand the etching of metals in both plasma and chemical systems. The study found that the etching of platinum foils in an oxygen plasma generated in a flow-type microwave system and that very rapid etching (~6 Å/s) took place even at low power inputs (200 W). The principal plasma parameters, including oxygen atom concentration, ion concentration, and electron temperature, were measured by Chou et al. as a function of distance below the microwave coupler. These were correlated to the rate of foil etching, which decreased with increasing distance from the coupler. On the basis of these correlations Chou et al. formulated a simple mechanistic model. The study by Chou et al. further found that the etching of platinum in an oxygen plasma jet results from the concomitant action of oxygen atoms and high energy electrons.

Nishikawa et al. in an article entitled "Platinum Etching and Plasma Characteristics in RF Magnetron and Electron Cyclotron Resonance Plasmas", Jpn. J. Appl. Phys., Vol. 34 (1995), pages 767–770, discloses a study wherein the properties of platinum etching were investigated using both rf

magnetron and electron cyclotron resonance (ECR) plasmas, together with measurement of the plasma parameters (neutral concentration, plasma density, etc.). Nishikawa et al. performed experiments in Cl_2 plasmas over a pressure ranging from 0.4 to 50 mTorr. In rf magnetron plasmas, the etch rate of Pt was constant at the substrate temperature of from 20 to 160° C. The etch rate and the plasma electron density increased with gas pressure decreasing from 50 to 5 mTorr. In ECR plasmas for rf power of 300 W, Nishikawa et al. found that the etch rate of Pt was almost constant (~100 nm/min) with gas pressure decreasing from 5 to 0.4 mTorr, while the plasma electron density gradually increased with decreasing gas pressure. The study by Nishikawa et al. discusses these experimental results with respect to the relationship between the etch yield and the ratio of neutral Cl_2 flux and ion flux incident on the substrate.

Yokoyama et al. in an article entitled "High-Temperature Etching of PZT/Pt/TiN Structure by High-Density ECR Plasma", Jpn. J. Appl. Phys., Vol. 34 (1995), pages 767–770, discloses a study wherein micron patterning technologies for the PZT/Pt/TiN/Ti structure with a spin on glass (SOG) mask are demonstrated using a high-density electron cyclotron resonance (ECR) plasma and a high substrate temperature above 300° C. A 30%-Cl_2/Ar gas was used to etch a lead zirconate titanate (PZT) film. No deposits remained, which resulted in an etched profile of more than 80°. A 40%-O_2/Cl_2 gas was used to etch a Pt film. The etching was completely stopped at the Ti layer. 30-nm-thick deposits remained on the sidewall. They were removed by Yokoyama et al. after dipping in hydrochloric acid. The etched profile of a Pt film was more than 80°. The Ti/TiN/Ti layer was etched with pure Cl_2 gas. The size shift from the SOG mask was less than 0.1 μm. Yokoyama et al. did not detect any interdiffusion between SOG and PZT by transmission electron microscopy and energy dispersive x-ray spectroscopy (TEM-EDX) analysis.

Yoo et al. in an article entitled "Control of Etch Slope During Etching of Pt in Ar/Cl_2/O_2 Plasmas", Jpn. J. Appl. Phys., Vol. 35 (1996), pages 2501–2504, teaches etching of Pt patterns of the 0.25 μm design rule at 20° C. using a magnetically enhanced reactive ion etcher (MERIE). Yoo et al. found that a major problem of etching with a MERIE was the redeposition of the etch products onto the pattern sidewall, making it difficult to reduce the pattern size. In both cases separately using a photoresist mask and an oxide mask, the redeposits of the etch products onto the sidewall were reduced by the addition of Cl_2 to Ar, although the etched slope was lowered to 45°. The redeposits were removed by an HCl cleaning process.

Kotecki in an article entitled "High-K Dielectric Materials for DRAM Capacitors", Semiconductor International, November 1996, pages 109–116, the potential advantages of incorporating high-dielectric materials into a storage capacitor of a dynamic random access memory (DRAM) are described and the requirements of the high dielectric layer are reviewed as they relate to use in a simple stack capacitor structure suitable for the gigabit generation. Kotecki teaches that when considering the use of high-dielectric materials in a stack capacitor structure, the following issues need to be addressed: electrode patterning, high-dielectric material/barrier interaction, electrode/high-dielectric material interaction, surface roughness (e.g. hilocking, etc.), step coverage, high-dielectric material uniformity (e.g. thickness, composition, grain size/orientation, etc.), and barrier (e.g. O_2 and Si diffusion, conductivity, contact resistance and interactions, etc.). Various materials and combinations of materials were studied by Kotecki for use with perovskite dielectrics including the noble metals (i.e. Pt, Ir, Pd) and conductive metal oxides (i.e. IrO_2 and RuO_2). The work function of these materials, their ability to be patterned by dry etching, the stability of the surface with regards to surface roughening and their suitability in a semiconductor fabricator are listed by Kotecki in the following Table I:

TABLE I

Comparison of the Properties of Various Electrode Materials Suitable for Use with Perovskite Dielectrics

Material Selection	Work Function	Dry Etch	Surface Stability	Deposition Method
Pt	5.6–5.7	difficult	potential problem	sputtering
Ru	4.7	easy/dangerous	potential problem	sputtering
RuO_2/Ru		easy/dangerous	good	reactive sputtering
Ir	5.0–5.8	difficult	good	sputtering
IrO_2/Ir		difficult	good	reactive sputtering
Pd	5.1–5.6	difficult	?	sputtering

Kotecki further teaches in the article entitled "High-K Dielectric Materials for DRAM Capacitors" that one of the major problems which needs to be overcome with respect to the manufacturing of DRAM chips using capacitors is the problem of electrode patterning. There are minimal volatile species produced during the dry etching of the noble metal electrodes such as Pt, Ru, Pd and Ir. Since the etch mechanism is primarily by physical sputtering, even during a RIE process, fences are typically formed on the sides of the photoresist. To eliminate the problem of fencing, it is possible to etch the fence layer and erode the sides of the photoresist during the etch process which leads to "clean" metal structures but with sloping sidewall angles and a loss of control over critical feature sizes. As the dimension of the feature shrinks to 0.18 μm or below, only limited tapering of the sidewall angle can be tolerated. Kotecki presents in the following Table II some of the high-dielectric materials which have been considered for use in a DRAM capacitor, the various methods which can be used to form the films, and the range of reported permittivites:

TABLE II

A Comparison of Various High-Dielectric Materials and Method for Formation and Dielectric Constants

Material	Deposition Methods	ϵ_r(thin films)
$SrTiO_3$	MOCVD, ECR-CVD, sol-gel, sputtering, PLD	90–240
(Ba, Sr)TiO_3	MOCVD, ECR-CVD, sol-gel, sputtering, PLD	160–600
PLT	MOCVD, sol-gel, sputtering, PLD	400–900
PZT and PLZT	MOCVD, sol-gel, sputtering, PLD	>1000

Milkove et al. reported in a paper entitled "New Insight into the Reactive Ion Etching of Fence-Free Patterned Platinum Structures" at the 43rd Symposium of AVS, October 1996, Philadelphia, Pa., that an investigation was undertaken to characterize the time progression of the Pt etch process during the reactive ion etching (RIE) of fence-free patterned structures. The experiment by Milkove et al. consisted of coprocessing two oxidized Si wafers possessing identical 2500 Å thick Pt film layers, but different photoresist (PR) mask thicknesses. Etching was suspended at 20, 40, 60 and 80% of the full etch process in order to cleave off

small pieces of wafer for analysis by a scanning electron microscopy (SEM). Using Cl_2-based RIE conditions known to produce fence-free etching for 2500 Å thick film layers, Milkove et al. discovered that a severe fence actually coats the PR mask during the first 20% of the etch process. As the etch continues the fence structure evolves, achieving a maximum height and width followed by progressive recession until disappearing completely prior to process endpoint. The data from Milkove et al. shows that the final profile of an etched Pt structure possess a functional dependence on the initial thickness and slope of the PR mask, as well as on the initial thickness of the Pt layer. Milkove et al. further reported in the paper entitled "New Insight Into The Reactive Ion Etching of Fence-free Patterned Platinum Structures" that the observed behavior of the transient fence provides the strongest evidence to date supporting the existence of a chemically assisted physical sputtering component associated with the RIE of Pt films in halogen-based plasmas.

Keil et al. teaches in an article entitled "The Etching of Platinum Electrodes for PZT Based Ferroelectric Devices", Electrochemical Society Proceedings, Vol. 96-12 (1996), pages 515–520, that the technical difficulties of fabricating capacitors employing platinum Pt etching is most often dominated by sputtering processes. While oxygen and/or various gaseous chlorides or fluorides are used to chemically enhance the etch process, the products of both etch mechanisms are usually of low volatility and tend to redeposit on the wafer. After etching, large wall-like structures extend up from the edges of the Pt region. These wall-like structures are frequently referred to as "veils" or "fences" or "rabbit ears" and can reach lengths which are more than double the thickness of the Pt film to which they are attached. The existence of such structures makes useful deposition of the PZT layer impossible. Keil et al. further teaches that even when one is able to attenuate redeposition to the point where only small "nub" like features are present, the high electric fields which will form at such "nubs" enhances the likelihood for dielectric breakdown. Although process conditions can be found which result in either low redeposition or even no redeposition, they most often also give an unacceptably tapered platinum profile angle. Keil et al. observed that redeposition becomes more severe as process conditions are pushed toward those which give increasingly vertical sidewalls. While a post etch wet clean in a solvent bath is frequently used, the heavy redeposition which attends the pursuit of vertical sidewalls regularly renders this approach minimally effective.

The foregoing prior art illustrates that generally a clean vertical dense area profile and CD (critical dimension) control of the etch profiles are critical factors for successful plasma etching of 1-Gbit (and beyond) DRAM ferroelectric devices possessing platinum electrodes. Redeposition and profile control are found to be strongly interlinked. Optimization of both profile angle and redeposition requires a tradeoff between the two. Where as vigorous post etch cleaning (e.g. wet cleaning with acid, mechanical polishing, etc.) can relieve some of the need to achieve a deposition free plasma etch, such post etch cleaning does not possess the accuracy that is desired as the platinum electrode itself is typically eroded and/or deteriorated by currently known post etch cleaning methods. The same would be true for an iridium electrode.

Therefore, what is needed and what has been invented is a method for etching a platinum layer and an iridium layer to produce a high density integrated circuit semiconductor device having platinum electrodes or iridium electrodes with a high degree (i.e., ≧85°) of platinum or iridium profile anisotropy. What is further needed and what has been invented is a semiconductor device including a plurality of platinum or iridium electrodes respectively having a platinum or iridium profile equal to or greater than about 85° and separated by a distance equal to or less than about 0.3 μm with each electrode having a critical dimension (e.g., a width) equal to or less than about 0.3 μm.

SUMMARY OF THE INVENTION

The present invention broadly provides a method of etching a platinum layer disposed on a substrate comprising the steps of:

a) providing a substrate supporting a platinum layer;

b) heating the substrate (such as with a pedestal supporting the substrate) of step (a) to a temperature greater than about 150° C.; and

c) etching the platinum layer including employing a high density plasma of an etchant gas comprising a halogen containing gas (e.g., a halogen such as chlorine) and a noble gas (e.g., argon) to produce the substrate supporting at least one etched platinum layer.

In another embodiment of the present invention, the present invention broadly provides:

a) providing a substrate supporting a iridium layer;

b) heating the substrate of step (a) to a temperature greater than about 150° C.; and

c) etching the iridium layer including employing a high density plasma of an etchant gas comprising a halogen-containing gas, and a noble gas to produce said substrate supporting at least one etched iridium layer. The etchant gas may additionally include a gas selected from the group consistng of O_2 and BCl_3. Alternatively, the etchant gas may additionally include a gas selected from the group consisting of O_2, HCl, HBr, and mixtures thereof. The substrate of step (a) may be heated by heating the pedestal supporting the substrate to a sufficient temperature to cause the substrate to possess a temperature greater than about 150° C.

In the foregoing methods, the platinum layer and the iridium layer are preferably a platinum electrode layer and an iridium electrode layer, respectively. The high density plasma of an etchant gas is a plasma of an etchant gas having an ion density greater than about $10^9/cm^3$, preferably greater than about $10^{11}/cm^3$. The etchant gas may also include a gas selected from the group consisting of BCl_3, HBr, and mixtures thereof. The platinum layer and the iridium layer may each additionally comprise a mask layer disposed on a selected part of the particular respective layer to selectively protect the particular respective layer during the etching step. In the embodiment of the present invention for etching iridium, if the mask layer is a hard mask layer comprising Ti and/or TiN, the etchant gas having $Ar/Cl_2/O_2$ chemistry with high O_2 concentration produces an iridium to Ti and/or TiN selectivity of greater than about 8 (preferably greater than about 10) during etching of iridium. The platinum layer and the iridium layer may each also additionally comprise a protective layer disposed on the selected part of the particular respective layer between the mask layer and the particular respective layer. The mask layer may be removed during or after the etching step. Similarly, the protective layer may be removed during or after the etching step.

The platinum layer is part of or is contained in a platinum wafer, and the method of etching a platinum layer additionally comprises disposing the platinum wafer including the platinum layer in a high density plasma chamber having a

coil inductor and a wafer pedestal; and performing the etching step (c) in the high density plasma chamber under the following process conditions:

Process	Parameters
Etchant Gas Flow	50 to 500 sccm
Halogen Gas (e.g., Cl_2)	20% to 95% by vol.
Noble Gas (e.g., Ar)	5% to 80% by vol.
Pressure, mTorr	0.1 to 300 milliTorr
RF Power (watts) of Coil Inductor	100 to 5000 watts
RF Power (watts) of Wafer Pedestal	50 to 3000 watts
Temperature (° C.) of Platinum Wafer	150° to 500° C.
Platinum Etch Rate (Å/min)	200 to 6000 Å/min
RF Frequency of Coil Inductor	100 K to 300 MHz
RF Frequency of Wafer Pedestal	100 K to 300 MHz

The etched platinum layer includes a platinum profile equal to or greater than about 85°, more preferably equal to or greater than about 87°, most preferably equal to or greater than about 88.5°. The etchant gas for the process conditions immediately above may alternatively comprise from about 10% to about 90% by vol. of a halogen (e.g., Cl_2), from about 5% to about 80% by vol. of a noble gas (e.g., argon), and from about 4% to about 25% by vol. HBr and/or BCl_3.

The iridium layer is part of or is contained in an iridium wafer, and the method of etching an iridium layer additionally comprises disposing the iridium wafer including the iridium layer in a high density plasma chamber having a coil inductor and a wafer pedestal; and performing the etching step (c) in the high density plasma chamber under the following process conditions:

Process	Parameters
Etchant Gas Flow	50 to 500 sccm
Halogen Gas (e.g., Cl_2)	10% to 60% by vol.
Noble Gas (e.g., Ar)	30% to about 80% by vol.
Oxygen	5% to 40% by vol.
Pressure, mTorr	0.1 to 300 milliTorr
RF Power (watts) of Coil Inductor	100 to 5000 watts
RF Power (watts) of Wafer Pedestal	50 to 3000 watts
Iridium Etch Rate (Å/min)	200 to 6000 Å/min
RF Frequency of Coil Inductor	100 K to 300 MHz
RF Frequency of Wafer Pedestal	100 K to 300 MHz

The etched iridium layer includes an iridium profile equal to or greater than about 80°, more preferably equal to or greater than about 82°, most preferably equal to or greater than about 85.0°. The etchant gas for the process conditions immediately above may alternatively comprise from about 5% to about 20% by vol. oxygen, from about 10% to about 60% by vol. of a halogen (e.g., Cl_2), from about 30% to about 80% by vol. of a noble gas (e.g., argon), and from about 5% to about 20% by vol. HBr and/or HCl.

The present invention also broadly provides a method for producing a capacitance structure including an electrode (i.e., a platinum or iridium electrode) comprising the steps of:

a) providing a substrate supporting a layer (i.e., a platinum electrode layer or an iridium electrode layer) and at least one mask layer disposed on a selected part of the layer;

b) heating the substrate of step (a) to a temperature greater than about 150° C.; and

c) etching the layer including employing a plasma of an etchant gas comprising a halogen (e.g., chlorine) and a noble gas (e.g., argon) to produce a capacitance structure having at least one electrode (i.e., platinum electrode or iridium electrode).

The at least one mask layer is removed during or after the etching step (c) immediately above. The layer of step (a) immediately above may additionally comprise a protective layer disposed on the selected part of the layer between the mask layer and the layer. The etched layer (i.e. the etched platinum layer or the etched iridium layer) produced by the etching step (c) immediately above includes a profile (i.e. a platinum profile or an iridium profile) equal to or greater than about 80° iridium and equal to or greater than about 85° for platinum, more preferably equal to or greater than about 87°, most preferably equal to or greater than about 88.5°.

In a preferred embodiment of the invention for etching platinum, the etchant gas of the plasma of step (c) more specifically includes a halogen (e.g., chlorine), a noble gas (e.g., argon), and a gas selected from the group consisting of HBr, BCl_3 and mixtures thereof. The platinum electrode layer is part of or is contained in a platinum electrode wafer, and the method for producing a capacitance structure including a platinum electrode layer additionally comprises disposing, prior to the etching step (c), the platinum electrode wafer in a high density plasma chamber having a coil inductor and a wafer pedestal; and performing the etching step (c) in the high density plasma chamber under the following previously indicated process conditions:

Process	Parameters
Etchant Gas Flow	50 to 500 sccm
Halogen Gas (e.g., Cl_2)	about 10% to about 90% by vol.
Noble Gas (e.g., Ar)	about 5% to about 80% by vol.
HBr and/or BCl_3	about 4% to about 25% by vol.
Pressure, mTorr	0.1 to 300 milliTorr
RF Power (watts) of Coil Inductor	100 to 5000 watts
RF Power (watts) of Wafer Pedestal	50 to 3000 watts
Temperature (° C.) of Platinum Electrode Wafer	about 150° to about 500° C.
Platinum Etch Rate (Å/min)	200 to 6000 Å/min
RF Frequency of Coil Inductor	100 K to 300 MHz
RF Frequency of Wafer Pedestal	100 K to 300 MHZ

The produced platinum electrodes are separated by a distance or space having a dimension equal to or less than about 0.3 μm. Each of the platinum electrodes include a dimension having a value equal to or less than about 0.6 μm, preferably equal to or less than about 0.3 μm. More preferably, each of the platinum electrodes have a width equal to or less than about 0.3 μm, a length equal to or less than about 0.6 μm, and a height equal to or less than about 0.6 μm. The plasma of the etchant gas for etching platinum comprises a high density inductively coupled plasma. The etchant gas preferably comprises a noble gas selected from the group consisting of helium, neon, argon, krypton, xenon, radon, and mixtures thereof. More preferably, the noble gas is selected from the group consisting of helium, neon, argon, and mixtures thereof. Most preferably, the noble gas is argon. As was previously indicated, the etchant gas of the high density inductively coupled plasma for etching platinum most preferably comprises, or preferably consists of or consists essentially of, chlorine, argon, and HCl and/or HBr.

In a preferred embodiment of the invention for etching iridium, the etchant gas of the plasma of step (c) more specifically includes oxygen, a halogen (e.g., chlorine), a noble gas (e.g., argon), and a gas selected from the group consisting of HBr, HCl and mixtures thereof. The iridium electrode layer is part of or is contained in an iridium electrode wafer, and the method for producing a capacitance structure including an iridium electrode layer additionally comprises disposing, prior to the etching step (c), the iridium electrode wafer in a high density plasma chamber having a coil inductor and a wafer pedestal; and performing the etching step (c) in the high density plasma chamber under the following previously indicated process conditions:

Process	Parameters
Etchant Gas Flow	50 to 500 sccm
Oxygen	about 5% to about 20% by vol.
Halogen Gas (e.g., Cl_2)	about 10% to about 60% by vol.
Noble Gas (e.g., Ar)	about 30% to about 80% by vol.
HBr and/or HCl	about 5% to about 20% by vol.
Pressure, mTorr	0.1 to 300 milliTorr
RF Power (watts) of Coil Inductor	100 to 5000 watts
RF Power (watts) of Wafer Pedestal	50 to 3000 watts
Temperature (° C.) of Iridium Electrode Wafer	about 150° to about 500° C.
Iridium Etch Rate (Å/min)	200 to 6000 Å/min
RF Frequency of Coil Inductor	100 K to 300 MHz
RF Frequency of Wafer Pedestal	100 K to 300 MHz

The plasma of the etchant gas for etching iridium comprises a high density inductively coupled plasma. The etchant gas preferably comprises a noble gas selected from the group consisting of helium, neon, argon, krypton, xenon, radon, and mixtures thereof. More preferably, the noble gas is selected from the group consisting of helium, neon, argon, and mixtures thereof. Most preferably, the noble gas is argon. As was previously indicated, the etchant gas of the high density inductively coupled plasma for etching iridium most preferably comprises, or preferably consists of or consists essentially of, chlorine, argon, and oxygen or BCl_3; alternatively, oxygen, chlorine, argon, and HCl and/or HBr.

The present invention further broadly provides a method of manufacturing a semiconductor device comprising the steps of:

a) forming a patterned resist layer, a mask layer and an electrode layer (i.e. a platinum electrode layer or an iridium electrode layer) on a substrate having circuit elements formed thereon;

b) etching a portion of the mask layer including employing a plasma of an etchant gas to break through and to remove the portion of the mask layer from the electrode layer to produce the substrate supporting the patterned resist layer, a residual mask layer, and the electrode layer;

c) removing the resist layer of step (b) to produce the substrate supporting the residual mask layer and the electrode layer;

d) heating the substrate of step (c) to a temperature greater than about 150° C.; and

e) etching the electrode layer of step (d) including employing a high density plasma of an etchant gas. In the embodiment of the invention for etching a platinum layer, the etchant gas preferably comprises a halogen gas (e.g., chlorine) and a noble gas (e.g., argon) to produce a semiconductor device having at least one platinum electrode. In the embodiment of the invention for etching an iridium layer, the etchant gas comprises oxygen, a halogen gas (e.g. chlorine) and a noble gas (e.g. argon) to produce a semiconductor device having at least one iridium electrode.

The present invention also further broadly provides a method of etching an electrode layer disposed on a substrate comprising the steps of:

a) providing a substrate supporting an electrode layer (i.e. a platinum electrode layer or an iridium electrode layer), a protective layer on the electrode layer, and a mask layer on the protective layer, and a patterned resist layer on the mask layer;

b) etching a portion of the mask layer including employing a plasma of an etchant gas to break through and to remove the portion of the mask layer from the protective layer to expose part of the protective layer and to produce the substrate supporting the electrode layer, the protective layer on the electrode layer, a residual mask layer on the electrode layer, and the patterned resist layer on the residual mask layer;

c) removing the patterned resist layer from the residual mask layer of step (b) to produce the substrate supporting the electrode layer, the protective layer on the electrode layer, and the residual mask layer on the protective layer;

d) heating the substrate of step (c) to a temperature greater than about 150° C.;

e) etching the exposed part of the protective layer to expose part of the electrode layer and to produce the substrate supporting the electrode layer, a residual protective layer on the electrode layer, and the residual mask layer on the residual protective layer; and

f) etching the exposed part of the electrode layer of step (e) including employing a high density plasma of an etchant gas. If the electrode layer being etched comprises platinum, the etchant gas comprises a halogen gas (e.g., chlorine) and a noble gas (e.g., argon) to produce the substrate supporting an etched platinum electrode layer having the residual protective layer on the etched platinum electrode layer, and the residual mask layer on the residual protective layer. If the electrode layer being etched includes iridium, the etchant gas comprises oxygen, a halogen gas (e.g. chlorine) and a noble gas (e.g. argon) to produce the substrate supporting an etched iridium electrode layer having the residual protective layer on the etched iridium electrode layer, and the residual mask layer on the residual protective layer.

The patterned resist layer is preferably removed from the residual mask layer before heating the substrate to a temperature greater than about 150° C. because such high temperatures would destroy the resist layer. The residual mask layer may be removed from the electrode layer either before or after heating of the substrate to a temperature greater than about 150° C., and during or after the etching step. The electrode layer (i.e. a platinum electrode layer or an iridium electrode layer) is part of or is contained in a wafer (i.e. a platinum electrode wafer or an iridium electrode wafer). The purpose of the protective layer is to ensure the adhesion between the mask layer and the platinum and iridium layers and also to respectively maintain the platinum profile and the iridium profile of the platinum electrode layer and the iridium electrode layer, respectively, especially

during the etching process of the present invention. Preferably, the residual protective layers are respectively removed from the etched platinum and iridium electrodes after the platinum and iridium etching step.

As previously indicated, etching of the platinum electrode layer to produce the platinum electrodes of the present invention is performed in a high density plasma chamber. The platinum etching step employs a high density plasma of an etchant gas preferably consisting of, or consisting essentially of, a halogen gas (e.g., chlorine), a noble gas (i.e., argon) and HBr and/or BCl_3. The high density plasma chamber possesses a separate control for ion flux and a separate control for ion energy. As previously indicated, the ion density of the high density plasma in the high density plasma chamber is greater than about $10^9/cm^3$.

The high density plasma chamber for the method of manufacturing a semiconductor device and for the method of etching a platinum electrode layer disposed on a substrate includes a coil inductor and a wafer pedestal; and the platinum etching step in both of the methods is performed in the high density plasma chamber under the following previously mentioned process conditions:

Process	Parameters
Etchant Gas Flow	50 to 500 sccm
Halogen Gas (e.g., Cl_2)	about 10% to about 90% by vol.
Noble Gas (e.g., argon)	about 5% to about 80% by vol.
HBr and/or BCl_3	about 4% to about 25% by vol.
Pressure, mTorr	0.1 to 300 milliTorr
RF Power (watts) of Coil Inductor	100 to 5000 watts
RF Power (watts) of Wafer Pedestal	50 to 3000 watts
Temperature (° C.) of Platinum Electrode Wafer	about 150° to about 500° C.
Platinum Etch Rate (Å/min)	200 to 6000 Å/min
RF Frequency of Coil Inductor	100 K to 300 MHz
RF Frequency of Wafer Pedestal	100 K to 300 MHz

As further previously indicated, etching of the iridium electrode layer to produce the iridium electrodes of the present invention is performed in a high density plasma chamber. The iridium etching step employs a high density plasma or a low density plasma of an etchant gas preferably consisting of, or consisting essentially of, or consisting essentially of, a halogen gas (e.g., chlorine) and a noble gas (i.e., argon), more preferably a halogen gas (e.g., chlorine), a noble gas (i.e., argon) and oxygen or BCl_3, or oxygen (O_2), a halogen gas (e.g. Cl_2), a noble gas (e.g Ar), and HCl and/or HBr. The high density plasma chamber possessess a separate control for ion flux and a separate control for ion energy. As previously indicated, the ion density of the high density plasma in the high density plasma chamber is greater than about $10^9/cm^3$.

The high density plasma chamber for the method of manufacturing a semiconductor device and for the method of etching iridium electrode layer disposed on a substrate includes a coil inuctor and a wafer pedestal; and the iridium etching step in both of the methods is performed in high density plasma chamber under the following previously mentioned process conditions:

Process	Parameters
Etchant Gas Flow	50 to 500
Oxygen	5% to 20% by volume
Halogen Gas (e.g., Cl_2)	about 10% to about 60% by vol.
Noble Gas (e.g., argon)	about 30% to about 80% by vol.
HBr and/or HCl	about 5% to about 20% by vol.
Pressure, mTorr	0.1 to 300 milliTorr
RF Power (watts) of Coil Inductor	100 to 5000 watts
RF Power (watts) of Wafer Pedestal	50 to 3000 watts
Temperature (° C.) of Iridium Electrode Wafer	about 150° to about 500° C.
Iridium Etch Rate (Å/min)	200 to 6000 Å/min
RF Frequency of Coil Inductor	100 K to 300 MHz
RF Frequency of Wafer Pedestal	100 K to 300 MHz

The present invention yet also further broadly provides a semiconductor device, more specifically a capacitance structure, comprising a substrate, and at least two electrodes (i.e., platinum electrodes or iridium electrodes) supported by the substrate. The electrodes have a profile equal to or greater than about 85°, preferably equal to or greater than about 87°, more preferably equal to or greater than about 88.5°. The electrodes are separated by a distance or space having a dimension equal to or less than about 0.3 μm. Each of the electrodes include a dimension having a value equal to or less than about 0.6 μm, preferably equal to or less than about 0.3 μm. More preferably, each of the electrodes have a width equal to or less than about 0.3 μm, a length equal to or less than about 0.6 μm, and a height equal to or less than about 0.6 μm.

The foregoing provisions along with the various ancillary provisions and features which will become apparent to those skilled in the art as the following description proceeds, are attained by the practice of the present invention, a preferred embodiment thereof shown with reference to the accompanying drawings, by way of example only, wherein:

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a side elevational view of a semiconductor wafer having a semiconductor substrate, a barrier layer disposed on the semiconductor substrate, an electrode layer (i.e., a platinum electrode layer or an iridium electrode layer) disposed on the barrier layer, a mask layer disposed on the electrode layer, and a patterned resist disposed on the mask layer;

FIG. **2** is a side elevational view of the semiconductor wafer of FIG. **1** additionally including a protective layer disposed on the electrode layer (i.e., a platinum electrode layer or an iridium electrode layer) between the mask layer and the electrode layer;

FIG. **3** is a vertical sectional view of a prior art plasma processing apparatus including a plasma etching reactor with an electromagnetic unit for enhancing a plasma;

FIG. **4** is a diagram of a flux produced by a magnetic field and illustrated as rotating around a center axis;

FIG. **5** is a side elevational view of the semiconductor wafer of FIG. **1** after etching and removing a portion of the mask layer from the surface of the electrode layer (i.e., a platinum electrode layer or an iridium electrode layer) to expose the electrode layer;

FIG. **6** is a side elevational view of the semiconductor wafer of FIG. **2** after etching and removing a portion of the

mask layer from the surface of the protective layer to expose the protective layer;

FIG. **7** is a side elevational view of the semiconductor wafer of FIG. **5** after the patterned resist layer has been removed from a portion of the mask layer with the removed patterned resist layer being represented as broken lines;

FIG. **8** is a side elevational view of the semiconductor wafer of FIG. **6** after etching and removing a portion of the protective layer off of the surface of the layer (i.e., a platinum electrode layer or an iridium electrode layer), and after removing the patterned resist layer from a portion of the mask layer with the removed patterned resist layer being represented as broken lines;

FIG. **9** is a side elevational view of the semiconductor wafer of FIG. **7** after the electrode layer (i.e., the platinum electrode layer or the iridium electrode layer) has been etched to produce an etched electrode layer;

FIG. **10** is a side elevational view of the semiconductor wafer of FIG. **8** after the electrode layer (i.e., the platinum electrode layer or the iridium electrode layer) has been etched to produce an etched electrode layer;

FIG. **11** is a side elevational view of the semiconductor wafer of FIG. **7** after the electrode layer (i.e., the platinum electrode layer or the iridium electrode layer) has been etched to produce an etched electrode layer with a residual mask layer on top thereof;

FIG. **12** is a side elevational view of the semiconductor wafer of FIG. **8** after the electrode layer (i.e., the platinum electrode layer or the iridium electrode layer) has been etched to produce an etched electrode layer with a residual mask layer on top of the residual protective layer;

FIG. **13** is a side elevational view of the semiconductor wafer of FIG. **11** with the residual mask layer removed from the surface of the etched electrode layer;

FIG. **14** is a side elevational view of the semiconductor wafer of FIG. **12** with the residual mask layer and the residual protective layer removed from the surface of the etched electrode layer (i.e., the etched platinum electrode layer or the iridium etched electrode layer);

FIG. **15** is a side elevational view of semiconductor wafer of FIG. **11** after the residual mask layer has been removed from the surface of the etched electrode layer (i.e., the etched platinum electrode layer or the etched iridium electrode layer) and with the barrier layer having been etched;

FIG. **16** is a side elevational view of semiconductor wafer of FIG. **12** after the residual mask layer and the residual protective layer have been removed from the surface of the etched electrode layer (i.e., the etched platinum electrode layer or the etched iridium electrode layer) and with the barrier layer having been etched;

FIG. **17** is a simplified cut-away view of an inductively coupled RF plasma reactor which may be employed in etching the electrode layer (i.e., the platinum electrode layer or the iridium electrode layer) to produce a semiconductor device;

FIG. **18** is a simplified cut-away view of another inductively coupled RF plasma reactor which may be employed in etching the electrode layer (i.e., the platinum electrode layer or the iridium electrode layer) to produce a semiconductor device;

FIG. **19** is a picture showing an elevational view of a test semiconductor wafer for Example I after a platinum electrode layer was etched in accordance with the process conditions listed in Example I;

FIG. **20** is a picture showing an elevational view of the test semiconductor wafer of FIG. **19** after the oxide mask was removed;

FIG. **21** is a drawing representing the elevational view in the picture of FIG. **19** with the respective parts identified by a reference numeral;

FIG. **22** is a drawing representing the elevational view in the picture of FIG. **20** with the respective parts identified by a reference numeral;

FIG. **23** is a picture showing an elevational view of a test semiconductor wafer for Example II after a platinum electrode layer was etched in accordance with the process conditions listed in Example II;

FIG. **24** is a drawing representing the elevational view in the picture of FIG. **23** with the respective parts identified by a reference numeral;

FIG. **25** is a picture showing an elevational view of a test semiconductor wafer for Example III after an iridium electrode layer was etched in accordance with the process conditions listed in Example III;

FIG. **26** is a drawing representing the elevational view in the picture of FIG. **25** with respective parts identified by a reference numeral;

FIG. **27** is a picture showing an elevational view of a test semiconductor wafer for Example IV after an iridium electrode layer was etched in accordance with the process conditions listed in Example IV; and

FIG. **28** is a drawing representing the elevational view in the picture of FIG. **27** with the respective parts identified by a reference numeral.

DESCRIPTION OF THE PREFERRED EMBODIMENTS OF THE INVENTION

Referring in detail now to the drawings wherein similar parts of the present invention are identified by like reference numerals, there is seen in FIG. **1** a wafer, generally illustrated as **10**, having a semiconductor substrate, generally illustrated as **12**. The semiconductor substrate **12** includes regions of circuit elements which do not appear in the drawings, but are well known to those skilled in the art. A barrier layer **14** is disposed over the semiconductor substrate **12** and a layer (i.e., an electrically conductive layer, such as a platinum layer or an iridium layer), generally illustrated as **15**, is disposed over the barrier layer **14**. The layer **15** is preferably an electrode layer **16** as shown in FIG. **1**. Because the electrode layer **16** is a preferred layer **15**, the remaining description of the present invention will use only the term "electrode layer **16**" in describing the present invention. However, it is to be understood that wherever "electrode layer **16**" is stated hereinafter, it is to also have the equivalence of "layer **15**" for purposes of the present invention. It is also to be understood that in a preferred embodiment of the present invention "electrode layer **16**" may be a "platinum electrode layer **16**" or an "iridium electrode layer **16**," unless otherwise indicated. Thus, whenever "platinum electrode layer **16**" is stated or mentioned hereinafter for a preferred embodiment of the invention, it is be understood that the electrode layer **16** includes platinum and the preferred embodiment of the present invention relates to etching platinum to produce the desired features of the present invention as set forth hereinafter. Similarly, whenever "iridium electrode layer **16**" is stated or mentioned hereinafter for a preferred embodiment of the present invention, it is to be understood that the electrode layer **16** includes iridium and the preferred embodiment of the present invention relates to etching iridium to produce the desired features of the present invention as set forth hereinafter.

Because the electrode layer **16** easily diffuses or reacts with certain elements (e.g. it a poly-Si plug) within the

semiconductor substrate **12**, the barrier layer **14** is required between the electrode layer **16** and the semiconductor substrate **12**. The barrier layer **14** also functions as an adhesive for coupling the semiconductor substrate **12** to the electrode layer **16**. A mask **18** is disposed over the electrode layer **16** and a patterned resist (i.e. a photoresist), generally illustrated as **20**, is selectively positioned on the mask layer **18** as best shown in FIG. **1**. As best shown in FIG. **1**, the patterned resist **20** includes a plurality of resist members **20***a*, **20***b*, **20***c*, and **20***d*. In another preferred embodiment of the invention as shown in FIG. **2**, a protective layer **22** is disposed between the electrode layer **16** and the mask layer **18**.

The barrier layer **14** may be any suitable barrier layer which is capable of dually functioning as an adhesive and a diffusion barrier to the electrode layer **16**. The barrier layer **14** may be of any suitable thickness. Preferably, the barrier layer **14** comprises titanium and/or a titanium alloy, such as TiN, and possesses a thickness ranging from about 50 Angstroms to about 600 Angstroms, more preferably from about 200 Angstroms to about 400 Angstroms, most preferably about 300 Angstroms. The barrier layer **14** is preferably disposed on the semiconductor substrate **12** by the RF magnetron sputtering method.

The electrode layer **16** comprises platinum or iridium as the preferred electrode material because platinum and iridium are inert to oxidation which tends to occur in the subsequent high temperature processes of depositing the high dielectric constant ferroelectric materials. The electrode layer **16** also comprises platinum or iridium as the preferred electrode material because platinum and iridium are good electric conductors. The thickness of the electrode layer **16** would depend upon the end use of the semiconductor or capacitance device which is to contain the electrode layer **16**. Typically, the thickness of the platinum electrode layer **16** ranges from about 500 Angstroms to about 4000 Angstroms, more preferably from about 1000 Angstroms to about 3000 Angstroms, most preferably about 2000 Angstroms. The electrode layer **16** is preferably disposed on the barrier layer **14** by the RF magnetron sputtering method.

The mask layer **18** may be any suitable insulation or metallic material that is capable of being etched in accordance with the procedure described hereinafter such that all traces of the mask layer **18** are essentially removed from the surface electrode layer **16** except that portion (identified as "**18***a*," "**18***b*," "**18***c*," and "**18***d*" below) of the mask layer **18** remaining under the patterned resist **20**. The mask layer **18** may also be of any suitable thickness. Preferably, the mask layer **18** comprises silicon dioxide (SiO_2) and/or silicon nitride (Si_3N_4) or any other suitable dielectric material.

In another preferred embodiment of the invention, the mask layer **18** comprises Ti and/or TiN, preferably TiN. As will be further explained below, it has been discovered that etching of an iridium electrode layer **16** superimposed with a mask layer **18** composing TiN, and in a high density plasma of an etchant gas comprising oxygen, a halogen gas (e.g., Cl_2), and a noble gas (e.g., argon), etched iridium electrodes are produced having an iridium profile where the angle a of the associated sidewalls with respect to a horizontal plane is equal to greater than about 80 degrees. A clean iridium surface is produced after removal of the mask layer **18** with no fence or veil formation. It has been further discovered, that during etching of the iridium electrode layer **16** in a high density plasma of the etchant gas having a gas chemistry of O_2/halogen gas(es)/noble gas(es), with the iridium electrode layer **16** supporting the mask layer **18** comprising TiN, the etch selectivity of iridium to the TiN is greater than about 8.0, preferably greater than about 10.0. It is to be understood that the spirit and scope of the preent invention includes etching of a platinum electrode layer **16** while supporting a mask layer **18** comprising TiN, with the etching of the platinum electrode layer **16** being conducted in a high density plasma of an etchant gas comprising oxygen, a halogen gas (e.g., Cl_2), and a noble gas (e.g., argon). A preferred thickness for the mask layer **18** ranges from about 500 Angstroms to about 9000 Angstroms, more preferably from about 2000 Angstroms to about 7000 Angstroms, most preferably about 3000 Angstroms. The mask layer **18** is preferably disposed on the electrode layer **16** by chemical vapor deposition.

The patterned resist **20** (i.e. the photoresist **20**, including resist members **20***a*, **20***b*, **20***c* and **20***d*) may be any suitable layer of material(s) that is capable of protecting any underlying material (e.g. the mask layer **18**) from being etched during the etching process of the present invention. Suitable materials for the patterned resist **20** include resist systems consisting of novolac resin and a photoactive dissolution inhibitor (all based on Süiss's discovery). Other suitable materials for the resist **20** are listed in an article from the July 1996 edition of Solid State Technology entitled "Deep-UV Resists: Evolution and Status" by Hiroshi Ito. The patterned resist **20** may have any suitable thickness; preferably, the thickness of the patterned resist **20** ranges from about 0.3 μm to about 1.40 μm, more preferably from about 0.5 μm to about 1.2 μm, most preferably about 0.8 μm. The patterned resist **20** is preferably disposed on the mask layer **18** by the spin coating method.

The protective layer **22** in the embodiment of the invention depicted in FIG. **2** is for protecting the corners (identified as "**16***g*" below) of an etched electrode layer (generally identified as "**16***e*" below) during the overetching process of the present invention. Another purpose of the protective layer **22** is for providing good adhesion to the mask layer **18** and the electrode layer **16**. The protective layer **22** may comprise any suitable materials or chemicals, such as titanium and/or titanium nitride etc., and may be conveniently disposed on the surface of the electrode layer **16**, such as by the RF magnetron sputtering method. The thickness of the protective layer **22** may be any suitable thickness, preferably ranging from about 50 Angstroms to about 1000 Angstroms, more preferably ranging from about 100 Angstroms to about 600 Angstroms, most preferably about 300 Angstroms.

In order to form or produce a semiconductor or capacitance device from the multilayered structure of FIG. **1** or FIG. **2**, the multilayered structure is initially placed in a suitable plasma processing apparatus to break through and remove or etch away the mask layer **18** from the surface of electrode layer **16**, except those mask layers **18***a*, **18***b*, **18***c* and **18***d* that are respectively below the resist members **20***a*, **20***b*, **20***c* and **20***d*, as best shown in FIG. **5**, or as best shown in FIG. **6** if the embodiment of the invention depicted in FIG. **2** is being employed.

A suitable prior art plasma processing apparatus is shown in FIG. **3** and described in U.S. Pat. No. 5,188,704 to Babie et al, fully incorporated herein by reference thereto as if repeated verbatim immediately hereinafter. The plasma process apparatus of FIG. **3** comprises a plasma reactor, generally illustrated as **30** and including walls, generally illustrated as **31** for forming and housing a reactor chamber **32** wherein a plasma **33** of neutral (n) particles, positive (+) particles, and negative (−) particles are found. Walls **31** include cylindrical wall **54** and cover **56**. Plasma processing

gases are introduced via inlets **34** into reactor chamber **32**. Plasma etching gases are introduced into chamber **32** through inlets **44**—**44**. A water cooled cathode **36** is connected to an RF power supply **38** at 13.56 MHz. An anode **39** is connected to the walls **31** which are grounded by line **40**. Helium gas is supplied through passageway **50** through cathode **36** to the space beneath wafer **10** which is supported peripherally by lip seal **52** so that the helium gas cools the wafer **10**. The wafer **10** is supported by a wafer support **46** that includes a plurality of clamps (not shown) which hold down the upper surface of wafer **10** at its periphery, as is well known to those skilled in the art. A pair of helmholtz configured electromagnetic coils **42** and **43** provide north and south poles within the chamber **32** and are disposed at opposite ends of the lateral cylindrical wall **54** and the walls **31**. The electromagnetic coils **42** and **43** provide a transverse magnetic field with the north and south poles at the left and right providing a horizontal magnetic field axis parallel to the surface of the wafer **10**. The transverse magnetic field is applied to slow the vertical velocity of the electrons which are accelerated radially by the magnetic field as they move towards the wafer **10**. Accordingly, the quantity of electrons in the plasma **33** is increased by means of the transverse magnetic field and the plasma **33** is enhanced as is well known to these skilled in the art.

The electromagnetic coils **42** and **43** which provide the magnetic field are independently controlled to produce a field intensity orientation which is uniform. The field can be stepped angularly around the wafer **10** by rotating the energization of the electromagnetic coils **42** and **43**, sequentially. The transverse magnetic field provided by the electromagnetic coils **42** and **43** is directed parallel to the surface of the wafer **10** being treated by the plasma **33**, and the cathode **36** of the plasma reactor **30** increases ionization efficiently of the electrons in the plasma **33**. This provides the ability to decrease the potential drop across the sheath of the cathode **36** and to increase the ion current flux present on the surface of the wafer **10**, thereby permitting higher rates of etching without requiring higher ion energies to achieve the result otherwise.

The preferred magnetic source employed to achieve magnetically enhanced reactive ion etching (MERIE) used in practicing the present invention is a variable rotational field provided by the electromagnetic coils **42** and **43** arranged in a Helmholtz configuration. The electromagnetic coils **42** and **43** are driven by 3-phase AC currents. The magnetic field with Flux B is parallel to the wafer **10**, and perpendicular to the electrical field as shown in FIG. **4**. Referring to FIG. **4**, the vector of the magnetic field H which produces flux B is rotating around the center axis of the electrical field by varying the phases of current flowing through the electromagnetic coils **42** and **43** at a typical rotational frequency of 0.01 to 1 Hz, particularly at 0.5 Hz. The strength of the magnetic flux B typically varies from 0 Gauss to about 150 Gauss and is determined by the quantities of the currents supplied to the electromagnetic coils **42** and **43**. While FIG. **3** illustrates one plasma processing apparatus that is suitable for removing the mask layer **18** (except mask layers **18***a*, **18***b*, **18***c* and **18***d*), it is to be understood that other plasma etchers may be employed, such as electron cyclotron resonance (ECR), helicon resonance or inductively coupled plasma (ICP), triode etchers, etc.

The plasma **33** may employ any suitable etchant gas to break through (i.e. to clean and etch away) the mask layer **18** except those mask layers **18***a*, **18***b*, **18***c* and **18***d* that are respectively below the resist members **20***a*, **20***b*, **20***c* and **20***d*, as best shown FIGS. **5** and **6**. For example, if the mask layer **18** contains silicon oxide, suitable etchant gas(es) may be selected from the group consisting of fluorine-containing gases (e.g. CHF_3, SF_6, C_2F_6, NF_3, etc.), bromine-containing gases (e.g. HBr, etc.), chlorine-containing gases (e.g. $CHCl_3$, etc.), rare or noble gases (e.g. argon, etc.), and mixtures thereof. Preferably and in one preferred embodiment of the invention, the etchant does not include an oxidant, such as oxygen, since the purpose of this step is to remove the mask layer **18** (except those mask layers **18***a*, **18***b*, **18***c* and **18***d* which are respectively protected by resist members **20***a*, **20***b*, **20***c* and **20***d*) and not to remove the patterned resist **20**. More preferably, the etchant gas comprises from about 20% by volume to about 40% by volume CHF_3 and from about 60% by volume to about 80% by volume argon. The preferred reactor conditions for a suitable plasma processing apparatus (such as the plasma processing apparatus of FIG. **3**) in removing the mask layer **18** (except mask layers **18***a*, **18***b*, **18***c* and **18***d*) are as follows:

Pressure	10–150 mTorr
RF Power	500–1500 watts
Rotational Magnetic Field	25–70 Gauss
Temperature of Wafer	25–100° C.
Mask Layer 18 Etch Rate	2000–10,000 Angstroms/min

The selectivity of mask layer **18** to patterned resist **20** is better than 3:1, depending on the materials employed for the mask layer **18** and the patterned resist **20**.

More generally, the process parameters for removing the mask layer **18** in a suitable plasma process apparatus (such as the plasma processing apparatus of FIG. **3**) fall into ranges as listed in the following Table III and based on flow rates of the gases CHF_3 and Ar also listed in the following Table III:

TABLE III

Process	Broad	Preferred
Gas Flow, sccm		
CHF_3	10 to 50 (20 to 40% by vol.)	20 to 40
Ar	50 to 90 (60 to 80% by vol.)	60 to 80
Pressure, mT	10 to 250	10 to 150
13.56 MHz RF Power (Watts)	500 to 2500	500 to 1500
Temperature (° C.) of Wafer	10 to 120	25 to 100
Magnetic Field Gauss	10 to 120	25 to 70

In another preferred embodiment of the invention, when the mask layer **18** comprises Ti and/or TiN (preferably TiN), suitable etchant gas(es) to break through (i.e., to clean and etch away) the Ti/TiN-containing mask layer **18** except for those mask layers **18***a*, **18***b*, **18***c* and **18***d* that are respectively below the resist numbers **20***a*, **20***b*, **20***c* and **20***d*, as best shown FIGS. **5** and **6**, may be selected from the group consisting of a noble gas (e.g., argon), a halogen (e.g., Cl_2), and a gas selected from the group consisting of HBr, BCl_3, and mixtures thereof. Preferably, the etchant gas comprises from about 10% by volume to about 30% by volume argon, from about 20% by volume to about 60% by volume chlorine, and from about 20% by volume to about 60% by volume HBr and/or BCl_3. The preferred reactor conditions for a suitable plasma processing apparatus (such as the plasma processing apparatus of FIG. **3**) in removing the mask layer **18** (except mask layer **18***a*, **18***b*, **18***c* and **18***d*)

comprising Ti and/or TiN are as follows:

Pressure	10–150 mTorr
RF Power	500–1500 watts
Rotational Magnetic Field	25–70 Gauss
Temperature of Wafer	25–100° C.
Mask Layer 18 Etch Rate	2000–10,000 Angstroms/min

The selectivity of the Ti/TiN-containing mask layer **18** to patterned resist **20** is better than 3:1, depending on the materials employed for the patterned resist **20**.

More generally, the process parameters for removing the Ti/TiN-containing mask layer **18** in a suitable plasma process apparatus (such as the plasma processing apparatus of FIG. **3**) fall into ranges as listed in the following Table IV and based on flow rates of the gases argon, chlorine and HBr and/or BCl_3 also listed in the following Table IV:

TABLE IV

Process	Broad	Preferred
Gas Flow, sccm		
Argon	10 to 50 (10 to 30% by vol.)	30 to 40
Chlorine	30 to 100 (20 to 60% by vol.)	60 to 80
HBr and/or BCl_3	30 to 100 (20 to 60% by vol.)	50 to 70
Pressure, mT	10 to 250	10 to 150
13.56 MHz RF Power (Watts)	500 to 2500	500 to 1500
Temperature (° C.) of Wafer	10 to 120	25 to 100
Magnetic Field Gauss	10 to 120	25 to 70

For the embodiment of the invention depicted in FIG. **2** wherein the protective layer **22** is disposed on the electrode layer **16** between the mask layer **18** and the electrode layer **16**, the protective layer **22** has to be removed or etched after removal of the mask layer **18** in order to expose the electrode layer **16**. The protective layer **22** may be etched and removed by any suitable manner and/or with any suitable plasma processing apparatus (such as with the plasma processing apparatus of FIG. **3**) including the plasma **33** employing a suitable etchant gas to break through and etch away the protective layer **22** except those protective layers **22***a*, **22***b*, **22***c* and **22***d* (see FIGS. **6** and **8**) immediately below mask layers **18***a*, **18***b*, **18***c* and **18***d*, respectively. For example, if TiN is used as the protective layer **22**, suitable etchant gas(es) may be selected from the group consisting of Cl_2, HBr, BCl_3, noble gases (e.g., Ar), and mixtures thereof. Preferably and in one embodiment of the present invention, the etchant gas for breaking through and etching away the protective layer **22**, except protective layers **22***a*, **22***b*, **22***c* and **22***d*, comprises from about 20% by volume to about 60% by volume Cl_2, from about 20% by volume to about 60% by volume HBr and/or BCl_3, and from about 10% by volume to about 30% by volume of a noble gas which is preferably Ar. Suitable reactor conditions for a suitable plasma processing apparatus (such as the plasma processing apparatus of FIG. **3**) to remove the protective layer **22** (except protective layers **22***a*, **22***b*, **22***c* and **22***d*) may be the same as those previously stated reactor conditions for the removal of the mask layer **18** (except mask layers **18***a*, **18***b*, **18***c* and **18***d*). It is to be understood that other plasma etchers may be employed to remove the protective layer **20**, such as ECR, ICP, Helicon Resonance, etc. As will be further explained below, the protective layers **22***a*, **22***b*, **22***c* and **22***d* are for protecting the corners (identified as "**16***g*" below) of an etched electrode layer (generally identified as "**16***e*" below) during the etching process of the present invention. It is believed that the protective layers **22***a*, **22***b*, **22***c* and **22***d* not only protect the corners of an etched electrode layer **16** during the etching process, but also assist in maintaining an existing profile and/or improves a profile (i.e., an etched platinum or iridium profile).

In another embodiment of the present invention for etching a platinum electrode layer **16**, the protective layer **22** (except protective layers **22***a*, **22***b*, **22***c* and **22***d*) may be etched by the high temperatures and etchant gases employed in the platinum-etching process of the present invention. More specifically and as will be further explained below, because the platinum electrode layer **16** is preferably etched under the following process conditions in a high density plasma chamber containing a high density inductively coupled plasma:

Process	Parameters
Etchant Gas flow	50 to 500 sccm
Halogen Gas (e.g., Cl_2)	20% to 95% by vol.
Noble Gas (e.g., Ar)	5% to 80% by vol.
Pressure, mTorr	0.1 to 300 milliTorr
RF Power (watts) of Coil Inductor	100 to 5000 watts
RF Power (watts) of Wafer Pedestal	50 to 3000 watts
Temperature (° C.) of Platinum Electrode Wafer	about 150 to about 500° C.
Platinum Etch Rate (Å/min)	200 to 6000 Å/min
RF Frequency of Coil Inductor	100 K to 300 MHz
RF Frequency of Wafer Pedestal	100 K to 300 MHz

the protective layer **22** may be etched and removed under the same foregoing conditions. Thus, the same apparatus and process conditions may be employed to etch and remove selective parts of the protective layer **22**, as well as to etch the platinum electrode layer **16**. In another preferred embodiment of the present invention and as will be also further explained below,the protective layer **22** and the platinum electrode layer **16** may be removed and etched respectively in a high density plasma chamber containing a high density inductively coupled plasma under the following process conditions:

Process	Parameters
Etchant Gas flow	50 to 500 sccm
Halogen Gas (e.g., Cl_2)	10% to 90% by vol.
Noble Gas (e.g., Ar)	5% to 80% by vol.
HBr and/or BCl_3	45% to 25% by vol.
Pressure, mTorr	0.1 to 300 milliTorr
RF Power (watts) of Coil Inductor	100 to 5000 watts
RF Power (watts) of Wafer Pedestal	50 to 3000 watts
Temperature (° C.) of Platinum Electrode Wafer	about 150 to 500° C.
Platinum Etch Rate (Å/min)	200 to 6000 Å/min
RF Frequency of Coil Inductor	100 K to 300 MHz
RF Frequency of Wafer Pedestal	100 K to 300 MHz

In another embodiment of the present invention for etching an iridium electrode layer **16**, the protective layer **22**

(except protective layers **22***a*, **22***b*, **22***c* and **22***d*) may be etched by the high temperatures and etchant gases employed in the iridium-etching process of the present invention. More specifically and as will be further explained below, because the iridium electrode layer **16** is preferably etched under the following process conditions in a high density plasma chamber containing a high density inductively coupled plasma:

Process	Parameters
Etchant Gas flow	50 to 500 sccm
Oxygen	5% to 40% by vol.
Halogen Gas (e.g., Cl_2)	10% to 60% by vol.
Noble Gas (e.g., Ar)	30% to 80% by vol.
Pressure, mTorr	0.1 to 300 milliTorr
RF Power (watts) of Coil Inductor	100 to 5000 watts
RF Power (watts) of Wafer Pedestal	50 to 3000 watts
Temperature (° C.) of Iridium Electrode Wafer	about 150 to about 500° C.
Iridium Etch Rate (Å/min)	200 to 6000 Å/min
RF Frequency of Coil Inductor	100 K to 300 MHz
RF Frequency of Wafer Pedestal	100 K to 300 MHz

the protective layer **22** may be etched under the same foregoing conditions. Thus, the same apparatus and process conditions may be employed to etch and remove selective parts of the protective layer **22**, as well as to etch the iridium electrode layer **16**. In another preferred embodiment of the present invention and as will be also further explained below, the protective layer **22** and the iridium electrode layer **16** may be removed and etched respectively in a high density plasma chamber containing a high density inductively coupled plasma under the following process conditions:

Process	Parameters
Etchant Gas flow	50 to 500 sccm
Oxygen	5% to 20% by vol.
Halogen Gas (e.g., Cl_2)	10% to 60% by vol.
Noble Gas (e.g., Ar)	30% to 80% by vol.
HBr and/or HCl	5% to 20% by vol.
Pressure, mTorr	0.1 to 300 milliTorr
RF Power (watts) of Coil Inductor	100 to 5000 watts
RF Power (watts) of Wafer Pedestal	50 to 3000 watts
Temperature (° C.) of Iridium Electrode Wafer	about 150 to 500° C.
Iridium Etch Rate (Å/min)	200 to 6000 Å/min
RF Frequency of Coil Inductor	100K to 300 MHz
RF Frequency of Wafer Pedestal	100K to 300 MHz

After selective parts of the mask layer **18** have been etched away from the surface of the electrode layer **16** to expose the latter and such that the only remnants of the mask layer **18** are the mask layers **18***a*, **18***b*, **18***c* and **18***d* situated immediately below the resist members **20***a*, **20***b*, **20***c*, and **20***d*, respectively, the resist members **20***a*, **20***b*, **20***c* and **20***d* are to be removed. The resist members **20***a*, **20***b*, **20***c* and **20***d* may be removed at any suitable time, preferably before the etching of the electrode layer **16** and before the heating of the semiconductor substrate **12** to a temperature greater than about 150° C. The same would hold true with respect to the embodiment of the invention illustrated in FIGS. **2**, **6** and **8** in that after selective parts of the protective layer **22** have been etched away from the surface of the electrode layer **16** to expose the latter and such that the only remnants of the protective layer **22** are the protective layers **22***a*, **22***b*, **22***c* and **22***d* situated respectively immediately below the mask layers **18***a*, **18***b*, **18***c* and **18***d*, the resist members **20***a*, **20***b*, **20***c* and **20***d* are to be removed. However, with respect to this embodiment of the present invention, the resist members **20***a*, **20***b*, **20***c* and **20***d* may be removed before the etching away of selective parts of the protective layer **22**. Alternatively, the resist members **20***a*, **20***b*, **20***c* and **20***d* may be removed after (or simultaneously during) the removal of selective parts of the protective layer **22** and before the heating of the semiconductor substrate **12** to a temperature greater than about 150° C. for purposes of etching the electrode layer **16**. Typically, at least a portion of the resist members **20***a*, **20***b*, **20***c* and **20***d* would be removed while selective parts of the protective layer **22** are being etched away to expose the electrode layer **16** that is not superimposed by the protective layers **22***a*, **22***b*, **22***c* and **22***d*.

The resist members **20***a*, **20***b*, **20***c* and **20***d* may be removed in any suitable manner such as by using oxygen plasma ashing which is well known to those skilled in the art. The resist members **20***a*, **20***b*, **20***c* and **20***d* may be respectively stripped from the mask layers **18***a*, **18***b*, **18***c* and **18***d* with any suitable plasma processing apparatus, such as the plasma processing apparatus shown in FIG. **3** and employing a plasma containing an etchant gas comprising oxygen. The resist members **20***a*, **20***b*, **20***c* and **20***d* have been respectively removed from the mask layers **18***a*, **18***b*, **18***c* and **18***d* in an advanced strip passivation (ASP) chamber of a plasma processing apparatus sold under the trade mark metal etch MKP Centura to Applied Materials, Inc. 3050 Bowers Avenue, Santa Clara, Calif. 95054-3299. In stripping the resist members **20***a*, **20***b*, **20***c* and **20***d* from the mask layers **18***a*, **18***b*, **18***c* and **18***d*, respectively, the ASP chamber may employ microwave downstream O_2/N_2 plasma with the following recipe: 120 seconds, 250° C., 1400 W, 3000 cc O_2, 300 cc N_2 and 2 Torr.

After the electrode layer **16** has been exposed as represented in FIGS. **7** and **8**, it is etched to develop a submicron pattern with a profile. As will be further stated below, before the electrode layer **16** is etched, the semiconductor substrate **12** supporting the electrode layer **16** is heated to a temperature greater than about 150° C., preferably greater than about 150° C. up to about 500° C., more preferably from about 200° C. to about 400° C., most preferably from about 250° C. to about 350° C. The semiconductor substrate **12** is preferably heated by the pedestal which supports the wafer **10** during the etching process.

The electrode layer **16** may be etched in any suitable plasma processing apparatus, such as in the reactive ion etch (RIE) plasma processing apparatus sold under the trademark AME8100 Etch™, or under the trademark Precision Etch 5000™, or under the trademark Precision Etch 8300™, all trademarks owned by Applied Materials Inc., 3050 Bowers Avenue, Santa Clara, Calif. 95054-3299. Another suitable plasma processing apparatus for etching the electrode layer **16** is that plasma processing apparatus sold under the trademark Metal Etch DPS Centura™ also owned by Applied Materials, Inc. It is also to be understood that other plasma etchers may be employed, such as ECR, ICP, Helicon Resonance, etc.

A suitable plasma processing apparatus for etching the electrode layer **16** employs a plasma of an etchant gas,

which is capable of producing good profiles (e.g. platinum or iridium profiles) equal to or greater than about 85 degrees, preferably equal to or greater than about 87 degrees, more preferably equal to or greater than about 88.5 degrees. The etchant gas broadly comprises, or consists of or consists essentially of, a halogen containing gas, such as a halogen gas (e.g., fluorine, chlorine, bromine, iodine, and astatine) and a noble gas such as helium, neon, argon, krypton, xenon, and radon. Preferably, the etchant gas comprises or consists of or consists essentially of a halogen (preferably chlorine) and a noble gas selected from the group consisting of helium, neon, and argon. The noble gas is preferably argon. The etchant gas more specifically comprises, or consists of or consists essentially of, preferably from about 20% by volume to about 95% by volume of the halogen gas (i.e., chlorine) and from about 5% by volume to about 80% by volume of the noble gas (i.e., argon); more preferably from about 40% by volume to about 80% by volume of the halogen gas (i.e., chlorine) and from about 20% by volume to about 60% by volume of the noble gas (i.e., argon); most preferably from about 55% by volume to about 65% by volume of the halogen gas (i.e., chlorine) and from about 35% by volume to about 45% by volume of the noble gas (i.e., argon).

The etchant gas may also broadly comprise oxygen, a halogen containing gas, such as a halogen gas (e.g., fluorine, chlorine, bromine, iodine, and astatine), and a noble gas such as helium, neon, argon, krypton, xenon, and radon. Preferably, the etchant gas comprises, or consists of or consists essentially of, a halogen (preferably chlorine) and a noble gas selected from the group consisting of helium, neon and argon. The noble gas is preferably argon. The etchant gas more specifically comprises, or consists of or consists essentially of, preferably from about 5% by volume to about 40% by volume oxygen, from about 10% by volume to about 60% by volume of the halogen gas (i.e., chlorine), and from about 30% by volume to about 80% by volume of the noble gas (i.e., argon); more preferably from about 10% by volume to about 30% by volume oxygen, from about 20% by volume to about 50% by volume of the halogen gas (i.e., chlorine), and from about 40% by volume to about 70% of the noble gas (i.e., argon); most preferably from about 10% by volume to about 20% by volume oxygen, from about 20% by volume to about 30% by volume halogen gas (i.e., chlorine), and from about 50% by volume to about 70% by volume of noble gas (i.e., argon).

In another preferred embodiment of the invention, the etchant gas comprises, preferably consists of or consists essentially of, the halogen (i.e., chlorine), the noble gas (i.e., argon), and a gas selected from the group consisting of HBr, BCl_3 and mixtures thereof. The etchant gas more specifically comprises, or consists of or consists essentially of, from about 10% by volume to about 90% by volume of the halogen gas (i.e., chlorine) and from about 5% by volume to about 80% by volume of the noble gas (i.e., argon) and from about 4% by volume to about 25% by volume of HBr and/or BCl_3; preferably from about 40% by volume to about 70% by volume of the halogen gas (i.e., chlorine) and from about 25% by volume to about 55% by volume of the noble gas (i.e., argon) and from about 5% by volume to about 20% by volume of HBr and/or BCl_3; and more preferably from about 50% by volume to about 60% by volume of the halogen gas (i.e., chlorine) and from about 35% by volume to about 45% by volume of the noble gas (i.e., argon) and from about 5% by volume to about 15% by volume of HBr and/or BCl_3. The etchant gas flow rate ranges from about 50 sccm to about 500 sccm. HBr and/or BCl_3 are for removal of residue (e.g., platinum or iridium residue) during etching of the electrode layer **16**. Plasmas containing argon are known to have a high energetic ion concentration and are often used for physical sputtering. The sputtering effect due to the ions is a function of the accelerating potential which exist between the plasma and the sample.

In a further preferred embodiment of the invention, the etchant gas comprises, preferably consists of or consists essentially of, oxygen, the halogen (i.e., chlorine), the noble gas (i.e., argon), and a gas selected from the group consisting of HBr, HCl and mixtures thereof. The etchant gas more specifically comprises, or consists of or consists essentially of, from about 5% by volume to about 20% by volume oxygen, from about 10% by volume to about 60% by volume of the halogen gas (i.e., chlorine) and from about 30% by volume to about 80% by volume of the noble gas (i.e., argon) and from about 5% by volume to about 20% by volume of HBr and/or HCl; preferably from about 5% by volume to about 15% by volume oxygen, from about 20% by volume to about 50% by volume of the halogen gas (i.e., chlorine) and from about 40% by volume to about 70% by volume of the noble gas (i.e., argon) and from about 5% by volume to about 15% by volume of HBr and/or HCl; and more preferably from about 5% by volume to about 10% by volume oxygen, from about 20% by volume to about 35% by volume of the halogen gas (i.e., chlorine) and from about 40% by volume to about 60% by volume of the noble gas (i.e., argon) and from about 5% by volume to about 10% by volume of HBr and/or HCl. The etchant gas flow rate ranges from about 50 sccm to about 500 sccm.

The reactor conditions for a suitable plasma processing apparatus, such as the plasma processing apparatus of FIG. **3**, in etching the electrode layer **16** are as follows:

Pressure	0.1~300 mTorr
RF Power	100–5000 watts
Rotational Magnetic Field	20~100 Gauss
Temperature of Wafer	about 150–about 500° C.
Platinum Layer 16 Etch Rate	200–6000 Angstroms/min

The selectivity of electrode layer **16** to mask **18** is better than 2:1, depending on the materials employed for the patterned resist **18**.

More generally, the process parameters for etching the electrode layer **16** in a suitable plasma processing apparatus, such as the plasma processing apparatus of FIG. **3**, fall into ranges as listed in the following Table V and based on the flow rate of etchant gas as also listed in Table V below:

TABLE V

Process	Broad	Preferred	Optimum
Gas Flow, sccm			
Etchant Gas	50 to 500	75 to 250	100 to 200
Pressure, mT	20 to 2000	30 to 300	50 to 150
13.56 MHz RF Power (Watts)	50 to 3000	500 to 2000	700 to 1200
Temperature (° C.) of Wafer	150 to 500	200 to 400	250 to 350
Magnetic Field Gauss	0 to 140	20 to 100	60 to 80

As previously indicated, a preferred etchant gas for etching the platinum electrode layer **16** is a mixture of chlorine and argon, or a mixture of chlorine, argon and HBr and/or BCl_3. Another preferred etchant gas for etching the electrode layer **16** is a mixture of oxygen, chlorine and argon, or a

mixture of oxygen, chlorine, argon and HBr and/or HCl. If the etchant gas is a mixture of chlorine and argon (i.e., from about 20% by volume to about 95% by volume chlorine and from about 5% by volume to about 80% by volume argon), or a mixture of oxygen, chlorine and argon (i.e., from about 5% to about 40% by volume oxygen, from about 10% to about 60% by volume chlorine, and from about 30% to about 80% by volume argon), or a mixture of chlorine, argon and HBr and/or BCl_3 (i.e., from about 10% by volume to about 90% by volume chlorine and from about 5% by volume to about 80% by volume argon and from about 4% by volume to about 25% by volume HBr and/or BCl_3), or a mixture of oxygen, chlorine, argon and HBr and/or HCl (i.e., from about 5% to about 20% by volume oxygen, from about 10% to about 60% by volume chlorine, from about 30% to about 80% by volume argon, and from about 5% to about 20% by volume HBr and/or HCl), and if the semiconductor substrate 12 is heated to a temperature greater than about 150° C., preferably to a temperature ranging from about 150° C. to about 500° C., the plasma processing apparatus for etching the electrode layer **16** (i.e., a platinum electrode layer **16** or an iridium electrode layer **16**) etches the electrode layer **16** in a high density plasma of the etchant gas at a high etch rate (i.e. an etch rate higher than 700 Å/min for iridium, and an etch rate higher than 1000 Å/min for platinum) and produces an etched electrode layer, generally illustrated as **16***e* (as best shown in FIGS. **9** and **10**). The etched platinum electrode layer **16***e* (i.e., etched platinum electrode layer **16***e* or etched iridium electrode layer **16***e*) includes etched electrode layers **16***a*, **16***b*, **16***c* and **16***d* (i.e., etched platinum or iridium electrode layers **16***a*, **16***b*, **16***c* and **16***d*) having corners **16***g* and sidewalls **16***s* and an excellent profile (i.e., an excellent platinum or iridium profile); that is, a profile where the angle of the sidewalls **16***s* (as also best shown in FIGS. **9** and **10**) with respect to a horizontal plane is equal to or greater than about 80 degrees for iridium, and equal to or greater than about 85 degrees for platinum, preferably equal to or greater than about 87°, and more preferably equal to or greater than about 88.5°. The produced electrodes (i.e., produced platinum electrodes) are separated by a distance or space having a dimension equal to or less than about 0.3 μm. Each of the electrodes include a dimension having a value equal to or less than about 0.6 μm, preferably equal to or less than about 0.3 μm. More preferably, each of the electrodes have a width equal to or less than about 0.6 μm, and a height equal to or less than about 0.6 μm.

It has also been discovered that the etched electrode layer **16***e* (i.e., etched electrode layers **16***a*, **16***b*, **16***c* and **16***d*) has essentially no wall-like structures extending up from the edges of the electrode region (i.e., the platinum region or the iridium region). These wall-like structures are frequently referred to as "veils" or "fences" or "rabbit ears." Therefore, the method of the present invention produces etched electrode layers **16***a*, **16***b*, **16***c* and **16***d* which are essentially veil-less. Because the produced etched electrode layers **16***a*, **16***b*, **16***c* and **16***d* are essentially veil-less and have no "fences" or "rabbit ears," they are ideally suited for receiving a dielectric BST or PZT layer and functioning as electrodes in a semiconductor device (i.e., a capacitance structure).

The high density plasma of the present invention may be defined as a plasma of the etchant gas of the present invention having an ion density greater than about $10^9/cm^3$, preferably greater than about $10^{11}/cm^3$. The source of the high density plasma may be any suitable high density source, such as electron cyclotron resonance (ECR), helicon resonance or inductively coupled plasma (ICP)-type sources. All three are in use on production equipment today. The main difference is that ECR and helicon sources employ an external magnetic field to shape and contain the plasma, while ICP sources do not.

The high density plasma for the present invention is more preferably produced or provided by inductively coupling a plasma in a decoupled plasma source etch chamber, such as that sold under the trademark DPS™ owned by Applied Materials, Inc. which decouples or separates the ion flux to the wafer **10** and the ion acceleration energy. The design of the etch chamber provides fully independent control of ion density of an enlarged process window. This is accomplished by producing plasma via an inductive source. While a cathode within the etch chamber is still biased with rf electric fields to determine the ion acceleration energy, a second rf source (i.e. an inductive source) determines the ion flux. This second rf source is not capacitive (i.e. it does not use electric fields like the cathode) since a large sheath voltage would be produced, interfering with the cathode bias and effectively coupling the ion energy and ion flux.

The inductive plasma source couples rf power through a dielectric window rather than an electrode. The power is coupled via rf magnetic fields (not electric fields) from rf current in a coil. These rf magnetic fields penetrate into the plasma and induce rf electric fields (therefore the term "inductive source") which ionize and sustain the plasma. The induced electric fields do not produce large sheath voltages like a capacitive electrode and therefore the inductive source predominantly influences ion flux. The cathode bias power plays little part in determining ion flux since most of the rf power (typically an order of magnitude less than the source power) is used in accelerating ions. The combination of an inductive plasma source and a capacitive wafer bias allows independent control of the ion flux and ion energy reaching the wafer **10** in the etch chamber, such as the DPST™ brand etch chamber.

DPST™ brand etch chambers for producing the high density plasma of the present invention for etching the electrode layer **16** to produce the etched electrode layers **16***a*, **16***b*, **16***c* and **16***d* may be any of the DPS™ brand etch chambers of the inductively coupled plasma reactor disclosed in U.S. Pat. No. 5,753,044, issued May 19, 1998, entitled "RF PLASMA REACTOR WITH HYBRID CONDUCTOR AND MULTI-RADIUS DOME CEILING" and assigned to the present assignee and fully incorporated herein by reference thereto as if repeated verbatim immediately hereinafter. Referring now to FIGS. **17** and **18** for two (2) embodiments of an inductively coupled plasma reactor from U.S. Pat. No. 5,753,044 there is seen an inductively coupled RF plasma reactor generally illustrated as **90**, having a reactor chamber, generally illustrated as **92**, wherein a high density plasma **94** of neutral (n) particles, positive (+) particles, and negative (−) particles are found. The reactor chamber **92** has a grounded conductive cylindrical sidewall **60** and a dielectric ceiling **62**. The inductively coupled RF plasma reactor **90** further comprises a wafer pedestal **64** for supporting the (semiconductor) wafer **10** in the center of the chamber **92**, a cylindrical inductor coil **68** surrounding an upper portion of the chamber **92** beginning near the plane of the top of the wafer **10** or wafer pedestal **64** and extending upwardly therefrom toward the top of the chamber **92**, an etching gas source **72** and gas inlet **74** for furnishing an etching gas into the interior of the chamber **92**, and a pump **76** for controlling the pressure in the chamber **92**. The coil inductor **68** is energized by a plasma source power supply or RF generator **78** through a

conventional active RF match network **80**, the top winding of the coil inductor **68** being "hot" and the bottom winding being grounded. The wafer pedestal **64** includes an interior conductive portion **82** connected to the bias RF power supply or generator **84** and an exterior grounded conductor **86**. (insulated from the interior conductive portion **82**). Thus, the plasma source power applied to the coil inductor **68** by the RF generator **78** and the DC bias RF power applied to the wafer pedestal **64** by generator **84** are separately controlled RF supplies. Separating the bias and source power supplies facilitates independent control of ion density and ion energy, in accordance with well-known techniques. To produce high density plasma **94** as an inductively coupled plasma, the coil inductor **68** is adjacent to the chamber **92** and is connected to the RF source power supply or the RF generator **78**. The coil inductor **68** provides the RF power which ignites and sustains the high ion density of the high density plasma **94**. The geometry of the coil inductor **68** can in large part determine spatial distribution of the plasma ion density of the high density plasma **94** within the reactor chamber **92**.

Uniformity of the plasma density spatial distribution of the high density plasma **94** across the wafer **10** is improved (relative to conical or hemispherical ceilings) by shaping the ceiling **62** in a multi-radius dome and individually determining or adjusting each one of the multiple radii of the ceiling **62**. The multiple-radius dome shape in the particular embodiment of FIG. **17** somewhat flattens the curvature of the ceiling **62** around the center portion of the ceiling **62**, the peripheral portion of the ceiling **62** having a steeper curvature.

As illustrated in FIG. **18** the coil inductor **68** may be coupled to the RF power source **78**, **80** in a mirror coil configuration that is known to those skilled in the art. In the mirror coil configuration of FIG. **18**, the RF source **78**, **80** is connected to the center winding of the coil inductor **68** while the top and bottom ends of the coil inductor **68** are both grounded. The mirror coil configuration has the advantage of reducing the maximum potential on the coil inductor **68**.

It has been discovered that by employing a high density plasma, such as the high density plasma **94** illustrated in FIGS. **17** and **18**, for etching the electrode layer **16** (i.e., a platinum electrode layer **16** or an iridium electrode layer **16**), and by heating the semiconductor substrate **12** to a temperature greater than about 150° C. before conducting the etching operation under process parameters which are stated below, a semiconductor device is produced with electrodes (i.e., platinum electrodes or iridium electrodes) having a profile with an angular value which is equal to or greater than about 80 degrees for iridium, and equal to or greater than about 85 degrees for platinum, more preferably equal to or greater than about 87 degrees, most preferably equal to or greater than about 88.5 degrees. The electrodes are essentially veil-less; that is, they have no "fences" or "rabbit ears." The electrodes are preferably separated by a distance or space having a dimension equal to or less than about 0.3 μm. Each of the electrodes include a dimension having a value equal to or less than about 0.6 μm, preferably equal to or less than about 0.3 μm. More preferably, each of the electrodes have a width equal to or less than about 0.3 μm, a length equal to or less than about 0.6 μm, and a height equal to or less than about 0.6 μm.

The preferred reactor conditions for a suitable inductively coupled RF plasma reactor, such as the inductively coupled RF plasma reactor **90** in FIGS. **17** and **18**, in etching the electrode layer **16** are as follows:

Pressure	0.1 to 300 mTorr
RF Power to Coil Inductor	100 to 5000 watts
RF Power to Wafer Pedestal	50 to 3000 watts
RF Frequency in Coil Inductor	100K to 300 MHz
RF Frequency in Wafer Pedestal	100K to 300 MHz
Temperature of Wafer	150 to 500° C.
Platinum Etch Rate	200 to 6000 Angstrom/min

More generally, the process parameters for etching the electrode layer **16** in a suitable inductively coupled plasma reactor, such as the inductively coupled plasma reactor **90** in FIGS. **17** and **18**, fall into ranges as listed on the basis of flow rates of the gases, including the halogen gas(es) (i.e., Cl_2) and the noble gas(es) (i.e., argon), as listed in Table VI below.

TABLE VI

Process	Broad	Preferred	Optimum
Gas Flow, sccm			
Cl_2	30 to 400	50 to 250	60 to 150
Ar	20 to 300	30 to 200	40 to 100
Pressure, mT	0.1 to 300	10 to 100	10 to 40
RF Power of Coil Inductor (Watts)	100 to 5000	650 to 2000	900 to 1500
RF Power of Wafer Pedestal (Watts)	50 to 3000	100 to 1000	150 to 400
Temperature of Wafer (° C.)	about 150 to about 500	200 to 400	250 to 350
Etch Rate (Å/min)	200 to 6000	500 to 3000	1000 to 2000
RF Frequency of Coil Inductor	100K to 300 MHz	400K to 20 MHz	2 to 13.5 MHz
RF Frequency of Wafer Pedestal	100K to 300 MHz	400K to 20 MHz	400K to 13.5 MHz

Also generally, the process parameters for etching the electrode layer **16** in a suitable inductively coupled plasma reactor, such as the inductively coupled plasma reactor **90** in FIGS. **17** and **18**, fall into ranges as listed on the basis of flow rates of the gases, including oxygen, the halogen gas(es) (i.e., Cl_2), and the noble gas(es) (i.e., argon), as listed in Table VII below.

TABLE VII

Process	Broad	Preferred	Optimum
Gas Flow, sccm			
O_2	10 to 60	10 to 40	15 to 30
Cl_2	30 to 100	30 to 70	50 to 70
Ar	50 to 250	100 to 200	100 to 150
Pressure, mT	0.1 to 300	10 to 100	10 to 40
RF Power of Coil Inductor (Watts)	100 to 5000	650 to 2000	900 to 1500
RF Power of Wafer Pedestal (Watts)	50 to 3000	100 to 1000	150 to 600
Temperature of Wafer (° C.)	about 150 to about 500	200 to 400	250 to 350
Etch Rate (Å/min)	200 to 6000	500 to 3000	500 to 2000
RF Frequency of Coil Inductor	100K to 300 MHz	400K to 20 MHz	2 to 13.5 MHz
RF Frequency of Wafer Pedestal	100K to 300 MHz	400K to 20 MHz	400K to 13.5 MHz

More generally further, and when the etchant gases are a mixture of the halogen gas(es) (i.e., chlorine), the noble

gas(es) (i.e., argon), and HBr and/or BCl_3, the process parameters for etching the electrode layer **16** in a suitable inductively coupled plasma reactor, such as the inductively coupled plasma reactor **90** in FIGS. **17** and **18**, fall into the ranges as listed on the basis of flow rates of the gases, including the halogen gas(es) (i.e., Cl_2) and the noble gas(es) (i.e., Ar) and HBr and/or BCl_3, as listed in Table VIII below:

TABLE VIII

Process	Broad	Preferred	Optimum
Gas Flow, sccm			
Cl_2	30 to 400	50 to 250	60 to 150
Ar	20 to 300	30 to 200	40 to 100
HBr and/or BCl_3	5 to 70	5 to 40	5 to 20
Pressure, mT	0.1 to 300	10 to 100	10 to 40
RF Power of Coil Inductor (Watts)	100 to 5000	650 to 2000	750 to 1000
RF Power of Wafer Pedestal (Watts)	50 to 3000	100 to 1000	150 to 400
Temperature of Wafer (° C.)	about 150 to about 500	200 to 400	250 to 350
Etch Rate (Å/min)	200 to 6000	500 to 3000	1000 to 2000
RF Frequency of Coil Inductor	100K to 300 MHz	400K to 20 MHz	2 to 13.5 MHz
RF Frequency of Wafer Pedestal	100K to 300 MHz	400K to 20 MHz	400 K to 13.5 MHz

Also more generally further, and when the etchant gases are a mixture of oxygen, the halogen gas(es) (i.e., chlorine), the noble gas(es) (i.e., argon), and HBr and/or BCl_3, the process parameters for etching electrode layer **16** in a suitable inductively coupled plasma reactor, such as the inductively coupled plasma reactor **90** in FIGS. **17** and **18**, fall into the ranges as listed on the basis of rates of the gases, including oxygen, the halogen gas(es) (i.e., Cl_2), the noble gas(ses) (i.e., Ar), and HBr and/or HCl, as listed in Table IX below:

TABLE IX

Process	Broad	Preferred	Optimum
Gas Flow, sccm			
O_2	10 to 60	10 to 40	15 to 30
Cl_2	30 to 100	30 to 70	50 to 70
Ar	50 to 250	100 to 200	100 to 150
HBr and/or HCl	10 to 60	10 to 40	15 to 30
Pressure, mT	0.1 to 300	10 to 100	10 to 40
RF Power of Coil Inductor (Watts)	100 to 5000	650 to 2000	750 to 1000
RF Power of Wafer Pedestal (Watts)	50 to 3000	100 to 1000	150 to 600
Temperature of Wafer (° C.)	about 150 to about 500	200 to 400	250 to 350
Etch Rate (Å/min)	200 to 6000	500 to 3000	500 to 2000
RF Frequency of Coil Inductor	100K to 300 MHz	400K to 20 MHz	2 to 13.5 MHz
RF Frequency of Wafer Pedestal	100K to 300 MHz	400K to 20 MHz	400 K to 13.5 MHz

Therefore, the foregoing process conditions are preferably based on flow rates of etchant gas(es) having a flow rate value ranging from about 5 to about 500 sccm. It will be appreciated by those skilled in the art that the process parameters of Tables V and VI, as well as other process parameters described herein, may vary in accordance with the size of the wafer **10**. As was previously mentioned, the etchant gas comprises or consists of or consists essentially of a halogen (preferably chlorine) and a noble gas selected from the group consisting of helium, neon, and argon. In another preferred embodiment of the invention, the etchant gas comprises, or consists of or consists essentially of, oxygen, a halogen (preferably chlorine), and a noble gas selected from the group consisting of helium, neon, and argon. The noble gas is preferably argon. As was also previously mentioned, the etchant gas more specifically-comprises, or consists of or consists essentially of, from about 20% by volume to about 95% by volume of the halogen gas (i.e., chlorine) and from about 5% by volume to about 80% by volume of the noble gas (i.e., argon); preferably from about 40% by volume to about 80% by volume of the halogen gas (i.e., chlorine) and from about 20% by volume to about 60% by volume of the noble gas (i.e., argon); more preferably from about 55% by volume to about 65% by volume of the halogen gas (i.e., chlorine) and from about 35% by volume to about 45% by volume of the noble gas (i.e., argon). As was further previously mentioned, the etchant gas more specifically comprises, or consists of or consists essentially of, from about 5% by volume to about 40% by volume oxygen, from about 10% by volume to about 60% by volume of the halogen gas (i.e., chlorine) and from about 30% by volume to about 80% by volume of the noble gas (i.e., argon); preferbly from about 10% by volume to about 30% by volume oxygen, from about 20% by volume to about 50% by volume of the halogen gas (i.e., chlorine) and from about 40% by volume to about 70% by volume of the noble gas (i.e., argon); more preferably from about 10% by volume to about 20% by volume oxygen, from about 20% by volume to about 30% by volume of the halogen gas (i.e., chlorine) and from about 50% by volume to about 70% by volume of the noble gas (i.e., argon). In yet another preferred embodiment of the invention and as was previously mentioned, the etchant gas comprises, preferably consists of or consists essentially of, the halogen (i.e., chlorine), the noble gas (i.e., argon), and a gas selected from the group consists of HBr, BCl_3 and mixtures thereof. In also yet another preferred embodiment of the invention and as was previously mentioned, the etchant gas comprises, preferably consists of or consists essentially of, oxygen, the halogen (i.e., chlorine), the noble gas (i.e., argon), and a gas selected from the group consists of HBr, BCl_3 and mixtures thereof. The etchant gas more specifically comprises, or consists of or consists essentially of from about 10% by volume to about 90% by volume of the halogen gas (i.e., chlorine) and from about 5% by volume to about 80% by volume of the noble gas (i.e., argon) and from about 4% by volume to about 25% by volume of HBr and/or BCl_3; preferably from about 40% by volume to about 70% by volume of the halogen gas (i.e., chlorine) and from about 25% by volume to about 55% by volume of the noble gas (i.e., argon) and from about 5% by volume to about 20% by volume of HBr and/or BCl_3; and more preferably from about 50% by volume to about 60% by volume of the halogen gas (i.e., chlorine) and from about 35% by volume to about 45% by volume of the noble gas (i.e., argon) and from about 5% by volume to about 15% by volume of HBr and/or BCl_3. As was also yet further previously mentioned, the etchant gas more specifically comprises, or consists of or consists essentially of, from about 5% by volume to about 20% by volume oxygen, from about 10% by volume to about 60% by volume of the halogen gas (i.e., chlorine) and from about 30% by volume to about 80% by volume of the noble gas (i.e., argon) and from about 5% by volume to about 20% by volume of HBr and/or HCl; preferably from about 5% by volume to about 15% by volume oxygen, from about 20% by volume to about 50% by volume of the halogen gas (i.e., chlorine), from about 40% by volume to about 70% by volume of the noble gas (i.e., argon) and from about 5% by

volume to about 15% by volume of HBr and/or HCl; and more preferably from about 5% by volume to about 10% by volume oxygen, from about 20% by volume to about 35% by volume of the halogen gas (i.e., chlorine) and from about 40% by volume to about 60% by volume of the noble gas (i.e., argon) and from about 5 by volume to about 10% by volume of HBr and/or HCl. Thus, the foregoing respective process conditions stated in Tables VI through IX may be based on such etchant gas constituency and on such percent (%) by volume value(s).

In the preferred embodiment of the present invention where the mask layers **18***a*, **18***b*, **18***c* and **18***d* comprise Ti and/or TiN, preferably TiN_1, and the electrode layer **16** is an iridium electrode layer **16**, the process parameters for etching the iridium electrode layer **16** in a suitable inductively coupled plasma reactor fall into ranges as listed on the basis of flow rates of the gases, including oxygen, the halogen gas(es), (i.e., Cl_2), and the noble gas(es) (i.e., argon), as listed in Table X below.

TABLE X

Process	Broad	Preferred	Optimum
Gas Flow, sccm			
O_2	10 to 60	10 to 40	15 to 30
Cl_2	30 to 100	30 to 70	50 to 70
Ar	50 to 250	100 to 200	100 to 150
Pressure, mT	0.1 to 300	10 to 100	10 to 40
RF Power of Coil Inductor (Watts)	100 to 5000	650 to 2000	750 to 1000
RF Power of Wafer Pedestal (Watts)	50 to 3000	100 to 1000	150 to 600
Temperature of Wafer (° C.)	about 150 to about 500	200 to 400	250 to 350
Iridium (Ir) Etch Rate (Å/min)	200 to 6000	500 to 3000	500 to 2000
Selectively of Ir to Ti or TiN of Mask Layers	0.2 to 50	1 to 20	6 to 10
RF Frequency of Coil Inductor	100K to 300 MHz	400K to 20 MHz	2 to 13.5 MHz
RF Frequency of Wafer Pedestal	100K to 300 MHz	400K to 20 MHz	400K to 13.5 MHz

When the etchant gases are a mixture of oxygen, the halogen gas(es) (i.e., chlorine), the noble gas(es) (i.e., argon), and HBr and/or HCl, the process parameters for etching iridium electrode layer **16** supporting a Ti/TiN mask layer **18** in a suitable inductively coupled plasma reactor fall into the ranges as listed on the basis of rates of the gases, including oxygen, the halogen gas(es) (i.e., Cl_2), the noble gas(ses) (i.e., Ar), and HBr and/or HCl, as listed in Table XI below:

TABLE XI

Process	Broad	Preferred	Optimum
Gas Flow, sccm			
O_2	10 to 60	10 to 40	15 to 30
Cl_2	30 to 100	30 to 70	50 to 70
Ar	50 to 250	100 to 200	100 to 150
HBr and/or HCl	10 to 60	10 to 40	15 to 30
Pressure, mT	0.1 to 300	10 to 100	10 to 40
RF Power of Coil Inductor (Watts)	100 to 5000	650 to 2000	750 to 1000
RF Power of Wafer Pedestal (Watts)	50 to 3000	100 to 1000	150 to 600
Temperature of Wafer (° C.)	about 150 to about 500	200 to 400	250 to 350
Iridium Etch Rate (Å/min)	200 to 6000	500 to 3000	500 to 2000
Selectivity of Ir to Ti or TiN of Mask Layers	0.2 to 50	1 to 20	6 to 10
RF Frequency of Coil Inductor	100K to 300 MHz	400K to 20 MHz	2 to 13.5 MHz
RF Frequency of Wafer Pedestal	100K to 300 MHz	400K to 20 MHz	400K to 13.5 MHz

For the embodiment of the invention illustrated in FIGS. **2**, **6**, **8** and **10**, the protective layers **22***a*, **22***b*, **22***c* and **22***d* protect the corners **16***g* of the etched electrode layers **16***a*, **16***b*, **16***c* and **16***d* during the etching process. Typically and as best shown in FIGS. **11** and **12**, some of the mask layers **18***a*, **18***b*, **18***c* and **18***d* would be etched during the etching process, leaving residual mask layers **18***r* on top of etched electrode layers **16***a*, **16***b*, **16***c* and **16***d*, or on top of the protective layers **22***a*, **22***b*, **22***c* and **22***d*. The protective layers **22***a*, **22***b*, **22***c* and **22**, respectively, insure that the corners **16***g* of the etched electrode layers **16***a*, **16***b*, **16***c* and **16***d* are protected during etching, especially in the event that the etching process removes essentially all of the mask layers **18***a*, **18***b*, **18***c* and **18***d*. Maintaining the corners **16***g* of the etched electrode layers **16***a*, **16***b*, **16***c* and **16***d* protects the quality of the profile formed during etching of the electrode layer **16** to produce the etched electrode layers **16***a*, **16***b*, **16***c* and **16***d*.

After the electrode layer **16** has been etched to produce the electrode layers **16***a*, **16***b*, **16***c* and **16***d*, the residual mask layers **18***r* (if not completely removed during the etching process) typically remain on top of the veil-less etched electrode layers **16***a*, **16***b*, **16***c* and **16***d*, or on top of the protective layers **22***a*, **22***b*, **22***c* and **22***d* which are respectively supported by the essentially veil-less etched electrode layers **16***a*, **16***b*, **16***c* and **16***d*, all as best shown in FIGS. **11** and **12**. The residual mask layers **18***r* are to be removed by any suitable means and/or in any suitable manner, such is by CHF_3/Ar plasma. If the residual masks layers **18***r* comprise Ti and/or TiN, the residual mask layers **18***r* may be removed by any suitable means and/or in any suitable manner, such as by the conditions given in Table IV above. Likewise for the embodiment of the invention depicted in FIG. **12**, the protective layers **22***a*, **22***b*, **22***c* and **22***d* are to be removed after removal of the residual mask layers **18***r* from the protective layers **22***a*, **22***b*, **22***c* and **22***d*. The protective layers **22***a*, **22***b*, **22***c* and **22***d* may be removed by any suitable means and/or in any suitable manner. For example, when the protective layers **22***a*, **22***b*, **22***c* and **22***d* comprise TiN removal is by Ar/Cl_2 plasma in a DPS™ brand chamber of the Metal Etch DPS Centura™ brand plasma processing apparatus under the following apparatus and process conditions as listed in Table XII below.

TABLE XII

Process	Broad	Preferred	Optimum
Gas Flow, sccm			
Cl_2	20 to 150	30 to 120	40 to 100
Ar	20 to 100	30 to 80	40 to 60
Pressure, mT	0.5 to 40	4 to 30	7 to 14

TABLE XII-continued

Process	Broad	Preferred	Optimum
RF Power of Coil Inductor (Watts)	500 to 3000	500 to 2000	800 to 1200
RF Power of Wafer Pedestal (Watts)	50 to 500	50 to 300	50 to 150
Temperature of Wafer	20 to 500	20 to 150	80 to 130
TiN Etch Rate (Å/min)	500 to 5000	1000 to 3500	1500 to 2500
RF Frequency of Coil Inductor	100K to 300 MHz	400K to 20 MHz	2 to 13.5 MHz
RF Frequency of Wafer Inductor	100K to 300 MHz	400K to 20 MHz	400K to 13.5 MHz

After removal of residual mask layers **18***r*, or the residual mask layers **18***r* and the protective layers **22***a*, **22***b*, **22***c* and **22***d* for the embodiment of the invention illustrated in FIG. **12**, the veil-less etched electrode layered structure of FIG. **13** or FIG. **14** remains. It should be noted, as best shown in FIGS. **15** and **16**, respectively, that the barrier layer **14** could be etched simultaneously during or after removal of the residual mask layers **18***r* (see FIG. **15**), or etched simultaneously during or after removal of the residual mask layers **18***r* and the protective layers **22***a*, **22***b*, **22***c* and **22***d* (see FIG. **16**).

It is to be understood that the patterned resist **20** (i.e., resist members **20***a*, **20***b*, **20***c* and **20***d*) for the embodiment of the invention depicted in FIG. **1**, or the patterned resist **20** (i.e., resist numbers **20***a*, **20***b*, **20***c* and **20***d*) and/or the mask layers **18***a*, **18***b*, **18***c* and **18***d* for the embodiment of the invention depicted in FIG. **2**, may be removed at any suitable time, preferably before the etching of the electrode layer **16**. Similarly, the protective layers **22***a*, **22***b*, **22***c* and **22***d* and/or mask layers **18***a*, **18***b*, **18***c* and **18***d* for the embodiment of the invention depicted in FIG. **2**, may also be removed at any suitable time, such as during the etching process or after the etching process.

The invention will be illustrated by the following set forth example which is being given to set forth the presently known best mode and by way of illustration only and not by way of any limitation. All parameters such as concentrations, mixing proportions, temperatures, pressure, rates, compounds, etc., submitted in this example are not to be construed to unduly limit the scope of the invention.

EXAMPLE I

A test semiconductor wafer was formulated with the following film stack:

0.8 μm patterned PR (photoresist)/5000 Å Oxide/100 Å Ti/1000 Å Pt/300 Å TiN.

The feature size of the patterned PR test semiconductor wafer was 0.3 μm block and 0.25 μm spacing. The oxide mask (i.e. the mask layer) was opened in the oxide etch chamber of a plasma processing apparatus sold under the trademark Oxide Etch MxP Centura™, owned by Applied Materials Inc., 3050 Bowers Avenue, Santa Clara, Calif. 95054-3299. The etchant gas for opening the oxide mask comprised about 68% by volume Ar and about 32% by volume CHF_3. The reactor and process conditions were as follows:

Reactor Conditions	
Pressure	60 mTorr
RF Power	850 watts
Rotational Magnetic Field	40 Gauss

-continued

Reactor Conditions	
Temperature of Test Wafer	100° C.
Oxide Mask Etch Rate	3000 Å/min

Process Conditions Based on the Flow Rate of Ar and CHF_3	
CHF_3	50 sccm
Ar	100 sccm
Pressure, mTorr	60 mTorr
RF Power Density	850 watts
Temperature (° C.) of Test Wafer	100° C.
Oxide Mask Etch Rate (Å/min)	3000 Å/min
Magnetic Field (Gauss)	40 Gauss

The photoresist was stripped from the oxide mask in an ASP chamber of the Metal Etch MxP Centura™ brand plasma processing apparatus under the following recipe using microwave downstream O_2/N_2 plasma: 120 seconds, 250° C., 1400 W, 3000 sccm O_2, 300 sccm N_2, and 2 Torr.

The Ti protective layer was etched with Ar, Cl_2 and BCl_3 as the etchant gases and in a DPS™ brand chamber of the Metal Etch DPS Centura™ brand plasma processing apparatus under the following reactor and process conditions:

Reactor Conditions	
Pressure	12 mTorr
RF Power to Coil Inductor	900 watts
RF Power to Wafer Pedestal	100 watts
Temperature of Test Wafer	110° C.
Ti Etch Rate	2000 Å/min

Process Conditions Based on the Flow Rate of Ar and Cl_2 and BCl_3	
Ar	40 sccm
Cl_2	30 sccm
BCl_3	30 sccm
Pressure	12 mTorr
RF Power to Coil Inductor	900 watts
RF Power to Wafer Pedestal	100 watts
Temperature of Test Wafer	110° C.
Ti Etch Rate	2000 Å/min

The platinum layer of the test semiconductor wafer was then etched with Ar and Cl_2 as the etchant gas and in a DPS™ brand chamber of the Metal Etch DPS Centura™ brand plasma processing apparatus under the following reactor and process conditions:

Reactor Conditions	
Pressure	12 mTorr
RF Power to Coil Inductor	900 watts
RF Power to Wafer Pedestal	150 watts
Temperature of Test Wafer	260° C.
Platinum Etch Rate	1500 Å/min

Process Conditions Based on the Flow Rate of Ar and Cl_2	
Ar	40 sccm
Cl_2	60 sccm
Pressure, mTorr	12 mTorr
RF Power to Coil Inductor	900 watts
RF Power to Wafer Pedestal	150 watts
Temperature (° C.) of Test Wafer	260° C.
Pt Etch Rate (Å/min)	1500 Å/min
Selectivity of Pt/Oxide Mask	1:1

The resulting etched platinum layer of the test semiconductor wafer is shown in FIG. **19** wherein a platinum profile of about 87 degrees is shown.

The oxide mask was then removed in a 6:1 HF solution to produce the veil-less test semiconductor wafer shown in FIG. **20**. The remaining Ti protective layer could be removed by any suitable means and/or in any suitable manner, such as by etching with Ar, BCl_3 and Cl_2 as the etchant gases and in a DPS™ brand chamber of the Metal Etch DPS Centura™ brand plasma processing apparatus under the following reactor and process conditions:

Reactor Conditions	
Pressure	12 mTorr
RF Power to Coil Inductor	900 watts
RF Power to Wafer Pedestal	100 watts
Temperature of Test Wafer	110° C.
Ti Etch Rate	2000 Å/min

Process Conditions Based on the Flow Rate of Ar Cl_2 and BCl_3	
Ar	40 sccm
Cl_2	30 sccm
BCl_3	30 sccm
Pressure	12 mTorr
RF Power to Coil Inductor	900 watts
RF Power to Wafer Pedestal	100 watts
Temperature of Test Wafer	110° C.
Ti Etch Rate	2000 Å/min

EXAMPLE II

A test semiconductor wafer was formulated with the following film stack:

0.8 μm patterned PR (photoresist)/5000 Å Oxide/600 Å TiN/2000 Å Pt/300 Å TiN

The feature size of the patterned PR test semiconductor wafer was 0.25 μm block and 0.2 μm spacing. The oxide mask (i.e. the mask layer) was opened in the oxide etch chamber of a plasma processing apparatus sold under the trademark Oxide Etch MxP Centura™, owned by Applied Materials Inc., 3050 Bowers Avenue, Santa Clara, Calif. 95054-3299. The etchant gas for opening the oxide mask comprised about 68% by volume Ar and about 32% by volume CHF_3. The reactor and process conditions were as follows:

Reactor Conditions	
Pressure	60 mTorr
RF Power	850 watts
Rotational Magnetic Field	40 Gauss
Temperature of Test Wafer	100° C.
Oxide Mask Etch Rate	3000 Å/min

Process Conditions Based on the Flow Rate of Ar and CHF_3	
CHF_3	50 sccm
Ar	100 sccm
Pressure, mTorr	60 mTorr
RF Power Density	850 watts
Temperature (° C.) of Test Wafer	100° C.
Oxide Mask Etch Rate (Å/min)	3000 Å/min
Magnetic Field (Gauss)	40 Gauss

The photoresist was stripped from the oxide mask in an ASP chamber of the Metal Etch MxP Centura™ brand plasma processing apparatus under the following recipe using microwave downstream O_2/N_2 plasma: 120 seconds, 250° C., 1400 W, 3000 sccm O_2, 300 sccm N_2, and 2 Torr.

The TiN protective layer was etched with Ar, Cl_2 and BCl_3 as the etchant gases and in a DPS™ brand chamber of the Metal Etch DPS Centura™ brand plasma processing apparatus under the following reactor and process conditions:

Reactor Conditions	
Pressure	12 mTorr
RF Power to Coil Inductor	900 watts
RF Power to Wafer Pedestal	100 watts
Temperature of Test Wafer	110° C.
TiN Etch Rate	2000 Å/min

Process Conditions Based on the Flow Rate of Ar and Cl_2 and BCl_3	
Ar	40 sccm
Cl_2	30 sccm
BCl_3	30 sccm
Pressure	12 mTorr
RF Power to Coil Inductor	900 watts
RF Power to Wafer Pedestal	100 watts
Temperature of Test Wafer	110° C.
TiN Etch Rate	2000 Å/min

The platinum layer of the test semiconductor wafer was then etched with Ar and Cl_2 and BCl_3 as the etchant gas and in a DPS™ brand chamber of the Metal Etch DPS Centura™ brand plasma processing apparatus under the following reactor and process conditions:

Reactor Conditions	
Pressure	12 mTorr
RF Power to Coil Inductor	900 watts
RF Power to Wafer Pedestal	150 watts

-continued

Reactor Conditions	
Temperature of Test Wafer	260° C.
Platinum Etch Rate	1500 Å/min

Process Conditions Based on the Flow Rate of Ar and Cl_2 and BCl_3	
Ar	40 sccm
Cl_2	60 sccm
BCl_3	10 sccm
Pressure, mTorr	12 mTorr
RF Power to Coil Inductor	900 watts
RF Power to Wafer Pedestal	150 watts
Temperature (° C.) of Test Wafer	260° C.
Pt Etch Rate (Å/min)	1500 Å/min
Selectivity of Pt/Oxide Mask	1:1

The resulting etched platinum layer of the test semiconductor wafer is shown in FIG. **23** wherein a platinum profile of about 87 degrees is shown. FIG. **24** is a drawing representing the elevational view in the picture of FIG. **23** with the respective parts identified by a reference numeral.

The oxide mask could have been removed in a 6:1 HF solution to produce a veil-less test semiconductor wafer similar to the one shown in FIG. **20**. The remaining TiN protective layer could have been removed by any suitable means and/or in any suitable manner, such as by etching with Ar, BCl_3 and Cl_2 as the etchant gases and in a DPS™ brand chamber of the Metal Etch DPS Centura™ brand plasma processing apparatus under the following reactor and process conditions:

Reactor Conditions	
Pressure	12 mTorr
RF Power to Coil Inductor	900 watts
RF Power to Wafer Pedestal	100 watts
Temperature of Test Wafer	110° C.
TiN Etch Rate	2000 Å/min

Process Conditions Based on the Flow Rate of Ar and Cl_2 and BCl_3	
Ar	40 sccm
Cl_2	30 sccm
BCl_3	30 sccm
Pressure	12 mTorr
RF Power to Coil Inductor	900 watts
RF Power to Wafer Pedestal	100 watts
Temperature of Test Wafer	110° C.
TiN Etch Rate	2000 Å/min

EXAMPLE III

A test semiconductor wafer was formulated with the following film stack:

1.2 μm patterned PR (photoresist)/4000 Å Oxide/100Å Ti/2000 Å Ir/1000 Å TiN

The feature size of the patterned PR test semiconductor wafer was 2.5 μm block and 4.0 μm spacing. The oxide mask (i.e. the mask layer) was opened in the oxide etch chamber of a plasma processing apparatus sold under the trademark Oxide Etch MxP Centura™, owned by Applied Materials Inc., 3050 Bowers Avenue, Santa Clara, Calif. 95054-3299. The etchant gas for opening the oxide mask comprised about 68% by volume Ar and about 32% by volume CHF_3. The reactor and process conditions were as follows:

Reactor Conditions	
Pressure	60 mTorr
RF Power	850 watts
Rotational Magnetic Field	40 Gauss
Temperature of Test Wafer	100° C.
Oxide Mask Etch Rate	3000 Å/min

Process Conditions Based on the Flow Rate of Ar and CHF_3	
CHF_3	50 sccm
Ar	100 sccm
Pressure, mTorr	60 mTorr
RF Power Density	850 watts
Temperature (° C.) of Test Wafer	100° C.
Oxide Mask Etch Rate (Å/min)	3000 Å/min
Magnetic Field (Gauss)	40 Gauss

The photoresist was stripped from the oxide mask in an ASP chamber of the Metal Etch MxP Centura™ brand plasma processing apparatus under the following recipe using microwave downstream O_2/N_2 plasma: 120 seconds, 250° C., 1400 W, 3000 sccm O_2, 300 sccm N_2, and 2 Torr.

The Ti protective layer was etched with Ar, Cl_2 and BCl_3 as the etchant gases and in a DPS™ brand chamber of the Metal Etch DPS Centura™ brand plasma processing apparatus under the following reactor and process conditions:

Reactor Conditions	
Pressure	12 mTorr
RF Power to Coil Inductor	900 watts
RF Power to Wafer Pedestal	100 watts
Temperature of Test Wafer	110° C.
Ti Etch Rate	2000 Å/min

Process Conditions Based on the Flow Rate of Ar and Cl_2 and BCl_3	
Ar	40 sccm
Cl_2	30 sccm
BCl_3	30 sccm
Pressure	12 mTorr
RF Power to Coil Inductor	900 watts
RF Power to Wafer Pedestal	100 watts
Temperature of Test Wafer	110° C.
Ti Etch Rate	2000 Å/min

The iridium layer of the test semiconductor wafer was then etched with O_2, Ar and Cl_2 as the etchant gas and in a DPS™ brand chamber of the Metal Etch DPS Centura™ brand plasma processing apparatus under the following reactor and process conditions:

Reactor Conditions	
Pressure	12 mTorr
RF Power to Coil Inductor	900 watts
RF Power to Wafer Pedestal	450 watts
Temperature of Test Wafer	300° C.
Iridium (Ir) Etch Rate	600 Å/min

Process Conditions Based on the Flow Rate of O_2, Ar and Cl_2	
O_2	15 sccm
Ar	100 sccm
Cl_2	50 sccm
Pressure, mTorr	12 mTorr
RF Power to Coil Inductor	900 watts
RF Power to Wafer Pedestal	450 watts
Temperature (° C.) of Test Wafer	300° C.
Ir Etch Rate (Å/min)	600 Å/min
Selectivity of Ir/Oxide Mask	2:1

The resulting etched iridium layer of the test semiconductor wafer is shown in the picture of FIG. **25** wherein an iridium profile of about 85 degrees is shown. FIG. **26** is a drawing representing the elevational view in the picture of FIG. **25** with the respective parts identified by a reference numeral.

The oxide mask was then removed in a 6:1 HF solution to produce the veil-less test semiconductor wafer. The remaining Ti protective layer could be removed by any suitable means and/or in any suitable manner, such as by etching with Ar, BCl_3 and Cl_2 as the etchant gases and in a DPS™ brand chamber of the Metal Etch DPS Centura™ brand plasma processing apparatus under the following reactor and process conditions:

Reactor Conditions	
Pressure	12 mTorr
RF Power to Coil Inductor	900 watts
RF Power to Wafer Pedestal	100 watts
Temperature of Test Wafer	110° C.
Ti Etch Rate	2000 Å/min

Process Conditions Based on the Flow Rate of Ar, Cl_2, BCl_3	
Ar	40 sccm
Cl_2	30 sccm
BCl_3	30 sccm
Pressure	12 mTorr
RF Power to Coil Inductor	900 watts
RF Power to Wafer Pedestal	100 watts
Temperature of Test Wafer	110° C.
Ti Etch Rate	2000 Å/min

EXAMPLE IV

A test semiconductor wafer was formulated with the following film stack:

1.2 μm patterned PR (photoresist)/1000 Å TiN/2000 Å Ir/1000 Å TiN

The feature size of the patterned PR test semiconductor wafer was 2.5 μm block and 4.0 μm spacing. The TiN mask (i.e. the mask layer) was opened in the metal etch chamber of a plasma processing apparatus sold under the trademark Metal Etch DPS Centura™, owned by Applied Materials Inc., 3050 Bowers Avenue, Santa Clara, Calif. 95054-3299. The etchant gas for opening the TiN mask comprised about 68% by volume Ar and about 32% by volume Cl_2. The reactor and process conditions were as follows:

Reactor Conditions	
Pressure	12 mTorr
RF Power to Coil Inductor	1200 watts
RF Power to Wafer Pedestal	100 watts
Temperature of Test Wafer	110° C.
TiN Etch Rate	2000 Å/min

Process Conditions Based on the Flow Rate of Ar and Cl_2	
Ar	100 sccm
Cl_2	50 sccm
Pressure	12 mTorr
RF Power to Coil Inductor	1200 watts
RF Power to Wafer Pedestal	100 watts
Temperature of Test Wafer	110° C.
TiN Etch Rate	2000 Å/min

The photoresist was stripped from the oxide mask in an ASP chamber of the Metal Etch MxP Centura™ brand plasma processing apparatus under the following recipe using microwave downstream O_2/N_2 plasma: 120 seconds, 250° C., 1400 W, 3000 sccm O_2, 300 sccm N_2, and 2 Torr.

The iridium layer of the test semiconductor wafer was then etched with O_2 Ar and Cl_2 as the etchant gas and in a DPS™ brand chamber of the Metal Etch DPS Centura™ brand plasma processing apparatus under the following reactor and process conditions:

Reactor Conditions	
Pressure	12 mTorr
RF Power to Coil Inductor	900 watts
RF Power to Wafer Pedestal	450 watts
Temperature of Test Wafer	320° C.
Iridium Etch Rate	600 Å/min

Process Conditions Based on the Flow Rate of O_2 and Ar and Cl_2	
O_2	15 sccm
Ar	100 sccm
Cl_2	50 sccm
Pressure, mTorr	12 mTorr
RF Power to Coil Inductor	900 watts
RF Power to Wafer Pedestal	150 watts
Temperature (° C.) of Test Wafer	320° C.
Iridium Etch Rate (Å/min)	1500 Å/min
Selectivity of Ir/TiN Mask	10:1

The resulting etched iridium layer of the test semiconductor wafer is shown in FIG. **27** wherein an iridium profile of about 80 degrees is shown. FIG. **28** is a drawing representing the elevational view in the picture of FIG. **27** with the respective parts identified by a reference numeral.

The remaining TiN mask layer could have been removed by any suitable means and/or in any suitable manner, such

as by etching with Ar and Cl_2 as the etchant gases and in a DPS™ brand chamber of the Metal Etch DPS Centura™ brand plasma processing apparatus under the following reactor and process conditions:

Reactor Conditions	
Pressure	12 mTorr
RF Power to Coil Inductor	1200 watts
RF Power to Wafer Pedestal	100 watts
Temperature of Test Wafer	110° C.
TiN Etch Rate	2000 Å/min

Process Conditions Based on the Flow Rate of Ar and Cl_2	
Ar	100 sccm
Cl_2	50 sccm
Pressure	12 mTorr
RF Power to Coil Inductor	1200 watts
RF Power to Wafer Pedestal	100 watts
Temperature of Test Wafer	110° C.
TiN Etch Rate	2000 Å/min

CONCLUSION

Thus, by the practice of the present invention there is provided a method for etching of the electrode layer **16**. The etched electrode layer **16** includes a plurality of etched electrode layers **16***a*, **16***b*, **16***c* and **16***d* having a profile where the angle α of the sidewalls **16***s* with respect to a horizontal plane is equal to or greater than about 80 degrees. The electrode layers **16***a*, **16***b*, **16***c* and **16***d* are separated by a distance or space having a dimension equal to or less than about 0.3 μm. Each of the electrode layers **16***a*, **16***b*, **16***c* and **16***d* include a dimension having a value equal to or less than about 0.6 μm, preferably equal to or less than about 0.3 μm. More preferably, each of the electrode layers **16***a*, **16***b*, **16***c* and **16***d* has a width equal to or less than about 0.3 μm, a length equal to or less than about 0.6 μm, and a height equal to or less than about 0.6 μm. Because the produced etched electrode layers **16***a*, **16***b*, **16***c* and **16***d* are essentially a "veil-less" with no "fences" or "rabbit ears," they are ideally suited for receiving a dielectric (e.g., a BST layer) in producing a semiconductor device. The etchant gas in Example I consisted of about 40% by vol. Ar and about 60% by vol. Cl_2, and produced an etched platinum layer with a platinum profile of about 87 degrees. In Example II, the etchant gas consisted of 54.5% by vol. (about 55% by vol.) Cl_2, 36.4% by vol. (about 36% by vol.) Ar, and 9.1% by vol. (about 9% by vol.) BCl_3, and the resulting etched platinum layer had a platinum profile of about 87 degrees. In Example III, the etchant gas consisted of about 9.1% by vol. O_2, about 60.6% by vol. argon, and about 30.3% by vol. Cl_2, and produced an etched iridium layer with an iridium profile of about 85 degrees. In Example IV, the etchant gas consisted of about 9.1% by vol. O_2, about 60.6% by vol. argon, and about 30.3% by vol. Cl_2, and produced an etched iridium layer with an iridium profile of about 80 degrees.

Thus, while the present invention has been described herein with reference to particular embodiments thereof, a latitude of modification, various changes and substitutions are intended in the foregoing disclosure, and it will be appreciated that in some instances some features of the invention will be employed without a corresponding use of other features without departing from the scope and spirit of the invention as set forth. Therefore, many modifications may be made to adapt a particular situation or material to the teachings of the invention without departing from the essential scope and spirit of the present invention. It is intended that the invention not be limited to the particular embodiment(s) disclosed as the best mode contemplated for carrying out this invention, but that the invention will include all embodiments and equivalents falling within the scope of the appended claims.

What is claimed is:

1. A method of etching an iridium layer disposed on a substrate comprising the steps of:

a) providing a substrate supporting an iridium layer;

b) heating said substrate of step (a) to a temperature greater than about 150° C.; and

c) etching said iridium layer including employing a high density plasma of an etchant gas comprising a halogen containing gas and a noble gas to produce said substrate supporting at least one etched iridium layer.

2. The method of claim **1** wherein said etchant gas additionally comprises a gas selected from the group consisting of O_2 and BCl_3.

3. The method of claim **1** wherein said etchant gas additionally comprises a gas selected from the group consisting of O_2, HCl, HBr, and mixtures thereof.

4. The method of claim **1** wherein said etched iridium layer includes an iridium profile equal to or greater than about 80°.

5. The method of claim **1** wherein said halogen containing gas consists essentially of chlorine and said noble gas consists essentially of argon.

6. The method of claim **5** wherein said etchant gas consists essentially of chlorine, argon and O_2.

7. The method of claim **1** wherein said iridium layer of step (a) additionally comprises a mask layer disposed on a selected part of said iridium layer to selectively protect said iridium layer during said etching step (c).

8. The method of claim **1** wherein said iridium layer of step (a) additionally comprises a TiN mask layer disposed on a selected part of said iridium layer to selectively protect said iridium layer during said etching step (c).

9. The method of claim **1** wherein said iridium layer of step (a) additionally comprises a Ti mask layer disposed on a selected part of said iridium layer to selectively protect said iridium layer during said etching step (c).

10. The method of claim **7** wherein said iridium layer of step (a) additionally comprises a protective layer disposed on said selected part of said iridium layer between said mask layer and said iridium layer.

11. The method of claim **8** wherein said iridium layer of step (a) additionally comprises a protective layer disposed on said selected part of said iridium layer between said TiN mask layer and said iridium layer.

12. The method of claim **9** wherein said iridium layer of step (a) additionally comprises a protective layer disposed on said selected part of said iridium layer between said Ti mask layer and said iridium layer.

13. The method of claim **7** additionally comprising removing said mask layer after said etching step (c).

14. The method of claim **1** wherein said high density plasma includes a high density inductively coupled plasma.

15. The method of claim **14** additionally comprising disposing said substrate including said iridium layer of step (a) in a high density plasma chamber including a coil inductor and a wafer pedestal; and performing said etching step (c) in said high density plasma chamber under the following process conditions:

Process	Parameters
Etchant Gas flow	50 to 500 sccm
Pressure, mTorr	0.1 to 300 milliTorr
RF Power (watts) of Coil Inductor	100 to 5000 watts
RF Power (watts) of Wafer Pedestal	50 to 3000 watts
Iridium Etch Rate (Å/min)	200 to 6000 Å/min
RF Frequency of Coil Inductor	100K to 300 MHz
RF Frequency of Wafer Pedestal.	100K to 300 MHz

16. The method of claim **8** wherein said high density plasma includes a high density inductively coupled plasma, and said etchant gas additionally comprises O_2.

17. The method of claim **16** additionally comprising disposing said substrate including said iridium layer of step (a) in a high density plasma chamber including a coil inductor and a wafer pedestal; and performing said etching step (c) in said high density plasma chamber under the following process conditions:

Process	Parameters
O_2	5% to 40% by vol.
Cl_2	10% to 60% by vol.
Ar	30% to 80% by vol.
Pressure, mTorr	0.1 to 300 milliTorr
RF Power (watts) of Coil Inductor	100 to 5000 watts
RF Power (watts) of Wafer Pedestal	50 to 3000 watts
Iridium Etch Rate (Å/min)	200 to 6000 Å/min
Selectivity of Ir to TiN	.2 to 50
RF Frequency of Coil Inductor	100K to 300 MHz
RF Frequency of Wafer Pedestal.	100K to 300 MHz

18. A method for producing a capacitance structure including an iridium electrode comprising the steps of:

a) providing a substrate supporting an iridium electrode layer and at least one mask layer disposed on a selected part of said iridium electrode layer;

b) heating said substrate of step (a) to a temperature greater than about 150° C.; and

c) etching said iridium electrode layer including employing a plasma of an etchant gas comprising a halogen containing gas and a noble gas to produce a capacitance structure having at least one iridium electrode.

19. A capacitance structure produced in accordance with the method of claim **18**.

20. A method of manufacturing a semiconductor device comprising the steps of:

a) forming a patterned resist layer, a TiN mask layer and an iridium electrode layer on a substrate having circuit elements formed thereon;

b) etching a portion of said TiN mask layer including employing a plasma of an etchant gas to break through and to remove said portion of said TiN mask layer from said iridium electrode layer to produce said substrate supporting said patterned resist layer, a residual TiN mask layer, and said iridium electrode layer;

c) removing said patterned resist layer of step (b) to produce said substrate supporting said residual TiN mask layer and said iridium electrode layer;

d) heating said substrate of step (c) to a temperature greater than about 150° C.; and

e) etching said iridium electrode layer of step (d) including employing a high density plasma of an etchant gas comprising a halogen containing gas and a noble gas to produce a semiconductor device having at least one iridium electrode.

21. The method of claim **20** additionally comprising removing said residual TiN mask layer after said etching step (e).

22. The method of claim **20** wherein said etchant gas of said high density plasma of step (e) consists essentially of oxygen, chlorine and argon.

23. A method of etching an iridium electrode layer disposed on a substrate comprising the steps of:

a) providing a substrate supporting an iridium electrode layer, a protective layer on said iridium electrode layer, a Ti mask layer on said protective layer, and a patterned resist layer on said mask layer;

b) etching a portion of said Ti mask layer including employing a plasma of an etchant gas to break through and to remove said portion of said Ti mask layer from said iridium electrode layer to expose part of said protective layer and to produce said substrate supporting said iridium electrode layer, said protective layer on said iridium electrode layer, a residual Ti mask layer on said protective layer, and said patterned resist layer on said residual Ti mask layer;

c) removing said patterned resist layer from said residual Ti mask layer of step (b) to produce said substrate supporting said iridium electrode layer, said protective layer on said iridium electrode layer, and said residual mask layer on said protective layer;

d) heating said substrate of step (c) to a temperature greater than about 150° C.;

e) etching said exposed part of said protective layer to expose part of said iridium electrode layer and to produce said substrate supporting said iridium electrode layer, a residual protective layer on said iridium electrode layer, and said residual mask layer on said residual protective layer; and

f) etching said exposed part of said iridium electrode layer of step (e) including employing a high density plasma of an etchant gas comprising a halogen containing gas and a noble gas to produce said substrate supporting an etched iridium electrode layer having said residual protective layer on said etched iridium electrode layer, and said residual Ti mask layer on said residual protective layer.

24. A method of etching an iridium electrode layer disposed on a substrate comprising the steps of:

a) providing a substrate supporting an iridium electrode layer, a protective layer on said iridium electrode layer, a mask layer on said protective layer, and a patterned resist layer on said mask layer;

b) etching a portion of said mask layer including employing a plasma of an etchant gas to break through and to remove said portion of said mask layer from said iridium electrode layer to expose part of said protective layer and to produce said substrate supporting said iridium electrode layer, said protective layer on said iridium electrode layer, a residual mask layer on said protective layer, and said patterned resist layer on said residual mask layer;

c) etching said exposed part of said protective layer to expose part of said iridium electrode layer and to

produce said substrate supporting said iridium electrode layer, a residual protective layer on said iridium electrode layer, said residual mask layer on said residual protective layer, and said patterned resist layer on said residual mask layer;

d) removing said patterned resist layer from said residual mask layer of step (c) to produce said substrate supporting said iridium electrode layer, said residual protective layer on said iridium electrode layer, and said residual mask layer on said residual protective layer;

e) heating said substrate of step (d) to a temperature greater than about 150° C.; and

f) etching said exposed part of said iridium electrode layer of step (d) including employing a high density plasma of an etchant gas comprising chlorine and a noble gas to produce said substrate supporting an etched iridium electrode layer having said residual protective layer on said etched iridium electrode layer, and said residual mask layer on said residual protective layer.

25. The method of claim **24** wherein said etchant gas of step (f) additionally comprises a gas selected from the group consisting of oxygen, HCl, HBr and mixtures thereof.

26. The method of claim **1** wherein said halogen containing gas is a halogen gas and said etchant gas comprises from about 20% by volume to about 95% by volume of the halogen gas and from about 5% by volume to about 80% by volume of the noble gas.

27. The method of claim **1** wherein said halogen containing gas is a halogen gas and said etchant gas comprises from about 40% by volume to about 80% by volume of the halogen gas and from about 20% by volume to about 60% by volume of the noble gas.

28. The method of claim **1** wherein said halogen containing gas is a halogen gas and said etchant gas comprises from about 55% by volume to about 65% by volume of the halogen gas and from about 35% by volume to about 45% by volume of the noble gas.

29. The method of claim **2** wherein said halogen containing gas is a halogen gas and said etchant gas comprises from about 5% by volume to about 40% by volume oxygen, from about 10% by volume to about 60% by volume of the halogen gas, and from about 30% by volume to about 80% by volume of the noble gas.

30. The method of claim **2** wherein said halogen containing gas is a halogen gas and said etchant gas comprises from about 10% by volume to about 30% by volume oxygen, from about 20% by volume to about 50% by volume of the halogen gas, and from about 40% by volume to about 70% by volume of the noble gas.

31. The method of claim **2** wherein said halogen containing gas is a halogen gas and said etchant gas comprises from about 10% by volume to about 20% by volume oxygen, from about 20% by volume to about 30% by volume of the halogen gas, and from about 50% by volume to about 70% by volume of the noble gas.

32. The method of claim **3** wherein said halogen containing gas is a halogen gas and said etchant gas comprises from about 10% by volume to about 90% by volume of the halogen gas, from about 5% by volume to about 80% by volume of the noble gas, and from about 4% by volume to about 25% by volume of a gas selected from the group consisting of HBr, BCl_3, and mixtures thereof.

33. The method of claim **3** wherein said halogen containing gas is a halogen gas and said etchant gas comprises from about 40% by volume to about 70% by volume of the halogen gas, from about 25% by volume to about 55% by volume of the noble gas, and from about 5% by volume to about 20% by volume of gas selected from the group consisting of HBr, BCl_3, and mixtures thereof.

34. The method of claim **3** wherein said halogen containing gas is a halogen gas and said etchant gas comprises from about 50% by volume to about 60% by volume of the halogen gas, from about 35% by volume to about 45% by volume of the noble gas, and from about 5% by volume to about 15% by volume of gas selected from the group consisting of HBr, BCl_3, and mixtures thereof.

35. The method of claim **3** wherein said halogen containing gas is a halogen gas and said etchant gas comprises from about 5% by volume to about 20% by volume oxygen, from about 10% by volume to about 60% by volume of the halogen gas, from about 30% by volume of about 80% by volume of the noble gas, and from about 5% by volume to about 20% by volume of a gas selected from the group consisting of HBr, HCl, and mixtures thereof.

36. The method of claim **3** wherein said halogen containing gas is a halogen gas and said etchant gas comprises from about 5% by volume to about 15% by volume oxygen, from about 20% by volume to about 50% by volume of the halogen gas, from about 40% by volume of about 70% by volume of the noble gas, and from about 5% by volume to about 15% by volume of a gas selected from the group consisting of HBr, HCl, and mixtures thereof.

37. The method of claim **3** wherein said halogen containing gas is a halogen gas and said etchant gas comprises from about 5% by volume to about 10% by volume oxygen, from about 20% by volume to about 35% by volume of the halogen gas, from about 40% by volume of about 60% by volume of the noble gas, and from about 5% by volume to about 10% by volume of a gas selected from the group consisting of HBr, HCl, and mixtures thereof.

38. The method of claim **1** wherein said temperature of said substrate ranges from about 200° C. to about 400° C.

39. The method of claim **1** wherein said temperature of said substrate ranges from about 250° C. to about 350° C.

40. The method of claim **18** wherein said etchant gas additionally comprises a gas selected from the group consisting of O_2 and BCl_3.

41. The method of claim **18** wherein said etchant gas additionally comprises a gas selected from the group consisting of O_2, HCl, HBr, and mixtures thereof.

42. The method of claim **18** wherein said etched iridium electrode layer includes an iridium profile equal to or greater than about 80°.

43. The method of claim **18** wherein said halogen containing gas consists essentially of chlorine and said noble gas consists essentially of argon.

44. The method of claim **43** wherein said etchant gas consists essentially of chlorine, argon and O_2.

45. The method of claim **18** wherein said mask layer comprises a TiN mask layer disposed on a selected part of said iridium electrode layer to selectively protect said iridium electrode layer during said etching step (c).

46. The method of claim **18** wherein said mask layer comprises a mask layer including Ti and TiN disposed on a selected part of said iridium electrode layer to selectively protect said iridium electrode layer during said etching. step (c).

47. The method of claim **18** wherein said mask layer comprises a Ti mask layer disposed on a selected part of said iridium electrode layer to selectively protect said iridium electrode layer during said etching step (c).

48. The method of claim **45** wherein said iridium electrode layer of step (a) additionally comprises a protective layer disposed on said selected part of said iridium electrode layer between said TiN mask layer and said iridium electrode layer.

49. The method of claim 46 wherein said iridium electrode layer of step (a) additionally comprises a protective layer disposed on said selected part of said iridium electrode layer between said mask layer and said iridium electrode layer.

50. The method of claim 47 wherein said iridium electrode layer of step (a) additionally comprises a protective layer disposed on said selected part of said iridium electrode layer between said Ti mask layer and said iridium electrode layer.

51. The method of claim 45 additionally comprising removing said mask layer after said etching step (c).

52. The method of claim 18 wherein said high density plasma includes a high density inductively coupled plasma.

53. The method of claim 52 additionally comprising disposing said substrate including said iridium electrode layer of step (a) in a high density plasma chamber including a coil inductor and a wafer pedestal; and performing said etching step (c) in said high density plasma chamber under the following process conditions:

Process	Parameters
Etchant Gas flow	50 to 500 sccm
Pressure, mTorr	0.1 to 300 milliTorr
RF Power (watts) of Coil Inductor	100 to 5000 watts
RF Power (watts) of Wafer Pedestal	50 to 3000 watts
Iridium Etch Rate (Å/min)	200 to 6000 Å/min
RF Frequency of Coil Inductor	100K to 300 MHz
RF Frequency of Wafer Pedestal.	100K to 300 MHz

54. The method of claim 45 wherein said high density plasma includes a high density inductively coupled plasma, and said etchant gas additionally comprises O_2.

55. The method of claim 54 additionally comprising disposing said substrate including said iridium electrode layer of step (a) in a high density plasma chamber including a coil inductor and a wafer pedestal; and performing said etching step (c) in said high density plasma chamber under the following process conditions:

Process	Parameters
O_2	5% to 40% by vol.
Cl_2	10% to 60% by vol.
Ar	30% to 80% by vol.
Pressure, mTorr	0.1 to 300 milliTorr
RF Power (watts) of Coil Inductor	100 to 5000 watts
RF Power (watts) of Wafer Pedestal	50 to 3000 watts
Iridium Etch Rate (Å/min)	200 to 6000 Å/min
Selectivity of Ir to TiN	.2 to 50
RF Frequency of Coil Inductor	100K to 300 MHz
RF Frequency of Wafer Pedestal.	100K to 300 MHz

56. The method of claim 18 wherein said halogen containing gas is a halogen gas and said etchant gas comprises from about 20% by volume to about 95% by volume of the halogen gas and from about 5% by volume to about 80% by volume of the noble gas.

57. The method of claim 18 wherein said halogen containing gas is a halogen gas and said etchant gas comprises from about 40% by volume to about 80% by volume of the halogen gas and from about 20% by volume to about 60% by volume of the noble gas.

58. The method of claim 18 wherein said halogen containing gas is a halogen gas and said etchant gas comprises from about 55% by volume to about 65% by volume of the halogen gas and from about 35% by volume to about 45% by volume of the noble gas.

59. The method of claim 40 wherein said halogen containing gas is a halogen gas and said etchant gas comprises from about 5% by volume to about 40% by volume oxygen, from about 10% by volume to about 60% by volume of the halogen gas, and from about 30% by volume to about 80% by volume of the noble gas.

60. The method of claim 40 wherein said halogen containing gas is a halogen gas and said etchant gas comprises from about 10% by volume to about 30% by volume oxygen, from about 20% by volume to about 50% by volume of the halogen gas, and from about 40% by volume to about 70% by volume of the noble gas.

61. The method of claim 40 wherein said halogen containing gas is a halogen gas and said etchant gas comprises from about 10% by volume to about 20% by volume oxygen, from about 20% by volume to about 30% by volume of the halogen gas, and from about 50% by volume to about 70% by volume of the noble gas.

62. The method of claim 41 wherein said halogen containing gas is a halogen gas and said etchant gas comprises from about 10% by volume to about 90% by volume of the halogen gas, from about 5% by volume to about 80% by volume of the noble gas, and from about 4% by volume to about 25% by volume of a gas selected from the group consisting of HBr, BCl_3, and mixtures thereof.

63. The method of claim 41 wherein said halogen containing gas is a halogen gas and said etchant gas comprises from about 40% by volume to about 70% by volume of the halogen gas, from about 25% by volume to about 55% by volume of the noble gas, and from about 5% by volume to about 20% by volume of gas selected from the group consisting of HBr, BCl_3, and mixtures thereof.

64. The method of claim 41 wherein said halogen containing gas is a halogen gas and said etchant gas comprises from about 50% by volume to about 60% by volume of the halogen gas, from about 35% by volume to about 45% by volume of the noble gas, and from about 5% by volume to about 15% by volume of gas selected from the group consisting of HBr, BCl_3, and mixtures thereof.

65. The method of claim 41 wherein said halogen containing gas is a halogen gas and said etchant gas comprises from about 5% by volume to about 20% by volume oxygen, from about 10% by volume to about 60% by volume of the halogen gas, from about 30% by volume of about 80% by volume of the noble gas, and from about 5% by volume to about 20% by volume of a gas selected from the group consisting of HBr, HCl, and mixtures thereof.

66. The method of claim 41 wherein said halogen containing gas is a halogen gas and said etchant gas comprises from about 5% by volume to about 15% by volume oxygen, from about 20% by volume to about 50% by volume of the halogen gas, from about 40% by volume of about 70% by volume of the noble gas, and from about 5% by volume to about 15% by volume of a gas selected from the group consisting of HBr, HCl, and mixtures thereof.

67. The method of claim 41 wherein said halogen containing gas is a halogen gas and said etchant gas comprises from about 5% by volume to about 10% by volume oxygen, from about 20% by volume to about 35% by volume of the

halogen gas, from about 40% by volume of about 60% by volume of the noble gas, and from about 5% by volume to about 10% by volume of a gas selected from the group consisting of HBr, HCl, and mixtures thereof.

68. The method of claim **18** wherein said temperature of said substrate ranges from about 200° C. to about 400° C.

69. The method of claim **18** wherein said temperature of said substrate ranges from about 250° C. to about 350° C.

70. The method of claim **20** wherein said etchant gas additionally comprises a gas selected from the group consisting of O_2 and BCl_3.

71. The method of claim **20** wherein said etchant gas additionally comprises a gas selected from the group consisting of O_2, HCl, HBr, and mixtures thereof.

72. The method of claim **20** wherein said etched iridium electrode layer includes an iridium profile equal to or greater than about 80°.

73. The method of claim **20** wherein said halogen containing gas consists essentially of chlorine and said noble gas consists essentially of argon.

74. The method of claim **73** wherein said etchant gas consists essentially of chlorine, argon and O_2.

75. The method of claim **20** wherein said iridium electrode layer of step (a) additionally comprises a protective layer disposed on said selected part of said iridium electrode layer between said mask layer and said iridium electrode layer.

76. The method of claim **20** additionally comprising removing said TiN mask layer after said etching step (c).

77. The method of claim **20** wherein said high density plasma includes a high density inductively coupled plasma.

78. The method of claim **77** additionally comprising disposing said substrate including said iridium electrode layer of step (a) in a high density plasma chamber including a coil inductor and a wafer pedestal; and performing said etching step (e) in said high density plasma chamber under the following process conditions:

Process	Parameters
Etchant Gas flow	50 to 500 sccm
Pressure, mTorr	0.1 to 300 milliTorr
RF Power (watts) of Coil Inductor	100 to 5000 watts
RF Power (watts) of Wafer Pedestal	50 to 3000 watts
Iridium Etch Rate (Å/min)	200 to 6000 Å/min
RF Frequency of Coil Inductor	100K to 300 MHz
RF Frequency of Wafer Pedestal.	100K to 300 MHz

79. The method of claim **77** wherein said etchant gas additionally comprises O_2.

80. The method of claim **79** additionally comprising disposing said substrate including said iridium electrode layer of step (a) in a high density plasma chamber including a coil inductor and a wafer pedestal; and performing said etching step (e) in said high density plasma chamber under the following process conditions:

Process	Parameters
O_2	5% to 40% by vol.
Cl_2	10% to 60% by vol.
Ar	30% to 80% by vol.
Pressure, mTorr	0.1 to 300 milliTorr
RF Power (watts) of Coil Inductor	100 to 5000 watts
RF Power (watts) of Wafer Pedestal	50 to 3000 watts
Iridium Etch Rate (Å/min)	200 to 6000 Å/min
Selectivity of Ir to TiN	.2 to 50
RF Frequency of Coil Inductor	100K to 300 MHz
RF Frequency of Wafer Pedestal.	100K to 300 MHz

81. The method of claim **20** wherein said halogen containing gas is a halogen gas and said etchant gas comprises from about 20% by volume to about 95% by volume of the halogen gas and from about 5% by volume to about 80% by volume of the noble gas.

82. The method of claim **20** wherein said halogen containing gas is a halogen gas and said etchant gas comprises from about 40% by volume to about 80% by volume of the halogen gas and from about 20% by volume to about 60% by volume of the noble gas.

83. The method of claim **20** wherein said halogen containing gas is a halogen gas and said etchant gas comprises from about 55% by volume to about 65% by volume of the halogen gas and from about 35% by volume to about 45% by volume of the noble gas.

84. The method of claim **70** wherein said halogen containing gas is a halogen gas and said etchant gas comprises from about 5% by volume to about 40% by volume oxygen, from about 10% by volume to about 60% by volume of the halogen gas, and from about 30% by volume to about 80% by volume of the noble gas.

85. The method of claim **70** wherein said halogen containing gas is a halogen gas and said etchant gas comprises from about 10% by volume to about 30% by volume oxygen, from about 20% by volume to about 50% by volume of the halogen gas, and from about 40% by volume to about 70% by volume of the noble gas.

86. The method of claim **70** wherein said halogen containing gas is a halogen gas and said etchant gas comprises from about 10% by volume to about 20% by volume oxygen, from about 20% by volume to about 30% by volume of the halogen gas, and from about 50% by volume to about 70% by volume of the noble gas.

87. The method of claim **71** wherein said halogen containing gas is a halogen gas and said etchant gas comprises from about 10% by volume to about 90% by volume of the halogen gas, from about 5% by volume to about 80% by volume of the noble gas, and from about 4% by volume to about 25% by volume of a gas selected from the group consisting of HBr, BCl_3, and mixtures thereof.

88. The method of claim **71** wherein said halogen containing gas is a halogen gas and said etchant gas comprises from about 40% by volume to about 70% by volume of the halogen gas, from about 25% by volume to about 55% by volume of the noble gas, and from about 5% by volume to about 20% by volume of gas selected from the group consisting of HBr, BCl_3, and mixtures thereof.

89. The method of claim **71** wherein said halogen containing gas is a halogen gas and said etchant gas comprises from about 50% by volume to about 60% by volume of the halogen gas, from about 35% by volume to about 45% by volume of the noble gas, and from about 5% by volume to

about 15% by volume of gas selected from the group consisting of HBr, BCl_3, and mixtures thereof.

90. The method of claim **71** wherein said halogen containing gas is a halogen gas and said etchant gas comprises from about 5% by volume to about 20% by volume oxygen, from about 10% by volume to about 60% by volume of the halogen gas, from about 30% by volume of about 80% by volume of the noble gas, and from about 5% by volume to about 20% by volume of a gas selected from the group consisting of HBr, HCl, and mixtures thereof.

91. The method of claim **71** wherein said halogen containing gas is a halogen gas and said etchant gas comprises from about 5% by volume to about 15% by volume oxygen, from about 20% by volume to about 50% by volume of the halogen gas, from about 40% by volume of about 70% by volume of the noble gas, and from about 5% by volume to about 15% by volume of a gas selected from the group consisting of HBr, HCl, and mixtures thereof.

92. The method of claim **71** wherein said halogen containing gas is a halogen gas and said etchant gas comprises from about 5% by volume to about 10% by volume oxygen, from about 20% by volume to about 35% by volume of the halogen gas, from about 40% by volume of about 60% by volume of the noble gas, and from about 5% by volume to about 10% by volume of a gas selected from the group consisting of HBr, HCl, and mixtures thereof.

93. The method of claim **20** wherein said temperature of said substrate ranges from about 200° C. to about 400° C.

94. The method of claim **20** wherein said temperature of said substrate ranges from about 250° C. to about 350° C.

95. The method of claim **23** wherein said etchant gas additionally comprises a gas selected from the group consisting of O_2 and BCl_3.

96. The method of claim **23** wherein said etchant gas additionally comprises a gas selected from the group consisting of O_2, HCl, HBr, and mixtures thereof.

97. The method of claim **23** wherein said etched iridium electrode layer includes an iridium profile equal to or greater than about 80°.

98. The method of claim **23** wherein said halogen containing gas consists essentially of chlorine and said noble gas consists essentially of argon.

99. The method of claim **98** wherein said etchant gas consists essentially of chlorine, argon and O_2.

100. The method of claim **23** wherein said high density plasma includes a high density inductively coupled plasma.

101. The method of claim **100** additionally comprising disposing said substrate including said iridium electrode layer of step (a) in a high density plasma chamber including a coil inductor and a wafer pedestal; and performing said etching step (f) in said high density plasma chamber under the following process conditions:

Process	Parameters
Etchant Gas flow	50 to 500 sccm
Pressure, mTorr	0.1 to 300 milliTorr
RF Power (watts) of Coil Inductor	100 to 5000 watts
RF Power (watts) of Wafer Pedestal	50 to 3000 watts
Iridium Etch Rate (Å/min)	200 to 6000 Å/min
RF Frequency of Coil Inductor	100K to 300 MHz
RF Frequency of Wafer Pedestal.	100K to 300 MHz

102. The method of claim **23** wherein said high density plasma includes a high density inductively coupled plasma, and said etchant gas additionally comprises O_2.

103. The method of claim **102** additionally comprising disposing said substrate including said iridium electrode layer of step (a) in a high density plasma chamber including a coil inductor and a wafer pedestal; and performing said etching step (f) in said high density plasma chamber under the following process conditions:

Process	Parameters
O_2	5% to 40% by vol.
Cl_2	10% to 60% by vol.
Ar	30% to 80% by vol.
Pressure, mTorr	0.1 to 300 milliTorr
RF Power (watts) of Coil Inductor	100 to 5000 watts
RF Power (watts) of Wafer Pedestal	50 to 3000 watts
Iridium Etch Rate (Å/min)	200 to 6000 Å/min
Selectivity of Ir to Ti	.2 to 50
RF Frequency of Coil Inductor	100K to 300 MHz
RF Frequency of Wafer Pedestal.	100K to 300 MHz

104. The method of claim **23** wherein said halogen containing gas is a halogen gas and said etchant gas comprises from about 20% by volume to about 95% by volume of the halogen gas and from about 5% by volume to about 80% by volume of the noble gas.

105. The method of claim **23** wherein said halogen containing gas is a halogen gas and said etchant gas comprises from about 40% by volume to about 80% by volume of the halogen gas and from about 20% by volume to about 60% by volume of the noble gas.

106. The method of claim **23** wherein said halogen containing gas is a halogen gas and said etchant gas comprises from about 55% by volume to about 65% by volume of the halogen gas and from about 35% by volume to about 45% by volume of the noble gas.

107. The method of claim **95** wherein said halogen containing gas is a halogen gas and said etchant gas comprises from about 5% by volume to about 40% by volume oxygen, from about 10% by volume to about 60% by volume of the halogen gas, and from about 30% by volume to about 80% by volume of the noble gas.

108. The method of claim **95** wherein said halogen containing gas is a halogen gas and said etchant gas comprises from about 10% by volume to about 30% by volume oxygen, from about 20% by volume to about 50% by volume of the halogen gas, and from about 40% by volume to about 70% by volume of the noble gas.

109. The method of claim **95** wherein said halogen containing gas is a halogen gas and said etchant gas comprises from about 10% by volume to about 20% by volume oxygen, from about 20% by volume to about 30% by volume of the halogen gas, and from about 50% by volume to about 70% by volume of the noble gas.

110. The method of claim **96** wherein said halogen containing gas is a halogen gas and said etchant gas comprises from about 10% by volume to about 90% by volume of the halogen gas, from about 5% by volume to about 80% by volume of the noble gas, and from about 4% by volume to about 25% by volume of a gas selected from the group consisting of HBr, BCl_3, and mixtures thereof.

111. The method of claim **96** wherein said halogen containing gas is a halogen gas and said etchant gas com-

prises from about 40% by volume to about 70% by volume of the halogen gas, from about 25% by volume to about 55% by volume of the noble gas, and from about 5% by volume to about 20% by volume of gas selected from the group consisting of HBr, BCl_3, and mixtures thereof.

112. The method of claim **96** wherein said halogen containing gas is a halogen gas and said etchant gas comprises from about 50% by volume to about 60% by volume of the halogen gas, from about 35% by volume to about 45% by volume of the noble gas, and from about 5% by volume to about 15% by volume of gas selected from the group consisting of HBr, BCl_3, and mixtures thereof.

113. The method of claim **96** wherein said halogen containing gas is a halogen gas and said etchant gas comprises from about 5% by volume to about 20% by volume oxygen, from about 10% by volume to about 60% by volume of the halogen gas, from about 30% by volume of about 80% by volume of the noble gas, and from about 5% by volume to about 20% by volume of a gas selected from the group consisting of HBr, HCl, and mixtures thereof.

114. The method of claim **96** wherein said halogen containing gas is a halogen gas and said etchant gas comprises from about 5% by volume to about 15% by volume oxygen, from about 20% by volume to about 50% by volume of the halogen gas, from about 40% by volume of about 70% by volume of the noble gas, and from about 5% by volume to about 15% by volume of a gas selected from the group consisting of HBr, HCl, and mixtures thereof.

115. The method of claim **96** wherein said halogen containing gas is a halogen gas and said etchant gas comprises from about 5% by volume to about 10% by volume oxygen, from about 20% by volume to about 35% by volume of the halogen gas, from about 40% by volume of about 60% by volume of the noble gas, and from about 5% by volume to about 10% by volume of a gas selected from the group consisting of HBr, HCl, and mixtures thereof.

116. The method of claim **23** wherein said temperature of said substrate ranges from about 200° C. to about 400° C.

117. The method of claim **23** wherein said temperature of said substrate ranges from about 250° C. to about 350° C.

118. The method of claim **24** wherein said etchant gas additionally comprises a gas selected from the group consisting of O_2 and BCl_3.

119. The method of claim **24** wherein said etchant gas additionally comprises a gas selected from the group consisting of O_2, HCl, HBr, and mixtures thereof.

120. The method of claim **24** wherein said etched iridium electrode layer includes an iridium profile equal to or greater than about 80°.

121. The method of claim **24** wherein said halogen containing gas consists essentially of chlorine and said noble gas consists essentially of argon.

122. The method of claim **121** wherein said etchant gas consists essentially of chlorine, argon and O_2.

123. The method of claim **24** wherein said high density plasma includes a high density inductively coupled plasma.

124. The method of claim **123** additionally comprising disposing said substrate including said iridium electrode layer of step (a) in a high density plasma chamber including a coil inductor and a wafer pedestal; and performing said etching step (f) in said high density plasma chamber under the following process conditions:

Process	Parameters
Etchant Gas flow	50 to 500 sccm
Pressure, mTorr	0.1 to 300 milliTorr
RF Power (watts) of Coil Inductor	100 to 5000 watts
RF Power (watts) of Wafer Pedestal	50 to 3000 watts
Iridium Etch Rate (Å/min)	200 to 6000 Å/min
RF Frequency of Coil Inductor	100K to 300 MHz
RF Frequency of Wafer Pedestal.	100K to 300 MHz

125. The method of claim **24** wherein said etchant gas additionally comprises O_2.

126. The method of claim **125** additionally comprising disposing said substrate including said iridium electrode layer of step (a) in a high density plasma chamber including a coil inductor and a wafer pedestal; and performing said etching step (f) in said high density plasma chamber under the following process conditions:

Process	Parameters
O_2	5% to 40% by vol.
Cl_2	10% to 60% by vol.
Ar	30% to 80% by vol.
Pressure, mTorr	0.1 to 300 milliTorr
RF Power (watts) of Coil Inductor	100 to 5000 watts
RF Power (watts) of Wafer Pedestal	50 to 3000 watts
Iridium Etch Rate (Å/min)	200 to 6000 Å/min
Selectivity of Ir to TiN	.2 to 50
RF Frequency of Coil Inductor	100K to 300 MHz
RF Frequency of Wafer Pedestal.	100K to 300 MHz

127. The method of claim **24** wherein said halogen containing gas is a halogen gas and said etchant gas comprises from about 20% by volume to about 95% by volume of the halogen gas and from about 5% by volume to about 80% by volume of the noble gas.

128. The method of claim **24** wherein said halogen containing gas is a halogen gas and said etchant gas comprises from about 40% by volume to about 80% by volume of the halogen gas and from about 20% by volume to about 60% by volume of the noble gas.

129. The method of claim **24** wherein said halogen containing gas is a halogen gas and said etchant gas comprises from about 55% by volume to about 65% by volume of the halogen gas and from about 35% by volume to about 45% by volume of the noble gas.

130. The method of claim **118** wherein said halogen containing gas is a halogen gas and said etchant gas comprises from about 5% by volume to about 40% by volume oxygen, from about 10% by volume to about 60% by volume of the halogen gas, and from about 30% by volume to about 80% by volume of the noble gas.

131. The method of claim **118** wherein said halogen containing gas is a halogen gas and said etchant gas comprises from about 10% by volume to about 30% by volume oxygen, from about 20% by volume to about 50% by volume of the halogen gas, and from about 40% by volume to about 70% by volume of the noble gas.

132. The method of claim **118** wherein said halogen containing gas is a halogen gas and said etchant gas com-

prises from about 10% by volume to about 20% by volume oxygen, from about 20% by volume to about 30% by volume of the halogen gas, and from about 50% by volume to about 70% by volume of the noble gas.

133. The method of claim **119** wherein said halogen containing gas is a halogen gas and said etchant gas comprises from about 10% by volume to about 90% by volume of the halogen gas, from about 5% by volume to about 80% by volume of the noble gas, and from about 4% by volume to about 25% by volume of a gas selected from the group consisting of HBr, BCl_3, and mixtures thereof.

134. The method of claim **119** wherein said halogen containing gas is a halogen gas and said etchant gas comprises from about 40% by volume to about 70% by volume of the halogen gas, from about 25% by volume to about 55% by volume of the noble gas, and from about 5% by volume to about 20% by volume of gas selected from the group consisting of HBr, BCl_3, and mixtures thereof.

135. The method of claim **119** wherein said halogen containing gas is a halogen gas and said etchant gas comprises from about 50% by volume to about 60% by volume of the halogen gas, from about 35% by volume to about 45% by volume of the noble gas, and from about 5% by volume to about 15% by volume of gas selected from the group consisting of HBr, BCl_3, and mixtures thereof.

136. The method of claim **119** wherein said halogen containing gas is a halogen gas and said etchant gas comprises from about 5% by volume to about 20% by volume oxygen, from about 10% by volume to about 60% by volume of the halogen gas, from about 30% by volume of about 80% by volume of the noble gas, and from about 5% by volume to about 20% by volume of a gas selected from the group consisting of HBr, HCl, and mixtures thereof.

137. The method of claim **119** wherein said halogen containing gas is a halogen gas and said etchant gas comprises from about 5% by volume to about 15% by volume oxygen, from about 20% by volume to about 50% by volume of the halogen gas, from about 40% by volume of about 70% by volume of the noble gas, and from about 5% by volume to about 15% by volume of a gas selected from the group consisting of HBr, HCl, and mixtures thereof.

138. The method of claim **119** wherein said halogen containing gas is a halogen gas and said etchant gas comprises from about 5% by volume to about 10% by volume oxygen, from about 20% by volume to about 35% by volume of the halogen gas, from about 40% by volume of about 60% by volume of the noble gas, and from about 5% by volume to about 10% by volume of a gas selected from the group consisting of HBr, HCl, and mixtures thereof.

139. The method of claim **24** wherein said temperature of said substrate ranges from about 200° C. to about 400° C.

140. The method of claim **24** wherein said temperature of said substrate ranges from about 250° C. to about 350° C.

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