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(54) **Title**: LOW VOLTAGE ISOLATION SWITCH, IN PARTICULAR FOR A TRANSMISSION CHANNEL FOR ULTRASOUND APPLICATIONS

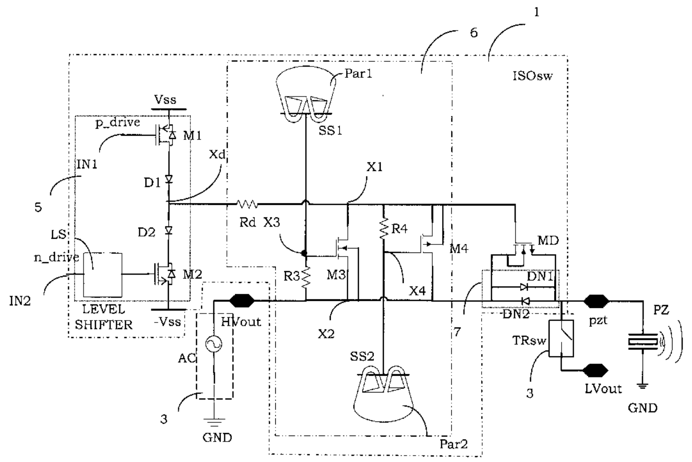

FIG. 3

(57) **Abstract**: A low voltage isolation switch (1) is described, inserted between an input terminal (HVout) suitable for receiving a high voltage signal (IM) and an output terminal (pzt) suitable for transmitting this high voltage signal (IM) to a load (PZ) of the type comprising at least one driving block (5) being inserted between a first and a second voltage reference (Vss, -Vss) and comprising a first driving transistor (M1), inserted, in series to a first driving diode (D1), between the first voltage reference (Vss) and a first driving central circuit node (Xd) and a second driving transistor (M2), in turn inserted, in series with a second driving diode (D2), between the driving central circuit node (Xd) and the second supply voltage reference (-Vss) as well as a control transistor (MD) connected across a diode block (7) comprising at least one first and one second transmission diode (DN1, DN2), connected in antiparallel, i.e. by having the anode terminal of the first diode connected to the cathode terminal of the second one and vice versa, between the input (HVout) and output (pzt) terminals of the low voltage isolation switch (1), this control transistor (MD) having a control terminal connected to the driving central circuit node (Xd) through a low voltage decoupling block (6), in turn inserted between a first and a second substrate terminal (SS1, SS2) and also comprising a first and a second parasite capacitive element (Par1, Par2) connected to these first and second

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substrate terminals (SS1, SS2) as well as comprising at least one first decoupling transistor (M3) and one second decoupling transistor inserted (M4), being in parallel to each other and having control terminals connected to the first and second parasite capacitive elements (Par1, Par2), respectively.

Title: Low voltage isolation switch, in particular for a transmission channel for ultrasound applications

DESCRIPTION

Technical Field

The present invention relates to a low voltage switch.

The invention also relates to a transmission channel of a high voltage signal to a load, in particular a piezoelectric transducer and to a corresponding driving method.

The invention particularly, but not exclusively, relates to a low voltage switch for a transmission channel for ultrasound applications and the following description is made with reference to this field of application by way of illustration only.

Background Art

As it is well known, the sonography or ultrasonography is a system of medical diagnostic testing that uses ultrasonic waves or ultrasounds and is based on the principle of the transmission of the ultrasounds and of the emission of echoes and is widely used in the internist, surgical and radiological field.

The ultrasounds being normally used are comprised between 2 and 20 MHz. The frequency is chosen taking into consideration that higher frequencies have a greater image resolving power, but penetrate less in depth in the subject under examination.

These ultrasounds are normally generated by a piezoceramic crystal being inserted in a probe maintained in direct contact with the skin of the subject with the interposition of a suitable gel (suitable for eliminating the air between probe and subject's skin, allowing the ultrasounds to penetrate into the anatomic segment being examined). The same probe is able to collect a return signal or echo, which is suitably processed by a computer and displayed on a monitor.

In particular, the ultrasounds that reach a variation point of the acoustic impedance, and thus for example an internal organ, are partially reflected and the reflected percentage conveys information about the impedance difference between the crossed tissues. It is to be noted that, the big impedance difference between a bone and a tissue being considered, with the sonography it is not possible to see behind a bone, which causes a total reflection of the ultrasounds, while air or gas zones give "shade", causing a partial reflection of the ultrasounds.

The time employed by an ultrasonic wave for travelling across the path of going, reflection and return is provided to the computer, which calculates the depth wherefrom the echo has come, thus identifying the division surface between the crossed tissues (corresponding to the variation point of the acoustic impedance and thus to the depth wherefrom the echo comes).

Substantially, an ultrasonographer, in particular a diagnostic apparatus based on the ultrasound sonography, essentially comprises three parts:

- a probe comprising at least one transducer, in particular of the ultrasonic type, which transmits and receives an ultrasound signal;
- an electronic system that drives the transducer for the generation of the ultrasound signal or pulse to be transmitted and receives an echo signal of return of this pulse at the probe, processing in consequence the received echo signal; and
- a displaying system of a corresponding processed sonographic image starting from the echo signal received by the probe.

In particular, the word transducer generally indicates an electric or electronic device that converts a type of energy relative to mechanical and physical quantities into electric signals. In a broad sense, a transducer is sometimes defined as any device that converts energy from a form to another, so that it can be re-processed either by men or by other machines. Many transducers are both sensors and actuators. An ultrasonic transducer usually comprises a piezoelectric crystal that is suitably biased for causing its deformation and the generation of the ultrasound signal or pulse.

Ultrasonic transducers for sonographic images are usually driven by high voltage driving circuits or drivers able to generate a sinusoidal signal of variable width comprised between 3 and 200Vpp and frequencies from 1MHz to 20MHz, this sinusoidal signal being a control signal for corresponding generators of the ultrasound pulse to be transmitted, in particular piezoelectric crystals.

The corresponding driving circuits are thus made of components that can sustain these high voltages and that, given the frequencies at stake, can supply currents high enough to a load applied at the output, in particular an ultrasonic transducer.

These needs lead to use components with rather big sizes. These components however add high parasite capacities in parallel to the transducer.

Moreover, the transducer itself is used also for the reception in a transmission channel for these ultrasound applications. Typically, an ultrasonic transducer transmits a high voltage pulse of the duration of a few us, and receives the echo of this pulse, generated by the reflection on the organs of a subject under examination, for the duration of about 250us, to go back to the transmission of a new high voltage pulse. For example, a first pulse IM1 and a second pulse IM2 are transmitted with an excursion peak to peak equal, in the example shown, to 190Vpp with reception by the transducer of corresponding echoes, indicated with E1 and E2, as schematically shown in Figure 1.

The echo signal or return acoustic wave is converted into an electric wave that is a signal of some millivolts of width, signal that is then amplified by low noise amplifier circuits, connected to the transducer itself, in turn disturbed by the parasite capacity due to the high voltage components of the driving circuit of the transducer. This reduces the quality of the echo signal.

The technical problem of the present invention is that of reducing the effect of the parasite capacities of the high voltage components of a driving circuit, in particular for an ultrasonic transducer in a transmission channel for ultrasound applications, having such structural and functional features as to ensure a correct transmission in this transmission channel of high voltage signals for the transmission of an ultrasonic pulse to an output terminal connected to this transducer, and at the same time to ensure the correct isolation of this terminal when receiving an echo signal, overcoming in this way the limits and/or drawbacks still limiting the systems realised according to the prior art.

Disclosure of Invention

The solution idea underlying the present invention is that of using an isolation switch realised with low voltage components, so that they have a very reduced parasite capacity, this switch being inserted in the transmission channel interposed between the output terminal connected to the ultrasonic transducer and the high voltage components of the driving circuit.

On the basis of this solution idea the technical problem is solved by a low voltage isolation switch inserted between an input terminal suitable for receiving a high voltage signal and an output terminal suitable for transmitting said high voltage signal to a load of the type comprising at least one driving block being inserted between a first and a second voltage reference and comprising a first driving transistor, inserted, in series with a first driving diode, between said first voltage reference and a first driving central circuit node and a second driving transistor, in turn inserted, in series with a second driving diode, between said driving central circuit node and said second supply voltage reference as well as a control transistor connected across a diode block comprising at least one first and one second transmission diode, connected in antiparallel, i.e. by having the anode terminal of the first diode connected to the cathode terminal of the second one and vice versa, between said input and output terminals of said low voltage isolation switch, said control transistor having a control terminal connected to said driving central circuit node through a low voltage decoupling block, in turn inserted between a first and a second substrate terminal and comprising a first and a second parasite capacitive element connected to said first and second substrate terminals, as well as comprising at least one first decoupling transistor and one second decoupling transistor inserted, being in parallel to each other and having control terminals connected to the first and second parasite capacitive elements, respectively.

More in particular, the invention comprises the following supplementary and optional features, taken alone or, if need be, in combination.

According to an aspect of the invention, said low voltage decoupling block may comprise an input resistive element being inserted between said driving central circuit node and a first inner circuit node, the first decoupling transistor being inserted between said first inner circuit node and a second inner circuit node and the second decoupling transistor inserted, in parallel to said first decoupling transistor, between said first and second inner circuit nodes.

According to this aspect of the invention, said first decoupling transistor may have a control terminal connected to a third inner circuit node, in turn connected to said second inner circuit node through a first decoupling resistive element, as well as to said first substrate terminal and said second decoupling transistor may have a control terminal connected to a fourth inner circuit node, in turn connected to said first inner circuit node through a second decoupling resistive element, as well as to said second substrate terminal.

Further, according to another aspect of the invention, said diode block may comprise the first and second transmission diodes, connected in antiparallel, between said output terminal and said low voltage decoupling block in correspondence with said second inner circuit node.

According to another aspect of the invention, said first driving transistor of said driving block may have a control terminal receiving a first driving signal and said second driving transistor has a control terminal connected to a level shifter receiving in turn a second driving signal.

Moreover, according to an aspect of the invention, said first driving transistor may be a P channel MOS transistor and said second driving transistor may be an N channel MOS transistor.

According to another aspect of the invention, said control transistor may be a diode-like configured low voltage N channel MOS transistor.

According to another aspect of the invention, said first decoupling transistor may be a diode-like configured low voltage N channel MOS transistor and said second decoupling transistor may be a diode-like configured low voltage P channel MOS transistor.

Moreover, according to an aspect of the invention, said low voltage isolation switch may be realised on a substrate of the SOI type and said first and second parasite capacitive elements can be realised by means of doped wells implanted in said substrate of the SOI type.

The problem is also solved by a transmission channel of a high voltage signal being on an input terminal of a connection terminal to a load, of the type comprising at least one matrix of high voltage switches inserted between said input terminal and a first high voltage output terminal, as well as a second low voltage output terminal connected to a transconductance cell and a transmission switch connected between said first output terminal and said second output terminal characterised in that it comprises at least one low voltage isolation switch realised as above indicated and having an input terminal connected to said first output terminal and an output terminal connected to said connection terminal.

According to an aspect of the invention, said transmission channel may comprise an array comprising a plurality of low switch isolation switches, connected in series to a plurality of channels of said matrix of switches and suitable for isolating a corresponding array of a plurality of loads.

Moreover, according to another aspect of the invention, said transmission channel may be used for the transmission of an ultrasound pulse as high voltage signal, said load being a piezoelectric transducer.

The problem is finally solved by a driving method of a transmission channel as above described, characterised in that it comprises:

- a transmission mode of said high voltage signal to said connection terminal to said load in which said matrix of switches is turned on, said transmission switch is switched off and said high voltage signal is transmitted through said low voltage isolation switch, and in particular through said diode block;
- a first receiving mode of an echo signal through said transmission switch in which said matrix of switches and said low voltage isolation switch are switched off and said transmission switch is turned on, said echo signal flowing from said connection terminal toward said second output terminal and then to said transconductance cell; and
- a second receiving mode of an echo signal through said matrix of switches in which said matrix of switches and said low voltage isolation switch are turned on and said transmission switch is switched off, said echo signal flowing from said connection terminal toward said first output terminal and then to said input terminal.

According to an aspect of the invention, in said transmission mode, said control transistor may be switched off by turning on said second driving transistor of said driving block and said high voltage signal may be transmitted through said first and second transmission diodes of said diode block bringing said first driving signal to a first high value and said second driving signal to a second low value, said low voltage decoupling block preventing a capacitive coupling of said second driving transistor.

According to this aspect of the invention, in said transmission mode, said low voltage decoupling block may have the following operation:

a. on the positive edges of said high voltage signal, said second decoupling transistor is turned on thanks to a voltage drop that develops on said second resistive element connected between its gate and source terminals and to a charge current flowing in said second parasite capacitive element that acts as an active element for activating said second driving transistor;

b. on the negative edges of said high voltage signal said first decoupling transistor is turned on thanks to a voltage drop that develops on said first resistive element connected between its gate and source terminals and to a charge current flowing in said first parasite capacitive element that acts as an active element for activating said first transistor.

Further, according to another aspect of the invention, prior to said first receiving mode, said control transistor may be switched off and said second driving transistor may be turned on, while said first driving transistor is switched off.

According to this aspect of the invention, in said first receiving mode, said transmission switch may be closed for transferring said echo signal to said second output terminal, said first and second driving signals being both brought to a first high value.

According to another aspect of the invention, in said second receiving mode, said control transistor may be turned on, said first driving transistor is turned on and said second driving transistor may be switched off while said transmission switch is kept open so that said echo signal reaches the matrix of switches through said control transistor, said first and second driving signals being both brought to a second low value.

The features and the advantages of the low voltage isolation switch, of the transmission channel and of the driving method according to the invention will be apparent from the following description of an embodiment thereof given by way of indicative and non limiting example with reference to the annexed drawings.

Brief Description of Drawings

In these drawings:

- Figure 1 schematically shows a first and a second ultrasound pulse generated by a driving circuit and thereby applied to an ultrasonic transducer according to the prior art;

- Figures 2A, 2B and 2C schematically show a transmission channel for ultrasound applications realised according to the invention, according to a first, a second and in a third operation condition, respectively;

- Figure 3 schematically shows a low voltage switch realised according to the invention;

- Figure 4 schematically shows the operation of the switch of Figure 3 according to different operation conditions of the same, and
- Figure 5 shows an embodiment of the transmission channel of Figures 2A-2C for the driving of a plurality of piezoelectric transducers.

Modes for Carrying Out the Invention

With reference to these figures, and in particular to Figures 2A, 2B and 2C, 10 globally and schematically indicates a transmission channel of an impulsive signal for an ultrasound transducer, in particular a piezoelectric transducer PZ.

By way of illustration, only an output section of the transmission channel 10 has been actually shown, which is connected to the piezoelectric transducer PZ and supplies it with an impulsive signal IM generated by suitable circuitry (not shown) and already present on an input terminal IN.

In particular, the transmission channel 10 firstly comprises a matrix 2 of high voltage switches (MATRIXsw) inserted between the input terminal IN and a first high voltage output terminal HVout, whereon the input impulsive signal IM is transmitted.

Furthermore, the transmission channel 10 comprises a second low voltage output terminal LVout suitable for being connected to a transconductance cell 4 (LNA) and a connection terminal pzt to a piezoelectric transducer PZ. Furthermore, the transmission channel 10 comprises at least one transmission switch 3 (TRsw) connected between the first output terminal HVout and the second output terminal LVout.

According to an embodiment of the invention, the transmission channel 10 also comprises an isolation switch 1 (ISOsw), in particular a low voltage switch, inserted between the first output terminal HVout and the connection terminal pzt. In this way, the first output terminal HVout is connected to the second output terminal LVout through the series of the low voltage isolation switch 1 and of the transmission switch 3.

The use of the low voltage isolation switch 1 allows to overcome the problem of the high parasite capacity due to the high voltage components of the matrix 2 of switches. In particular, as it will be clarified hereafter in the description, this low voltage isolation switch 1 comprises only low voltage components that have a very reduced parasite capacity.

According to a first operation condition, in particular a transmission mode of a pulse IM to the connection terminal pzt to the piezoelectric transducer PZ, as shown in Figure 2A according to the path indicated as Path1, the matrix 2 of switches is turned on for transmitting this pulse IM from the input terminal IN to the first output terminal HVout. Moreover, the transmission switch 3 is switched off and the pulse IM is transmitted through the low voltage isolation switch 1, thanks to the presence into the low voltage isolation switch 1 of a diode block 7 connected to the connection terminal pzt, as it will be explained hereafter in the description.

According to a second operation condition, in particular a receiving mode of an echo signal E through the transmission switch 3, as shown in Figure 2B according to the path indicated as Path2, the matrix 2 of switches and the low voltage isolation switch 1 are switched off and the transmission switch 3 is turned on, the echo signal E flowing from the connection terminal pzt to the piezoelectric transducer PZ toward the second output terminal LVout and then to the transconductance cell 4.

Finally, according to a third operation condition, in particular a second receiving mode of an echo signal E through the matrix 2 of switches, as shown in Figure 2C according to the path indicated as Path1, the matrix 2 of switches and the low voltage isolation switch 1 are turned on and the transmission switch 3 is switched off, the echo signal E flowing from the connection terminal pzt to the piezoelectric transducer PZ toward the first output terminal HVout and then to the input terminal IN.

The low voltage isolation switch 1 according to the invention is shown in greater detail in Figure 3.

In particular, by way of illustration, in this Figure 3, the matrix 2 of switches is simply indicated as high voltage block AC connected to the first output terminal HVout.

In essence, the first output terminal HVout of the matrix 2 of switches is an input terminal of the low voltage isolation switch 1 suitable for receiving a high voltage signal, while the connection terminal pzt is an output terminal of the low voltage isolation switch 1 suitable for transmitting this high voltage signal to a load, in particular the piezoelectric transducer PZ.

The low voltage isolation switch 1 comprises a driving block 5 being inserted between a first and a second voltage reference, respectively a positive supply Vss and a negative supply –Vss, and comprises a first driving transistor M1, inserted, in series with a first driving diode D1, between the positive supply voltage reference Vss and a first driving central circuit node Xd and having a control or gate terminal receiving a first driving signal, p_drive.

The driving block 5 also comprises a second driving transistor M2, in turn inserted, in series with a second driving diode D2, between the driving central circuit node Xd and the negative supply voltage reference -Vss and having a control or gate terminal connected to a level shifter LS (LEVEL SHIFTER) receiving in turn a second driving signal n_drive. In particular, the level shifter LS has the aim of adapting the voltage levels of the first driving signal n_drive, usually generated by a logic circuitry and thus plausibly with a low logic level or "0" corresponding to a ground value GND and a high logic level or "1" corresponding to a positive supply voltage value Vss. The level shifter LS is thus a logic level shifter form [Vss; 0] to [0; -Vss].

In the embodiment of Figure 3, the first driving transistor M1 is a P channel MOS transistor, while the second driving transistor M2 is an N channel MOS transistor. Moreover, these driving transistors are high voltage transistors, since on the first output terminal HVout a high voltage signal is present, transferred in consequence to the driving central circuit node Xd, that follows the value of this first output terminal HVout, decreased by a value equal to the positive supply voltage Vss, if any, when the transistor M4 is on, with a high voltage dynamics that is sustained according to an inverse condition by the driving transistors, M1 and M2.

The low voltage isolation switch 1 also comprises a control transistor MD having a control or gate terminal connected to the driving central circuit node Xd through a low voltage decoupling block 6. This control transistor MD is in particular connected to the ends of a diode block 7 in turn connected to the connection terminal pzt and comprising at least one first DN1 and one second transmission diode DN2, connected in antiparallel, i.e. by having the anode terminal of the first diode connected to the cathode terminal of the second one and vice versa, between this connection terminal pzt and the low voltage decoupling block 6. In particular, the first transmission diode DN1 has the cathode terminal connected to the connection terminal pzt and the anode terminal connected to the low voltage decoupling block 6, while the second transmission diode DN2 has the anode terminal connected to the connection terminal pzt and the cathode terminal connected to the low voltage decoupling block 6.

In the example of the figure, the control transistor MD is a low voltage diode-like configured N channel MOS transistor.

According to an embodiment of the invention, the low voltage decoupling block 6 comprises an input resistive element Rd inserted between the driving central circuit node Xd and a first inner circuit node X1, as well as a first decoupling transistor M3 inserted between this first inner circuit node X1 and a second inner circuit node X2 and having a control or gate terminal connected to a third inner circuit node X3, in turn connected to the second inner circuit node X2 through a first decoupling resistive element R3, as well as to a first substrate terminal SS1.

Furthermore, the low voltage decoupling block 6 comprises a second decoupling transistor M4 inserted, in parallel to the first decoupling transistor M3, between the first X1 and the second inner circuit node X2 and having a control or gate terminal connected to a fourth inner circuit node X4, in turn connected to the first inner circuit node X1 through a second decoupling resistive element R4, as well as to a second substrate terminal SS2.

In particular, the diode block 7 is connected to the low voltage decoupling block 6 in correspondence with the second inner circuit node X2.

In the example of the figure, the first decoupling transistor M3 is a low voltage diode-like configured N channel MOS transistor, while the second decoupling transistor M4 is a low voltage diode-like configured P channel MOS transistor.

According to an embodiment of the invention, the low voltage decoupling block 6 also comprises a first parasite capacitive element Par1 connected to the first substrate terminal SS1 and having a first capacitive value Cp1 and a second parasite capacitive element Par2 connected to the second substrate terminal SS2 and having a second capacitive value Cp2, whose operation will be described hereafter.

In a preferred embodiment, the low voltage isolation switch 1 is realised on a substrate of the SOI type. Moreover, the first and second parasite capacitive elements, Par1 and Par2, are realised by means of doped wells implanted in this substrate SOI.

Let's now see the operation principle of the low voltage isolation switch 1, making reference in particular to Figure 4.

According to the first operation condition, in particular of transmission, a high voltage pulse is on the first output terminal HVout and should be transferred to the connection terminal pzt to the piezoelectric transducer PZ. Prior to this transmission, the control transistor MD is switched off by turning on the second driving transistor M2 of the driving block 5. In this way in fact the gate-source capacity of the control transistor MD is suitably discharged and the high voltage pulse is transmitted through the transmission diodes DN1 and DN2 of the diode block 7, suitably in push-pull. In this case, the first driving signal p_drive is brought to a first high value (for example equal to 3.3V) while the second driving signal n_drive is brought to a second low value (in particular 0V).

It is to be noted that for ultrasound applications, the high voltage pulse applied to the first output terminal HVout has high peak to peak values (~200V) and high slopes (~5V/ns), with the risk of breakage of the gate oxide of the second driving transistor M2, being considered the values reached due to the coupling of its gate-source voltage. According to an embodiment of the invention, the low voltage decoupling block 6 prevents this capacitive coupling thanks to the presence of the first M3 and second decoupling transistor M4 and of the parasite capacitive elements Par1 and Par2 that operate as driving circuits of the gate-source voltage of these transistors M3 and M4.

In particular, the low voltage decoupling block 6 has the following operation (as shown in Figure 4):

a. On the positive edges (arrow UP) of the input high voltage pulse being on the first output terminal HVout of the matrix 2 of switches, the second decoupling transistor M4 is turned on thanks to the voltage drop (Δu1) that develops on the second resistive element R4 connected between its gate and source terminals. In fact, a charge current (Fu1) flows in the second parasite capacitive element Par2 towards the substrate.

In essence, the second parasite capacitive element Par2 (having a parasite capacity equal to Cp2 towards the substrate SOI SUBSTRATE) acts as active element for activating the second driving transistor M4 (Fu2 and Fu3).

b. On the negative edges (arrow DOWN) of the input high voltage pulse being on the first output terminal HVout of the matrix 2 of switches, the operation of the low voltage decoupling block 6 is mirrored for the first decoupling transistor M3. In particular, the first decoupling transistor M3 is turned on thanks to the voltage drop (Δd1) that develops on the first resistive element R3 connected between its gate and source terminals. In fact, a charge current (Fd1) flows in the first parasite capacitive element Par1 towards the substrate.

In substance, the first parasite capacitive element Par1 (having a parasite capacity equal to Cp1 towards the substrate SOI SUBSTRATE) acts as an active element for activating the first driving transistor M3 (Fd2 and Fd3).

According to the second operation condition, in particular when receiving an echo signal through the transmission switch 3, the control transistor MD allows to isolate the matrix 2 of switches and thus to reduce the parasite capacitive load being seen by the piezoelectric transducer PZ. In this case, the control transistor MD is then switched off prior to the arrival of this echo signal. In particular, prior to the arrival of the echo signal, the second driving transistor M2 is turned on and the first driving transistor M1 is switched off. In this way, by closing the transmission switch 3, the echo signal is transferred to the second output terminal LVout and then, as previously seen, to the transconductance cell 4. In this case, the first driving signal p_drive and the second driving signal n_drive are both brought to the first high value (for example equal to 3.3V).

According to the third operation condition, in particular when receiving the echo signal through the matrix 2 of switches, the control transistor MD is turned on. In particular, the first driving transistor M1 is turned on and the second driving transistor M2 is switched off while the transmission switch 3 is kept open.

The echo signal thus reaches the matrix 2 of switches exactly through the control transistor MD. In this case, the first driving signal p_drive and the second driving signal n_drive are both brought to the second low value (for example equal to 0V).

It is to be noted that the first and second parasite capacitive elements Par1 and Par2 behave as "parachutes" for the inner circuit nodes X3 and X4 they are connected to.

According to an embodiment of the invention, as shown in Figure 5, a transmission channel 10 comprises an array 8 of low voltage isolation switches 1, being connected in series to a plurality of channels of the matrix 2 of switches and suitable for isolating a corresponding array 9 of piezoelectric transducers PZ1...PZn. The matrix 2 of switches also comprises a plurality of control terminals In1...Inm for the driving of the columns of switches.

In conclusion, the low voltage switch as described is able to transmit high voltage signals (for example at +/- 100V) or to isolate, when open, a terminal of connection to a piezoelectric transducer, thus ensuring a high immunity to the capacitive couplings of a corresponding input signal, ensuring at the same time a correct operation of the transmission channel that comprises it under all its operation conditions.

According to an aspect of the invention, the low voltage decoupling block 6 comprises a pair of decoupling transistors, M3 and M4, which are connected in parallel to each other and have control or gate terminals connected to the parasite capacitive elements, Par1 and Par2, respectively, such decoupling transistors being thus dynamically controlled by having their control terminals capacitively coupled to one of the substrate terminals, SS1 and SS2.

Obviously, a technician of the field, with the aim of meeting incidental and specific needs, will be allowed to introduce several modifications and variations to the above described circuit, all within the scope of protection of the invention as defined by the following claims.

CLAIMS

1. Low voltage isolation switch (1) inserted between an input terminal (HVout) suitable for receiving a high voltage signal (IM) and an output terminal (pzt) suitable for transmitting said high voltage signal (IM) to a load (PZ) of the type comprising at least one driving block (5) being inserted between a first and a second voltage reference (Vss, –Vss) and comprising a first driving transistor (M1), inserted, in series with a first driving diode (D1), between said first voltage reference (Vss) and a first driving central circuit (Xd) and a second driving transistor (M2), in turn inserted, in series with a second driving diode (D2), between said driving central circuit node (Xd) and said second supply voltage reference (-Vss) as well as a control transistor (MD) connected across a diode block (7) comprising at least one first and one second transmission diode (DN1, DN2), connected in antiparallel, i.e. by having the anode terminal of the first diode connected to the cathode terminal of the second one and vice versa, between said input (HVout) and output (pzt) terminals of said low voltage isolation switch (1), said control transistor (MD) having a control terminal connected to said driving central circuit node (Xd) through a low voltage decoupling block (6), in turn inserted between a first and a second substrate terminal (SS1, SS2) and comprising a first and a second parasite capacitive element (Par1, Par2) connected to said first and second substrate terminals (SS1, SS2) as well as comprising at least one first decoupling transistor (M3) and one second decoupling transistor inserted (M4), being in parallel to each other and having control terminals connected to said first and second parasite capacitive elements (Par1, Par2), respectively.

2. Low voltage isolation switch (1) according to claim 1, wherein said low voltage decoupling block (6) comprises an input resistive element (Rd) inserted between said driving central circuit node (Xd) and a first inner circuit node (X1), said first decoupling transistor (M3) being inserted between said first inner circuit node (X1) and a second inner circuit node (X2) and said second decoupling transistor inserted (M4), being in parallel to said first decoupling transistor (M3) between said first and second inner circuit node (X1, X2).

3. Low voltage isolation switch (1) according to claim 2, wherein said first decoupling transistor (M3) has a control terminal connected to a third inner circuit node (X3), in turn connected to said second inner circuit node (X2) through a first decoupling resistive element (R3), as well as to said first substrate terminal (SS1) and said second decoupling terminal (M4) has a control terminal connected to a fourth inner circuit node (X4), being in turn connected to said first inner circuit node (X1) through a second decoupling resistive element (R4), as well as to said second substrate terminal (SS2).

4. Low voltage isolation switch (1) according to claim 1, wherein said first driving transistor (M1) of said driving block (5) has a control terminal receiving a first driving signal (p_drive) and said second driving transistor (M2) has a control terminal connected to a level shifter (LS) receiving in turn a second driving signal (n_drive).

5. Low voltage isolation switch (1) according to claim 1, wherein said first decoupling transistor (M3) is a diode-like configured low voltage N channel MOS transistor and said second decoupling transistor (M4) is a diode-like configured low voltage P channel MOS transistor.

6. Low voltage isolation switch (1) according to any of the preceding claims, wherein said low voltage isolation switch is realised on a substrate of the SOI type and said first and second parasite capacitive elements (Par1, Par2) are realised by means of doped wells implanted in said substrate of the SOI type.

7. Transmission channel (10) of a high voltage signal (IM) being on an input terminal (IN) to a connection terminal (pzt) to a load (PZ), of the type comprising at least one matrix of high voltage switches (2) being inserted between said input terminal (IN) and a first high voltage output terminal (HVout), as well as a second low voltage output terminal (LVout) connected to a transconductance cell (4) and a transmission switch (3) connected between said first output terminal (HVout) and said second output terminal (LVout) characterised in that it comprises at least one low voltage isolation switch (1) realised according to any of the preceding claims, having an input terminal connected to said first output terminal (HVout) and an output terminal connected to said connection terminal (pzt).

8. Transmission channel (10) according to claim 7, characterised in that it comprises an array (9) comprising a plurality of low switch isolation switches (1), connected in series to a plurality of channels of said matrix of switches (2) and suitable for isolating a corresponding array (9) of a plurality of loads (PZ1...PZn).

9. Transmission channel (10) according to claim 8, characterised in that it is used for the transmission of an ultrasound pulse (IM) as high voltage signal and in that said load is a piezoelectric transducer.

10. Method for driving a transmission channel (10) according to any claim 7 to 9, characterised in that it comprises:

- a transmission mode of said high voltage signal (IM) to said connection terminal (pzt) to said load (PZ) in which said matrix of switches (2) is turned on said transmission switch (3) is turned off and said high voltage signal (IM) is transmitted through said low voltage isolation switch (1), and through said diode block (7);
- a first receiving mode of an echo signal (E) through said transmission

switch (3) in which said matrix of switches (2) and said low voltage isolation switch (1) are switched off and said transmission switch (3) is turned on, said echo signal (E) flowing from said connection terminal (pzt) toward said second output terminal (LVout) and then to said transconductance cell (4); and

- a second receiving mode of an echo signal (E) through said matrix of switches (2) in which said matrix of switches (2) and said low voltage isolation switch (1) are turned on and said transmission switch (3) is switched off, said echo signal (E) flowing from said connection terminal (pzt) toward said first output terminal (HVout) and then to said input terminal (IN).

11. Driving method according to claim 10, characterised in that, in said transmission mode, said control transistor (MD) is switched off by turning on said second driving transistor (M2) of said driving block (5) and said high voltage signal (IM) is transmitted through said first and second transmission diodes (DN1, DN2) of said diode block (7) bringing said first driving signal (p_drive) to a first high value and said second driving signal (n_drive) to a second low value, said low voltage decoupling block (6) preventing a capacitive coupling of said second driving transistor (M2).

12. Driving method according to claim 11, characterised in that, in said transmission mode, said low voltage decoupling block (6) has the following operation:

a. on the positive edges of said high voltage signal (IM), said second decoupling transistor (M4) is turned on thanks to a voltage drop (Δu1) that develops on said second resistive element (R4) connected between its gate and source terminals and to a charge current (Fu1) flowing in said second parasite capacitive element (Par2) that acts as an active element for activating said second driving transistor (M4);

b. on the negative edges of said high voltage signal (IM) said first decoupling transistor (M3) is turned on thanks to a voltage drop (Δd1) that develops on said first resistive element (R3) connected between its gate and source terminals and to a charge current (Fd1) flowing in said first parasite capacitive element (Par1) that acts as an active element for activating said first driving transistor (M3).

13. Driving method according to claim 11, characterised in that, prior to said first receiving mode, said control transistor (MD) is switched off and said second driving transistor (M2) is turned on, while said first driving transistor (1) is switched off.

14. Driving method according to claim 13, characterised in that, in said first receiving mode, said transmission switch (3) is closed for transferring said echo signal to said second output terminal (LVout), said first and second driving

signals (p_drive, n_drive) being both brought to a first high value.

15. Driving method according to claim 14, characterised in that, in said second receiving mode, said control transistor (MD) is turned on, said first driving transistor (M1) is turned on and said second driving transistor (M2) is switched off while said transmission switch (3) is kept open so that said echo signal reaches the matrix of switches (2) through said control transistor (MD), said first and second driving signals (p_drive, n_drive) being both brought to a second low value.

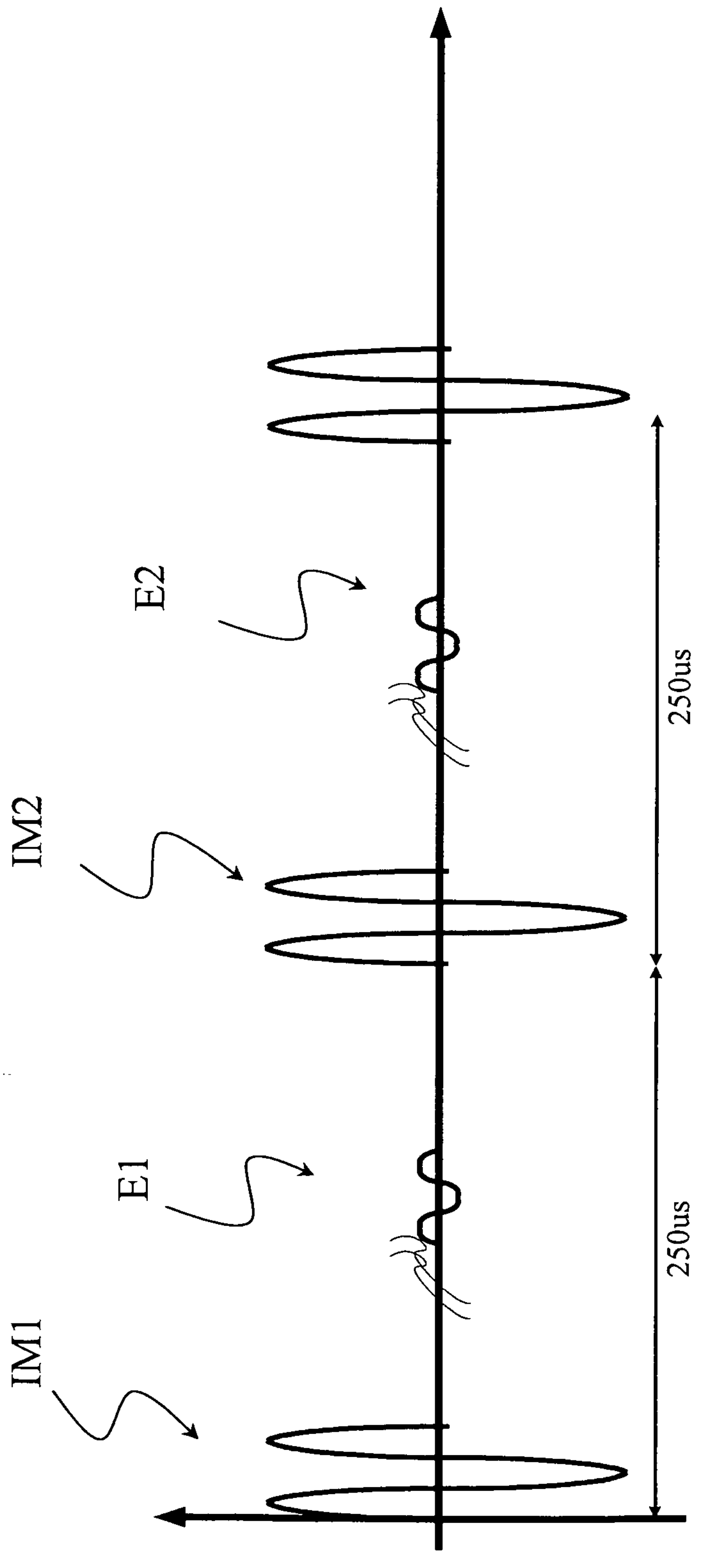
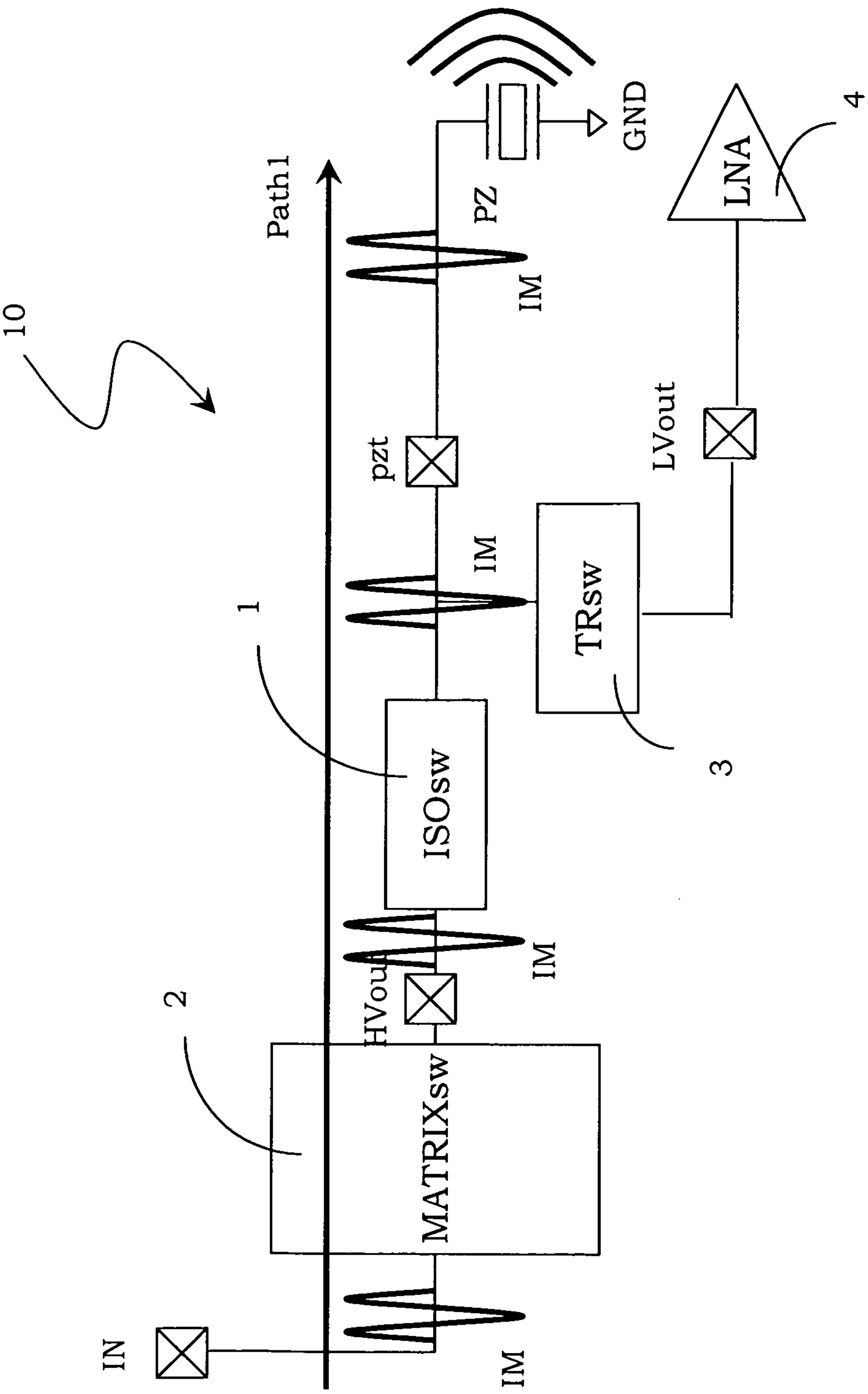


FIG. 1
PRIOR ART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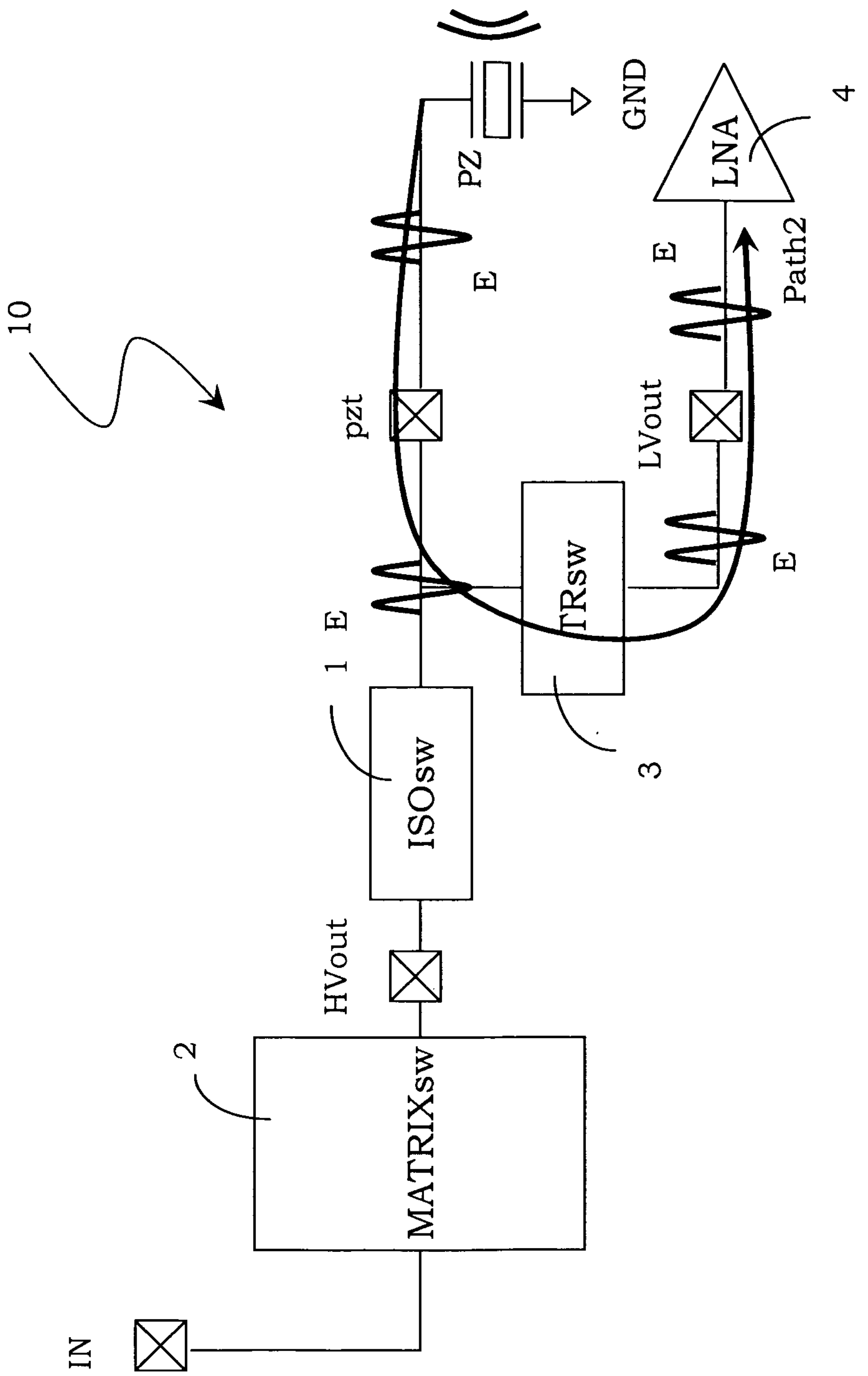
Path1
PZ
GND
LNA
4
IM
pzt
LVout
IM
1
TRsw
3
ISOsw
2
HVout
IM
MATRIXsw
IN
IM

FIG. 2A



10
PZ
GND
LNA
4
E
E
Path2
pzt
LVout
TRsw
E
1
E
ISOsw
3
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MATRIXsw
IN

FIG. 2B

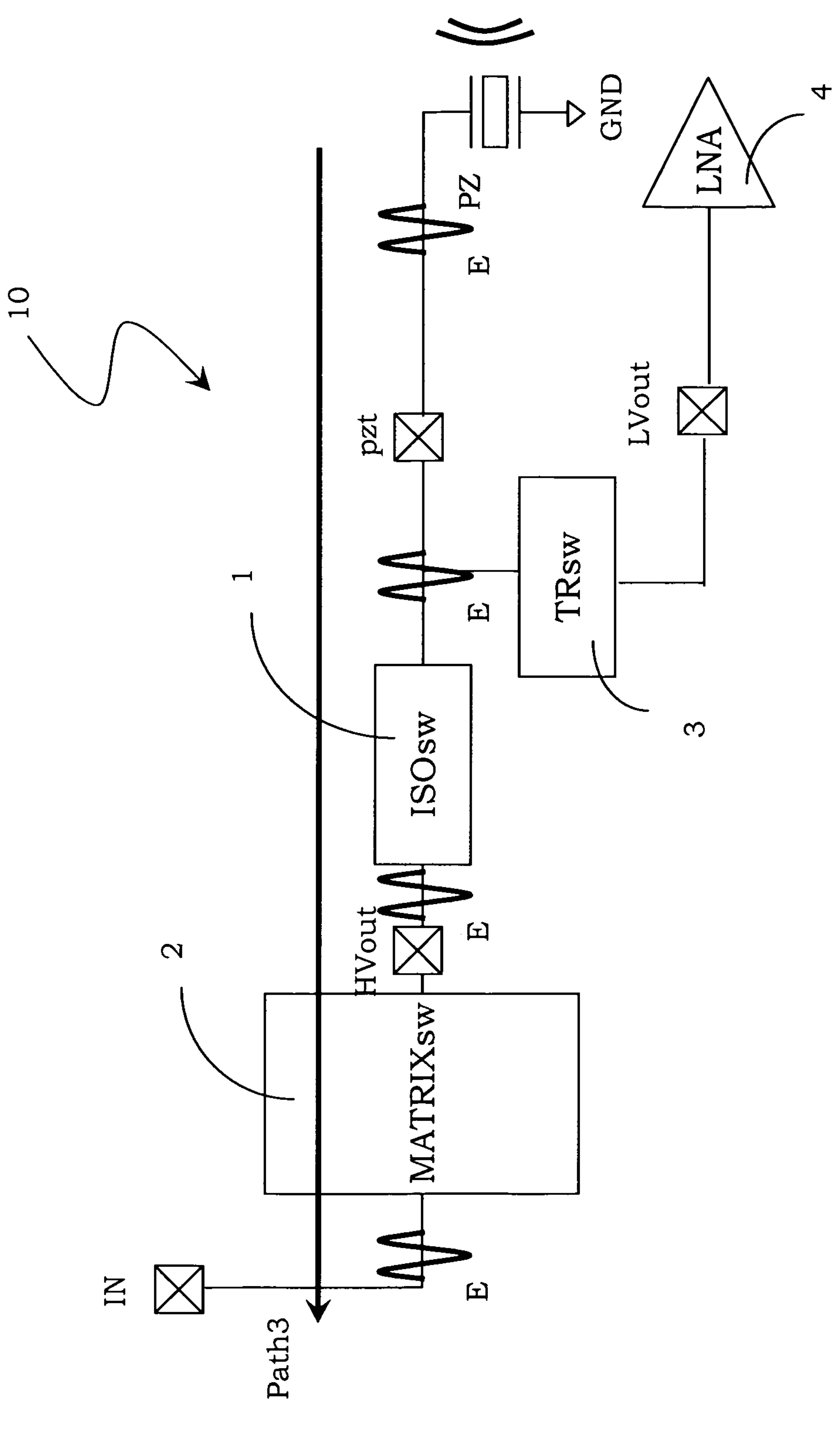
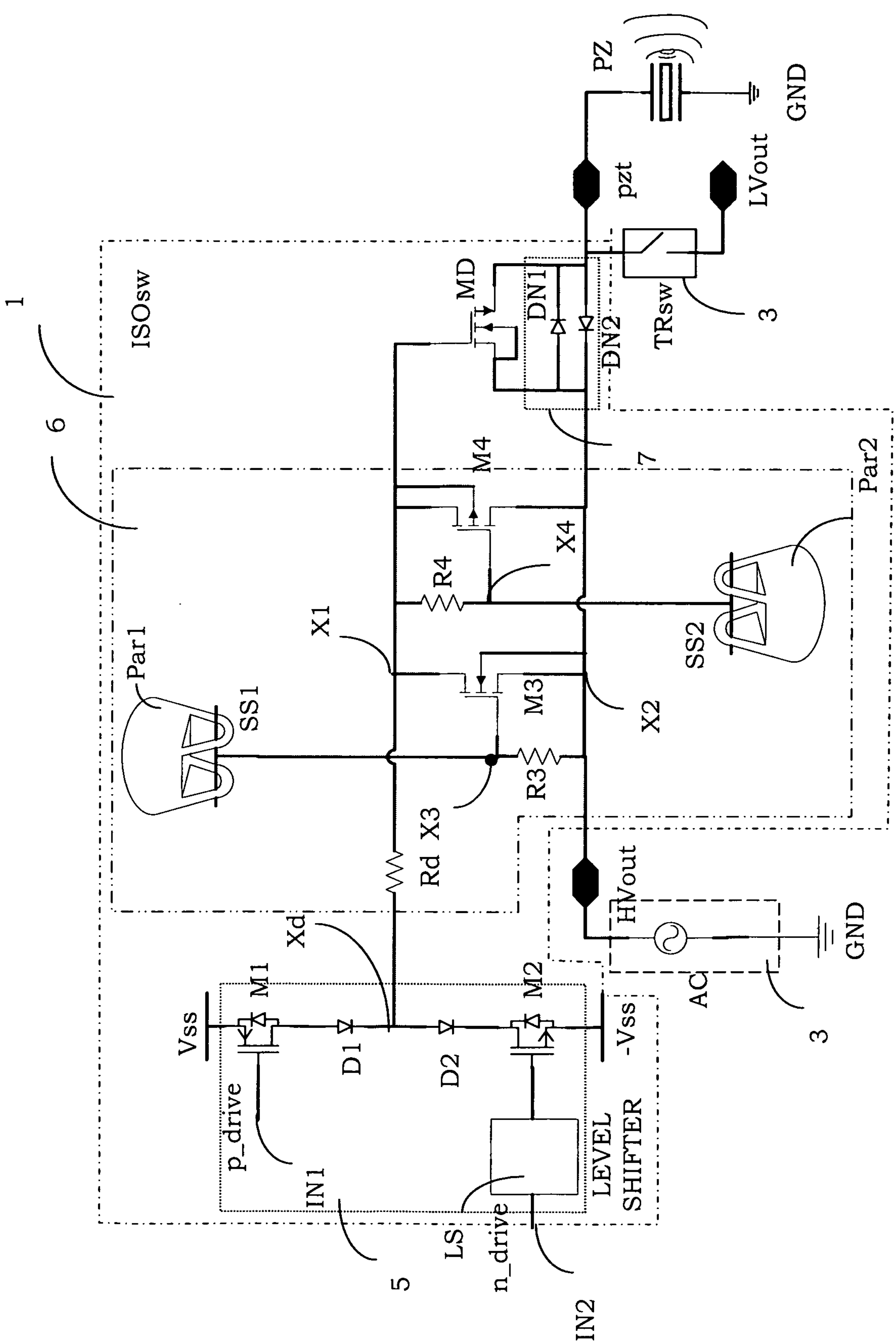
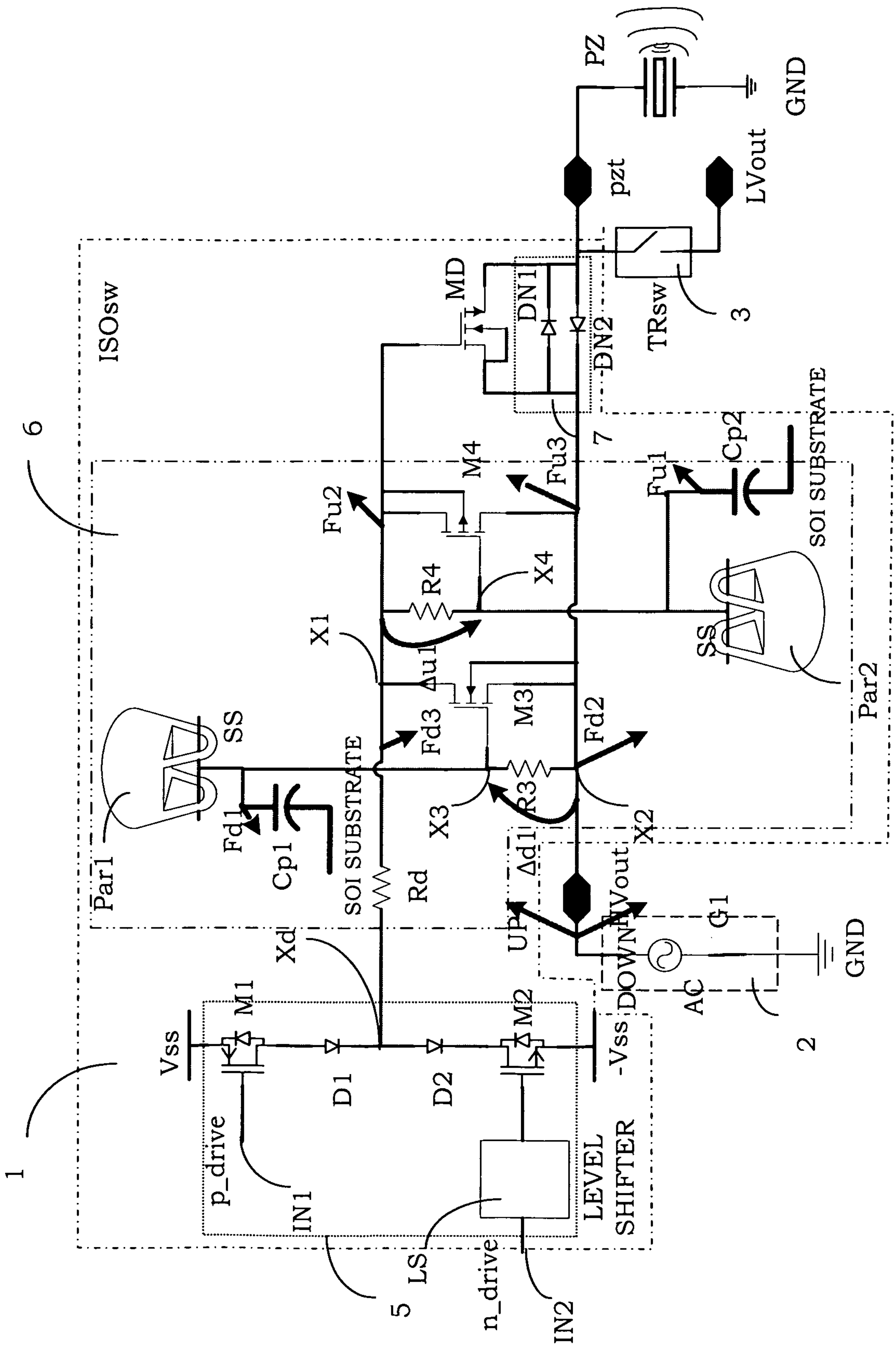

10
IN
Path3
E
MATRIXsw
2
HVout
E
ISOsw
1
E
pzt
E
PZ
GND
TRsw
3
LVout
LNA
4

FIG. 2C



1
ISOsw
6
Par1
SS1
X1
R4
M4
X4
MD
DN1
DN2
7
TRsw
3
PZ
GND
pzt
LVout
Par2
SS2
M3
X2
R3
X3
Rd
HVout
AC
GND
3
Xd
M1
M2
Vss
-Vss
D1
D2
p_drive
IN1
LEVEL SHIFTER
LS
n_drive
IN2
5

FIG. 3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Fu2
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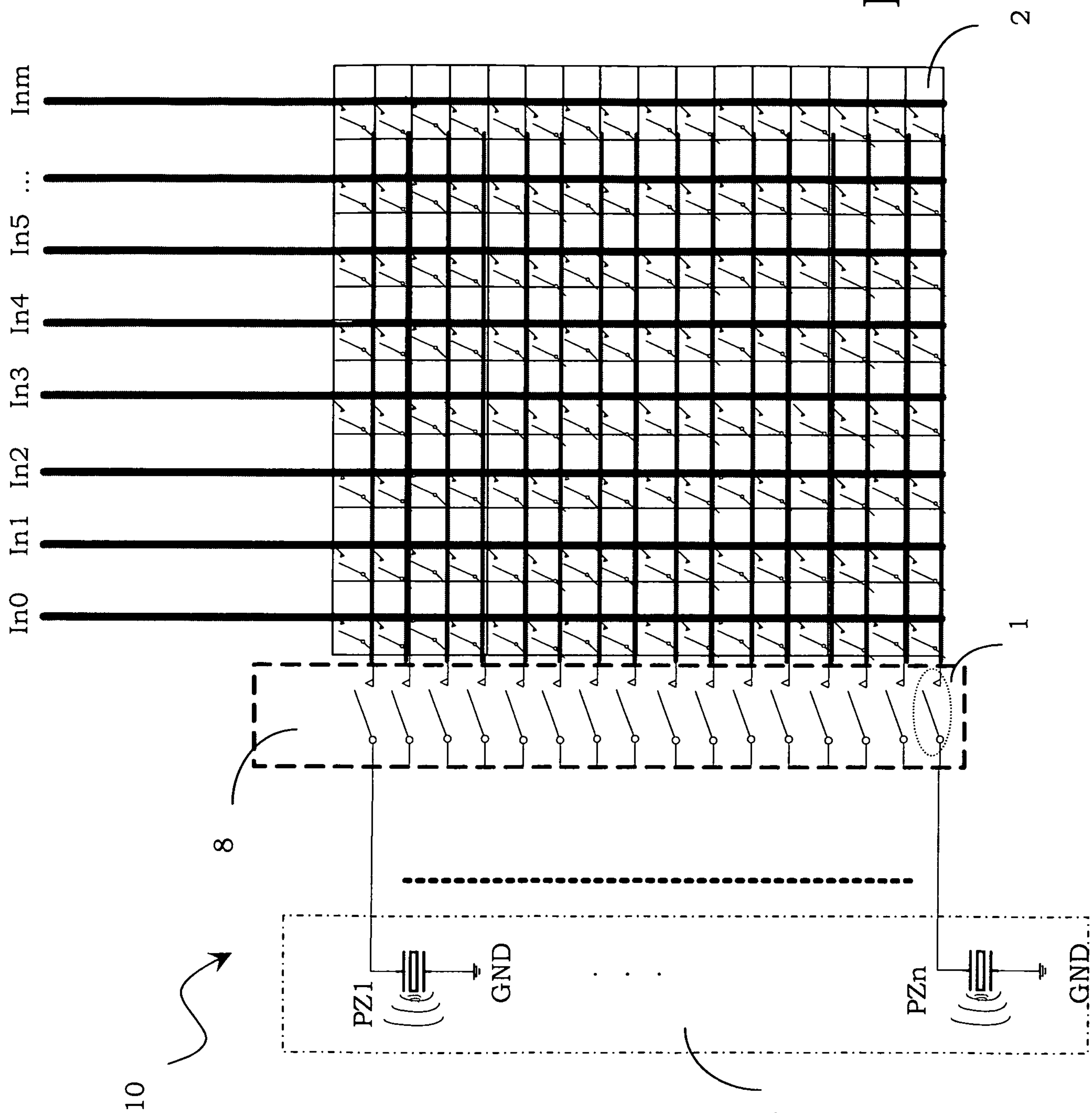
SOI SUBSTRATE
R4
X4
X1
Δu1
M3
SS
Par2
Fd3
Fd2
R3
X3
X2
Par1
Fd1
Cp1
SOI SUBSTRATE
Rd
Δd1
Vout
UP
DOWN
G1
AC
GND
2
Xd
M1
M2
Vss
-Vss
D1
D2
p_drive
IN1
LEVEL SHIFTER
LS
n_drive
IN2
5
1

FIG. 4

FIG. 5



INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2010/005929

A. CLASSIFICATION OF SUBJECT MATTER
INV. H03K17/693 H03K17/74 H03K17/06 H03K17/687 B06B1/02
H03K17/0812
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03K B06B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2009/206676 A1 (CHU CHING [US] ET AL) 20 August 2009 (2009-08-20) paragraph [0014] - paragraph [0017]; figure 1 -----	1-15
A	US 6 269 052 B1 (OPPELT RALPH [DE]) 31 July 2001 (2001-07-31) the whole document -----	1-15
A	US 6 050 945 A (PETERSEN DAVID A [US] ET AL) 18 April 2000 (2000-04-18) the whole document -----	1-15
	-/--	

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
16 May 2011	23/05/2011

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Jepsen, John

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C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	LOCKWOOD G R ET AL: "THE DESIGN OF PROTECTION CIRCUITRY FOR HIGH-FREQUENCY ULTRASOUND IMAGING SYSTEMS", IEEE TRANSACTIONS ON ULTRASONICS, FERROELECTRICS AND FREQUENCY CONTROL, IEEE, US LNKD- DOI:10.1109/58.67834, vol. 38, no. 1, 1 January 1991 (1991-01-01), pages 48-55, XP000172455, ISSN: 0885-3010 the whole document -----	1-15
A	DE 83 37 585 U1 (SWF AUTO-ELECTRIC GMBH) 25 April 1985 (1985-04-25) page 16, paragraph 2 - page 18, paragraph 3; figures 2,3 -----	1-15

1

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/EP2010/005929

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US 6050945	A	18-04-2000	NONE		
DE 8337585	U1	25-04-1985	DE	3347442 A1	11-07-1985