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Jain et al.

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(54) **POWER-COLLAPSIBLE BOUNDARY SCAN**

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(51) **Int. Cl.**

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G01R 31/3185	(2006.01)
G01R 31/28	(2006.01)

(52) **U.S. Cl.**
CPC ***G01R 31/3177*** (2013.01); ***G01R 31/2815*** (2013.01); ***G01R 31/318533*** (2013.01); ***G06F 11/26*** (2013.01)

(58) **Field of Classification Search**
CPC G01R 31/3177; G01R 31/2815; G01R 31/318533; G06F 11/26
USPC 714/727, 724, 726, 729
See application file for complete search history.

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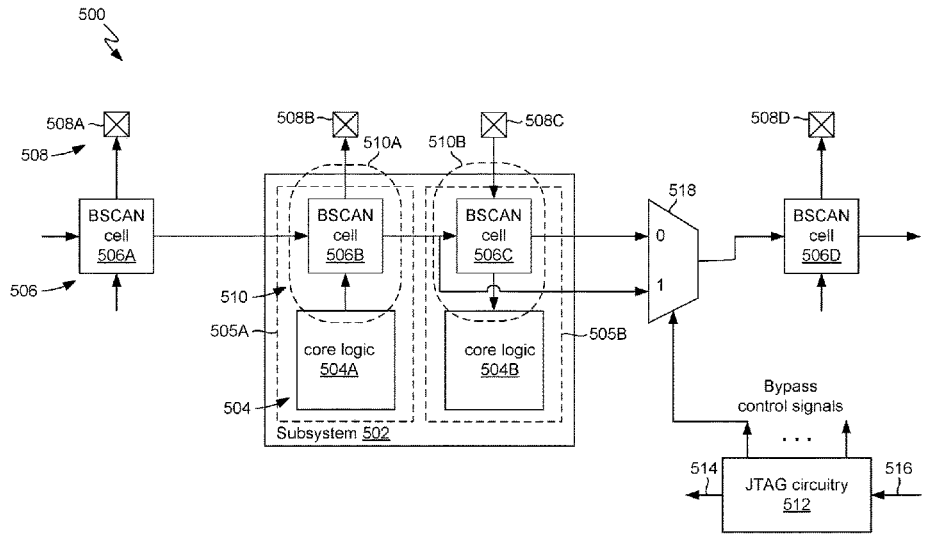
(57) **ABSTRACT**

Physical or off-chip interfaces may be selectively bypassed in a boundary scan chain. A bypass control signal may be produced that indicates whether to bypass a selected one of the interfaces. In response to a first state of a bypass control signal, a multiplexer may couple the scan chain output of an interface boundary scan cell to the scan chain input of a successor boundary scan cell of the interface boundary scan cell. In response to a second state of the bypass control signal, the multiplexer may couple the scan chain output of a predecessor boundary scan cell of the interface boundary scan cell to the scan chain input of the successor boundary scan cell, bypassing the interface boundary scan cell.

14 Claims, 10 Drawing Sheets



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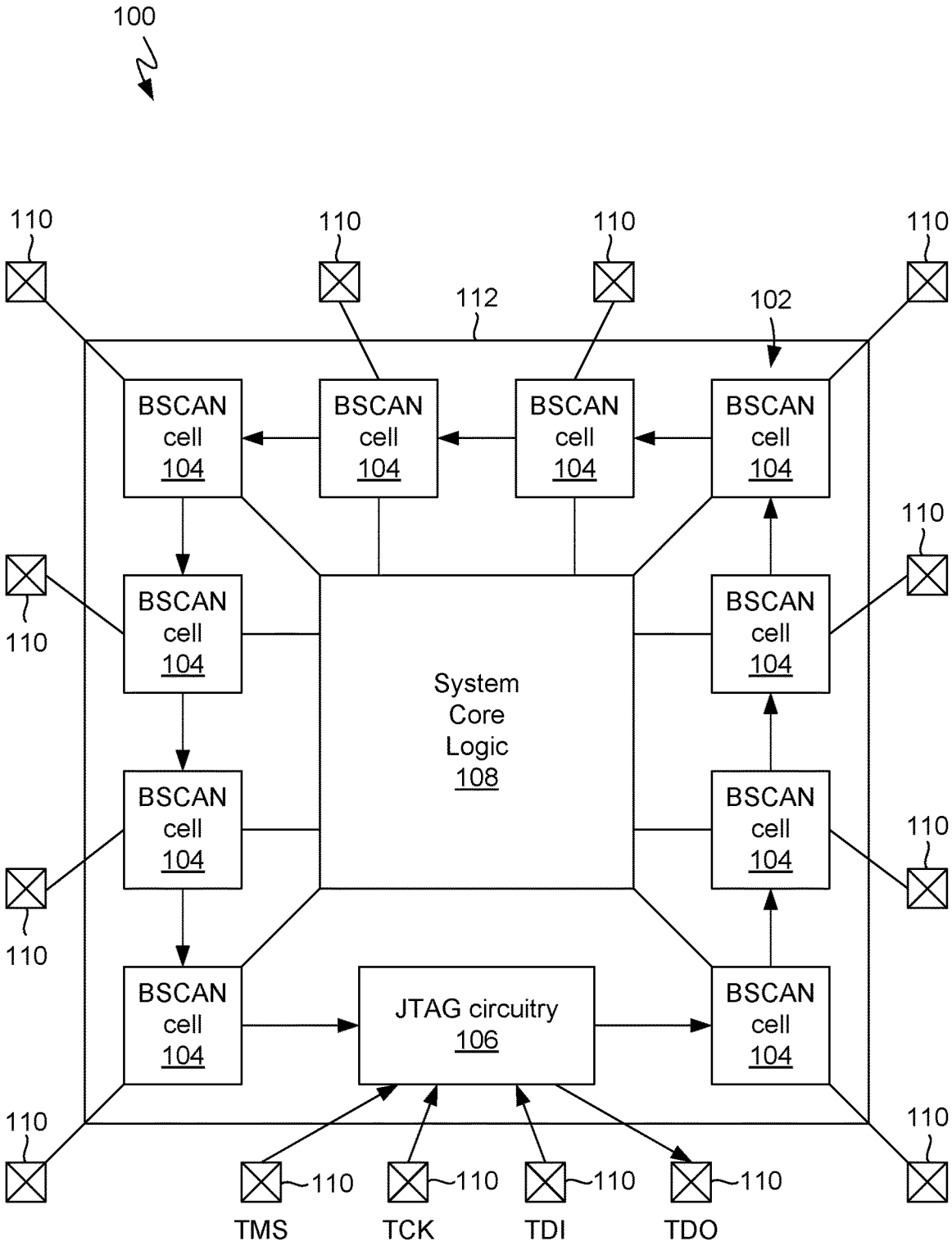

FIG. 1
(PRIOR ART)

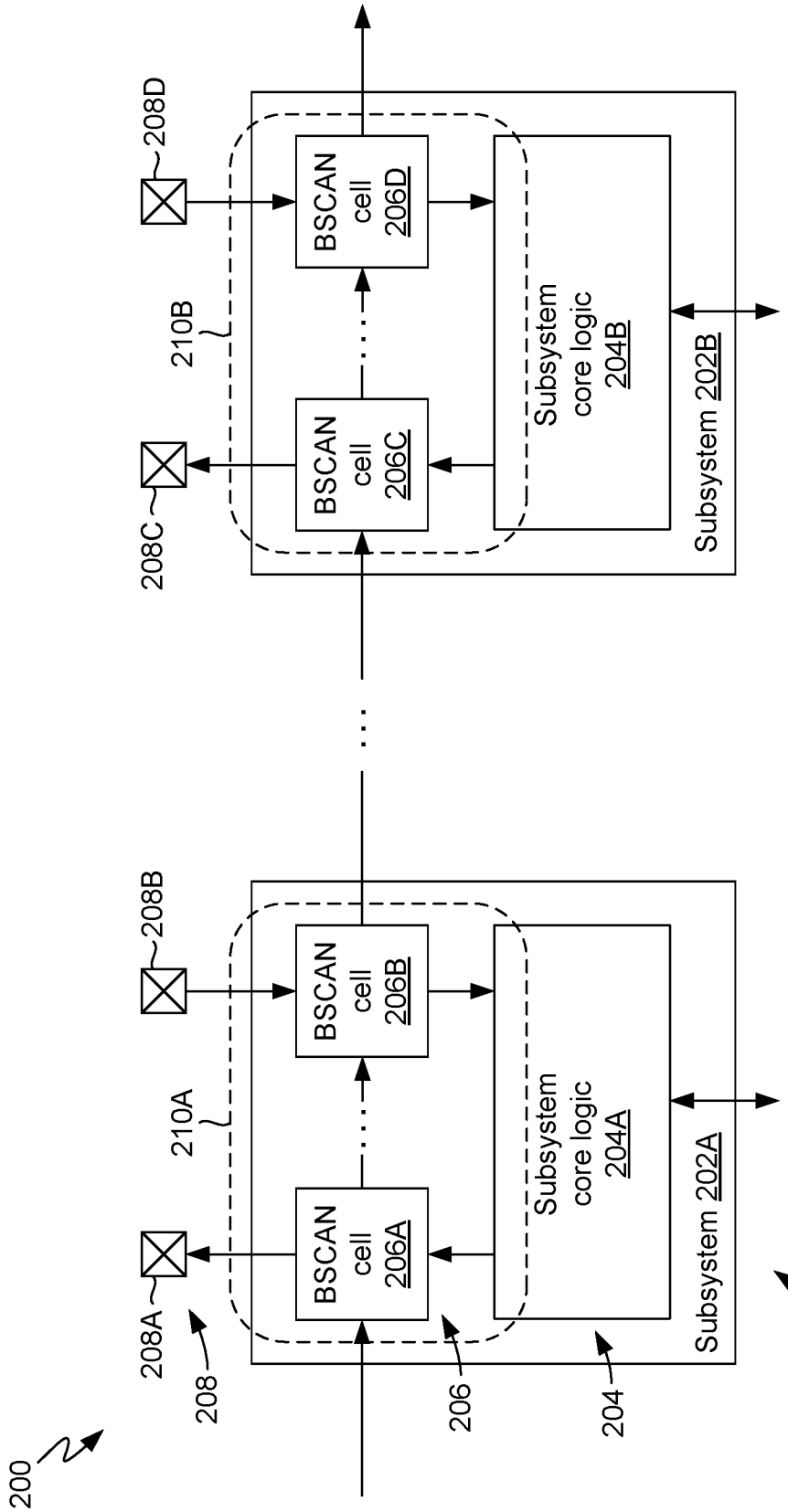

FIG. 2
(PRIOR ART)

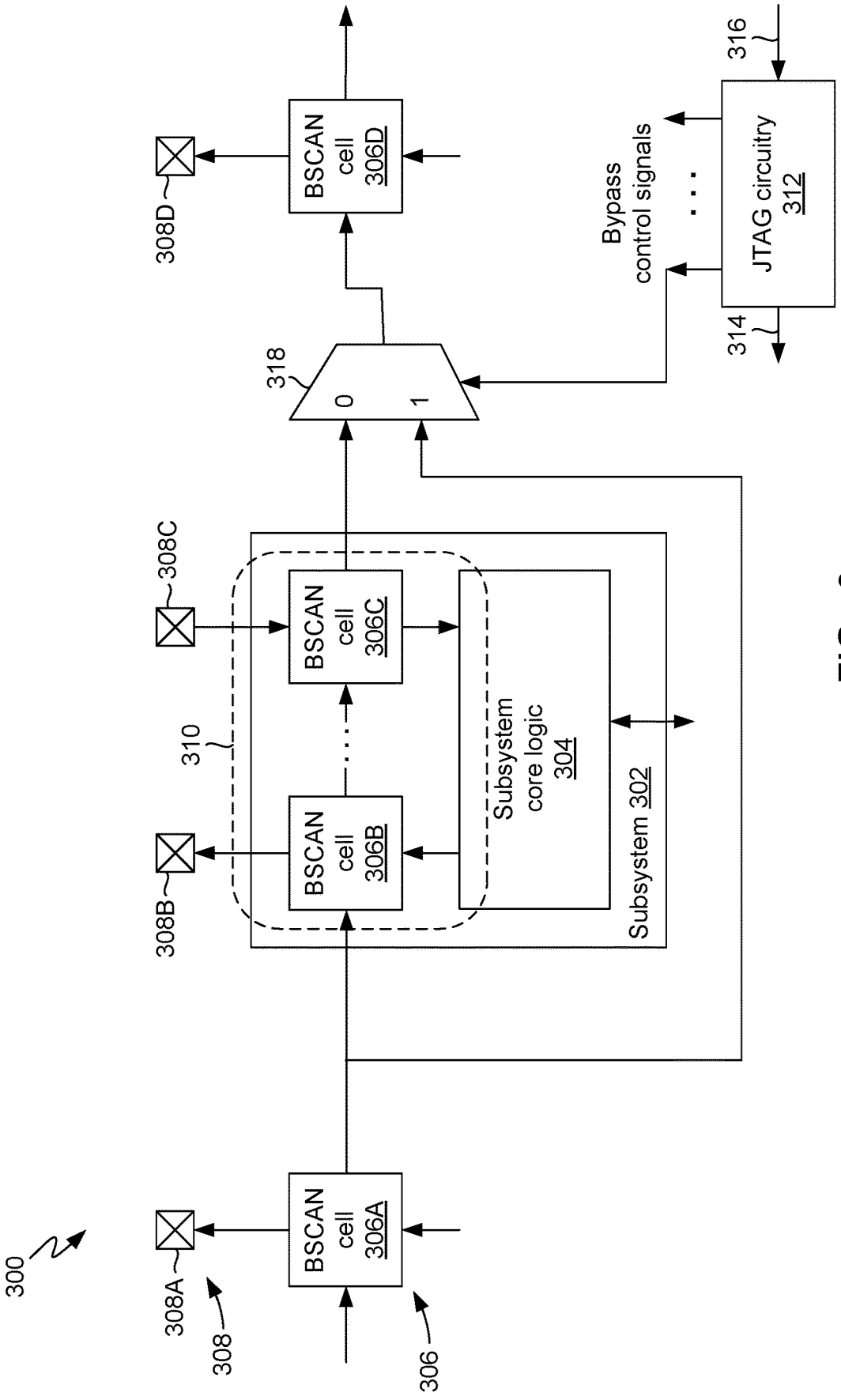
300
308A
308
306
BSCAN cell 306A
308B
BSCAN cell 306B
310
308C
BSCAN cell 306C
Subsystem core logic 304
Subsystem 302
308D
BSCAN cell 306D
318
0
1
Bypass control signals
JTAG circuitry 312
316
314

FIG. 3

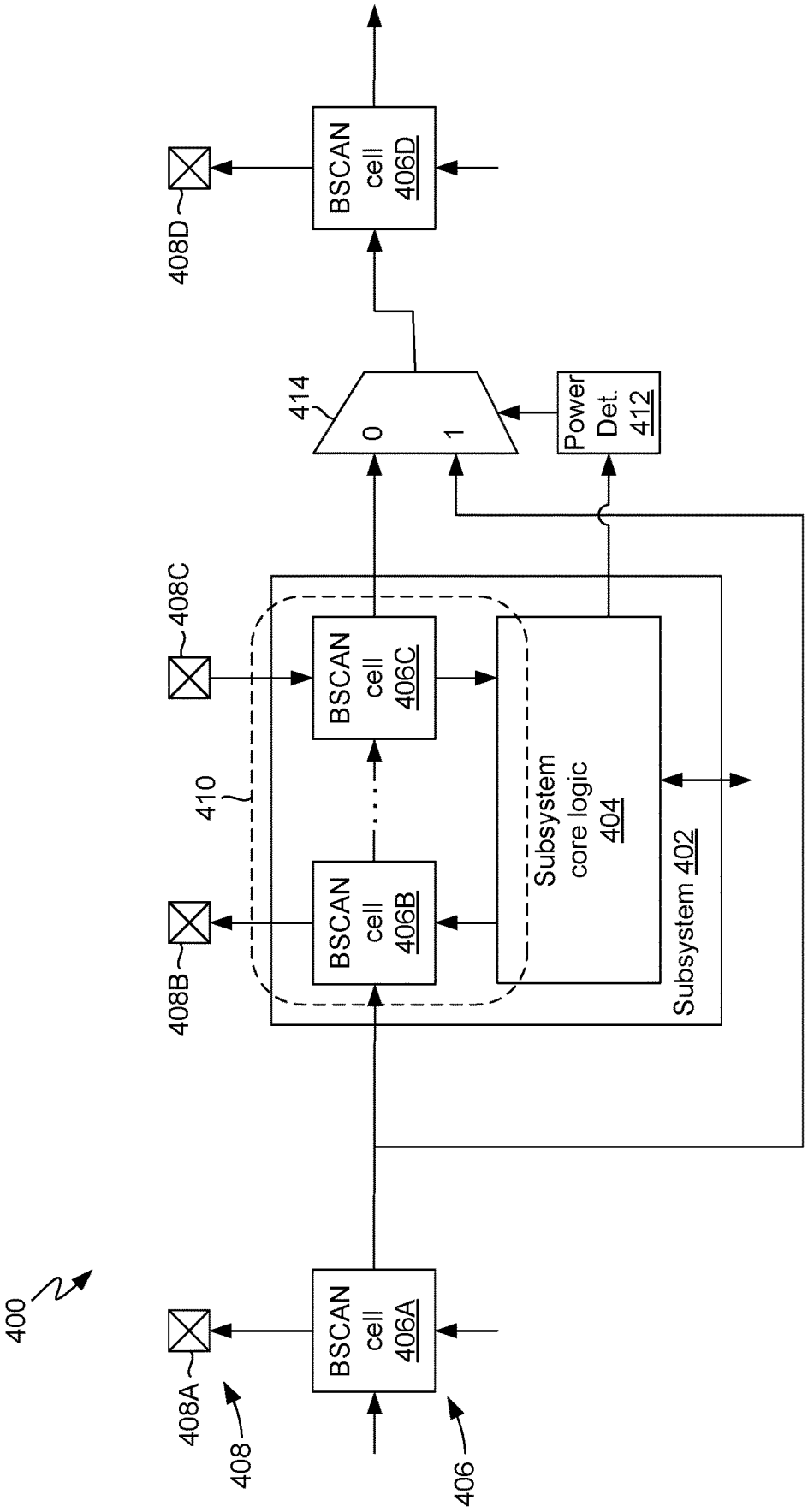
400
408A
408
406
BSCAN cell 406A
408B
BSCAN cell 406B
410
408C
BSCAN cell 406C
Subsystem core logic 404
Subsystem 402
414
0
1
Power Det. 412
408D
BSCAN cell 406D

FIG. 4

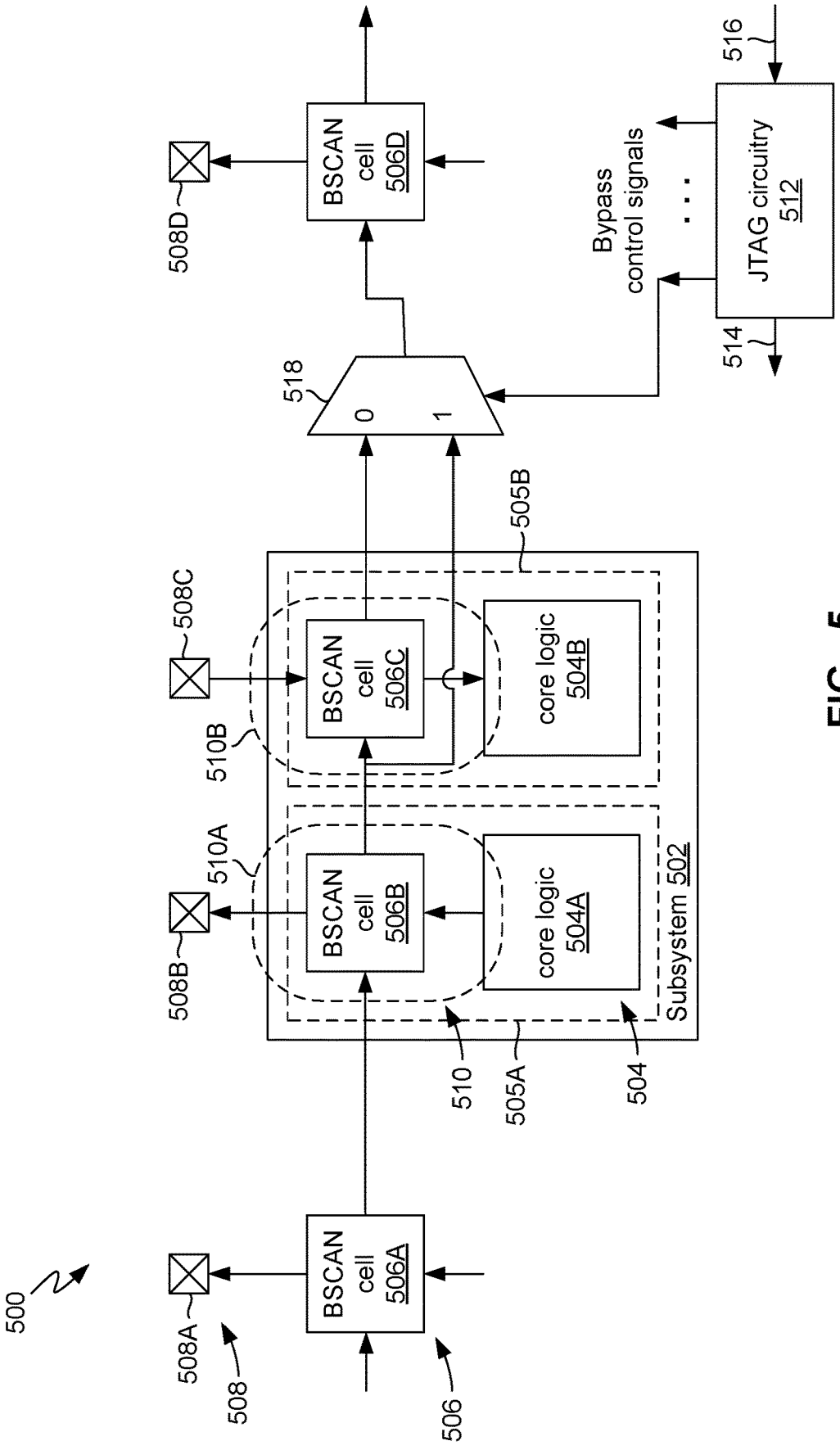
500
508A
508
506
BSCAN cell 506A
508B
510A
BSCAN cell 506B
core logic 504A
Subsystem 502
510
505A
504
508C
510B
BSCAN cell 506C
core logic 504B
505B
508D
BSCAN cell 506D
518
0
1
Bypass control signals
JTAG circuitry 512
514
516

FIG. 5

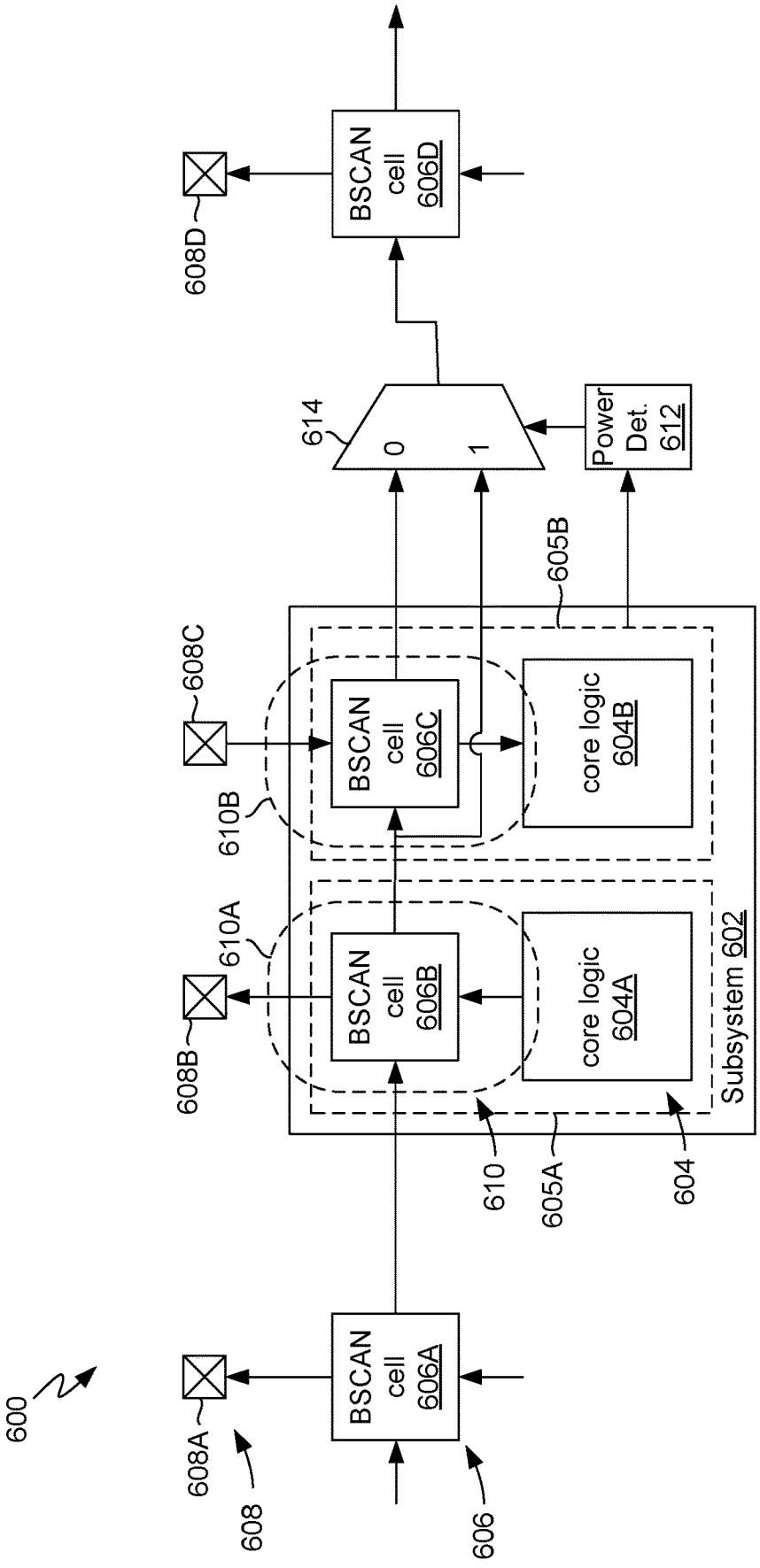
600
608A
608
606
BSCAN cell 606A
608B
610A
BSCAN cell 606B
core logic 604A
608C
610B
BSCAN cell 606C
core logic 604B
Subsystem 602
610
605A
604
605B
614
0
1
Power Det. 612
608D
BSCAN cell 606D

FIG. 6

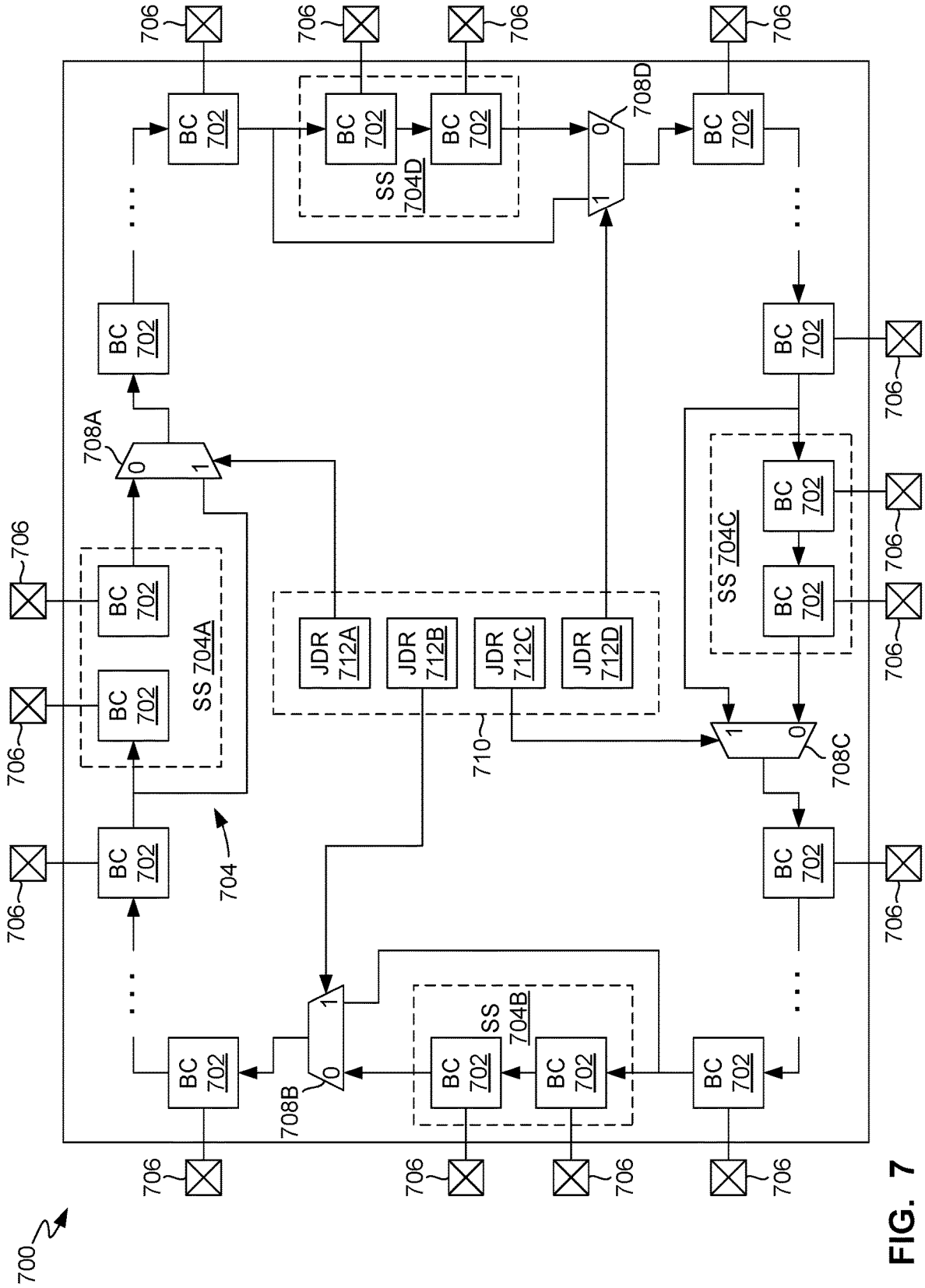
700
704
706
BC 702
SS 704A
SS 704B
SS 704C
SS 704D
708A
708B
708C
708D
710
JDR 712A
JDR 712B
JDR 712C
JDR 712D
0
1

FIG. 7

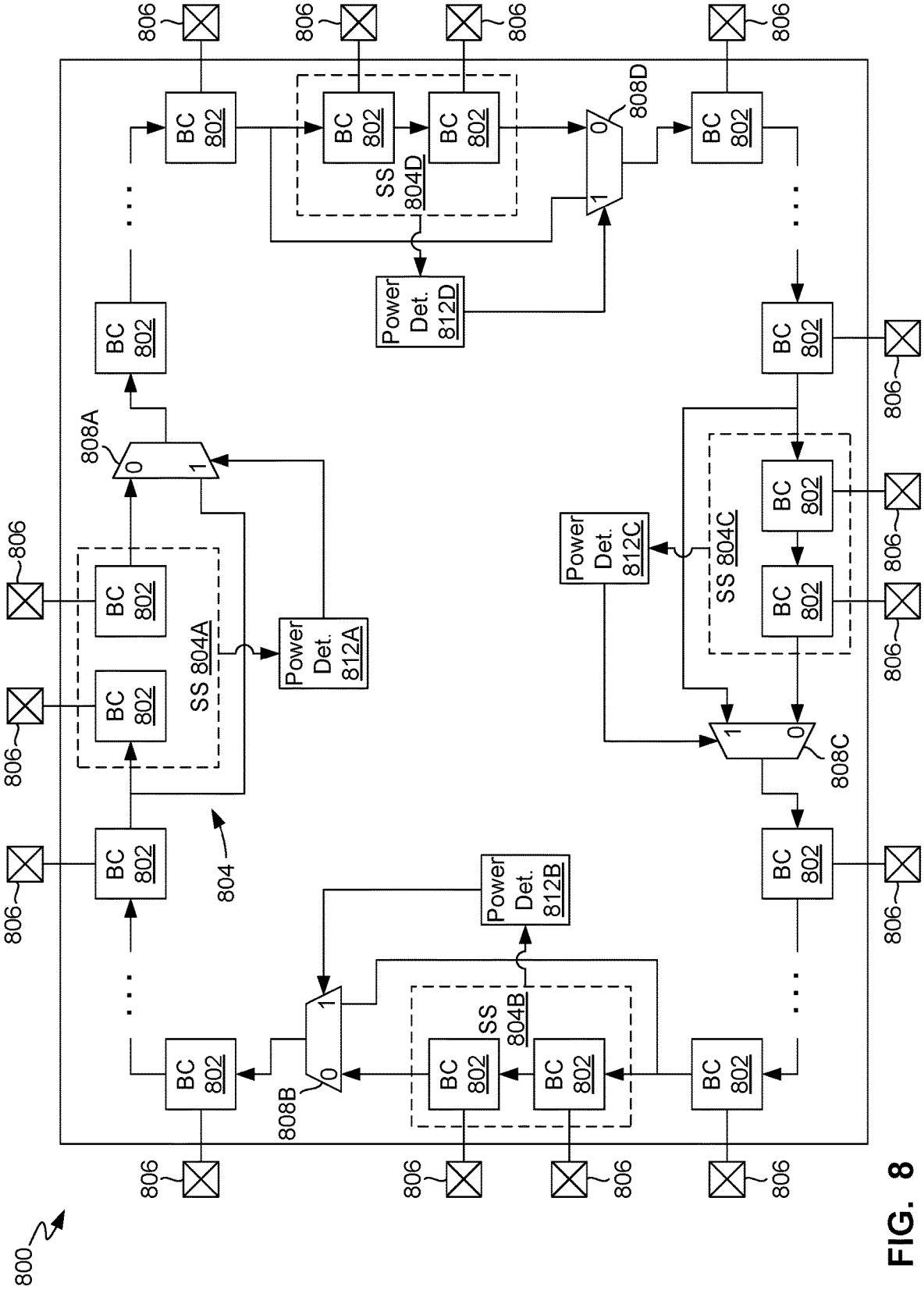
800
806
BC 802
SS 804A
SS 804B
SS 804C
SS 804D
804
808A
808B
808C
808D
Power Det. 812A
Power Det. 812B
Power Det. 812C
Power Det. 812D
0
1

FIG. 8

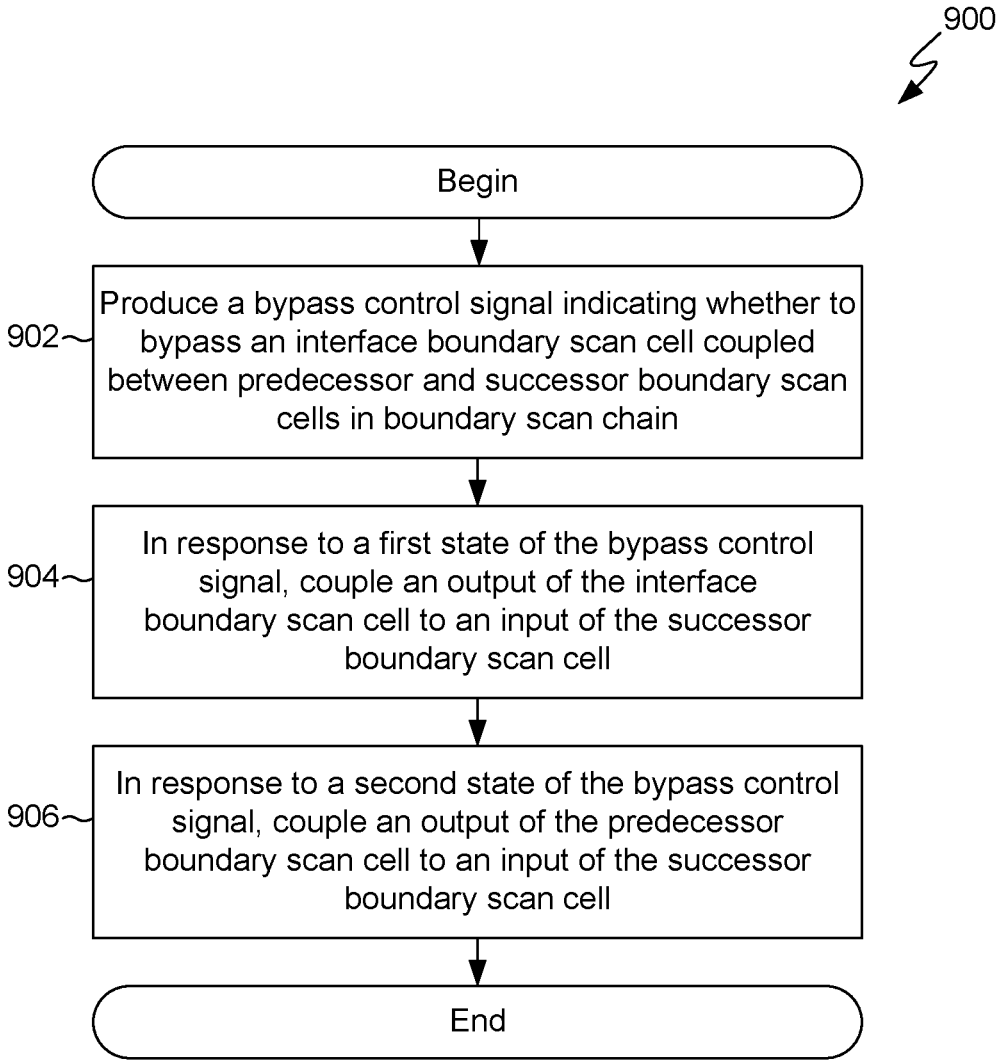
900
Begin
Produce a bypass control signal indicating whether to bypass an interface boundary scan cell coupled between predecessor and successor boundary scan cells in boundary scan chain
902
In response to a first state of the bypass control signal, couple an output of the interface boundary scan cell to an input of the successor boundary scan cell
904
In response to a second state of the bypass control signal, couple an output of the predecessor boundary scan cell to an input of the successor boundary scan cell
906
End

FIG. 9

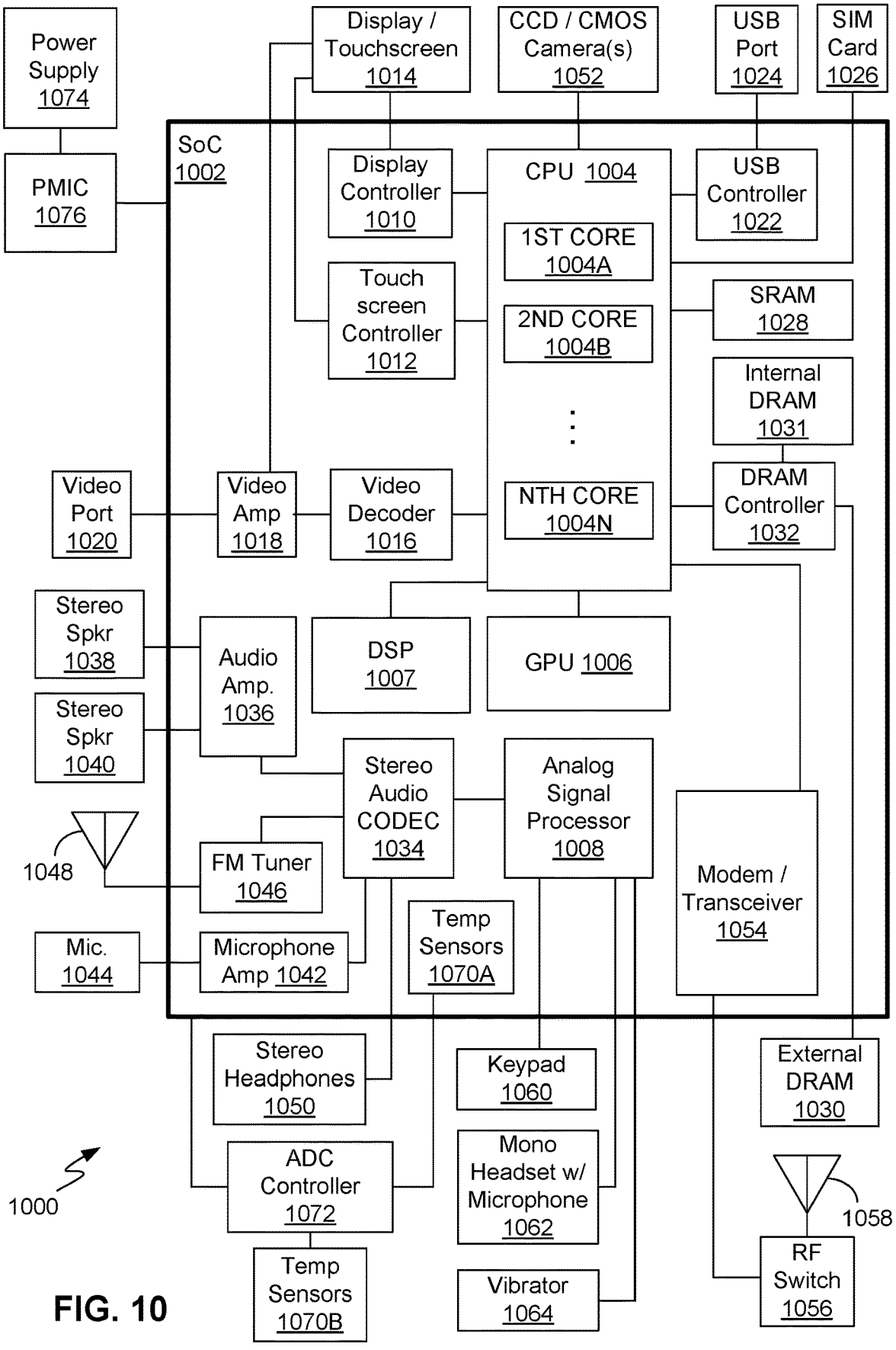
Power Supply 1074
PMIC 1076
SoC 1002
Display / Touchscreen 1014
CCD / CMOS Camera(s) 1052
USB Port 1024
SIM Card 1026
Display Controller 1010
CPU 1004
1ST CORE 1004A
2ND CORE 1004B
NTH CORE 1004N
USB Controller 1022
Touch screen Controller 1012
SRAM 1028
Internal DRAM 1031
DRAM Controller 1032
Video Port 1020
Video Amp 1018
Video Decoder 1016
Stereo Spkr 1038
Stereo Spkr 1040
Audio Amp. 1036
DSP 1007
GPU 1006
Stereo Audio CODEC 1034
Analog Signal Processor 1008
1048
FM Tuner 1046
Modem / Transceiver 1054
Mic. 1044
Microphone Amp 1042
Temp Sensors 1070A
Stereo Headphones 1050
Keypad 1060
External DRAM 1030
ADC Controller 1072
Mono Headset w/ Microphone 1062
1000
1058
Temp Sensors 1070B
Vibrator 1064
RF Switch 1056

FIG. 10

POWER-COLLAPSIBLE BOUNDARY SCAN

DESCRIPTION OF THE RELATED ART

Portable computing devices ("PCD"s) are becoming necessities for people on personal and professional levels. These devices may include mobile phones, tablet computers, palmtop computers, portable digital assistants ("PDA"s), portable game consoles, and other portable electronic devices. PCDs commonly contain integrated circuits or systems-on-a-chip ("SoC"s) that include numerous subsystems designed to work together to deliver functionality to a user. For example, an SoC may contain any number of processing engines or other subsystems, such as central processing units ("CPU"s) with multiple cores, graphical processing units ("GPU"s), digital signal processors ("DSP"s), wireless transceiver units (also referred to as modems), etc. An SoC may also include peripheral device interfaces, such as one or more Universal Serial Bus ("USB") interfaces. In addition to one or more SoCs, a PCD may include components such as memory chips, power management chips, audio amplifiers, microphones, speakers, cameras, etc. Each such component has pins that may be soldered to lands or pads on a printed circuit board ("PCB"). The PCB has electrically conductive (e.g., copper) traces that provide signal paths between the pads, and thus between pins of the various chips and other components.

An SoC subsystem may include off-chip interface circuitry, also referred to as a physical interface or PHY, which interfaces the core logic of a subsystem to associated SoC signal pins. In addition to the signal pins, an SoC may include power supply pins through which the physical interfaces may receive the power needed for their operation.

Although an SoC or similar chip may have many subsystems, a PCD may not utilize all of their physical interfaces. The power supply pins associated with unused interfaces may be tied to ground to help minimize leakage current and thereby conserve battery power.

Boundary scan is a testing technology developed by the Joint Test Action Group ("JTAG"), an industry consortium. A chip, such as an SoC, may include JTAG circuitry that enables signals on individual pins to be input and output in a test mode. A circuit element known as a boundary scan "cell" in the physical interface is interposed in the input/output data signal path between subsystem core logic and the corresponding signal pin. The boundary scan cells are arranged in a chain to form a serial scan path. The JTAG circuitry enables the boundary scan cells to be written to and read back by shifting test data serially through the chain of cells. Such a boundary scan test feature can be used not only to test a chip but also to test the integrity of the signal paths or traces between chips on a PCB.

SUMMARY OF THE DISCLOSURE

Systems, methods, computer program products, and other embodiments are disclosed for selectively bypassing off-chip interfaces in a boundary scan chain of an integrated circuit chip.

An exemplary method for selectively bypassing off-chip interfaces in a boundary scan chain of an integrated circuit chip may include producing a bypass control signal indicating whether to bypass an interface boundary scan cell coupled between a predecessor boundary scan cell and a successor boundary scan cell in the boundary scan chain. The method may further include coupling, in response to a first state of the bypass control signal, an output of the interface boundary scan cell to an input of the successor boundary scan cell. The method may also include coupling, in response to a second state of the bypass control signal, an output of the predecessor boundary scan cell to an input of the successor boundary scan cell.

An exemplary system for selectively bypassing off-chip interfaces in a boundary scan chain of an integrated circuit chip may include an interface boundary scan cell in the boundary scan chain, a predecessor boundary scan cell preceding the interface boundary scan cell in the boundary scan chain, and a successor boundary scan cell succeeding the interface boundary scan cell in the boundary scan chain. The system may further include a multiplexer having a first input coupled to an output of the interface boundary scan cell, a second input coupled to an output of the predecessor boundary scan cell, and an output coupled to an input of the successor boundary scan cell. The output of the predecessor boundary scan cell may be coupled to an input of the interface boundary scan cell. The system may also include bypass control logic configured to produce a bypass control signal controlling whether the multiplexer selects the first input or the second input.

Another exemplary system for selectively bypassing off-chip interfaces in a boundary scan chain of an integrated circuit chip may include a plurality of subsystem off-chip interfaces. Each subsystem off-chip interface may be included in one of a corresponding plurality of power domains of the integrated circuit chip. Each subsystem off-chip interface may include at least one of the interface boundary scan cells of the boundary scan chain. The system may further include a plurality of multiplexers, each of which may be associated with one of the subsystem off-chip interfaces. Each multiplexer may have a first input coupled to an output of the interface boundary scan cell, a second input coupled to an output of a predecessor boundary scan cell preceding the interface boundary scan cell in the boundary scan chain, and an output coupled to an input of a successor boundary scan cell succeeding the interface boundary scan cell in the boundary scan chain. The output of the predecessor boundary scan cell may be further coupled to an input of the interface boundary scan cell. The system may also include bypass control logic configured to produce a plurality of bypass control signals, each controlling whether a corresponding one of the plurality of multiplexers selects the first input or the second input.

Still another system for selectively bypassing off-chip interfaces in a boundary scan chain of an integrated circuit chip may include means for producing a bypass control signal indicating whether to bypass an interface boundary scan cell coupled between a predecessor boundary scan cell and a successor boundary scan cell in the boundary scan chain. The system may further include means for coupling, in response to a first state of the bypass control signal, an output of the interface boundary scan cell to an input of the successor boundary scan cell. The system may also include means for coupling, in response to a second state of the bypass control signal, an output of the predecessor boundary scan cell to an input of the successor boundary scan cell.

BRIEF DESCRIPTION OF THE DRAWINGS

In the Figures, like reference numerals refer to like parts throughout the various views unless otherwise indicated. For reference numerals with letter character designations such as "102A" or "102B", the letter character designations may differentiate two like parts or elements present in the same Figure. Letter character designations for reference numerals

may be omitted when it is intended that a reference numeral to encompass all parts having the same reference numeral in all Figures.

FIG. **1** is a block diagram illustrating an integrated circuit chip having a boundary scan chain, in accordance with the prior art.

FIG. **2** is a block diagram illustrating a portion of a boundary scan chain of an integrated circuit chip, in accordance with the prior art.

FIG. **3** is a block diagram illustrating a system for selectively bypassing off-chip interfaces in a boundary scan chain, in accordance with exemplary embodiments.

FIG. **4** is a block diagram illustrating another system for selectively bypassing off-chip interfaces in a boundary scan chain, in accordance with exemplary embodiments.

FIG. **5** is a block diagram illustrating still another system for selectively bypassing off-chip interfaces in a boundary scan chain, in accordance with exemplary embodiments.

FIG. **6** is a block diagram illustrating yet another system for selectively bypassing off-chip interfaces in a boundary scan chain, in accordance with exemplary embodiments.

FIG. **7** is a block diagram illustrating a chip having selectively bypassable off-chip interfaces, in accordance with the prior art.

FIG. **8** is a block diagram illustrating another chip having selectively bypassable off-chip interfaces, in accordance with the prior art.

FIG. **9** is a flow diagram illustrating a method for selectively bypassing off-chip interfaces in a boundary scan chain, in accordance with exemplary embodiments.

FIG. **10** is a block diagram of a computing device, in accordance with exemplary embodiments.

DETAILED DESCRIPTION

The word "exemplary" is used herein to mean "serving as an example, instance, or illustration." The word "illustrative" may be used herein synonymously with "exemplary." Any aspect described herein as "exemplary" is not necessarily to be construed as preferred or advantageous over other aspects. The term "coupled" is used herein to mean connected via zero or more intervening elements. The term "directly connected" may be used herein to mean connected via zero intervening elements.

As illustrated in FIG. **1**, a conventional or prior art integrated circuit chip **100** may include a boundary scan feature in accordance with the testing standard known as Institute of Electrical and Electronic Engineers ("IEEE") standard 1149.1: Standard Test Access Port and Boundary Scan Architecture. The boundary scan feature and standard are also commonly referred to as "JTAG" boundary scan, a reference to the Joint Test Action Group whose findings and recommendations were used as the basis for IEEE standard 1149.1.

The boundary scan feature is based on a boundary scan chain **102**, sometimes also referred to as a boundary scan register ("BSR"). The boundary scan chain **102** may comprise any number of boundary scan ("BSCAN") cells **104** arranged in a chain. That is, a scan chain input of one of the boundary scan cells **104** is coupled to a scan chain output of another of the boundary scan cells **104**. Boundary scan testing is controlled by JTAG circuitry **106**, which is commonly interposed between the first and last boundary scan cells **104** in the boundary scan chain **102**. Each boundary scan cell **102** is interposed in an input/output (i.e., input, output, or bidirectional) data signal path between system core logic **108** and a respective or associated signal pin **110** of the chip **100**. The system core logic **108** may also be referred to as application logic, as it represents the logic that effects the application(s) or mission-mode function(s) of the chip **100**, as opposed to testing or diagnostic functions. Although only the signal pins **110** are shown in FIG. **1** for purposes of clarity, the chip **100** includes additional pins through which the chip **100** may be supplied with power, as well as pins that may be connected to ground.

Each boundary scan cell **104** is configured not only to transparently buffer data communicated between the system core logic **108** and the associated pin **110** but also to capture the logic state or data value on the associated pin **110**. Thus, in addition to a scan chain input connection and a scan chain output connection, each boundary scan cell **104** has two input/output data connections, one connected to the system core logic **108** and the other connected to the associated pin **110**.

The JTAG circuitry **106** enables the boundary scan chain **102** to be written to and read back by shifting test data serially through its constituent boundary scan cells **104**. As the boundary scan cells **104** reflect the data values on the associated pins **110**, the data values on the associated pins **110** may be read or output by shifting the data serially through the boundary scan cells **104** and then out of the chip **100** through a pin **110** commonly referred to as test data out ("TDO"). Similarly, as the boundary scan cells **104** can set or establish data values on the associated pins **110**, the data values on the associated pins **110** may be set or input by shifting the data serially into the chip **100** through a pin **110** commonly referred to as test data out ("TDI") and then through the boundary scan cells **104**. With respect to the direction in which data values are shifted through the boundary scan chain **102**, a first boundary scan cell **104** having an output coupled to an input of a second boundary scan cell **104** may be referred to as a "predecessor" of the second boundary scan cell **104**, and the second boundary scan cell **104** may be referred to as a "successor" of the first boundary scan cell **104**. The JTAG circuitry **106** may shift the data using a clock signal provided through a corresponding test clock ("TCK") pin **110**. Whether the JTAG circuit **106** reads data from the chip **100** or writes data to the chip **100** in the above-described manner may be determined by a mode signal provided through a corresponding test mode select ("TMS") pin **110**. The boundary scan cells **104** are included on the same die **112** as the system core logic **108**, the JTAG circuitry **106**, and other elements of the chip **100**.

As illustrated in FIG. **2**, a chip **200** having an architecture that is a variant of the above-described architecture of the chip **100** (FIG. **1**) may include two or more subsystems **202**, such as subsystems **202**A, **202**B, etc., instead of, or in addition to, above-described system core logic **108** (FIG. **1**). Further subsystems **202** that may be included but are not individually shown for purposes of clarity are indicated by the ellipsis symbol (" . . . ") between the subsystems **202**A and **202**B. The subsystems **202** may include subsystem core logic **204**. For example, the subsystems **202**A and **202**B may include core logic **204**A and **204**B, respectively. Although not shown for purposes of clarity, the various subsystems **202** may communicate with each other or with other elements of the chip **200** via one or more internal busses or interconnects, as conceptually indicated by the double-ended arrows. The chip **200** may include signal pins **208**, such as pins **208**A, **208**B, **208**C, **208**D, etc., as well as power supply and ground pins (not shown).

In the architecture shown in FIG. **2**, a boundary scan chain may include boundary scan cells **206**, such as boundary scan cells **206**A, **206**B, **206**C, **206**D, etc. Boundary scan cells

206A and 206B may be interposed between subsystem core logic 204A and pins 208A and 208B, respectively. Boundary scan cells 206C and 206D may be interposed between subsystem core logic 204B and pins 208C and 208D, respectively. Further boundary scan cells 206 that may be included in the boundary scan chain but are not individually shown for purposes of clarity are indicated by the ellipsis symbol (" . . . ") between the boundary scan cells 206A and 206B, between the boundary scan cells 206B and 206C, and between the boundary scan cells 206C and 206D, etc. Note that for purposes of clarity in FIG. 2 only a portion of the entire boundary scan chain is shown, and JTAG circuitry that controls the boundary scan test is not shown. In the portion shown in FIG. 2, the scan chain output of the boundary scan cell 206A is connected to the scan chain input of the boundary scan cell 206B, the scan chain output of the boundary scan cell 206B is connected to the scan chain input of the boundary scan cell 206C, and the scan chain output of the boundary scan cell 206C is connected to the input of the boundary scan cell 206D. In the chip 200, the boundary scan feature may operate in essentially the same manner as described above with regard to the chip 100 (FIG. 1). That is, JTAG circuitry may shift data values through the boundary scan cells 206A-206D as well as all other boundary scan cells 206 that form the boundary scan chain.

A portion of the subsystem 202 that includes one or more boundary scan cells 206 as well as a portion of the associated subsystem core logic 204 may be referred to as an off-chip interface 210 (sometimes also referred to as a physical interface or "PHY") because it carries data signals between the pins 208 and the remaining portions of the subsystem core logic 204. For example, the subsystems 202A and 202B may include off-chip interfaces 210A and 210B, respectively. Although for purposes of clarity only the pins 110 that carry data signals are shown in FIG. 2, the chip 100 includes additional pins through which the chip 200 may be supplied with power.

Although a chip may have many subsystems, a computing device of which the chip is a part may not utilize all of their off-chip interfaces. For example, there may be six off-chip camera interfaces to accommodate up to six cameras, yet an original equipment manufacturer or "OEM" may design a computing device having only two cameras, each coupled to a respective camera interface. That is, some of the camera interfaces may be unused. The power supply voltage (and ground) pins associated with the other four, unused camera interfaces may be tied to ground to help minimize leakage current and thereby conserve battery power, or the power domain supplying the interface may be collapsed (i.e., deactivated) in some other manner. Data cannot be shifted through a boundary scan cell that is not powered. Embodiments described below of systems and methods for selectively bypassing off-chip interfaces in a boundary scan chain address this deficiency in the prior art.

As illustrated in FIG. 3, a chip 300 may include one or more subsystems 302, each having subsystem core logic 304. The chip 300 may be, for example, an SoC having numerous subsystems 302 and power domains. Although not shown for purposes of clarity, each subsystem 302 may communicate with other subsystems 302 of the chip 300 through, for example, one or more internal busses or similar data communication interconnects. The chip 300 may include signal pins 308, such as pins 308A, 308B, 308C, 308D, etc., as well as power supply and ground pins (not shown).

The chip 300 may have a boundary scan chain that includes boundary scan cells 306, such as boundary scan cells 306A, 306B, 306C, 306D, etc. The boundary scan cells 306B and 306C are interposed in input/output data signal paths between the subsystem core logic 304 and respective or associated signal pins 308B and 308C. Although any boundary scan cell 306 may be configured as an input, output or bidirectional data buffer, in the illustrated example: the boundary scan cell 306B may be configured as an output buffer, i.e., to buffer data provided by the subsystem core logic 304 to the pin 308B; and the boundary scan cell 306C may be configured as an input buffer, i.e., to buffer data provided by the pin 308C to the subsystem core logic 304. The boundary scan cells 306A and 306D may similarly be configured as output buffers in the illustrated example.

A physical interface or off-chip interface 310 includes boundary scan cells 306B, 306C, etc., as well as a portion of the associated subsystem core logic 304. The off-chip interface 310 may be, for example, a multi-lane serial interface, a USB interface, a PCIe interface, or any other type of interface not inconsistent with the present disclosure.

In the portion of the boundary scan chain shown in FIG. 3, the scan chain output of the boundary scan cell 306A is connected to the scan chain input of the boundary scan cell 306B, the scan chain output of the boundary scan cell 306B is connected to the scan chain input of the boundary scan cell 306C, and the scan chain output of the boundary scan cell 306C is connected to the scan chain input of the boundary scan cell 306D. In the illustrated example, while boundary scan cells 306B and 306C are associated with subsystem 302 and subsystem core logic 304, boundary scan cells 306A and 306D may be associated with other subsystems or core logic (not separately shown in FIG. 3 for purposes of clarity).

The chip 300 may include JTAG circuitry 312 that is configured to control the boundary scan cells 306 and thus control a boundary scan test in a conventional manner. Accordingly, first and last boundary scan cells 306 (not separately indicated for purposes of clarity) may be coupled to a scan chain output 314 and scan chain input 316, respectively, of the JTAG circuitry 312. As described below, the JTAG circuitry 312 is not only configured to control a boundary scan test but is also configured as bypass control logic to selectively control bypassing off-chip interfaces 310 in the boundary scan chain.

The subsystem 302 or a portion thereof, such as the off-chip interface 310, may be supplied with the power necessary for it to operate through a power domain that is different or distinct from one or more other power domains through which one or more other subsystems 302 (not shown in FIG. 3 for purposes of clarity) are supplied with power. The power domain supplying the subsystem 302 or its off-chip interface 310 may be powered through the above-mentioned one or more power supply voltage pins.

It may be noted that if the subsystem 302 is not supplied with power, the off-chip interface 310 is not operational, including the associated boundary scan cells 306B, 306C, etc. If the subsystem 302 is not supplied with power, the boundary scan chain is interrupted, and a conventional boundary scan test involving the off-chip interface 310 cannot be performed. Bypassing or excluding unpowered off-chip interfaces 310 from the boundary scan chain in a manner described below maintains the ability to perform a boundary scan test involving other (powered) off-chip interfaces 310.

The chip 300 may further include one or more multiplexers 318, each of which may be associated with one of the off-chip interfaces 310. In the embodiment illustrated in FIG. 3: a first input of the multiplexer 318 is directly connected to the scan chain output of the (interface) bound-

ary scan cell **306**C of the interface **310**; a second input of the multiplexer **318** is directly connected to the scan chain output of the (predecessor) boundary scan cell **306**A (i.e., which precedes the boundary scan cell **306**C in the boundary scan chain); and the output of the multiplexer **318** is directly connected to a scan chain input of the (successor) boundary scan cell **306**D (i.e., which succeeds or follows the boundary scan cell **306**C in the boundary scan chain).

In the embodiment illustrated in FIG. **3**, the JTAG circuitry **312** is configured to produce one or more bypass control signals, each coupled to the selector input of a respective multiplexer **318**. The bypass control signals may reflect the contents of a data register (not separately shown) in the JTAG circuitry **312**. As well understood by one of ordinary skill in the art, some of the JTAG signals described above with regard to FIG. **1** (e.g., TMS, TCK, TDI) can be used to write a value to such a JTAG data register.

In response to a bypass control signal, the multiplexer **318** selects one of its above-referenced first and second inputs. For example, in response to the bypass control signal having a value of "0" the multiplexer **318** may select its first input to couple to its output, and in response to the bypass control signal having a value of "1" the multiplexer **318** may select its second input to couple to its output. In the embodiment illustrated in FIG. **3**, if the bypass control signal has a value of "0" the multiplexer **318** does not bypass or exclude the boundary scan cells **306**B, **306**C, etc., of the interface **310** from the boundary scan chain but rather passes the signal from the boundary scan cell **306**C to the boundary scan cell **306**D. In the embodiment illustrated in FIG. **3**, if the bypass control signal has a value of "1" the multiplexer **318** passes the signal from the boundary scan cell **306**A to the boundary scan cell **306**D, effectively bypassing or excluding the boundary scan cells **306**B, **306**C, etc., of the interface **310** from the boundary scan chain. In summary, the multiplexer **318** is configured in the embodiment illustrated in FIG. **3** to selectively bypass the off-chip interface **310** in response to a bypass control (i.e., selection) signal provided by a JTAG data register of the JTAG circuitry **312**. In the embodiment illustrated in FIG. **3**, the multiplexer **318** is configured to bypass not only the boundary scan cell **306**C to which it is directly connected but also any number of additional boundary scan cells **306**B, etc., that may be included in the off-chip interface **310**.

More generally, in other embodiments, the first input of such a multiplexer may be coupled to the scan chain output of any interface boundary scan cell, i.e., any boundary scan cell of the associated off-chip interface. The second input of such a multiplexer may be coupled to the scan chain output of any other boundary scan cell of the off-chip interface that precedes that interface boundary scan cell in the boundary scan chain, or still more generally, to the scan chain output of any predecessor boundary scan cell, i.e., any boundary scan cell that precedes that interface boundary scan cell in the boundary scan chain. That is, in such other embodiments (not shown) there may be any number of intervening boundary scan cells between an interface boundary scan cell and a predecessor boundary scan cell, and any such intervening boundary scan cells are also predecessor boundary scan cells of the interface boundary scan cell. Further, in such other embodiments the output of the multiplexer may be coupled to the scan chain input of any successor boundary scan cell, i.e., any boundary scan cell that succeeds or follows the interface boundary scan cell in the boundary scan chain. That is, in such other embodiments (not shown) there may be any number of intervening boundary scan cells between an interface boundary scan cell and a successor boundary scan cell, and any such intervening boundary scan cells are also successor boundary scan cells of the interface boundary scan cell. It may be noted that in such other embodiments the boundary scan output of the predecessor boundary scan cell is further coupled to the boundary scan input of the interface boundary scan cell.

Also, in such other embodiments (not shown), the multiplexer may be included in a selector circuit along with one or more other multiplexers or similar selector circuitry, and the selector circuit may be configured to bypass one or more boundary scan cells in response to one or more bypass control signals provided by the bypass control logic. Further, although in the illustrated embodiments the multiplexer has exactly two inputs, in other embodiments a multiplexer may have more than two inputs.

As illustrated in FIG. **4**, in another embodiment a chip **400** may include one or more subsystems **402**, each having subsystem core logic **404**. The chip **400** may be, for example, an SoC having numerous subsystems **402** and power domains. Although not shown for purposes of clarity, each subsystem **402** may communicate with other subsystems **402** of the chip **400** through, for example, one or more internal busses or similar data communication interconnects. The chip **400** may include signal pins **408**, such as pins **408**A, **408**B, **408**C, **408**D, etc., as well as power supply and ground pins (not shown).

The chip **400** may have a boundary scan chain that includes boundary scan cells **406**, such as boundary scan cells **406**A, **406**B, **406**C, **406**D, etc. The boundary scan cells **406**B and **406**C are interposed in input/output data signal paths between the subsystem core logic **404** and respective or associated signal pins **408**B and **408**C. Although any boundary scan cell **406** may be configured as an input, output or bidirectional data buffer, in the illustrated example: the boundary scan cell **406**B may be configured as an output buffer, i.e., to buffer data provided by the subsystem core logic **404** to the pin **408**B; and the boundary scan cell **406**C may be configured as an input buffer, i.e., to buffer data provided by the pin **408**C to the subsystem core logic **404**. The boundary scan cells **406**A and **406**D may similarly be configured as output buffers in the illustrated example.

A physical interface or off-chip interface **410** includes boundary scan cells **406**B, **406**C, etc., as well as a portion of the associated subsystem core logic **404**. The off-chip interface **410** may be, for example, a multi-lane serial interface, a USB interface, a PCIe interface, or any other type of interface not inconsistent with the present disclosure.

In the portion of the boundary scan chain shown in FIG. **4**, the scan chain output of the boundary scan cell **406**A is connected to the scan chain input of the boundary scan cell **406**B, the scan chain output of the boundary scan cell **406**B is connected to the scan chain input of the boundary scan cell **406**C, and the scan chain output of the boundary scan cell **406**C is connected to the scan chain input of the boundary scan cell **406**D. In the illustrated example, while boundary scan cells **406**B and **406**C are associated with subsystem **402** and subsystem core logic **404**, boundary scan cells **406**A and **406**D may be associated with other subsystems or core logic (not separately shown in FIG. **4** for purposes of clarity).

Although not shown in FIG. **4** for purposes of clarity, the chip **400** may include JTAG circuitry that is configured to control the boundary scan cells **406** and thus control a boundary scan test in a conventional manner. Unlike in the embodiment described above with regard to FIG. **3**, in this embodiment the JTAG circuitry is not configured as bypass control logic. Rather, in this embodiment power signal detection logic **412** is included and configured as bypass

control logic to selectively control bypassing the off-chip interface **410** in a manner described below.

Similarly to the subsystem **302** described above with regard to FIG. **3**, the subsystem **402** may be supplied with the power necessary for to operate through a power domain that is different or distinct from one or more other power domains through which one or more other subsystems **402** (not shown in FIG. **4** for purposes of clarity) are supplied with power. The power domain supplying the subsystem **402** or its off-chip interface **410** may be powered through the above-mentioned one or more power supply voltage pins.

The chip **400** may further include one or more multiplexers **414**, each of which may be associated with one of the off-chip interfaces **410**. In the embodiment illustrated in FIG. **3**: a first input of the multiplexer **414** is directly connected to the scan chain output of the (interface) boundary scan cell **406**C; a second input of the multiplexer **414** is directly connected to the scan chain output of the (predecessor) boundary scan cell **406**A; and the output of the multiplexer **414** is directly connected to a scan chain input of the (successor) boundary scan cell **406**D.

In the embodiment illustrated in FIG. **4**, the power signal detection logic **412** is configured to detect, and to produce a signal indicating, whether the power domain that is configured to supply power to the subsystem **402** or portion thereof (e.g., off-chip interface **410**) is powered, i.e., is receiving power through, for example, a power supply pin. This signal indicating whether the power domain is powered serves as a bypass control signal in this embodiment and is accordingly coupled to the selector input of the multiplexer **412**.

In response to the bypass control signal, the multiplexer **412** selects one of its above-referenced first and second inputs. For example, in response to the bypass control signal having a value of "0" the multiplexer **412** may select its first input to couple to its output, and in response to the bypass control signal having a value of "1" the multiplexer **412** may select its second input to couple to its output. In the embodiment illustrated in FIG. **4**, if the bypass control signal has a value of "0" the multiplexer **412** does not bypass or exclude the boundary scan cells **406**B, **406**C, etc., of the interface **410** from the boundary scan chain but rather passes the signal from the (interface) boundary scan cell **406**C to the (successor) boundary scan cell **406**D. In the embodiment illustrated in FIG. **4**, if the bypass control signal has a value of "1" the multiplexer **412** passes the signal from the (predecessor) boundary scan cell **406**A to the (successor) boundary scan cell **406**D, effectively bypassing or excluding the boundary scan cells **406**B, **406**C, etc., of the interface **410** from the boundary scan chain. In summary, the multiplexer **412** is configured in the embodiment illustrated in FIG. **4** to selectively bypass the off-chip interface **410** in response to a bypass control (i.e., selection) signal provided by the power signal detection logic **412**. In the embodiment illustrated in FIG. **4**, the multiplexer **412** is configured to bypass not only the boundary scan cell **406**C to which it is directly connected but also any number of additional boundary scan cells **406**B, etc., that may be included in the off-chip interface **410**.

As illustrated in FIG. **5**, in yet another embodiment a chip **500** may include one or more subsystems **502**. In this embodiment, the core logic **504** of the subsystem **502** may be distributed, comprising core logic **504**A and **504**B. Core logic **504**A and **504**B may be in power domains **505**A and **505**B, respectively. As in other embodiments described above, the chip **500** may be an SoC having numerous subsystems **502** and power domains. The chip **500** may include signal pins **508**, such as pins **508**A, **508**B, **508**C, **508**D, etc., as well as power supply and ground pins (not shown).

The chip **500** may have a boundary scan chain that includes boundary scan cells **506**, such as boundary scan cells **506**A, **506**B, **506**C, **506**D, etc. The boundary scan cells **506**B and **506**C are interposed in input/output data signal paths between the subsystem core logic **504** and respective or associated signal pins **508**B and **508**C. Although any boundary scan cell **506** may be configured as an input, output or bidirectional data buffer, in the illustrated example: the boundary scan cell **506**B may be configured as an output buffer, i.e., to buffer data provided by the core logic **504**A to the pin **408**B; and the boundary scan cell **506**C may be configured as an input buffer, i.e., to buffer data provided by the pin **508**C to the core logic **504**B. The boundary scan cells **506**A and **506**D may similarly be configured as output buffers in the illustrated example.

In this embodiment, the subsystem **502** may have multiple physical or off-chip interfaces **510**, such as a first off-chip interface **510**A that includes boundary scan cell **506**B and a portion of the associated core logic **504**A, and a second off-chip interface **510**B that includes boundary scan cell **506**C and a portion of the associated core logic **504**B. Although not shown for purposes of clarity, the chip **500** may further include supply voltage pins through which power may be supplied to the subsystem **502** or portions thereof, such as the off-chip interfaces **510**A and **510**B. In this embodiment, one or more supply voltage pins may be configured to power off-chip interface **510**A (in power domain **505**A) and one or more other supply voltage pins may be configured to power off-chip interface **510**B (in power domain **505**B).

In the portion of the boundary scan chain shown in FIG. **5**, the scan chain output of the boundary scan cell **506**A is connected to the scan chain input of the boundary scan cell **506**B, the scan chain output of the boundary scan cell **506**B is connected to the scan chain input of the boundary scan cell **506**C, and the scan chain output of the boundary scan cell **506**C is connected to the scan chain input of the boundary scan cell **506**D. In the illustrated example, boundary scan cells **506**B and **506**C are associated with core logic **504**A and **504**B, respectively. Boundary scan cells **506**A and **506**D may be associated with other subsystems or core logic (not separately shown in FIG. **5** for purposes of clarity).

The chip **500** may include JTAG circuitry **512** that is configured to control the boundary scan cells **506** and thus control a boundary scan test in a conventional manner. Accordingly, first and last boundary scan cells **506** (not separately indicated for purposes of clarity) may be coupled to a scan chain output **514** and scan chain input **516**, respectively, of the JTAG circuitry **512**.

The chip **500** may further include one or more multiplexers associated with off-chip interfaces. For example, the multiplexer **518** may be associated with the off-chip interface **510**B by the following connections: a first input of the multiplexer **518** is directly connected to the scan chain output of the (interface) boundary scan cell **506**C; a second input of the multiplexer **518** is directly connected to the scan chain output of the (predecessor) boundary scan cell **506**B; and the output of the multiplexer **518** is directly connected to a scan chain input of the (successor) boundary scan cell **506**D.

Similarly to the embodiment described above with regard to FIG. **3**, the JTAG circuitry **512** is configured to produce one or more bypass control signals, each coupled to the selector input of a respective multiplexer **518**. The bypass

control signals may reflect the contents of a data register (not separately shown) in the JTAG circuitry **512**, as described above with regard to FIG. **3**.

In response to the bypass control signal, the multiplexer **518** selects one of its above-referenced first and second inputs. For example, in response to the bypass control signal having a value of "0" the multiplexer **518** may select its first input to couple to its output, and in response to the bypass control signal having a value of "1" the multiplexer **518** may select its second input to couple to its output. In the embodiment illustrated in FIG. **5**, if the bypass control signal has a value of "0" the multiplexer **518** does not bypass or exclude the boundary scan cell **506**C of the interface **510**B from the boundary scan chain but rather passes the signal from the (interface) boundary scan cell **506**C to the (successor) boundary scan cell **506**D. In the embodiment illustrated in FIG. **5**, if the bypass control signal has a value of "1" the multiplexer **518** passes the signal from the (predecessor) boundary scan cell **506**B to the (successor) boundary scan cell **506**D, effectively bypassing or excluding the (interface) boundary scan cell **506**C from the boundary scan chain, while maintaining the boundary scan cell **506**B in the boundary scan chain. In summary, in this embodiment the multiplexer **518** is configured to selectively bypass fewer than all of the off-chip interfaces **510** of the subsystem **502** in response to a bypass control (i.e., selection) signal provided by a JTAG data register of the JTAG circuitry **512**. Alternatively, in another embodiment (not shown) the multiplexer **518** could be configured to selectively bypass all of the off-chip interfaces **510**, similarly to the embodiments described above with regard to FIGS. **3-4**.

As illustrated in FIG. **6**, in still another embodiment a chip **600** may include one or more subsystems **602**. As in the embodiment described above with regard to FIG. **5**, in this embodiment the core logic **604** of the subsystem **602** may be distributed, comprising core logic **604**A and **604**B. Core logic **604**A and **604**B may be in power domains **605**A and **605**B, respectively. As in other embodiments described above, the chip **600** may be an SoC having numerous subsystems **602** and power domains. The chip **300** may include signal pins **308**, such as pins **308**A, **308**B, **308**C, **308**D, etc., as well as power supply and ground pins (not shown).

The chip **600** may have a boundary scan chain that includes boundary scan cells **606**, such as boundary scan cells **606**A, **606**B, **606**C, **606**D, etc. The boundary scan cells **606**B and **606**C are interposed in input/output data signal paths between the subsystem core logic **604** and respective or associated signal pins **608**B and **608**C. Although any boundary scan cell **606** may be configured as an input, output or bidirectional data buffer, in the illustrated example: the boundary scan cell **606**B may be configured as an output buffer, i.e., to buffer data provided by the core logic **604**A to the pin **608**B; and the boundary scan cell **606**C may be configured as an input buffer, i.e., to buffer data provided by the pin **608**C to the core logic **604**B. The boundary scan cells **606**A and **606**D may similarly be configured as output buffers in the illustrated example.

In this embodiment, the subsystem **602** may have multiple physical or off-chip interfaces **610**, such as a first off-chip interface **610**A that includes boundary scan cell **606**B and a portion of the associated core logic **604**A, and a second off-chip interface **610**B that includes boundary scan cell **606**C and a portion of the associated core logic **604**B. In this embodiment, one or more supply voltage pins may be configured to power off-chip interface **610**A (in power domain **605**A) and one or more other supply voltage pins may be configured to power off-chip interface **610**B (in power domain **605**B).

In the portion of the boundary scan chain shown in FIG. **6**, the scan chain output of the boundary scan cell **606**A is connected to the scan chain input of the boundary scan cell **606**B, the scan chain output of the boundary scan cell **606**B is connected to the scan chain input of the boundary scan cell **606**C, and the scan chain output of the boundary scan cell **606**C is connected to the scan chain input of the boundary scan cell **606**D. In the illustrated example, boundary scan cells **606**B and **606**C are associated with core logic **604**A and **604**B, respectively. Boundary scan cells **606**A and **606**D may be associated with other subsystems or core logic (not separately shown in FIG. **6** for purposes of clarity).

Although not shown in FIG. **6** for purposes of clarity, the chip **600** may include JTAG circuitry that is configured to control the boundary scan cells **606** and thus control a boundary scan test as described above with regard to other embodiments. Similarly to the embodiment described above with regard to FIG. **4**, in this embodiment power signal detection logic **612** is included and configured as bypass control logic to selectively control bypassing the off-chip interface **610**B in a manner described below.

The chip **600** may further include one or more multiplexers associated with off-chip interfaces. For example, the multiplexer **614** may be associated with the off-chip interface **610**B by the following connections: a first input of the multiplexer **614** is directly connected to the scan chain output of the (interface) boundary scan cell **506**C; a second input of the multiplexer **614** is directly connected to the scan chain output of the (predecessor) boundary scan cell **606**B; and the output of the multiplexer **614** is directly connected to a scan chain input of the (successor) boundary scan cell **606**D.

In the embodiment illustrated in FIG. **6**, the power signal detection logic **612** is configured to detect, and to produce a signal indicating, whether the power domain that is configured to supply power to the power domain **605**B or portion thereof (e.g., off-chip interface **610**B) is powered. This signal indicating whether the power domain is powered serves as a bypass control signal in this embodiment and is accordingly coupled to the selector input of the multiplexer **614**.

In response to the bypass control signal, the multiplexer **614** selects one of its above-referenced first and second inputs. For example, in response to the bypass control signal having a value of "0" the multiplexer **614** may select its first input to couple to its output, and in response to the bypass control signal having a value of "1" the multiplexer **614** may select its second input to couple to its output. In the embodiment illustrated in FIG. **6**, if the bypass control signal has a value of "0" the multiplexer **614** does not bypass or exclude the boundary scan cell **606**C of the interface **610**B from the boundary scan chain but rather passes the signal from the (interface) boundary scan cell **606**C to the (successor) boundary scan cell **606**D. In the embodiment illustrated in FIG. **6**, if the bypass control signal has a value of "1" the multiplexer **614** passes the signal from the (predecessor) boundary scan cell **606**B to the (successor) boundary scan cell **606**D, effectively bypassing or excluding the (interface) boundary scan cell **606**C from the boundary scan chain, while maintaining the boundary scan cell **606**B in the boundary scan chain. In summary, in this embodiment the multiplexer **614** is configured to selectively bypass fewer than all of the off-chip interfaces **610** of the subsystem **602** in response to a bypass control (i.e., selection) signal pro-

vided by the power signal detection logic **612**. Alternatively, in another embodiment (not shown) the multiplexer **614** could be configured to selectively bypass all of the off-chip interfaces **610**, similarly to the embodiments described above with regard to FIGS. **3-4**.

As illustrated in FIG. **7**, in another embodiment a chip **700** may have a boundary scan chain comprising any number of boundary scan cells ("BC"s) **702**. The chip **700** may include any number of subsystems **704**, such as subsystems **704**A, **704**B, **704**C, **704**D, etc., each of which may be powered through a different power domain. Each subsystem **704** may include, in addition to the one or more boundary scan cells **702** shown, core logic as described above with regard to other embodiments, although such core logic is not shown in FIG. **7** for purposes of clarity. The boundary scan cells **702** that are included in or associated with each subsystem **704** may be included in an off-chip or physical interface (not separately indicated in FIG. **7**) of that subsystem **704**. Note in the embodiment illustrated in FIG. **7** that while some of the some of the boundary scan cells **702** are associated with each subsystem **704**, others of the boundary scan cells **702** are not associated with any subsystem **704**. Such other boundary scan cells **702** may instead be associated with other logic (not shown), such as, for example centralized or system core logic similar to the system core logic **108** described above with regard to FIG. **1**. Such other boundary scan cells **702** may be interposed in what are sometimes referred to as general-purpose input/output ("GPIO") data paths. Such system core logic (not shown) may be powered through yet a different power domain than the power domains through which the subsystems **704** are powered.

Each boundary scan cell **702** may be interposed in an input/output data signal path between core logic and a respective or associated signal pin **706** of the chip **700**. As in the embodiments described above, in the embodiment illustrated in FIG. **7** any signal pin **706** may serve as an input, output, or bidirectional off-chip connection, depending on the configuration of its associated core logic.

The chip **700** may further include multiplexers **708**A, **708**B, **708**C, and **708**D, associated with the subsystems **704**A, **704**B, **704**C, and **704**D, respectively. A JTAG data register **710** may comprise a register bit cell **712**A having an output coupled to the selector input of the multiplexer **708**A, a register bit cell **712**B having an output coupled to the selector input of the multiplexer **708**B, a register bit cell **712**C having an output coupled to the selector input of the multiplexer **708**C, and a register bit cell **712**D having an output coupled to the selector input of the multiplexer **708**D. The JTAG data register **710** may be included in the JTAG circuitry (not separately indicated in FIG. **7**) that controls the boundary scan test. Similarly to the embodiments described above with regard to FIGS. **3** and **5**, the outputs of the JTAG data register **710** serve as bypass control signals to control whether a selected subsystem **702** is bypassed in the boundary scan chain.

As illustrated in FIG. **8**, in a further embodiment a chip **800** may have a boundary scan chain comprising any number of boundary scan cells ("BC"s) **802**. The chip **800** may include any number of subsystems **804**, such as subsystems **804**A, **804**B, **804**C, **804**D, etc., each of which may be powered through a different power domain. Each subsystem **804** may include, in addition to the one or more boundary scan cells **802** shown, core logic as described above with regard to other embodiments, although such core logic is not shown in FIG. **8** for purposes of clarity. The boundary scan cells **802** that are included in or associated with each subsystem **804** may be included in an off-chip or physical interface (not separately indicated in FIG. **8**) of that subsystem **804**. Similarly to the embodiment described above with regard to FIG. **7**, in this embodiment some of the some of the boundary scan cells **802** are associated with each subsystem **804**, while others of the boundary scan cells **802** are not associated with any subsystem **804**. Such other boundary scan cells **802** may instead be associated with other logic (not shown), such as, for example centralized or system core logic similar to the system core logic **108** described above with regard to FIG. **1**. Such other boundary scan cells **802** may be interposed in GPIO data paths. Such system core logic (not shown) may be powered through yet a different power domain than the power domains through which the subsystems **804** are powered.

Each boundary scan cell **802** may be interposed in an input/output data signal path between the above-referenced core logic and a respective or associated signal pin **806** of the chip **800**. As in the embodiments described above, in the embodiment illustrated in FIG. **8** any signal pin **806** may serve as an input, output, or bidirectional off-chip connection, depending on the configuration of its associated core logic.

The chip **800** may further include multiplexers **808**A, **808**B, **808**C, and **808**D, associated with the subsystems **804**A, **804**B, **804**C, and **804**D, respectively. The chip **800** may also include power signal detection logic **812**A, **812**B, **812**C, and **812**D. The power signal detection logic **812**A, **812**B, **812**C, and **812**D may be configured as bypass control logic to detect, and to produce respective signals indicating, whether the subsystems **802**A, **802**B, **802**D, and **802**D are powered. These signals produced by the power signal detection logic **812**A, **812**B, **812**C, and **812**D are coupled to the selector inputs of the multiplexers **808**A, **808**B, **808**C, and **808**D, respectively. Similarly to the embodiments described above with regard to FIGS. **4** and **6**, the boundary scan cells **802** associated with any of the subsystems **804** that are unpowered may be bypassed in the boundary scan chain.

As illustrated by the flow diagram in FIG. **9**, a method **900** for selectively bypassing off-chip interfaces in a boundary scan chain of an integrated circuit chip may include the following. As indicated by block **902**, the method **900** may include producing a first bypass control signal indicating whether to bypass a first interface boundary scan cell coupled between a first predecessor boundary scan cell and a first successor boundary scan cell in the boundary scan chain. Registers and power detector circuits are examples of means for performing functions associated with block **902**. Although in the exemplary embodiments described with regard to FIGS. **3** and **5**, the registers are JTAG data registers, in other embodiments such registers may be of any kind, including, for example, programmable registers, programmable fuses, non-volatile memory locations, etc.

As indicated by block **904**, the method **900** may include coupling an output of the first interface boundary scan cell to an input of the first successor boundary scan cell in response to a first state of the bypass control signal. A multiplexer is an example of a means for performing functions associated with block **904**. As indicated by block **906**, the method **900** may include coupling an output of the first predecessor boundary scan cell to an input of the first successor boundary scan cell in response to a second state of the first bypass control signal. A multiplexer is an example of a means for performing functions associated with block **906**.

As described above with regard to FIGS. **3-8**, embodiments of systems for selectively bypassing off-chip interfaces in a boundary scan chain of an integrated circuit chip

may include any number of off-chip interfaces, subsystems, boundary scan cells, etc. Accordingly, the above-described method **900** may be extended to include further instances of blocks **902-906**, relating to further (e.g., second, third, etc.) bypass control signals, and further (e.g., second, third, etc.) predecessor boundary scan cells, further (e.g., second, third, etc.) successor boundary scan cells.

As illustrated in FIG. **10**, exemplary embodiments of systems and methods for selectively bypassing off-chip interfaces in a boundary scan chain of an integrated circuit chip may be provided in a portable computing device ("PCD") **1000**.

The PCD **1000** may include an SoC **1002**. The SoC may be an example of any of the above-described chips **300** (FIG. **3**), **400** (FIG. **4**), **500** (FIG. **5**), **600** (FIG. **6**), **700** (FIG. **7**) or **800** (FIG. **8**).

The SoC **1002** may include a CPU **1004**, a GPU **1006**, a DSP **1007**, an analog signal processor **1008**, or other processors. The CPU **1004** may include multiple cores, such as a first core **1004**A, a second core **1004**B, etc., through an Nth core **1004**N.

A display controller **1010** and a touch-screen controller **1012** may be coupled to the CPU **1004**. A touchscreen display **1014** external to the SoC **1002** may be coupled to the display controller **1010** and the touch-screen controller **1012**. The PCD **1000** may further include a video decoder **1016** coupled to the CPU **1004**. A video amplifier **1018** may be coupled to the video decoder **1016** and the touchscreen display **1014**. A video port **1020** may be coupled to the video amplifier **1018**. A universal serial bus ("USB") controller **1022** may also be coupled to CPU **1004**, and a USB port **1024** may be coupled to the USB controller **1022**. The USB interface or a portion thereof may be an example of a bypassable off-chip interface. A subscriber identity module ("SIM") card **1026** may also be coupled to the CPU **1004**.

One or more memories may be coupled to the CPU **1004**. The one or more memories may include both volatile and non-volatile memories. Examples of volatile memories include static random access memory ("SRAM") **1028** and dynamic RAMs ("DRAM"s) **1030** and **1031**. Such memories may be external to the SoC **1002**, such as the DRAM **1030**, or internal to the SoC **1002**, such as the DRAM **1031**. A DRAM controller **1032** coupled to the CPU **1004** may control the writing of data to, and reading of data from, the DRAMs **1030** and **1031**. In other embodiments, such a DRAM controller may be included within a processor, such as the CPU **1004**. The DRAM controller **1032** may be an example of the memory controller **102** (FIG. **1**) or **202** (FIG. **2**).

A stereo audio CODEC **1034** may be coupled to the analog signal processor **1008**. Further, an audio amplifier **1036** may be coupled to the stereo audio CODEC **1034**. First and second stereo speakers **1038** and **1040**, respectively, may be coupled to the audio amplifier **1036**. In addition, a microphone amplifier **1042** may be coupled to the stereo audio CODEC **1034**, and a microphone **1044** may be coupled to the microphone amplifier **1042**. A frequency modulation ("FM") radio tuner **1046** may be coupled to the stereo audio CODEC **1034**. An FM antenna **1048** may be coupled to the FM radio tuner **1046**. Further, stereo headphones **1050** may be coupled to the stereo audio CODEC **1034**. Other devices that may be coupled to the CPU **1004** include one or more digital (e.g., CCD or CMOS) cameras **1052**.

A modem or RF transceiver **1054** may be coupled to the analog signal processor **1008**. An RF switch **1056** may be coupled to the RF transceiver **1054** and an RF antenna **1058**. In addition, a keypad **1060**, a mono headset with a microphone **1062**, and a vibrator device **1064** may be coupled to the analog signal processor **1008**.

The SoC **1002** may have one or more internal or on-chip thermal sensors **1070**A and may be coupled to one or more external or off-chip thermal sensors **1070**B. An analog-to-digital converter ("ADC") controller **1072** may convert voltage drops produced by the thermal sensors **1070**A and **1070**B to digital signals. A power supply **1074** and a power management integrated circuit ("PMIC") **1076** may supply power to the SoC **1002**.

Firmware or software may be stored in any of the above-described memories, such as DRAM **1030** or **1031**, SRAM **1028**, etc., or may be stored in a local memory directly accessible by the processor hardware on which the software or firmware executes. Execution of such firmware or software may control aspects of any of the above-described methods or configure aspects any of the above-described systems. Any such memory or other non-transitory storage medium having firmware or software stored therein in computer-readable form for execution by processor hardware may be an example of a "computer program product," "computer-readable medium," etc., as such terms are understood in the patent lexicon.

Embodiments of systems and methods for selectively bypassing off-chip interfaces in a boundary scan chain may enable a boundary scan test to be performed even though one or more of the off-chip interfaces may be unpowered. Alternative embodiments will become apparent to one of ordinary skill in the art to which the invention pertains without departing from its spirit and scope. Therefore, although selected aspects have been illustrated and described in detail, it will be understood that various substitutions and alterations may be made therein without departing from the spirit and scope of the present invention, as defined by the following claims.

What is claimed is:

1. A method for selectively bypassing off-chip interfaces in a boundary scan chain of an integrated circuit chip, comprising:

producing a first bypass control signal for a multiplexer indicating whether to bypass a first interface boundary scan cell coupled between a first predecessor boundary scan cell and a first successor boundary scan cell in the boundary scan chain, the first predecessor boundary scan cell and the first interface boundary scan cell being part of a first power domain and having direct connections to the multiplexer, the first successor boundary scan cell and multiplexer being part of a second power domain separate and independent of the first power domain;

coupling with the multiplexer, in response to a first state of the first bypass control signal, an output of the first interface boundary scan cell to an input of the first successor boundary scan cell; and

coupling with the multiplexer, in response to a second state of the first bypass control signal, an output of the first predecessor boundary scan cell to an input of the first successor boundary scan cell;

wherein producing the first bypass control signal comprises providing the first bypass control signal from one or more registers included in test circuitry configured to control a boundary scan test using the boundary scan chain.

2. The method of claim **1**, wherein the test circuitry conforms to an IEEE 1149.1 standard.

3. The method of claim 1, wherein producing the first bypass control signal for the multiplexer comprises providing the first bypass control signal in response to detecting whether an off-chip interface having the first interface boundary scan cell is powered.

4. A method for selectively bypassing off-chip interfaces in a boundary scan chain of an integrated circuit chip, comprising:

a first interface boundary scan cell in the boundary scan chain, a first predecessor boundary scan cell preceding the first interface boundary scan cell in the boundary scan chain, and a first successor boundary scan cell succeeding the first interface boundary scan cell in the boundary scan chain; the first predecessor boundary scan cell and the first interface boundary scan cell being part of a first power domain and having direct connections to a first multiplexer, the first successor boundary scan cell and the first multiplexer being part of a second power domain separate and independent of the first power domain;

the first multiplexer having a first input coupled to an output of the first interface boundary scan cell, the first multiplexer having a second input coupled to an output of the first predecessor boundary scan cell, the first multiplexer having an output coupled to an input of the first successor boundary scan cell, the output of the first predecessor boundary scan cell further coupled to an input of the first interface boundary scan cell; and

bypass control logic configured to produce a first bypass control signal controlling whether the first multiplexer selects the first input or the second input the bypass control logic comprising one or more registers included in test circuitry configured to control a boundary scan test using the boundary scan chain.

5. The system of claim 4, wherein the bypass control logic is configured to produce the first bypass control signal based on contents of the one or more registers.

6. The system of claim 5, wherein the test circuitry conforms to an IEEE 1149.1 standard.

7. The system of claim 4, wherein the bypass control logic comprises power signal detection logic configured to detect whether an off-chip interface having the first interface boundary scan cell is powered, and further configured to produce the first bypass control signal based on whether the off-chip interface is powered.

8. A system for selectively bypassing off-chip interfaces in a boundary scan chain of an integrated circuit chip, comprising:

a plurality of subsystem off-chip interfaces, each subsystem off-chip interface included in one of a corresponding plurality of power domains of the integrated circuit chip, each subsystem off-chip interface having an interface boundary scan cell and a predecessor boundary scan cell in the boundary scan chain, each predecessor boundary scan cell and the each interface boundary scan cell of each subsystem off-chip interface being part of a separate power domain associated with a respective subsystem off-chip interface;

a plurality of multiplexers, each multiplexer associated with one of the subsystem off-chip interfaces and having a power domain separate from power domains of the off-chip interfaces, each multiplexer having a first input coupled to an output of the interface boundary scan cell, each multiplexer having a second input coupled to an output of a predecessor boundary scan cell preceding the interface boundary scan cell in the boundary scan chain, each multiplexer having an output coupled to an input of a successor boundary scan cell succeeding the interface boundary scan cell in the boundary scan chain, the output of the predecessor boundary scan cell further coupled to an input of the interface boundary scan cell; the successor boundary scan cells and the multiplexers sharing a common power domain which is separate from each power domain of the off-chip interfaces; and

bypass control logic configured to produce a plurality of bypass control signals, each bypass control signal controlling whether a corresponding one of the plurality of multiplexers selects the first input or the second input; the bypass control logic comprising one or more registers included in test circuitry configured to control a boundary scan test using the boundary scan chain.

9. The system of claim 8, wherein the bypass control logic is configured to control the multiplexer based on contents of the one or more registers.

10. The system of claim 9, wherein the test circuitry conforms to an IEEE 1149.1 standard.

11. The system of claim 8, wherein the bypass control logic comprises power signal detection logic configured to detect whether an off-chip interface having the interface boundary scan cell is powered, and further configured to control the multiplexer based on whether the off-chip interface is powered.

12. A system for selectively bypassing off-chip interfaces in a boundary scan chain of an integrated circuit chip, comprising:

means for producing a bypass control signal for a multiplexer indicating whether to bypass an interface boundary scan cell coupled between a predecessor boundary scan cell and a successor boundary scan cell in the boundary scan chain, the first predecessor boundary scan cell and the first interface boundary scan cell being part of a first power domain and having direct connections to the multiplexer, the first successor boundary scan cell and multiplexer being part of a second power domain separate and independent of the first power domain;

means for coupling to the multiplexer, in response to a first state of the bypass control signal, an output of the interface boundary scan cell to an input of the successor boundary scan cell; and

means for coupling to the multiplexer, in response to a second state of the bypass control signal, an output of the predecessor boundary scan cell to an input of the successor boundary scan cell, wherein producing the first bypass control signal comprises providing the first bypass control signal from one or more registers included in test circuitry configured to control a boundary scan test using the boundary scan chain.

13. The system of claim 12, wherein the test circuitry conforms to an IEEE 1149.1 standard.

14. The system of claim 12, wherein the means for producing the bypass control signal for the multiplexer comprises means for providing the bypass control signal in response to detecting whether an off-chip interface having the interface boundary scan cell is powered.

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