Title: METHOD TO OPTIMIZE AND REDUCE INTEGRATED CIRCUIT, PACKAGE DESIGN, AND VERIFICATION CYCLE TIME

Abstract:

Periodic optimizations of the design of integrated circuits, packages, and verification methodologies are performed to reduce cycle time.

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METHOD TO OPTIMIZE AND REDUCE INTEGRATED CIRCUIT,
PACKAGE DESIGN, AND VERIFICATION CYCLE TIME

[0001] This various embodiments described herein relate in general to improvements in integrated circuit packaging, and, more specifically, to methods and apparatus for configuring integrated circuit chips in multiple packages that can be regarded as different products.

[0002] BACKGROUND

[0003] The design of integrated circuits (IC) products involves difficult and complex processes. For example, IC customers may request an IC product that has certain functionalities that may be fulfilled with one or more pre-existing packaged ICs. In this scenario, sometimes new or "combo" IC packages are designed in or on which the pre-existing IC packages are combined and interconnected. The new IC packages, in turn, are delivered to the customer to be connected in the customer's particular application. The overall goal for package designers is to deliver IC packages having a variety of circuit functionalities quickly, efficiently, and as economically as possible.

[0004] Meeting these goals, however, poses many problems for package designers. Although computer-aided design tools are widely available, the package design process is still very complex. The process typically involves designing a package to which the pre-existing ICs can be mounted, with interconnects arranged so that a package can be delivered to the customer to meet his own fabrication needs. In order to do this, the package must be tested with the pre-existing IC packages in place, a process in itself which takes a considerable amount of time. Each product must be individually designed, fabricated, and tested. However, if a customer (or another customer) desires a related product, it must be individually designed from scratch, again requiring time and resources to build. This can often be frustrating for the customer.

[0005] Oftentimes, multiple pre-existing IC packages are connected in a single package; however, if it is desired to divide the product into multiple packages, each package needs to be regarded as a new product. This again requires a new package design to be completed from scratch. Additionally, even though a portion of the product existed in the old design, the new product needs to be evaluated and tested to guarantee its performance in the new package. This traditional approach requires each package to be simulated and custom designed to meet the electrical requirement and substrate
manufacture process, which can take twelve months or more to complete. To support
an integrated circuit chip being used in two different products, either the resources
needed to be doubled, or the development cycle time made longer.

[0006] What is needed is a method and apparatus to save design and verification cycle
time in integrated circuit and integrated circuit package design.

[0007] SUMMARY

[0008] According to a broad embodiment, a method is disclosed to optimize and reduce
integrated circuit, package design, and verification cycle time for multi-die product and
its derived product from multi-die package into single die or any combination of the
dice into package.

[0009] Thus, according to broad embodiments of the invention, the integrated circuit
and package design and routing can be reused and applied to multiple products that may
use the integrated circuit being developed.

includes designing an integrated circuit package having a plurality of integrated circuit
connection sets. Each of the integrated circuit connection sets are configured to be
connected to a corresponding integrated circuit selected from among a plurality of
integrated circuits. Different integrated circuit products can be produced depending
upon which selected integrated circuit is connected to its corresponding connection set,
and the integrated circuit package can be cut to exclude integrated circuit connection
sets corresponding to integrated circuits that are not selected. The method also includes
connecting at least one of the selected integrated circuits on at least one of the
corresponding integrated circuit connection sets to selectively form the integrated circuit
product.

[0011] In performing the method, the plurality of integrated circuits are connected to a
corresponding integrated circuit connection set, and the resulting integrated circuit
package is tested. Subsequently, if an integrated circuit product is desired to be
fabricated having a function that is subset of the function provided by the resulting
integrated circuit package, the resulting integrated circuit package is cut during a design
phase to include only the portions necessary to perform the desired function, and the
integrated circuit that performs the desired subset function connected.
[0012] Another embodiment of a method for fabricating an integrated circuit product includes fabricating a first integrated circuit package having a plurality of integrated circuit connection sets. Each of the integrated circuit connection sets are configured to be connected to a corresponding integrated circuit selected from among a plurality of integrated circuits. The corresponding integrated circuits of the plurality of integrated circuits are connected to the integrated circuit connection sets to form a complete integrated circuit package and the complete integrated circuit package is tested. Thereafter, a second integrated circuit package is designed based on the first integrated circuit package, the second integrated circuit package including less than all of the corresponding integrated circuits of the plurality of integrated circuits to form the integrated circuit product. During the design of the second integrated circuit package, the complete integrated circuit package may be cut to form the second integrated circuit package.

[0013] An embodiment of an integrated circuit (IC) product includes a package containing an IC chip having IC chip contacts and a substrate having a plurality of substrate contacts. A plurality of IC interconnects carried by the substrate are connected to the IC chip contacts and to the substrate contacts. The IC product is cut during its design as a subset of a fully tested IC package which included the IC product and at least one other IC product.

[0014] An embodiment of an article of manufacture includes a substrate and a plurality of integrated circuit connection sets. Each of the sets of the integrated circuit connection sets are independently configured to enable a corresponding integrated circuit to be selectively connected thereto. Thus, different integrated circuit products can be produced depending upon which corresponding integrated circuit is selected and connected.

[0015] BRIEF DESCRIPTION OF THE DRAWINGS

[0016] Figure 1 is a flow diagram showing an illustrative embodiment of a method for fabricating an integrated circuit package.

[0017] Figure 2a is a cut-away top view of an illustrative complete integrated circuit package, taken at 2a - 2a in Figure 3a, containing a number of integrated circuits from which a plurality of integrated circuit products can be formed.
[0018] Figure 2b is a cut-away top view, taken at 2b - 2b in Figure 3b, of one of the integrated circuit products that can be formed by cutting the complete integrated circuit package of Figure 2a.

[0019] Figure 3a is a cut-away side view of the complete integrated circuit package (which may also be an integrated circuit product) taken at 3a-3a in Figure 2a.

[0020] Figure 3b is a side view of the integrated circuit product taken at 3b-3b in Figure 2b.

[0021] Figure 4a is a cut-away top view, taken at 4a - 4a in Figure 5a, of an illustrative another complete integrated circuit package containing a number of integrated circuits from which a plurality of integrated circuit products can be formed.

[0022] Figure 4b is a cut-away top view, taken at 4b - 4b in Figure 5b, of one of the integrated circuit products that can be formed by cutting the complete integrated circuit package of Figure 4a.

[0023] Figure 5a is a cut-away side view of the complete integrated circuit package (which may also be an integrated circuit product) taken at 5a-5a in Figure 4a.

[0024] Figure 5b is a side view of the integrated circuit product taken at 5b-5b in Figure 4b.

[0025] Figure 6a is a cut-away top view of the integrated circuit package of Figure 4a, taken at 6a-6a in Figure 5a, showing an illustration of the package interconnects of the complete integrated circuit package.

[0026] Figure 6b is a cut-away top view of the integrated circuit product of Figure 4b, taken at 6b-6b in Figure 5b, showing an illustration of the package interconnects of the integrated circuit product.

[0027] In the various figures of the drawing, like reference numbers are used to denote like or similar parts.

[0028] DETAILED DESCRIPTION

[0029] An embodiment of a method by which integrated circuit products may be designed and fabricated is illustrated in the flow diagram 10 of Figure 1, to which reference is now made. As shown in box 12, an integrated circuit package having a plurality of integrated circuit connection sets is designed. A connection set example is
described in greater detail below in conjunction with Figures 4 - 6. Each of the integrated circuit connection sets is configured to be connected to a corresponding integrated circuit selected from among a plurality of integrated circuits, each having different functionality, to enable different integrated circuit products to be produced depending upon which selected integrated circuit is connected to its corresponding connection set.

[0030] The connection sets may be, for example, metallization traces or patterns, formed in well-known manner. The metallization patterns, however, are formed in a manner such that they can be cut or separated during a design phase to enable the functionalities of the selected integrated circuits to be separated, if desired, and still perform according to the product specifications.

[0031] As shown in box 14, after the package substrate has been form with the various connection sets, each of the selected integrated circuits are connected to its corresponding integrated circuit connection set to form a complete integrated circuit package. As shown in box 16, the resulting complete integrated circuit package is then tested. The resulting complete integrated circuit package, containing the various selected integrated circuit packages, at this point, comprises a complete integrated circuit product in and of itself, and can be delivered to those customers desiring the functionality provided thereby.

[0032] However, often customers want only a subset of the complete integrated circuit package; for example, a customer may need the functionality of only one of the selected integrated circuits contained on the complete integrated circuit package. Thus, as shown in box 18, the integrated circuit package can be cut to exclude integrated circuit connection sets corresponding to integrated circuits that are not selected.

[0033] Thus, since the complete integrated circuit package has been fully tested, for the design of a package having a subset of the complete integrated circuit package, the complete circuit package is cut during the design phase of the subset package, using the particular computer design tool used. Then, the selected integrated circuit is connected to its corresponding integrated circuit connection set to selectively form said integrated circuit product. Since the complete integrated circuit package has been fully tested, as mentioned, the new integrated circuit product needs little, if any additional testing. Thus, the overall design time of the subset product is substantially reduced.
[0034] The method described above can be further appreciated from the complete integrated circuit package 20 and integrated circuit product 22 shown in Figures 2a, 2b, 3a, and 3b, to which reference is now additionally made. Figure 2a is a cut-away top view of an illustrative complete integrated circuit package 20 containing a number of integrated circuits 22, 24, and 26 from which a plurality of integrated circuit products can be formed. In the drawings of Figures 2a and 2b, only the footprint of the integrated circuits 22, 24, and 26 are shown to illustrate the respective placements of the integrated circuits for this example, the integrated circuit contacts best being seen in Figures 3a and 3b.

[0035] As shown in Figures 2a and 3a, the complete integrated circuit package 20 includes a substrate 28 onto which integrated circuits 22, 24, and 26 are carried. The substrate 28 includes a number of contact points 30 which connect to the contacts 32 of the integrated circuits 22, 24, and 26 (see Figure 3b). In the embodiment illustrated, the integrated circuits 22, 24, and 26 are pre-packaged chips having contacts 32 by which electrical connection to the encapsulated integrated circuit chips may be made. It should be noted however that the particular embodiment of the integrated circuit chips with which the method described herein can be practiced can be of any construction consistent with the end package configuration to be achieved.

[0036] The substrate 28 includes a number of integrated circuit connection sets (not shown), of the type described below in the embodiment shown in Figure 6, which interconnect the connections 32 of the integrated circuit 22, 24, and 26 to respective contacts 36 on the backside of the substrate 28. The integrated circuit connection sets are fabricated to interconnect a selected integrated circuit to the corresponding connections 36 of the substrate 28. Furthermore, each of the selected integrated circuits that may be connected to its corresponding integrated circuit connection set may be of different functionality. Thus, for example, in the embodiment of Figures 2a and 3a, the complete integrated circuit package 20 may provide complete functionality for a mobile phone modem, with the integrated circuit 24 providing, for example, functionality for an audio section, integrated circuit 26 providing functionality of a digital section, and integrated circuit 22 providing functionality for an rf section.

[0037] Once the complete integrated circuit package is designed, for example, using computer aided design tools, it may be tested to the extent necessary to determine that it operates properly, and may serve as its own integrated circuit product. However, if a
customer desires an integrated circuit product that has the functionality of only a subset of the complete integrated circuit package, it can easily be designed, for example, by using the computer aided design tools to cut the complete integrated circuit package to include only the integrated circuit chip, or chips, having the desired functionality, and its, or their, supporting integrated circuit connection set.

[0038] Thus, an integrated circuit package such as the integrated circuit product 40 can be cut from the complete integrated circuit package 20 during a computer aided design process. Subsequently, the integrated circuit package 22 may be connected to the corresponding integrated circuit connection set to complete the integrated circuit product 40, as shown in Figures 2b and 3b. The integrated circuit product 40 may be, for example, an integrated circuit product having the functionality of an rf section which is usable by a customer by itself. Since the integrated circuit product 40 was previously tested during the design and test of the complete integrated circuit package 20, only minimal testing need be performed. It should be noted that although the fabrication of the integrated circuit product 40 is shown and described, integrated circuit products can also be formed of the individual integrated circuits 24, 26, or any combination thereof.

[0039] Another embodiment of a complete integrated circuit package 50 and subset product 52 is shown in Figures 4a, 4b, 5a, 5b, 6a, and 6b, to which reference is now additionally made. In the embodiment 50, two integrated circuits 54 and 56 are designed and fabricated in the complete integrated circuit package. The complete integrated circuit package 50 includes a substrate 58 having various connection points 60 to which the integrated circuit packages 54 and 56 are connected, in known manner.

[0040] The substrate 58 has a number of integrated circuit connection sets to which the contacts 62 of the integrated circuits packages 54 and 56 are connected. The integrated circuit connection sets may be fabricated as a metallization layer or pattern, shown, for example in Figures 6a and 6b. Thus, as shown, the integrated circuit connection set 64 may correspond to the connections required of a selected integrated circuit package, such as the integrated circuit package 54, and the integrated circuit connection set 66 may correspond to the connections required of a selected integrated circuit package, such as the integrated circuit package 56. The integrated circuit connection sets 64 and 66 serve to connect the contacts 62 of the integrated circuit packages 54 and 56 to the appropriate connections 70 on the bottom side of the substrate 58. Since the complete integrated circuit package may be selectively cut to form individual integrated circuit
products, the layout of the integrated circuit connection sets may be designed so that such selective cutting can be employed without damaging the functionality of the cut integrated circuit products.

[0041] Once the complete integrated circuit package 50 is designed, for example, using computer aided design tools, it may be tested to the extent necessary to determine that it operates properly, and may serve as its own integrated circuit product. However, if a customer desires an integrated circuit product that has the functionality of only a subset of the complete integrated circuit package, it can easily be designed, for example, by using the computer aided design tools to cut the complete integrated circuit package to include only the integrated circuit chip, or chips, having the desired functionality, and its, or their, supporting integrated circuit connection set.

[0042] Thus, an integrated circuit package such as the integrated circuit product 52 can be cut from the complete integrated circuit package 50 during a computer aided design process. Subsequently, the integrated circuit package 54 may be connected to the corresponding integrated circuit connection set to complete the integrated circuit product 52, as shown in Figures 4b and 5b. Since the integrated circuit product 52 was previously tested during the design and test of the complete integrated circuit package 50, only minimal testing need be performed. It should be noted that although the fabrication of the integrated circuit product 52 is shown and described, integrated circuit products can also be formed of the individual integrated circuit 56.

[0043] In view of the above, it will be appreciated that the technique described above can reduce the development cycle and can guarantee the performance of a reused integrated circuit chip in any package design. That is, an ideal situation is to be able to reuse the integrated circuit, package design, and routing that is originally developed and to apply to multiple products without increasing the development cycle time and resources, while guaranteeing the performance in any package.

[0044] At least some of the benefits that can be realized using this technique is that only one IC design is needed, only need one package design is needed, and only one electrical simulation is needed to verify the electrical performance on multiple products using the same package.

[0045] Figure 7, to which reference is now additionally made, shows an exemplary wireless communication system 70 in which an embodiment of an integrated circuit of
the type described herein may be advantageously employed. For purposes of illustration, Figure 7 shows remote units 72, 74, and 76 and two base stations 78. Typical wireless communication systems, of course, may have many more remote units and base stations. Any of the remote units 72, 74, and 76, as well as the base stations 78, may include an integrated circuit of the type described herein.

[0046] Figure 7 shows forward link signals 80 from the base stations 78 to the remote units 72, 74, and 76 and reverse link signals 82 from the remote units 72, 74, and 76 to base stations 78.

[0047] In Figure 7, remote unit 72 is shown as a mobile telephone, remote unit 74 is shown as a portable computer, and remote unit 76 is shown as a fixed location remote unit in a wireless local loop system, for example, in a house 84 or other structure. The remote units, for instance, may be cell phones, hand-held personal communication systems (PCS) units, portable data units such as personal data assistants, or fixed location data units such as meter reading equipment. Although Figure 7 illustrates certain exemplary remote units that may include an integrated circuit of the type described herein, the integrated circuit is not limited to these exemplary illustrated remote units. One or more integrated circuits of the type described herein may be suitably employed in any electronic device. For example, the electronic device may also be a set top box, a music player, a video player, an entertainment unit, a navigation device, a computer, a portable data unit, a fixed location data unit, or the like, as shown in box 86 in Figure 7. Other suitable electronic devices are manifold.

[0048] The words "example" or "exemplary" are used herein to mean "serving as an instance, illustration, nature, or character of the rest." Any embodiment described herein as "an example" or "exemplary" is not necessarily to be construed as preferred or advantageous over other embodiments.

[0049] Although embodiments of the invention have been described and illustrated with a certain degree of particularity, it should be understood that the present disclosure has been made by way of example only, and that numerous changes in the combination and arrangement of parts may be resorted to without departing from the spirit and scope of the invention, as hereinafter claimed.
CLAIMS:

1. A method for fabricating an integrated circuit product, comprising:
   designing an integrated circuit package having a plurality of integrated circuit connection sets, each of said integrated circuit connection sets being configured to be connected to a corresponding integrated circuit selected from among a plurality of integrated circuits;
   wherein said integrated circuit package can be cut to exclude integrated circuit connection sets corresponding to integrated circuits that are not selected; and
   connecting at least one of said selected integrated circuits on at least one of said corresponding integrated circuit connection sets to selectively form an integrated circuit product.

2. The method of claim 8 wherein said connecting comprises connecting a selected integrated circuit to each corresponding integrated circuit connection set, and testing a resulting integrated circuit package.

3. The method of claim 8 wherein said connecting comprises connecting all of said selected integrated circuits to corresponding integrated circuit connection sets, and testing a resulting integrated circuit package.

4. The method of claim 11 further comprising cutting said tested resulting integrated circuit package during a design phase before said at least one of said selected integrated circuit chips is connected, wherein only the portion of the integrated circuit connection sets corresponding to said at least one of said selected integrated circuits is fabricated into said integrated circuit product.

5. The method of claim 8 wherein said integrated circuit connection sets comprise metallization patterns.

6. The method of claim 8 wherein each of the plurality of integrated circuits has a different functionality.

7. The method of claim 8 further wherein said connecting comprises connecting a plurality of said selected integrated circuits onto corresponding integrated circuit connection sets to selectively form one of said integrated circuit products.
8. The method of claim 8 further wherein said connecting comprises connecting one of said selected integrated circuits onto a corresponding integrated circuit connection set to selectively form one of said integrated circuit products.

9. A method for fabricating an integrated circuit product, comprising:
   designing an integrated circuit package having a plurality of integrated circuit connection sets, each of said integrated circuit connection sets being configured to be connected to a corresponding integrated circuit selected from among a plurality of integrated circuits;
   wherein different integrated circuit products can be produced depending upon which selected integrated circuit is connected to its corresponding connection set;
   wherein said integrated circuit package can be cut to exclude integrated circuit connection sets corresponding to integrated circuits that are not selected; and
   connecting at least one of said selected integrated circuits on at least one of said corresponding integrated circuit connection sets to selectively form said integrated circuit product.

10. The method of claim 9 wherein said connecting comprises connecting a selected integrated circuit to each corresponding integrated circuit connection set, and testing a resulting integrated circuit package.

11. The method of claim 9 wherein said connecting comprises connecting all of said selected integrated circuits to corresponding integrated circuit connection sets, and testing a resulting integrated circuit package.

12. The method of claim 11 further comprising cutting said tested resulting integrated circuit package during a design phase before said at least one of said selected integrated circuit chips is connected, wherein only the portion of the integrated circuit connection sets corresponding to said at least one of said selected integrated circuits is fabricated into said integrated circuit product.

13. The method of claim 9 wherein said integrated circuit connection sets comprise metallization patterns.

14. The method of claim 9 wherein each of the plurality of integrated circuits has a different functionality.
15. The method of claim 9 further wherein said connecting comprises connecting a plurality of said selected integrated circuits onto corresponding integrated circuit connection sets to selectively form one of said integrated circuit products.

16. The method of claim 9 further wherein said connecting comprises connecting one of said selected integrated circuits onto a corresponding integrated circuit connection set to selectively form one of said integrated circuit products.

17. A method for fabricating an integrated circuit product, comprising:
   - fabricating a first integrated circuit package having a plurality of integrated circuit connection sets, each of said integrated circuit connection sets being configured to be connected to a corresponding integrated circuit selected from among a plurality of integrated circuits;
   - connecting said corresponding integrated circuits of said plurality of integrated circuits to said integrated circuit connection sets to form a complete integrated circuit package;
   - testing said complete integrated circuit package; and
   - designing a second integrated circuit package based on said first integrated circuit package, said second integrated circuit package including less than all of said corresponding integrated circuits of said plurality of integrated circuits to form said integrated circuit product.

18. The method of claim 17 wherein said designing comprises cutting said complete integrated circuit package to form said second integrated circuit package.

19. The method of claim 18 wherein said designing comprises designing said second integrated circuit package including one of said corresponding integrated circuits of said plurality of integrated circuits to form said integrated circuit product.

20. The method of claim 17 wherein each of the plurality of integrated circuits has a different functionality.

21. An integrated circuit (IC) product, comprising:
   - a package containing an IC chip having IC chip contacts;
   - a substrate;
   - a plurality of substrate contacts on said substrate; and
a plurality of IC interconnects carried by said substrate connected to said IC chip contacts and to said substrate contacts;
said IC product being cut during its design as a subset of a tested IC package which included said IC product and at least one other IC product.

22. The integrated circuit product of claim 21 wherein said interconnects are metallization patterns on said substrate.

23. The integrated circuit assembly of claim 21 wherein each of said IC products has a different functionality.

24. The integrated circuit assembly of claim 21 wherein each of said at least one other IC product comprises a package containing an additional IC chip having additional IC chip contacts, a plurality of additional substrate contacts on said substrate, and a plurality of additional IC interconnects carried by said substrate connected to said additional IC chip contacts and to said additional contacts.

25. The integrated circuit of claim 21 in which the integrated circuit is integrated into a device selected from the group consisting of a mobile phone, a set top box, a music player, a video player, an entertainment unit, a navigation device, a computer, a hand-held personal communication systems (PCS) unit, a portable data unit, and a fixed location data unit.

26. An integrated circuit (IC) product, comprising:
   means for providing a package containing an IC chip having IC chip contacts;
   means for providing a substrate;
   means for providing a plurality of substrate contacts on said substrate; and
   means for providing a plurality of IC interconnects carried by said substrate connected to said IC chip contacts and to said substrate contacts;
said IC product being cut during its design as a subset of a tested IC package which included said IC product and at least one other IC product.

27. An article of manufacture, comprising:
   a substrate,
a plurality of integrated circuit connection sets, each of said sets of said integrated circuit connection sets being independently configured to enable a
corresponding integrated circuit to be selectively connected thereto, whereby different
integrated circuit products can be produced depending upon which corresponding
integrated circuit is selected and connected.

28. The article of manufacture of claim 27 wherein said different integrated circuit
products can be produced by cutting said substrate and integrated circuit connection sets
during design to include only the integrated circuit product formed by said selected
integrated circuit.

29. The article of manufacture of claim 28 further comprising testing said plurality
of integrated circuit connection sets and all of said corresponding integrated circuits
before said cutting.

30. The article of manufacture of claim 27 wherein said integrated circuit
connection sets are metallization traces.

31. The article of manufacture of claim 27 further comprising a plurality of contacts
on said substrate to which the integrated circuits can be selectively connected.

32. The article of manufacture of claim 27 in which the article of manufacture is
integrated into a device selected from the group consisting of a mobile phone, a set top
box, a music player, a video player, an entertainment unit, a navigation device, a
computer, a hand-held personal communication systems (PCS) unit, a portable data unit,
and a fixed location data unit.

33. An article of manufacture, comprising:
   means for providing a substrate,
   means for providing a plurality of integrated circuit connection sets, each of said
sets of said integrated circuit connection sets being independently configured to enable a
corresponding integrated circuit to be selectively connected thereto, whereby different
integrated circuit products can be produced depending upon which corresponding
integrated circuit is selected and connected.
DESIGNING AN INTEGRATED CIRCUIT PACKAGE HAVING A PLURALITY OF INTEGRATED CIRCUIT CONNECTION SETS CONFIGURED TO BE CONNECTED TO A CORRESPONDING INTEGRATED CIRCUIT SELECTED FROM AMONG A PLURALITY OF INTEGRATED CIRCUITS, EACH HAVING DIFFERENT FUNCTIONALITY

CONNECTING THE SELECTED INTEGRATED CIRCUIT TO EACH CORRESPONDING INTEGRATED CIRCUIT CONNECTION SET

TESTING A RESULTING INTEGRATED CIRCUIT PACKAGE

CUTTING THE TESTED RESULTING INTEGRATED CIRCUIT PACKAGE DURING A DESIGN PHASE BEFORE THE A SELECTED ONE OF THE SELECTED INTEGRATED CIRCUIT CHIPS IS CONNECTED, WHEREIN ONLY THE PORTION OF THE INTEGRATED CIRCUIT CONNECTION SETS CORRESPONDING TO THE SELECTED INTEGRATED CIRCUIT IS FABRICATED INTO SAID INTEGRATED CIRCUIT PRODUCT

FIG. 1
**DECLARATION OF NON-ESTABLISHMENT OF INTERNATIONAL SEARCH REPORT**

(PCT Article 17(2) (a), Rules 13fer.1 (c) and Rule 39)

<table>
<thead>
<tr>
<th>Applicant's or agent's file reference</th>
<th>IMPORTANT DECLARATION</th>
<th>Date of mailing (day/month/year)</th>
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<td>082608WO</td>
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**International application No.**

PCT/US20 11/052744

**International filing date**

22 September 2001 (22-09-2001)

**International filing date (Earliest) Priority date**

22 September 2000 (22-09-2000)

**Applicant**

QUALCOMM INCORPORATED

This International Searching Authority hereby declares, according to Article 17(2)(a), that **no international search report will be established** on the international application for the reasons indicated below:

1. ☐ The subject matter of the international application relates to:
   a. ☐ scientific theories
   b. ☐ mathematical theories
   c. ☐ plant varieties
   d. ☐ animal varieties
   e. ☐ essentially biological processes for the production of plants and animals, other than microbiological processes and the products of such processes
   f. ☐ schemes, rules or methods of doing business
   g. ☐ schemes, rules or methods of performing purely mental acts
   h. ☐ schemes, rules or methods of playing games
   i. ☐ methods for treatment of the human body by surgery or therapy
   j. ☐ methods for treatment of the animal body by surgery or therapy
   k. ☐ diagnostic methods practised on the human or animal body
   l. ☐ computer programs for which this International Searching Authority is not equipped to search prior art

2. ✗ The failure of the following parts of the international application to comply with prescribed requirements prevents a meaningful search from being carried out:
   - [ ] the description
   - [x] the claims
   - [ ] the drawings

3. ☐ A meaningful search could not be carried out without the sequence listing; the applicant did not, within the prescribed time limit:
   - [ ] furnish a sequence listing on paper complying with the standard provided for in Annex C of the Administrative Instructions, and such listing was not available to the International Searching Authority in a form and manner acceptable to it.
   - [ ] furnish a sequence listing in electronic form complying with the standard provided for in Annex C of the Administrative Instructions, and such listing was not available to the International Searching Authority in a form and manner acceptable to it.
   - [ ] pay the required late furnishing fee for the furnishing of a sequence listing in response to an invitation under Rule 13fer.1 (a) or (b).

4. Further comments:

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Form PCT/ISA/203 (July 2009)
The present application contains 33 claims, of which 7 are independent. There is no clear distinction between the independent claims because of overlapping scope. There are so many claims, and they are drafted in such a way that the claims as a whole are not in compliance with the provisions of clarity and conciseness of Article 6 PCT, as it is partly customarily burdensome for a skilled person to establish the subject-matter for which protection is sought.

Additionally, the independent claims 21, 26, 27 and 33 comprise product-by-process definitions, resulting in a further lack of clarity (Guidelines, 5.26). And indeed it is not possible, by looking at the circuit claimed, to determine whether said circuit was cut during the design phase or it was designed without performing a cut.

Dependent claims 2 - 8 introduce a further lack of clarity, as said claims depend on claim 8, which depends on itself (Article 6 PCT). It is further unclear how a circuit can be tested in the design phase, before said circuit is fabricated (Article 6 PCT). It is to be noted that the same objection can be equally raised under Article 5 PCT.

For the above-mentioned reasons, the non-compliance with the substantive provisions is considered to be to such an extent, that a meaningful search of the whole claimed subject-matter could not be carried out (Article 17(2) PCT and Guidelines 9.30).

There being no reasonable basis in the application that clearly indicates the subject-matter which might be expected to form the subject of the claims later in the procedure, no search at all was deemed possible. Additionally, the description does not contain a single embodiment but so many embodiments that in view of the drafting of the claims an expected fallback position could not be determined.

The applicant's attention is drawn to the fact that claims relating to inventions in respect of which no international search report has been established need not be the subject of an international preliminary examination (Rule 66.1(e) PCT). The applicant is advised that the EPO policy when acting as an International Preliminary Examination Authority is normally not to carry out a preliminary examination on matter which has not been searched. This is the case irrespective of whether or not the claims are amended following receipt of the search report or during any Chapter II procedure. If the application proceeds into the regional phase before the EPO, the applicant is reminded that a search may be carried out during examination before the EPO (see EPO Guidelines C-VI, 8.2), should the problems which led to the Article 17(2) declaration be overcome.