ELEVATED PHOTODIODE WITH A STACKED SCHEME

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ABSTRACT

A device includes an image sensor chip having formed therein an elevated photodiode, and a device chip underlying and bonded to the image sensor chip. The device chip has a read out circuit electrically connected to the elevated photodiode.
ELEVATED PHOTODIODE WITH A STACKED SCHEME

[0001] This application claims the benefit of the following provisionally filed U.S. patent application Ser. No. 61/677,851, filed Jul. 31, 2012, and entitled “Elevated Photodiode with Stacked Scheme,” which application is hereby incorporated herein by reference.

BACKGROUND

[0002] Image sensors, and in particular Back Side Illumination (BSI) image sensors are becoming increasingly popular and used in a variety of applications. As is the trend with integrated circuit technology, the trend is toward smaller and smaller features for image sensors, to allow for lower cost and greater packing density. When pixels pitch scale down to the sub-micrometer range, the photodiode area is limited and thus it becomes difficult to maintain the performance such as Signal to Noise Ratio (SNR), Quantum Efficiency (QE), sensitivity, and the like.

[0003] Elevated photodiodes may overcome some shortcomings in conventional structures and methods for making such structures. Specific process tuning is needed, however, for so-called elevated photodiodes, and the same would be constrained by Application Specific Integrated Circuit (ASIC) process conditions.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] For a more complete understanding of the embodiments, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

[0005] FIG. 1 is a schematic cross-sectional view of a first embodiment structure in accordance with some exemplary embodiments;

[0006] FIG. 2 is a schematic cross-sectional view of a first embodiment structure in accordance with some exemplary embodiments;

[0007] FIGS. 3a through 3c illustrate cross-sectional views of intermediate steps in the manufacturing of the illustrative embodiment device in FIG. 1 in accordance with some exemplary embodiments; and

[0008] FIGS. 4a through 4c illustrate cross-sectional views of intermediate steps in the manufacturing of the illustrative embodiment device in FIG. 2 in accordance with some exemplary embodiments.

DETAILED DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

[0009] The making and using of the embodiments of the disclosure are discussed in detail below. It should be appreciated, however, that the embodiments provide many applicable inventive concepts that can be embodied in a wide variety of specific contexts. The specific embodiments discussed are illustrative, and do not limit the scope of the disclosure.

[0010] A package including a first chip including elevated photodiodes stacked on a second chip and the method of forming the same are provided in accordance with various exemplary embodiments. The intermediate stages of forming the package are illustrated. The variations of the embodiments are discussed. Throughout the various views and illustrative embodiments, like reference numbers are used to designate like elements.

[0011] Before addressing the illustrated embodiments specifically, aspects of various illustrated and contemplated embodiments are discussed generally. Embodiments of the present disclosure provide for a stacked device including a sensor wafer with an elevated photoelectrical conversion layer (sometimes referred to herein as a photoelectron conversion layer) and a device wafer, to form an elevated photodiode image sensor. In some embodiments, image sensor wafer 100 and device wafer 200 (FIG. 1) are stacked for face-to-face bonding. In other embodiments, image sensor wafer 100 and device wafer 200 (FIG. 2) are stacked for face-to-back bonding. In some embodiments, isolation structures are formed between pixels to improve cross-talk isolation performance. Various embodiments of the present disclosure may provide for a high fill factor of the resulting image sensor. Immunity to electrical crosstalk between adjacent pixels is an advantageous feature of some embodiments. Embodiments of the invention also provide for a flexible process tuning on each wafer.

[0012] Turning now to the illustrated embodiments, FIG. 1 schematically illustrates in cross-section view an illustrative embodiment device in which image sensor wafer 100 and device wafer 200 are stacked in a face-to-face bonding arrangement. Two pixel units 110 are illustrated on image sensor wafer 100, although many more pixel units 110 are typically formed on image sensor wafer 100. One skilled in the art will recognize the components of image sensor wafer 100, including the illustrated pixel units 110, and such components are not described in detail herein for clarity. Likewise, the components of device wafer 200, whereby electrical signals from pixel units 110 can be received and processed are schematically illustrated herein, but are not described in detail, as those details are not necessary for an understanding of the present disclosure and/or will be apparent to those skilled in the art once informed by the present disclosure.

[0013] FIG. 2 illustrates a stacked image sensor wafer 100 and device wafer 200, wherein wafers 100 and 200 are configured in a face-to-back bonding configuration. Note the different configuration of image sensor wafer 100, particularly the location of the storage nodes 112 and interconnect structures 114, for the face-to-back bonding configuration.

[0014] Intermediate steps in the manufacture of a package, such as the package illustrated in FIG. 1, are schematically illustrated in FIGS. 3a through 3c. FIG. 3a illustrates a structure in an intermediate stage of manufacture. At the stage illustrated in FIG. 3a, image sensor wafer 100, which includes a plurality of identical image sensor chips 100 therein, is formed. Storage nodes 112 and interconnect structures 114 have been formed on sensor wafer 100, and image sensor wafer 100 has been bonded in a face-to-face configuration to device wafer 200 (wherein appropriate active and passive devices and interconnects have been previously formed). Storage nodes 112 are formed of implanted regions. In some embodiments, storage nodes 112 are connected to transfer gate transistors 118, which are configured to electrically interconnect and disconnect storage nodes 112 and corresponding floating diffusion region 116 in the same pixel unit 110. In alternative embodiments, transfer gate transistors 118 are formed in device wafer 200 rather than in image sensor wafer 100. In the illustrated embodiments, interconnect structures 114 are illustrated as including one level of
interconnection. It is appreciated that a plurality of layers of dielectric layers 121, which may include low-k dielectric layers in some embodiments.

[0015] Image sensor wafer 100 also includes semiconductor substrate 120, which may be a silicon substrate, or may be formed of other semiconductor materials such as silicon germanium, silicon carbon, III-V compound semiconductor materials, or the like. Throughout the description, the side of substrate 120 including interconnect structures 114 is referred to as the front side of substrate 120 (which side is also referred to as the front side of image sensor wafer 100), and the opposite side is referred to as the back side. Accordingly, in FIG. 3a, the front side of image sensor wafer 100 faces down.

[0016] Two pixel units 110 are illustrated on image sensor wafer 100 for simplicity. Significantly more pixel units 110 are within the contemplated scope of this disclosure. Pixel units 110 are separated by isolation features 124, such as Deep Trench Isolation (DTI) structures, which are formed of, or comprise, a dielectric material such as an oxide (silicon oxide, for example) and/or a nitride (silicon nitride, for example). DTI structures 124 may extend from the back surface of substrate 120 into substrate 120. Furthermore, in some embodiments, DTI structures 124 may penetrate substrate 120, and extend from the front surface 120A (the surface facing down) to the back surface 120B of substrate 120. In the top view of the structure in FIG. 3a, DTI structures 124 may be interconnected to form a continuous grid, with pixel units 110 include portions in the grid openings, and portions outside and vertically aligned to the grid openings of the grid. Alternatively stated, DTI structures 124 include a plurality of rings, each encircling a portion of each pixel units 110.

[0017] FIG. 3a also illustrates a cross-sectional view of device wafer 200, which comprises a plurality of identical device chips 200T therein. Device wafer 200 includes substrate 220, and logic circuit 223 formed at the front surface of substrate 220. Substrate 220 is a silicon substrate in some embodiments. Alternatively, substrate 220 is formed of other semiconductor materials such as silicon germanium, silicon carbon, III-V compound semiconductor materials, or the like. In accordance with some exemplary embodiments, logic circuit 223 includes read out circuits 222. Each of read out circuits 222 may include a plurality of transistors, such as row selector 226, source follower 228, and reset transistor 230. Row selectors 226, source followers 228, and reset transistors 230 may form portions of pixel units 110, with each of pixel units 110 including one of row selectors 226, one of source followers 228, and one of reset transistors 230. Accordingly, each of pixel units 110 may extend into device wafer 200 to include one of read out circuits 222.

[0018] Logic circuit 222 may also include one or more of Image Signal Processing (ISP) circuits such as Analog-to-Digital Converters (ADCs), Correlated Double Sampling (CDS) circuits, row decoders, and the like, which may also be considered as parts of the read out circuits. Interconnect structure 214 is formed over, and electrically coupled to, logic circuit 223. Interconnect structure 214 includes a plurality of metal layers in a plurality of dielectric layers 221, with metal lines and vias disposed in dielectric layers 221. In some exemplary embodiments, dielectric layers 221 include low-k dielectric layers. The low-k dielectric layers may have low k values lower than about 3.0. Dielectric layers 221 may further include a passivation layer formed of non-low-k dielectric materials having k values greater than 3.9. In some embodiments, the passivation layer includes a silicon oxide layer, a silicon nitride layer, an Un-doped Silicate Glass (USG) layer, and/or the like.

[0019] Metal pads 142 and 242 are formed at the surfaces of wafers 100 and 200, respectively, wherein metal pads 142 and 242 may have their top surfaces substantially level with the top surfaces of the top ones of dielectric layers 121 and 221, respectively. Metal pads 142 and 242 may also comprise copper, aluminum, and possibly other metals. Metal pads 142 are bonded to the respective metal pads 242, so that the devices in wafers 100 and 200 are electrically coupled to each other. In some embodiments, as a result of the bonding, each of the pixel units 110 includes a portion in wafer 100 and a portion in wafer 200, which are electrically connected to each other to form an integrated functional pixel unit that may generate electrical signals in response to photon stimulation, and store and output the electrical signals in response to the commands for reading and resetting the electrical signals.

[0020] As shown in FIG. 3a, the backside of image sensor wafer 100 is thinned down (symbolized by arrow 145) after the bonding of wafers 100 and 200. The resulting semiconductor substrate 120 may have a thickness smaller than about 10 μm, or smaller than about 5 μm. Image sensor wafer 100 can be thinned down, e.g., by mechanical grinding/polishing, through chemical mechanical polishing, through etching, or the like. The thickness is an artifact of the technology node and the desired device properties, and can be adjusted through routine experimentation.

[0021] As shown in FIG. 3b, portions of the backside of substrate 120 are further thinned down to expose respective storage nodes 112 in the respective pixel units 110. The thinning down may be performed by selectively etching substrate 120, and DTI structures 124 are not etched. As a result, back surface 120B of substrate 120 is lower than the top ends 124A of DTI structures 124. Pixel electrodes 144 are formed in electrical communication with respective storage nodes 112. In some embodiments, pixel electrodes 144 are also referred to as bottom electrodes 144.

[0022] While other conductive materials are within the contemplated scope of the present disclosure, examples of available materials for bottom electrodes 144 include Al, TiN, Cr, and the like. Bottom electrodes 144 can be deposited using techniques such as Chemical Vapor Deposition (CVD), Physical Vapor Deposition (PVD), Plasma Enhanced Chemical Vapor Deposition (PECVD), Metal Organic Chemical Vapor Deposition (MOCVD), sputtering, and the like. In the illustrated embodiments, bottom electrodes 144 are formed to a thickness of between about 0.3 μm and about 0.8 μm. Bottom electrodes 144 may be in contact with the respective underlying storage nodes 112 to establish the electrical connection.

[0023] Photoelectrical conversion layers 146 are formed over and in electrical communication with (and may be in contact with) bottom electrodes 144, as shown in FIG. 3c. Transparent top electrode 148 is formed over and in electrical communication with photoelectrical conversion layers 146. By way of example, and not by way of limitation, photoelectrical conversion layers 146 could comprise amorphous silicon, a quantum dot layer, an organic material, or the like. Likewise, top electrode 148 could comprise Indium Tin Oxide (ITO), although one skilled in the art will recognize suitable alternatives through routine experimentation once informed by the present disclosure. Photoelectrical conver-
sion layers 146 may be separated from each other by DTI structures 124. Top electrode 148 may be a continuous layer having its bottom surface contacting the top surfaces of photoelectrical conversion layers 146 and DTI structure 124. Each of Bottom electrodes 144, photoelectrical conversion layers 146 and the respective overlying portion of top electrode 148 forms an elevated photodiode 149, which is different from conventional photodiodes that are built in semiconductor substrates.

[0024] Referring back to FIG. 1, in accordance with some exemplary embodiments, additional components such as color filters 150, micro-lenses 152, and the like, are further formed on the backside of image sensor wafer 100. The resulting stacked wafers 100 and 200 are then shaved apart into packages, wherein each of the packages includes one chip 100 from image sensor wafer 100 and one chip 200 from device wafer 200.

[0025] FIGS. 4a through 4c illustrate intermediate steps in the manufacture of a package, such as a face-to-back structure illustrated in FIG. 2. Unless specified otherwise, the materials and formation methods of the components in these embodiments are essentially the same as the like components, which are denoted by like reference numerals in the embodiments shown in FIGS. 1 and 3a through 3c. The details regarding the formation process, the materials, and the specification, of the components shown in FIGS. 2 and 4a through 4c may thus be found in the discussion of the embodiment shown in FIGS. 1 and 3a through 3c.

[0026] As discussed above, image sensor wafer 100 that is used for a face-to-back configuration differs from image sensor wafer 100 suitable for a face-to-face configuration. For example, as shown in FIG. 4a, photodiodes 149 (including the transparent top electrode 148, photoelectrical conversion layers 146, and bottom electrodes 144) are formed over both substrate 120 and interconnect structure 114. Storage nodes 112 and respective photodiodes 149 are electrically connected to each other through one or more intervening conductive interconnect structure 114, as shown. Isolation structures 124 in these embodiments may have top surfaces level with the top surfaces of photoelectrical conversion layers 146, and bottom surfaces level with the bottom surfaces of bottom electrodes 144.

[0027] Image sensor wafer 100 is substantially complete in the stage of manufacture illustrated in FIG. 4a with color filter 150 and/or micro-lens 152 having been formed adjacent to photodiodes 149. Image sensor wafer 100 is shown mounted to carrier 54, such as a glass substrate. This may be accomplished using adhesive layer 56 to adhere carrier 54 to image sensor wafer 100. Quartz, silicon, or other materials could be used in lieu of glass. After mounting image sensor wafer 100 to carrier 54, the backside of image sensor wafer 100 is thinned (symbolized by arrow 145), for example, using a process similar to those described regarding FIG. 3a.

[0028] Note in these embodiments, it is not necessary to expose storage nodes 112 in the wafer thinning process. This is partially because the electrical contact to the storage nodes 112 is made from the top of the storage node, i.e. the surface away from the backside surface of wafer 100. After image sensor wafer 100 is thinned to a desired thickness, oxide layer 58 is formed on the backside, as shown in FIG. 4b. In some embodiments, oxide layer 58 comprises silicon oxide, and may be formed using a deposition method such as PECVD. Vias 60, sometimes referred to as through-vias 60, and sometimes referred to as through-substrate vias or through-silicon vias (TSVs) are also formed extending from the surface of the backside of image sensor wafer 100 up to the interconnect structure 114. Various electrical connections can be made in this manner. Although one via 60 is shown in FIG. 4b, multiple vias and hence multiple electrical connections can be formed. Furthermore, each of pixel units 110 may include one or more via. Dashed lines 125 are drawn to represent the likely electrical connections between vias 60 and the devices in wafer 100.

[0029] FIG. 4c illustrates the process of bonding the back side of image sensor wafer 100 to the front side of a device wafer. Dashed lines 225 are also drawn to represent the electrical connections between vias 60 and logic circuits 223. Device wafer 200 may be essentially the same as illustrated in FIG. 3a, for instance. In the embodiments of FIG. 4c, however, it is desirable that device wafer 200 has an appropriate bonding surface on its front side (the side with interconnect structure 214) to ensure adequate adhesion and bonding to image sensor wafer 100. Care should be taken to properly align image sensor wafer 100 and device wafer 200 in the bonding process to ensure that contacts formed on the respective wafers 100 and 200 align with one another to form good electrical contact between the devices on the respective wafers 100 and 200. Carrier 54 and adhesive layer 56 can then be removed, and a singulation is performed to saw the bonded wafers 100 and 200 into a plurality of packages, each including one chip 100 from wafer 100, and one chip 200 from wafer 200, resulting in the structure illustrated in FIG. 2 in accordance with exemplary embodiments.

[0030] The illustrated embodiments provide the advantageous feature that the processes of the image sensor wafers can be optimized for forming the pixel elements. Furthermore, processes can be optimized for forming the supporting circuitry such as the read out circuits in the device wafers. This is advantageous since the image sensor wafers and the device wafers have different process requirements. Accordingly, by separating the manufacturing processes, the manufacturing processes of the image sensor wafers and the device wafers do not affect each other. Furthermore, by forming elevated photodiodes, the fill factors of the photodiodes may be maximized since it is not affected by the metal routing or any transistor in the respective wafer.

[0031] In accordance with some embodiments, a device includes an image sensor chip having formed therein an elevated photodiode; and a device chip underlying and bonded to the image sensor chip, the device chip having a read out circuit electrically connected to the elevated photodiode.

[0032] In accordance with other embodiments, a device includes an image sensor chip and a device chip. The image sensor chip includes a first semiconductor substrate, an elevated photodiode overlying the first semiconductor substrate, and a first interconnect structure electrically coupled to the elevated photodiode. The device chip is underlying and bonded to the image sensor chip. The device chip includes a second semiconductor substrate, and a read out circuit at a top surface of the second semiconductor substrate. The read out circuit is electrically coupled to the elevated photodiode. The device chip further includes a second interconnect structure overlying the first semiconductor substrate.

[0033] In accordance with yet other embodiments, a method includes forming an elevated photodiode over a semi-
conductor substrate of an image sensor wafer, and bonding together the image sensor wafer and a device wafer, wherein the device wafer includes a read out circuit electrically coupled to the elevated photodiode.

Although the embodiments and their advantages have been described in detail, it should be understood that various changes, substitutions and alterations can be made herein without departing from the spirit and scope of the embodiments as defined by the appended claims. Moreover, the scope of the present application is not intended to be limited to the particular embodiments of the process, machine, manufacture, and composition of matter, means, methods and steps described in the specification. As one of ordinary skill in the art will readily appreciate from the disclosure, processes, machines, manufacture, compositions of matter, means, methods, or steps, presently existing or later to be developed, that perform substantially the same function or achieve substantially the same result as the corresponding embodiments described herein may be utilized according to the disclosure. Accordingly, the appended claims are intended to include within their scope such processes, machines, manufacture, compositions of matter, means, methods, or steps. In addition, each claim constitutes a separate embodiment, and the combination of various claims and embodiments are within the scope of the disclosure.

1. A package comprising:
   an image sensor chip having formed therein an elevated photodiode; and
   a device chip underlying and bonded to the image sensor chip, the device chip having a read out circuit electrically connected to the elevated photodiode.

2. The package of claim 1, wherein the image sensor chip comprises:
   a semiconductor substrate underlying the elevated photodiode; and
   a first interconnect structure underlying the semiconductor substrate and electrically coupled to the elevated photodiode through features in the semiconductor substrate.

3. The package of claim 2, wherein the image sensor chip further comprises a storage node in the semiconductor substrate, wherein the storage node inter-couples the elevated photodiode and the first interconnect structure.

4. The package of claim 3, wherein the elevated photodiode further comprises:
   a bottom electrode over and contacting the storage node;
   a photoelectrical conversion layer over the bottom electrode; and
   a top electrode over the photoelectrical conversion layer.

5. The package of claim 1, wherein the image sensor chip comprises:
   a semiconductor substrate; and
   a through-via extending from a top surface to a bottom surface of the semiconductor substrate, wherein the through via electrically couples the read out circuit to the elevated photodiode.

6. The package of claim 5, wherein the image sensor chip further comprises an interconnect structure over the semiconductor substrate, and wherein the elevated photodiode is over the interconnect structure.

7. The package of claim 1 further comprising a deep trench isolation forming an isolation ring encircling a bottom electrode and a photoelectrical conversion layer of the elevated photodiode.

8. The package of claim 7, wherein the isolation ring extends through a semiconductor substrate of the image sensor chip.

9. A package comprising:
   an image sensor chip comprising:
   a first semiconductor substrate;
   an elevated photodiode overlying the first semiconductor substrate;
   a first interconnect structure electrically coupled to the elevated photodiode; and
   a device chip underlying and bonded to the image sensor chip, wherein the device chip comprises:
   a second semiconductor substrate;
   a read out circuit at a top surface of the second semiconductor substrate, wherein the read out circuit is electrically coupled to the elevated photodiode; and
   a second interconnect structure overlying the first semiconductor substrate.

10. The package of claim 9, wherein the first interconnect structure is underlying the first semiconductor substrate, and wherein the read out circuit is electrically coupled to the elevated photodiode through the first and the second interconnect structures.

11. The package of claim 10 further comprising a storage node in the first semiconductor substrate and coupled between the elevated photodiode and the first interconnect structure.

12. The package of claim 9, wherein the first interconnect structure is over the first semiconductor substrate, wherein the read out circuit is electrically coupled to the elevated photodiode through a via penetrating through the first semiconductor substrate.

13. The package of claim 9 further comprising a deep trench isolation comprising:
   a first portion forming an isolation ring encircling a bottom electrode and a photoelectrical conversion layer of the elevated photodiode; and
   a second portion penetrating through the first semiconductor substrate of the image sensor chip.

14. The package of claim 9 further comprising:
   a color filter overlying and aligned to the elevated photodiode; and
   a micro-lens overlying and aligned to the color filter.

15-20. (canceled)

21. A package comprising:
   an image sensor chip comprising:
   a semiconductor substrate:
   a storage node in the semiconductor substrate;
   an elevated photodiode over the semiconductor substrate, wherein the elevated photodiode comprises:
   a bottom electrode over and electrically coupled to the storage node;
   a photoelectrical conversion layer over the bottom electrode; and
   a top electrode over the photoelectrical conversion layer;
   an interconnect structure underlying the semiconductor substrate and electrically coupled to the elevated photodiode through the storage node; and
   a device chip underlying and bonded to the image sensor chip, the device chip having a read out circuit electrically coupled to the elevated photodiode through the interconnect structure and the storage node.
22. The package of claim 21 further comprising:
a color filter overlying and aligned to the elevated photo-
diode; and
a micro-lens overlying and aligned to the color filter.
23. The package of claim 21 further comprising a deep
trench isolation comprising:
a first portion forming an isolation ring encircling the bot-
tom electrode and the photoelectrical conversion; and
a second portion penetrating through the semiconductor
substrate of the image sensor chip.
24. The package of claim 23, wherein a sidewall of the first
portion of the deep trench isolation is continuously connected
to a sidewall of the second portion of the deep trench iso-
lation, with no discontinuity formed therebetween.
25. The package of claim 21 further comprising a transfer
gate transistor having a source-drain path electrically coupled
between the storage node and the interconnect structure.
26. The package of claim 21, wherein the read out circuit
comprises a row selector, a source follower, and a reset tran-
sistor, and wherein the row selector, the source follower, and
the reset transistor form a portion of a pixel unit.

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