

United States Patent

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[54] METHOD OF PRODUCING A PLANAR-TRANSISTOR

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[51] Int. Cl. B01J 17/00, H01L 5/00

[58] Field of Search 29/576 T, 578, 589, 590; 148/187, 189

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Primary Examiner—John F. Campbell

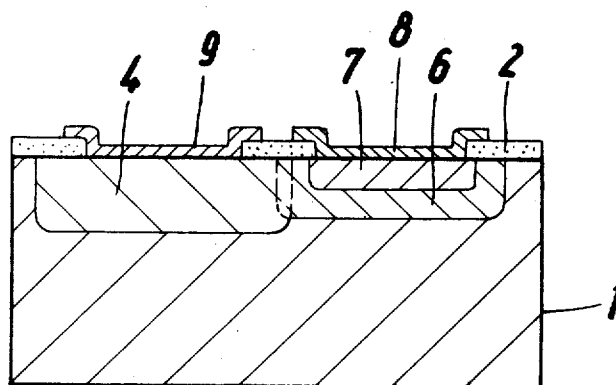
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[57] ABSTRACT

A method of producing a planar transistor by forming a window in a passivating layer on a semiconductor body, diffusing into the semiconductor body through this window an emitter region and a base region in either order, forming a second window adjacent the first window and diffusing a base contact region there through to a depth such as to make contact with the base region. Electrodes are then provided in the first window for the emitter region and in the second window for the base region. Either window may be formed first depending on the diffusing arrangements.

16 Claims, 20 Drawing Figures



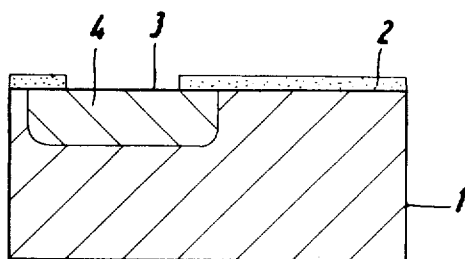


Fig. 1

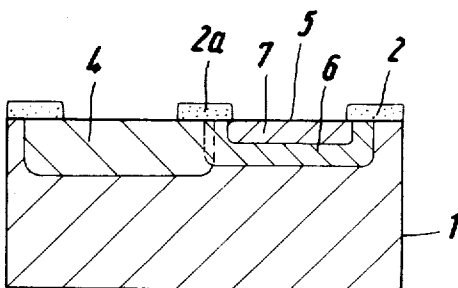


Fig. 2

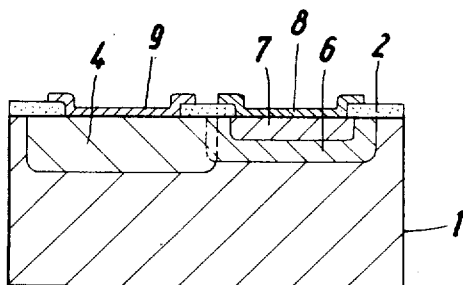
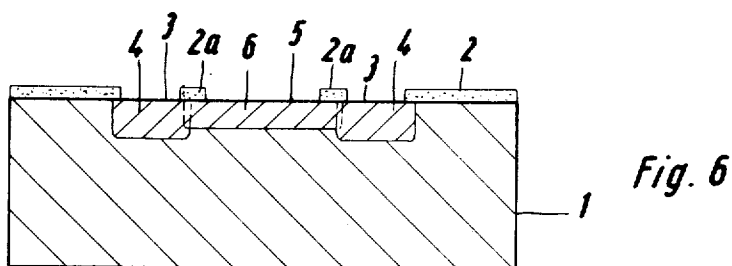
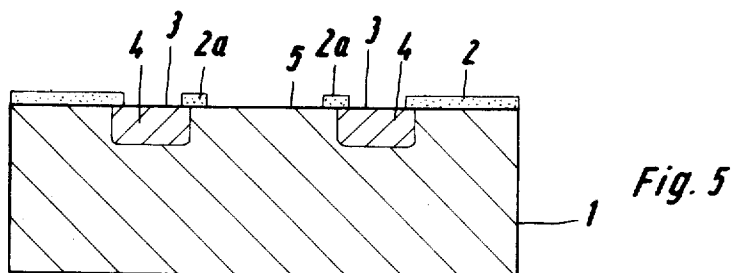
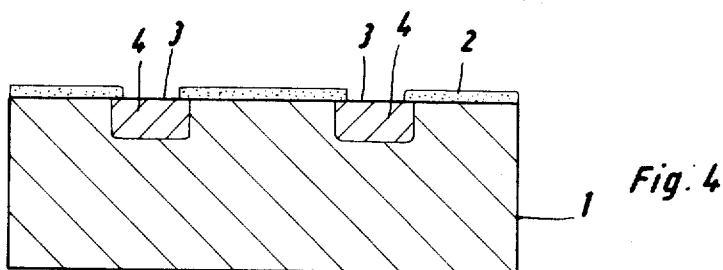


Fig. 3

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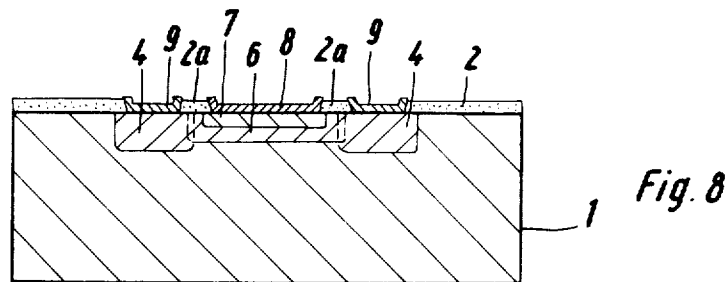
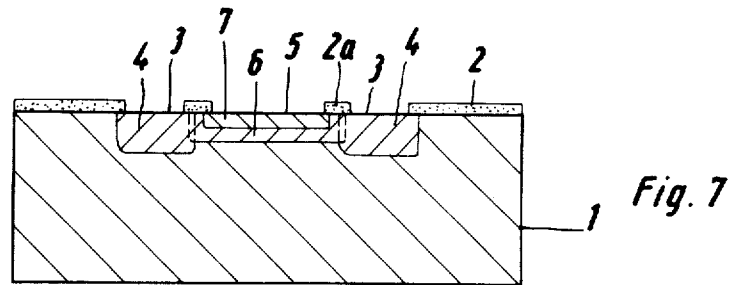
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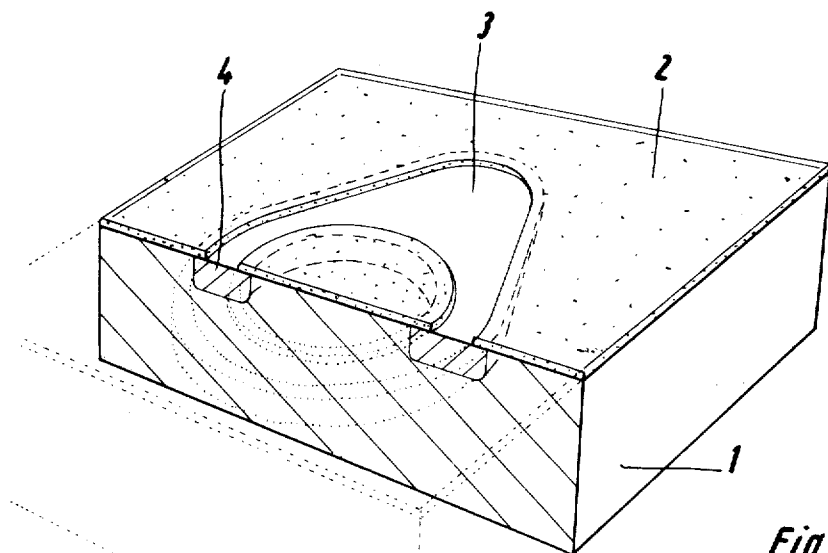


Fig. 9

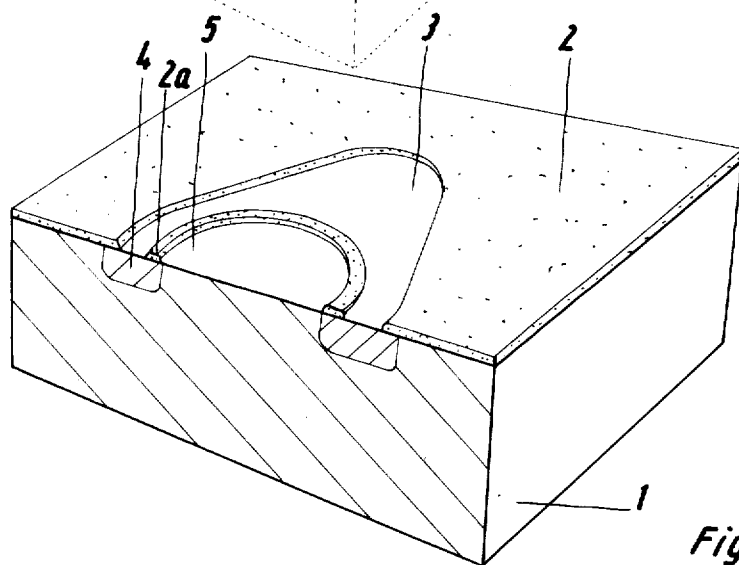


Fig. 10

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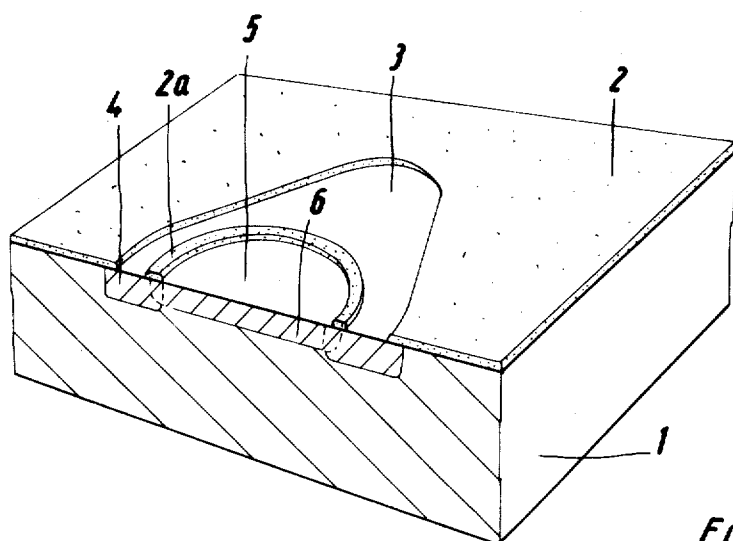


Fig. 11

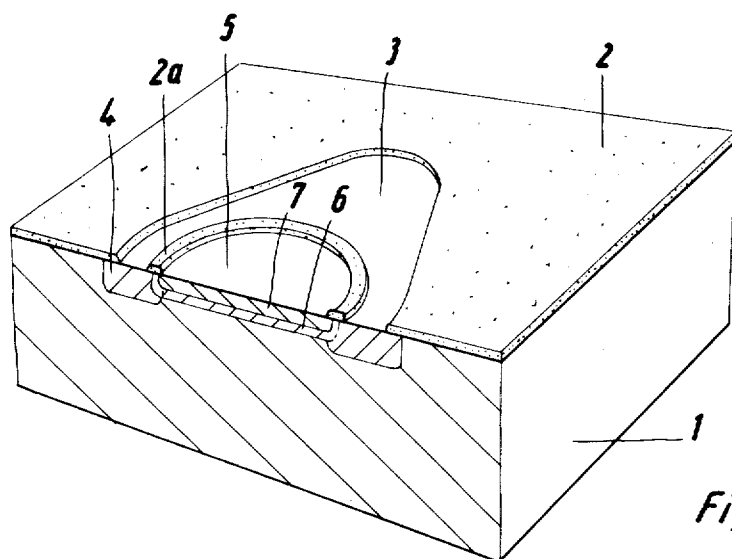
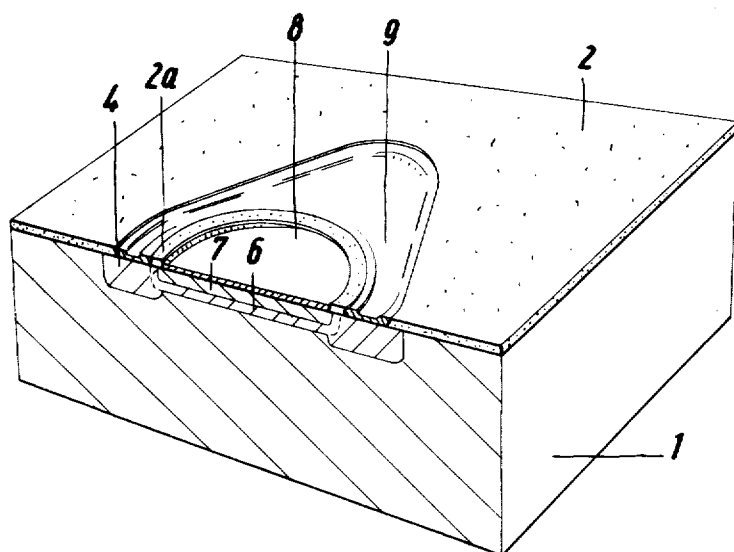


Fig. 12

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Fig. 13



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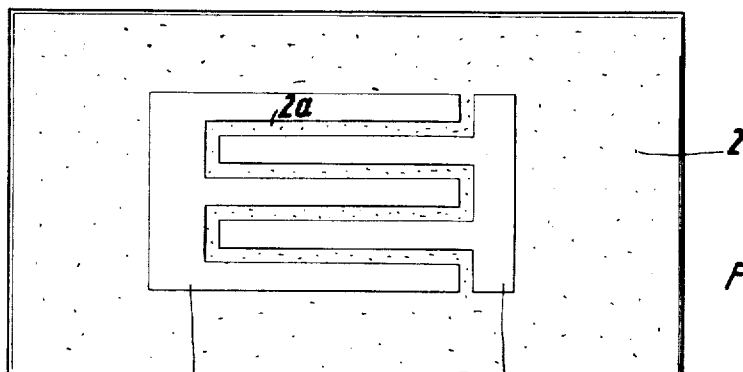


Fig. 14

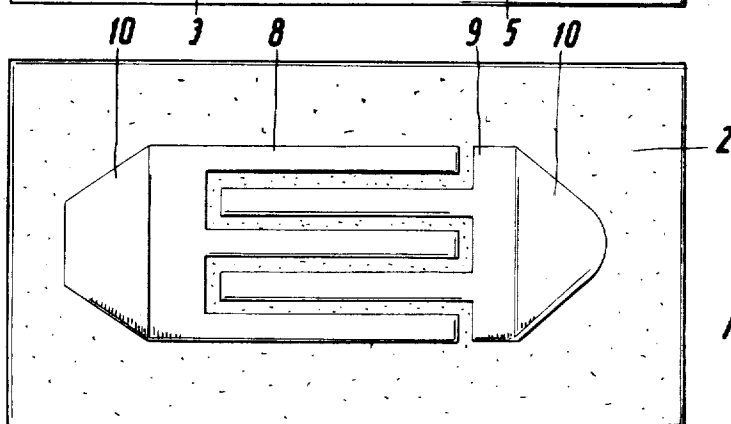


Fig. 15

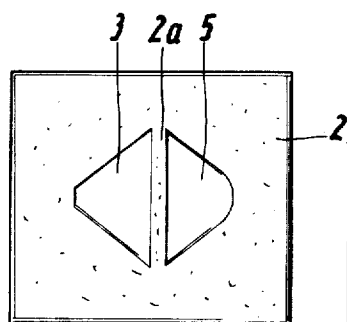


Fig. 16

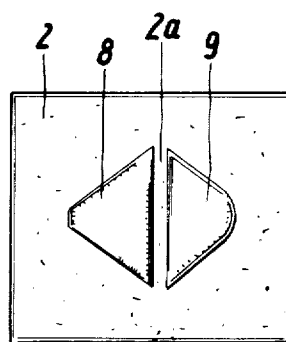


Fig. 17

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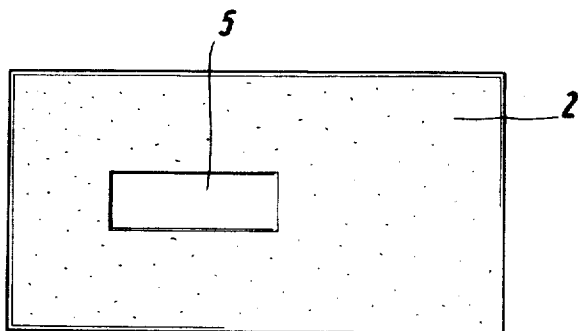


Fig. 18

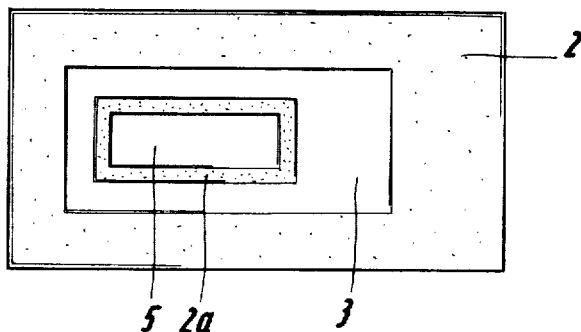


Fig. 19

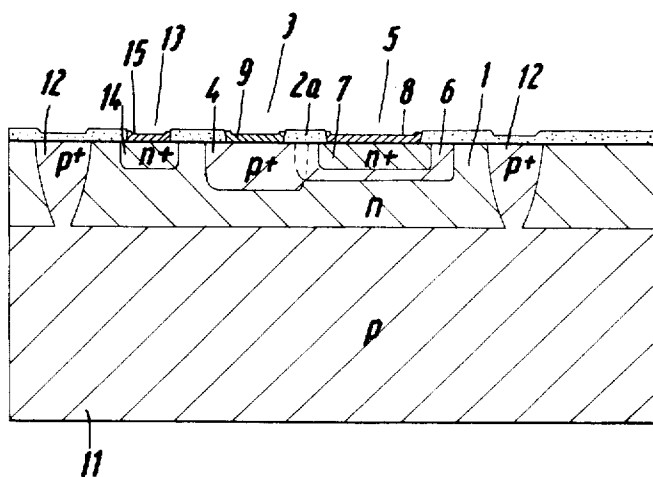


Fig. 20

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METHOD OF PRODUCING A PLANAR-TRANSISTOR

BACKGROUND OF THE INVENTION

This invention relates to a method of producing a planar transistor.

In the production of planar transistors it is known that the starting point is a semiconductor body, the surface of which is coated with a diffusion-inhibiting passivation layer which consists, for example of silicon dioxide or silicon nitride. If silicon is used as semiconductor material, the passivation layer, which is frequently simply called an insulating layer, may be produced by oxidizing the silicon surface for example. A layer of silicon dioxide or also a layer of silicon nitride may, however, be provided on the semiconductor surface by means of a pyrolytic processes. With semiconductor bodies other than those of silicon, this process is actually inevitable. According to the present-day technique, the base window is first etched, by means of the photo-etching technique, in the passivation layer produced on the semiconductor surface, and then the base region of the transistor is diffused into the semiconductor body through this window. Then the semiconductor surface including the base window is coated with a second passivation layer and the emitter window is etched in the second passivation layer, again by means of a photo-etching technique, in such a manner that it is above the (larger) area of the base window. After indiffusion of the emitter region through the emitter window, the planar transistor is, in principle, finished because the collector region is formed by the semiconductor body. Non-rectifying contacts now have only to be provided at the surface of the emitter region and the surface of the base region, separately from one another, while contact is made to the collector region by providing a contact on the semiconductor body in general, at the side opposite the emitter region.

One disadvantage of this known method of producing planar transistors consists in that, after the indiffusion of the base region, a second passivation process has to be carried out with subsequent adjustment of the emitter region for the photo-etching technique. Particularly with very fine structures (small base area), rejects may occur as a result of this adjustment. In addition, the base area in the known planar transistors is always considerably larger than the emitter area which makes the base-collector capacitance relatively high.

SUMMARY OF THE INVENTION

It is an object of the invention to provide a method which of producing a planar transistor in which these disadvantages are obviated or substantially reduced.

According to the invention there is provided a method of producing a planar transistor comprising forming a passivation layer on a semiconductor body, forming a first window in said passivating layer, diffusing a base region and an emitter region into said semiconductor body through said first window, making electrical contact to said emitter region through said window, forming a second window adjacent said first window and diffusing through said second region a base contact region of the same conductivity as said base region and of an extent sufficient to provide contact between said base region and said base contact region.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will now be described in greater detail, by way of example, with reference to the accompanying drawings in which:

FIG. 1 is a sectional view of a semiconductor body at a first stage of a method of producing a planar transistor in accordance with a first embodiment of the invention,

FIG. 2 is a section view similar to FIG. 1 but showing a second stage of the first embodiment,

FIG. 3 is a sectional view similar to FIG. 1 but, showing a third stage of the first embodiment.

FIG. 4 is a sectional view of a semiconductor body at a first stage of producing a planar transistor in accordance with a second embodiment of the invention;

FIG. 5 is a sectional view similar to FIG. 4 but showing a second stage of the second embodiment;

FIG. 6 is a sectional view similar to FIG. 4, but showing a third stage of the second embodiment;

FIG. 7 is a sectional view similar to FIG. 4, but showing a fourth stage of the second embodiment;

FIG. 8 is a sectional view similar to FIG. 4 but showing a fifth stage of the second embodiment;

FIG. 9 is a perspective view partly in section of the semiconductor body as shown in FIG. 4;

FIG. 10 is a perspective view partly in section of the semiconductor body as shown in FIG. 5;

FIG. 11 is a perspective view partly in section of the semiconductor body as shown in FIG. 6;

FIG. 12 is a perspective view partly in section of the semiconductor body as shown in FIG. 7;

FIG. 13 is a perspective view partly in section of the semiconductor body as shown in FIG. 8;

FIG. 14 is a plan view of a semiconductor body at a stage prior to the application of electrodes and showing a modification of the arrangement of diffusion windows.

FIG. 15 is a plan view similar to FIG. 14 with electrodes applied;

FIG. 16 is a plan view of a semiconductor body prior to the application of a electrodes showing a further modification of the diffusion windows, and

FIG. 17 is a plan view similar to FIG. 16 with the electrodes applied.

FIG. 18 is a plan view of a passivation layer on a semiconductor body at a first stage of a method of producing a planar transistor in accordance with a further embodiment of the invention.

FIG. 19 is a plan view similar to FIG. 18 but showing a second stage of the embodiment begun in FIG. 18.

FIG. 20 is a sectional view of a semiconductor body containing an n-p-n transistor produced according to the invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Basically, the method of the invention consists in that in the production of a planar transistor, the emitter region and the base region of the transistor is diffused through the same window in a passivation layer on the surface of the semiconductor body, and in that contact should be made to the emitter region likewise through this window, whereas contact to the base region on the other hand should be made through a separate base

contact window adjacent to the emitter contact window. The electrical connection necessary in the semiconductor body, between the base electrode and the base region, is produced by means of a diffusion region of the same conductivity type as the base region which is diffused into the semiconductor body through the base contact window. Both the aperture in the passivation layer designated as an emitter contact window and the aperture in the passivation layer designated as a base contact window have a plurality of function with this method, because the emitter contact window serves at the same time as emitter-diffusion and base-diffusion window and the base contact window also serves as diffusion window for the connecting region to the base region.

With the method according to the invention, the base contact window is preferably first produced in the passivation layer and then the region of the same conductivity type as the base region, which established the connection to the base region, is diffused into the semiconductor body through the base contact window. Only then is the emitter contact window produced and the base region and the emitter region are diffused into the semiconductor body through this window.

In a preferred embodiment of the invention, the base contact window remains open during the base diffusion and emitter diffusion. In this case, the region having the same conductivity type as the base region is indiffused with such a high surface concentration that its type of conductivity is not altered despite counter-doping by the emitter diffusion impurities penetrating into the open base contact window during the emitter diffusion and its conductivity does not drop below the value necessary for a connection between the base region and the base electrode. The region of the same conductivity type as the base region is preferably diffused deeper into the semiconductor body than the base region.

Between the base contact window and the emitter contact window, which are separated from one another, is part of the passivation layer which may be termed a web. The width of this web is preferably less than the sum of the penetration depths of the base region and the region of the same conductivity type as the base region.

In one embodiment of the invention, an annular base contact window is introduced into the passivation layer, and after the diffusion of the region of the same conductivity type as the base region, the emitter contact window, through which the base region and the emitter region are diffused into the semiconductor body, is introduced into the portion of the passivation layer surrounded by the annular base contact window. There is also the possibility of making the base contact window and the emitter contact window comb-shaped for example and arranging the two comb structures so that they interengage.

In another form of construction of the invention, the emitter contact window is first introduced into the passivation layer and the emitter region is diffused into the semiconductor body through this window. Only after this is the base contact window introduced into the passivation layer and at the same time the base region and the region of the same conductivity type as the base region are diffused into the semiconductor body

through the emitter contact window and base contact window respectively. This method is preferably used when the impurities producing the base region diffuse more quickly than the impurities producing the emitter region. The base contact window, which is produced later than the emitter contact window in this method may be disposed in the form of a ring around the emitter contact window.

A further embodiment of the invention consists in that, after non-rectifying contact has been made to the emitter region and the contact region of the same conductivity type as the base region, the entire passivation layer is removed and replaced by a fresh passivation layer which is applied pyrolytically by cathode sputtering or by vapor-deposition, and is only partially removed again over the electrodes.

The passivation layer consists, for example, of silicon dioxide or of silicon nitride. The diffusion regions may be produced for example by means of the so-called powder diffusion under protective gas or under vacuum. Whereas contact is made to the emitter region and to the base region at one surface of the semiconductor body, contact is preferably made to the collector region at the opposite side of the semiconductor body by applying an electrode to the semiconductor body. In integrated switching circuits, on the other hand, the making of contact to the collector region is generally likewise effected at the emitter side.

The making of non-rectifying contact to the emitter region and the region of the type of conductivity of the base region may be effected, for example, by means of an electrodeless electrolytic deposition of metal layer which consist for example of gold, platinum metals, silver, nickel or copper. A layer of glass formed during the diffusion in an oxidizing atmosphere is removed before the metal deposition in the contact windows.

The invention may be used for example in the manufacture of planar transistors of npn or pnp type with a semiconductor body of silicon, germanium or an $A^{III}-B^V$ compound. Radio-frequency and radio-frequency power transistors can be produced in accordance with the invention for example and may naturally also be elements of an integrated circuit.

Referring to FIG. 1 to 3 of the drawings, in order to produce a planar transistor in accordance with the invention, the starting point is a semiconductor body 1 as shown in FIG. 1, one surface of which is covered with a passivating layer 2 which consists of silicon dioxide or of silicon nitride for example. Introduced into the passivating layer 2 is a base contact window 3 through which impurities are diffused which produce the same type of conductivity in the semiconductor body as has the base region of the transistor. During this diffusion, the semiconductor region 4 of the same conductivity type as the base region is formed, the purpose of which is to establish an electrical connection to the base region still to be produced. The region 4 may therefore be termed a contact region which electrically connects the base region to the base electrode still to be produced inside the base contact window 3. Thus the base contact window has two functions, serving on the one hand as a diffusion window during the production of a contact region 4 of the same conductivity type as the base region and on the other hand, as its name implies, as a contact window for the base electrode.

After the production of the region 4 by diffusion, a further aperture 5 is introduced into the passivating layer as shown in FIG. 2, as an emitter contact window. Like the base contact window 3, however, the emitter contact window 5 has a plurality of functions because not only is contact made to the emitter region through this window but also the base region 6 is diffused through it as shown in FIG. 2 followed by the emitter region 7 as shown in FIG. 3.

During the diffusions, the following points should be observed. The indiffusion of the contact region 4 of the same conductivity type as the base region is effected more deeply and with a substantially higher surface concentration than the subsequent base diffusion during which the base region 6 is formed in the semiconductor body. During the production of the contact region 4, the surface concentration is selected so high that during the subsequent emitter diffusion no blocking p-n junction develops between the base region and the area of the contact region 4 covered by the emitter diffusion. In this connection, it should be borne in mind that during the emitter diffusion not only the emitter contact window 5 but also the base contact window 3 is open so that the emitter diffusion impurities pass not only through the emitter contact window but also through the base contact window into the semiconductor body. Accordingly, the emitter diffusion impurities cause a counter-doping in one area of the contact region 4 but this should not go so far that a reversal of the doping in the contact region 4 comes about. The reversal of the doping can be prevented by selecting the surface concentration appropriately high during the production of the contact region 4.

As FIG. 2 shows, the emitter contact window 5 is separated from the base contact window 3 by a web 2a which is part of the passivating layer 2. The width of this web 2a is so dimensioned that the sum of the penetration depth of the contact region 4 and of the base region 6 is greater than the width of the web 2a. This ensures that the contact region 4 and the base region 6 overlap under the web 2a. In order to establish an electrical connection between the base region and the base electrode by means of the contact region 4, it is a prerequisite that the contact region and the base region should overlap or at least touch one another.

The non-rectifying electrodes necessary for making contact at the emitter region and the contact region can be applied particularly simply in the method according to the invention. Because both the contact region 4 and also the emitter region 7 preferably have a surface concentration above the so-called degeneracy, that is to say have a quasi-metallic conductivity, a simple metal-to-semiconductor contact is sufficient for the non-blocking contact-making. Such contacts can be produced in a simple manner by cathode sputtering or by vapor-deposition and annealing of metal layers or, in accordance with the invention, because of the high surface conductivities, they may be produced in the two regions by means of currentless precious metal depositions, Gold, silver and metals in the platinum group, or even nickel and copper, are particularly suitable for this.

Currentless metalizing may be obtained for example by simply dipping the finished semiconductor body in an appropriate metal bath, in which a metal layer is

deposited on the semiconductor surface only in the apertures in the passivation layer. In this manner, metallizing of the emitter region and of the contact region of the same conductivity type as the base region, and hence the emitter electrode 8 and the base electrode 9 as shown in FIG. 3, are obtained without the masking and vapor-deposition process otherwise usual. Contact may be made to the collector region, for example at the opposite side, by providing an electrode on the semiconductor body or by soldering the semiconductor body to a header.

The production of the emitter electrode and the base electrode is not only very simple according to the invention but also has the advantage that the electrodes can be precisely situated because the same apertures and hence the same structure in the passivation layer are used both for the diffusion of the regions to which contact is to be made and also for making contact thereto by metal deposition. The metal layers deposited, which represent the emitter electrode and base electrode, may also be alloyed on or sintered on.

The invention has the advantage in comparison with known methods that two difficult adjusting processes are saved, namely firstly between the base diffusion and the emitter diffusion and secondly before the production of the electrodes for making contact to the base region and the emitter region. In known methods, a diffusion window is used for the base diffusion different from that for the emitter diffusion so that a precise adjustment has to be made before the emitter diffusion, because the emitter window cannot be situated at random within the area of the base region. With known methods, the same applies to the adjustment during the production of the base contact window and the emitter contact window. In contrast, in the invention, as a result of saving two important adjusting operations, the output is increased in the manufacture of planar transistors and above all the manufacture of very firm transistor structures and integrated switching circuits is more economical.

A further example of an embodiment of the invention is described below wherein the starting point for producing a planar transistor as shown in FIG. 4 is again a semiconductor body 1 of the same conductivity type as the collector region. The collector body 1 consists, for example, of silicon of n-type conductivity while the passivation layer 2 consists for example of a layer of quartz about 3000 Å thick, produced by oxidation, and a layer of silicon nitride about 300 Å thick deposited pyrolytically thereon.

In this example, an annular base contact window 3, through which the contact region 4 is diffused into the semiconductor body 1, is etched in the passivation layer 2. The contact region 4 which is produced by indiffusion of boron for example is likewise annular in construction. The boron diffusion is effected to a depth of about 10μ with a surface concentration of, for example $5 \cdot 10^{20}$ impurity atoms per cm^3 .

After the production of the contact region 4, a further aperture is formed in the passivation layer 2, as shown in FIG. 5, namely the emitter contact window 5 which is situated concentrically inside the base contact window 3. A narrow annular web 2a remains between the emitter contact window and the base contact window as part of the passivation layer 2. The width of this

web may amount to about 5μ for example. The base region 6 is now diffused into the semiconductor body 1 through the emitter contact window 5 as shown in FIG. 6, likewise by means of a boron diffusion for example. With this boron diffusion, the diffusion depth amounts to 2μ for example and the surface concentration to about 3.10^{19} impurity atoms per cm^3 . The two boron profiles, which originate from the contact diffusion and the base diffusion, overlap below the web 2a.

After the base diffusion, the borate glass formed during this diffusion is removed from the emitter contact window 5 and then the emitter region 7 is diffused into the semiconductor body through this window as shown in FIG. 7. The emitter region may be produced, for example, by indiffusion of phosphorus which is diffused into the semiconductor body to a depth of about 1.5μ with a surface concentration of 2.10^{20} impurity atoms per cm^3 . The emitter-to-base p-n junction is formed as a result of the emitter diffusion while, despite diffusion of the emitter impurities through the base contact window, the contact region 4 below it cannot have its doping reversed because of the higher boron concentration.

After the emitter diffusion, the phosphate glass is removed above the emitter region 7 as well as above the contact region 4. If the diffusions are carried out not in an oxidizing atmosphere but under high vacuum or in an atmosphere of rare gas or hydrogen, for example as powder diffusions, no borate or phosphate glass at all is formed so that the removal of the glass is eliminated. In this case, the diffusions may be carried out in succession without any intermediate process.

In order to make contact to the semiconductor device, the silicon body 1 may be boiled in a gold bath for currentless gilding for example. In the course of this, a layer of gold a few tenths of a micron thick is deposited only on the emitter region 7 and on the contact region 4. After brief annealing at 350° to 400°C for example, the electrodes 8 and 9 are formed as shown in FIG. 8, as a result of which contact is made to the n-p-n silicon transistor except for the collector region. The making of contact to the collector region may again be effected, for example by providing a collector electrode on the semiconductor body.

FIGS. 9 to 13 correspond to FIGS. 4 to 8 and represent a perspective illustration (partly in section) of the example described in connection with FIGS. 4 to 8.

While the base contact window and the emitter contact window are disposed side by side in the planar transistor shown in FIGS. 1 to 3, and the base contact window is disposed concentrically round the emitter contact window in the planar transistor of FIGS. 4 to 13, FIG. 14 shows a further embodiment of the invention in plan view wherein both the base contact window 3 present in the passivation layer 2 and also the emitter contact window 5 have a comb structure and the two windows interengage in comb form.

In the plan view shown in FIG. 15, the electrodes have already been introduced into the contact-making windows and both the emitter electrode 8 and also the base electrode 9 are constructed in comb form in accordance with the comb-like shape of the emitter contact window and of the base contact window. According to FIG. 15, further contact areas 10 which facilitate

the fitting of lead-in wires, are provided on both electrodes. These extended contact areas 10, which are referred to in English language literature as "enlarged contacts" may be produced for example by vapor-deposition of a metal layer over one entire surface after the production of the emitter electrode and of the base electrode, which metal layer is subsequently removed again by means of a photo-etching process with the exception of the two enlarged contacts 10. Whereas the emitter electrode and base electrode may consist of platinum for example, the enlarged contacts 10 consist of aluminum for example.

FIG. 16 shows an example of an embodiment of the invention wherein, as in FIGS. 1 to 3, the contact windows are disposed side by side. The base contact window 3 and the emitter contact window 5 are not rectangular, however, but triangular. Accordingly, the base electrode 9 and the emitter electrode 8 also have a triangular structure as shown in FIG. 17.

The planar transistor described with reference to FIGS. 4 to 13 is an n-p-n silicon transistor. The same transistor may naturally also have the configuration of FIGS. 1 to 3 or of FIGS. 14 to 15 as well as FIG. 16. The manufacture of a p-n-p silicon transistor is described below and may naturally likewise have each of the configurations illustrated in the previous Figures. In order to manufacture a p-n-p silicon transistor, the starting point is a silicon body 1 of p-type conductivity which is likewise covered with a passivating layer 2. Phosphorus for example is diffused instead of boron to a depth of 5μ with a surface concentration of 10^{21} impurity atoms per cm^3 , into the silicon body through the base contact window produced in the passivating layer. After the production of the emitter contact window 5, phosphorus is again diffused into the silicon body, namely to produce the base region 6 with a diffusion depth of 1μ for example and a surface concentration of 5.10^{19} impurity atoms per cm^3 . If the phosphorus diffusion is effected in an oxidizing atmosphere, then the phosphate glass formed during this diffusion is removed after the phosphorus diffusion. After the base diffusion, the emitter diffusion is effected by indiffusion of boron for example with a surface concentration of 5.10^{20} impurity atoms per cm^3 for example and diffusion depth likewise of 1μ for example. Since the base region is likewise further diffused into the semiconductor body during the emitter diffusion, the finished transistor has an effective base width of scarcely half a micron. The width of the web 2a which separates the base contact-making window for the emitter contact-making window amounts to 2μ for example.

After the boron diffusion, the borate glass is etched away and the silicon body is boiled in a platinum bath for currentless platinizing so that a layer of platinum 8 or 9 is deposited on the emitter region 7 and the contact region 4 of the type of conductivity of the base region, for example as shown in FIG. 15. After annealing at 700° to 800°C , a layer of aluminum about 1μ thick is vapor-deposited under high vacuum over the whole of one surface of the semiconductor body. Then the enlarged contacts 10, to which it is easier to make contact by means of wires than to the annealed in platinum layers 8 and 9, are exposed by means of a photoetching process (FIG. 15).

Whereas hitherto the manufacture of silicon planar transistors has been described, hereinafter the manufacture of a p-n-p germanium planar transistor according to the invention is described, it being manufacture in a similar manner to the silicon transistors. A layer of silicon nitride about 300 Å thick is deposited on a germanium semiconductor body 1 of 0.3 ohm/cm for example, as a passivating layer 2. Then the base contact window 3 is etched in the silicon nitride layer 2 by means of the photo-etching technique. Next the indiffusion of gallium for example to a depth of 4 μ and a surface concentration of $7 \cdot 10^{19}$ impurity atoms per cm³ for example is effected in order to produce the contact region 4. After this diffusion, an emitter contact window 5 is etched in the silicon nitride layer 2, again by means of the photo-etching technique, in such a manner that only a web 2a of 2 μ of a width for example remains between the two contact windows. Next indium for example is diffused into the semiconductor body to a depth of 1.5 μ with a surface concentration of $1 \cdot 10^{19}$ impurity atoms per cm³ for example, in order to produce the base region 6. An arsenic diffusion with a diffusion depth of about 0.7 μ and a surface concentration of about $5 \cdot 10^{19}$ impurity atoms per cm³ produces the emitter region 7.

In order to make contact to the emitter region and the base region, the germanium body is boiled in a gold bath, during which the layers of gold 8 and 9 are deposited on the contact region 4 and the emitter region 7 respectively. These gold layers are subsequently alloyed in at 370° C. Thus the transistor is ready for mounting. According to the invention, however, it is also possible to etch the silicon nitride layer 2 away from the whole semiconductor body and to apply a pyrolytic layer of quartz, for example 5000 Å, to the semiconductor surface at 350° C. This layer of quartz is partially removed again over the gold contacts by means of a photoetching process in order to permit the making of further contact to the transistor by means of lead-in wires or conducting paths.

The silicon planar transistors described before may, of course, also be produced by means of layers of quartz and/or silicon nitride produced pyrolytically or by high-frequency cathode sputtering. In this case, it is also possible to remove the passivation layers after the metallizing of the emitter region and the contact region of the same conductivity type as the base region, in order to apply a fresh or thicker passivation layer. The passivation layer deposited at a relatively lower temperature is then only partially removed again over the electrodes obtained by metallizing.

Finally, a p-n-p germanium planar transistor can be manufactured according to the invention, remembering only that acceptor atoms (gallium, indium, aluminum boron) diffuse much more slowly into germanium than donor atoms (phosphorus, arsenic, antimony, bismuth). In order to allow for this fact, the base contact window is not as fore opened first in the passivation layer, but the emitter contact window.

In the manufacture of a p-n-p germanium planar transistor according to the invention, therefore, the starting point is a semiconductor body covered with a passivation layer 2 as shown in FIG. 18, in the passivation layer of which the emitter contact window 5 is introduced as a first aperture. The passivation layer 2

consists for example of a layer of silicon nitride about 300 Å-thick which is applied for example by means of high-frequency sputtering on a semiconductor body of p-type conductivity, for example of 2 ohmcm material.

The emitter region is now first diffused into the semiconductor body through the emitter contact window 5, by diffusing gallium for example to a depth of 1.5 μ with a surface concentration of $8 \cdot 10^{19}$ impurity atoms per cm³ for example into the germanium body of p-type conductivity through the emitter window.

Then an annular base contact window 3, disposed concentrically round the emitter contact window 5, is etched into the passivation layer, as shown in FIG. 19, in such a manner that a web 2a of silicon nitride, for example 2.5 μ wide, remains between the two windows. Then impurities, which produce the n-type conductivity in the semiconductor body, are diffused into the semiconductor body both through the emitter contact window and through the base contact window, without any intermediate process, and both the base region and also the contact region of the conductivity same as the base region are formed. Arsenic for example may be diffused into the semiconductor body through both windows, with a surface concentration of $2 \cdot 10^{19}$ impurity atoms per cm³ for example, in order to produce the base region and the contact region. The penetration depth of the impurities penetration through the emitter contact window and through the base contact window are different with this diffusion. Whereas the penetration depth below the base contact window amounts to 5 μ for example, the high gallium concentration in the emitter region inhibits the indiffusion of the arsenic so that the basic region, in contrast to the contact region, only has a penetration depth of 2.5 μ for example. This penetration depth is nevertheless greater than that of the emitter region so that the emitter region lies inside the base region as a transistor requires.

After the arsenic diffusion, a layer of palladium is provided in a currentless manner on the emitter region and on the contact region and then gold is deposited thereon again without current. After annealing at a temperature of 350° C for example, the transistor is ready for mounting. The entire layer of silicon nitride may be etched away again, however, and a layer of quartz of 10,000 Å for example may be deposited on the germanium body at 350° C for example. After partial etching away of this layer of quartz in order to expose the electrodes, the p-n-p transistor is ready for mounting.

Not only silicon or germanium planar transistors can be produced in accordance with the invention but also for example planar transistors of an A^{III}B^V compound. In this case, a layer of silicon nitride for example is used as a passivation layer. The manufacturing process is similar to that of a germanium planar transistor. Zinc and tin for example may be used as diffusion material for producing the emitter region and the contact region. It should be noted in this case that the diffusions must take place in a closed system such as a quartz ampula which is at the same temperature all round. In compound semiconductors with a low melting point (for example indium antimonide) the layer of silicon nitride must be applied at a lower temperature, for example by means of high-frequency cathode sputtering.

Although, for the sake of simplicity, the invention has hitherto always been described only in connection with the manufacture of an individual transistor in practice preferably the wafer technique is used in which a plurality of individual transistors are produced simultaneously on a common semiconductor wafer.

The invention may also be used to advantage in the manufacture of integrated switching circuits, namely in the production of the planar transistors in these switching circuits. An integrated switching circuit with an n-p-n transistor according to the invention is illustrated in cross-section in FIG. 20. An integrated switching circuit with a p-n-p transistor is built up in a similar manner. The integrated switching circuit shown in FIG. 20 consists of a p-type substrate 11 of silicon on which there is provided an epitaxial layer 1 of silicon of n-type conductivity. This epitaxial layer 1 is provided with a passivation layer 2 as well as with separation regions 12 which divide the epitaxial layer into various boxes. The planar transistor of FIG. 20 is produced in such a box. In order to produce the planar transistor, an aperture 3 is introduced into the passivating layer 2 at a base contact window, in accordance with the previous examples, and through it the contact region 4 is diffused into the epitaxial layer 1. Then the emitter contact window 5 is produced in such a way that the web 2a remains between the two windows. The base region 6 is now diffused into the epitaxial layer through the emitter contact window 5. Before the emitter diffusion, another aperture 13 is formed in the passivating layer and serves to make contact to the collector region. In contrast to the planar transistors previously described, in the integrated circuit shown in FIG. 20, the collector region is only accessible at the emitter side because of the substrate. After the opening of the collector contact window 13, the emitter diffusion takes place during which the collector contact region 14 is diffused into the epitaxial layer beside the emitter region 7. Finally layers of gold are deposited, by boiling in a currentless gold bath for example, simultaneously in the emitter contact window, in the base contact window and in the collector contact window, and form, after an annealing process, the emitter contact 8, the base contact 9 and the collector contact 15. P-n-p transistors can be produced in a completely similar manner in integrated switching circuits. If germanium is used as a semiconductor material, the collector contact region produced simultaneously with the p⁺-type emitter region must be protected by a masking layer, such as layer of quartz for example, before the following n⁺-type base diffusion. This protective layer is only removed again before the production of the contacts.

As already stated, in the method according to the invention important operational steps are saved in comparison with known methods. In addition, the invention offers particular advantages for fine, complicated and at the same time relatively large-area structures, particularly because of the ideal adjustment of emitter diffusion and base diffusion as well as of the metallizing, as a result of the manufacturing process.

It will be understood that the above description, of the present invention is susceptible to various modifications changes and adaptations.

What I claim as new and desire to secure by letters patent of the United States is:

1. A method of producing a planar transistor comprising forming a passivation layer on a semiconductor body, forming a first window in said passivation layer, diffusing a base contact region into said semiconductor body through said first window, subsequently forming a second window adjacent said first window, and, while said first window is open, diffusing through said second window a base region and an emitter region into said semiconductor body, the diffusing of said base region bringing said base region into electrical contact with said base contact region.

2. A method as defined in claim 1, wherein said base contact region is indiffused with a surface concentration high enough to prevent said base contact region from changing its conductivity type under counter-doping by the emitter diffusion impurities penetrating into said first window during the emitter diffusion, and high enough to prevent its conductivity from dropping below the value necessary for a connection between the base region and a base electrode.

3. A method as defined in claim 2, wherein said base contact region is diffused deeper into the semiconductor body than said base region.

4. A method as defined in claim 1, wherein said first and second windows are separated by a web of the material of the passivation layer having a width less than the sum of the penetration depths of the base region and of the base contact region.

5. A method as defined in claim 1, wherein said first window is formed as an annulus and said second window is formed within said annulus.

6. A method as defined in claim 1, wherein said first and second windows are formed with an interengaging comb-like structure.

7. A method as defined in claim 1 further comprising making non-rectifying contact with said emitter region and said base contact region by electrode and thereafter removing the entire passivation layer, replacing said passivating layer by a fresh passivation layer applied pyrolytically and removing said passivating layer again only over the electrodes.

8. A method as defined in claim 1 further comprising making non-rectifying contact with said emitter region and said base contact region by electrodes and thereafter removing the entire passivation layer, replacing said passivating layer by a fresh passivation layer applied through cathode sputtering and removing said passivating layer again only over the electrodes.

9. A method as defined in claim 1, wherein said passivation layer is formed of silicon oxide.

10. A method as defined in claim 1, wherein said passivation layer is formed of silicon nitride.

11. A method as defined in claim 1 wherein said diffused regions are formed by means of powder diffusion.

12. A method as defined in claim 1, wherein contact is made to the collector region of said transistor at the surface of the semiconductor body opposite to said emitter region.

13. A method as claimed in claim 1, including making non-rectifying contact to said emitter region and said base contact region by means of an electrolytic deposition, without electrodes, of metal layers.

14. A method as defined in claim 13, wherein the metal of said metal layers consists of gold, platinum metals, silver, nickel or copper.

15. A method as defined in claim 1, wherein said semiconductor body consists of silicon, germanium or an A^{III}B^V compound.

16. A method as defined in claim 1, further comprising contacting said base region through said base contact region in said first window and said emitter region through said second window.

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