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- (54) Title: OLED ARRAY SUBSTRATE, DISPLAY APPARATUS CONTAINING THE SAME, AND METHOD FOR FORM-
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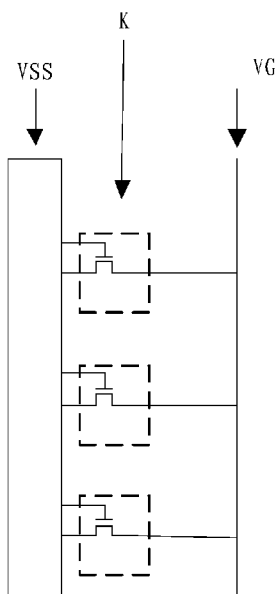


Figure 2

- (57) Abstract: The present disclosure provides an organic light-emitting diode (OLED) array substrate. The OLED array substrate includes a display area with OLEDs arranged in arrays, electrostatic discharge lines, and peripheral electrostatic discharge areas with conductive areas electrically connected to a cathode of the OLEDs and electrically connected to the electrostatic discharge lines through switch modules.



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OLED ARRAY SUBSTRATE, DISPLAY APPARATUS CONTAINING THE SAME, AND METHOD FOR FORMING THE SAME

CROSS-REFERENCES TO RELATED APPLICATIONS

[001] This PCT patent application claims priority of Chinese Patent Application No.
5 201510146172.4, filed on March 30, 2015, the entire content of which is incorporated
by reference herein.

FIELD OF THE INVENTION

[002] The present invention generally relates to the display technologies and, more
particularly, relates to an OLED array substrate, display apparatus containing the same,
10 and method for forming the same.

BACKGROUND

[003] An Organic Light-Emitting Diode (OLED) display panel includes an array
substrate or a Thin-Film Transistor (TFT) substrate. As a key component of the OLED
display panel, the performance of the array substrate is crucial to the display panel.

15 [004] In the process of forming/depositing the cathode of an OLED display panel, an
undesirably amount of electrostatic charges may be generated. The electrostatic
charges may cause serious damage to the circuit on the array substrate. Certain defects
may also be formed in the display panel.

[005] Current array substrates may be susceptible to damages caused by electrostatic
20 charges, which may lead to short circuits on the display panel.

BRIEF SUMMARY OF THE DISCLOSURE

[006] The present invention addresses the above problems in the prior art. The
present disclosure provides an OLED array substrate, the method for manufacturing
the OLED array substrate, and the display apparatus containing the OLED array
25 substrate to reduce damages caused by the electrostatic charges generated during the
cathode deposition process.

[007] One aspect of the present disclosure includes an organic light-emitting diode (OLED) array substrate. The OLED array substrate includes a display area with OLEDs arranged in arrays, electrostatic discharge lines, and peripheral electrostatic discharge areas with conductive areas electrically connected to a cathode of the OLEDs and electrically connected to the electrostatic discharge lines through switch modules.

[008] Optionally, the switch modules are configured to form electrical connection between the conductive areas and the electrostatic discharge lines under an electrostatic voltage generated by electrostatic charges.

[009] Optionally, the electrostatic discharge lines include high-voltage electrostatic discharge lines and low-voltage electrostatic discharge lines; and a conductive area is connected to a high-voltage electrostatic discharge line through first switch modules, and is connected to a low-voltage electrostatic discharge line through second switch modules.

[0010] Optionally, when positive electrostatic charges are generated in the conductive area and create a positive electrostatic voltage, the first switch modules are turned on; and when negative electrostatic charges are generated in the conductive area and create a negative electrostatic voltage, the second switch modules are turned on.

[0011] Optionally, a control terminal and a first terminal of the first switch module are connected to the conductive area; and a second terminal of the first switch module is connected to the high-voltage electrostatic discharge line.

[0012] Optionally, a control terminal and a first terminal of the second switch module are connected to the low-voltage electrostatic discharge line, and a second terminal of the second switch module is connected to the conductive area.

[0013] Optionally, the first switch modules and the second switch modules are N-type transistors.

[0014] Optionally, a control terminal and a first terminal of the first switch module are connected to the high-voltage electrostatic discharge line, and a second terminal of the first switch module is connected to the conductive area.

[0015] Optionally, a control terminal and a first terminal of the second switch module are connected to the conductive area, and a second terminal of the second switch module is connected to the low-voltage electrostatic discharge line.

[0016] Optionally, the first switch modules and the second switch modules are P-type transistors.

[0017] Optionally, the switch module includes at least two cascaded transistors.

[0018] Optionally, the OLED array substrate further includes gate lines and data lines arranged to be perpendicular to the gate lines, wherein gate lines and data lines are connected to the low-voltage electrostatic discharge line through a first electrostatic discharge structure and are connected to the high-voltage electrostatic discharge line through a second electrostatic discharge structure.

[0019] Another aspect of the present disclosure provides an OLED display apparatus. The OLED display apparatus includes any one of the disclosed OLED array substrates.

[0020] Another aspect of the present disclosure provides a method for forming an OLED array substrate. The method includes forming switch modules electrically connected to conductive areas and electrostatic discharge lines; and forming, subsequently, a cathode of OLEDs in the array substrate, wherein the conductive areas are connected to the cathode such that during a process for forming the cathode of the OLEDs, electrostatic voltages generated by electrostatic charges in the conductive areas turn on the switch modules and the electrostatic charges are discharged through the electrostatic discharge lines.

[0021] Another aspect of the present disclosure provides an electrostatic discharge circuit for discharging electrostatic charges generated during a formation process of a cathode layer of an organic light-emitting diode (OLED) array substrate. The electrostatic discharge circuit includes electrostatic discharge lines, peripheral electrostatic discharge areas with conductive areas, the conductive areas being electrically connected to the cathode layer, and switch modules connecting the conductive areas and the electrostatic discharge lines, wherein the electrostatic charges in the conductive areas are discharged through the switch modules and electrostatic discharge lines.

[0022] Optionally, the switch modules are configured to be turned on by electrostatic voltages generated by electrostatic charges in the conductive areas such that the electrostatic charges are discharged through the electrostatic discharge lines.

[0023] Other aspects of the present disclosure can be understood by those skilled in the art in light of the description, the claims, and the drawings of the present disclosure.

BRIEF DESCRIPTION OF THE DRAWINGS

[0024] The following drawings are merely examples for illustrative purposes according to various disclosed embodiments and are not intended to limit the scope of the present disclosure. It should be noted that the disclosed drawings only illustrate portions of the array substrate that are related to the electrostatic discharge for illustrative purposes.

[0025] Figure 1 illustrates an exemplary OLED array substrate according to the disclosed embodiments of the present disclosure;

[0026] Figure 2 illustrates an exemplary circuit of a conductive area, electrostatic discharge lines, and switch modules according to the disclosed embodiments of the present disclosure;

[0027] Figure 3a illustrates an exemplary circuit of a conductive area, high-voltage electrostatic discharge lines, and first switch modules (N-type transistors) according to the disclosed embodiments of the present disclosure;

[0028] Figure 3b illustrates an exemplary circuit of a conductive area, low-voltage electrostatic discharge lines, and second switch modules (N-type transistors) according to the disclosed embodiments of the present disclosure;

[0029] Figure 4a illustrates another exemplary circuit of a conductive area, high-voltage electrostatic discharge lines, and first switch modules (P-type transistors) according to the disclosed embodiments of the present disclosure;

[0030] Figure 4b illustrates another exemplary circuit of a conductive area, low-voltage electrostatic discharge lines, and second switch modules (P-type transistors) according to the disclosed embodiments of the present disclosure;

[0031] Figure 5 illustrates an exemplary first switch module according to the disclosed embodiments of the present disclosure;

[0032] Figure 6 illustrates an exemplary second switch module according to the disclosed embodiments of the present disclosure;

[0033] Figure 7a illustrates an exemplary circuit of gate lines/data lines, a conductive area, high-voltage electrostatic discharge lines, low-voltage electrostatic discharge lines, and third switch modules according to the disclosed embodiments of the present disclosure;

[0034] Figure 7b illustrates another exemplary circuit of gate lines/data lines, a conductive area, high-voltage electrostatic discharge lines, low-voltage electrostatic discharge lines, and third switch modules according to the disclosed embodiments of the present disclosure;

[0035] Figure 8 illustrates existing circuit of gate lines/data lines, a conductive area, high-voltage electrostatic discharge lines, low-voltage electrostatic discharge lines, third switch modules, and fourth switch modules; and

5 [0036] Figure 9 illustrates another exemplary circuit of gate lines/data lines, a conductive area, high-voltage electrostatic discharge lines, low-voltage electrostatic discharge lines, third switch modules, and fourth switch modules according to the disclosed embodiments of the present disclosure.

DETAILED DESCRIPTION

10 [0037] For those skilled in the art to better understand the technical solution of the invention, reference will now be made in detail to exemplary embodiments of the invention, which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers will be used throughout the drawings to refer to the same or like parts. It should be noted that the terms "first" and "second" are used to merely distinguish two objects and have little indication about the differences in structures and components between two objects.

[0038] One aspect of the present disclosure provides an OLED array substrate.

[0039] The disclosed OLED array substrate can be exemplified in embodiment 1.

Figure 1 illustrates the structure of an exemplary OLED array substrate of the present disclosure. In Figure 1, 1 may represent a glass substrate, 2 may represent peripheral electrostatic discharge areas, 3 may represent electrostatic discharge wiring areas, 4 may represent the active area (AA) or display area, 5 may represent fan-out wiring areas, and 6 may represent chip on film (COF) binding areas. As shown in Figure 1, the OLED array substrate exemplified in embodiment 1 may include the display area 4 and peripheral electrostatic discharge areas 2, and the display area 4 may include
20 OLEDs arranged in arrays. The peripheral electrostatic discharge areas 2 may include conductive areas electrically connected to the cathode of the OLEDs. The main portion of the electrostatic discharge areas 2 may be conductive areas. The electrostatic discharge areas 2 may include patterned metal and indium tin oxide (ITO). The metal can be any suitable metal for electrostatic discharge areas 2 such as Al. The
25 OLED array substrate may also include electrostatic discharge lines or circuit arranged in the electrostatic discharge wiring areas 3 in Figure 1 (not shown). The conductive areas may be connected to the electrostatic discharge lines through switch modules
30

arranged in the electrostatic discharge wiring areas 3 in Figure 1 (not shown). The electrostatic voltage generated by the electrostatic charges in the conductive areas may turn on the switch modules so that the electrostatic charges generated in the conductive areas may be discharged through the electrostatic discharge lines.

5 [0040] Figure 2 illustrates an exemplary connection of a conductive area, the electrostatic discharge lines, and the switch module. As shown in Figure 2, the conductive area VSS may be connected to the electrostatic discharge line VG through a switch module K. Electrostatic charges generated in the conductive area may turn on the switch modules K such that the electrostatic charges generated in the conductive
10 area VSS may be discharged through the electrostatic discharge line VG.

[0041] In Figure 2, the portions circled in dashed lines may be the added switch modules K, as compared to an existing OLED array substrate illustrated in Figure 8, which does not place a switch module between the conductive area VSS and the electrostatic discharge lines. For illustrative purposes, Figure 2 only shows three
15 switch modules K. It should be noted that the number of the switch modules K may be determined according to various applications and is not limited by the explicitly disclosed embodiments of the present disclosure. For example, one or more switch modules K can be included/added. The conductive areas VSS may be often arranged in opposing positions of the OLED array substrate, and the switch modules K may be
20 arranged between each of the conductive area and a corresponding electrostatic discharge line VG to improve discharge performance.

[0042] The conductive areas VSS may represent the areas electrically connected to the subsequently-formed (e.g., subsequently-deposited) cathode of the OLEDs. When the cathode of the OLEDs is being formed, an undesirably large amount of
25 electrostatic charges may be generated such that circuit near the conductive areas may be damaged and short circuits may occur. Normal display functions of the corresponding display panel may therefore be adversely affected.

[0043] In the OLED array substrate provided by the present disclosure, switch modules may be arranged between conductive areas and electrically connected to the
30 cathode of the OLEDs and the electrostatic discharge lines. Thus, when electrostatic charges are generated in the conductive areas, for example, during the deposition of the cathode of the OLEDs, the electrostatic charges may turn on the switch modules and the generated electrostatic charges may be discharged through the electrostatic

discharge lines. Damages to the array substrate caused by electrostatic charges may be avoided or reduced, and manufacturing yield of the display products can be improved.

[0044] The disclosed OLED array substrate can also be exemplified in embodiment 2.

The array substrate in Figure 3a illustrates the circuit of a conductive area, a high-voltage electrostatic discharge line, and first switch modules (N-type transistor).

Figure 3b illustrates the circuit of a conductive area, a low-voltage electrostatic discharge line, and second switch modules (N-type transistor). Figure 4a illustrates the circuit of a conductive area, a high-voltage electrostatic discharge line, and first switch modules (P-type transistor). Figure 4b illustrates the circuit of a conductive area, a low-voltage electrostatic discharge line, and second switch modules (P-type transistor).

[0045] Different from embodiment 1, in embodiment 2, the electrostatic discharge lines (i.e., corresponding to VG in Figure 2) may include a high-voltage electrostatic discharge line VGH and a low-voltage electrostatic discharge line VGL. A conductive area VSS may be connected to the high-voltage electrostatic discharge line VGH through the first switch modules K1, as shown in Figures 3a and 4a. The conductive area VSS may also be connected to the low-voltage electrostatic discharge line VGL through the second switch modules K2, as shown in Figures 3b and 4b. When the conductive area VSS generates positive electrostatic voltage, the first switch modules K1 may be turned on, and when the conductive area VSS generates negative electrostatic voltage, the second switch modules K2 may be turned on.

[0046] The first switch module K1 may include N-type transistors and/or P-type transistors. The second switch module K2 may also include N-type transistors and/or P-type transistors.

[0047] For example, a first switch module K1 may include at least two cascaded N-type transistors or at least two cascaded P-type transistors. A second switch module K2 may also include at least two cascaded N-type transistors or at least two cascaded P-type transistors. The threshold voltages of the cascaded transistors may be increased such that devices or circuits may be protected from undesirably high leakage currents.

[0048] In certain embodiments of the present disclosure, a conductive area VSS may be connected to both the high-voltage electrostatic discharge line VGH and the low-voltage electrostatic discharge line VGL. First switch modules K1 may be used to connect the conductive area VSS with the high-voltage electrostatic discharge line VGH. Second switch modules K2 may be used to connect the conductive area VSS

with the low-voltage electrostatic discharge line VGL. Details of the working principles of the arrangements described above are aforementioned and omitted herein.

[0049] For example, Figure 5 illustrates an first electrostatic discharge structure ESD1 connected to a first switch module K1. ESD 1 may include two cascaded N-type transistors. The two cascaded N-type transistors may be connected to a conductive area VSS on the left side and connected to the high-voltage electrostatic discharge line VGH on the right side. When no electrostatic charges are in the conductive area VSS, the voltage on the left side of the two cascaded N-type transistors may be lower than the voltage provided by the high-voltage electrostatic discharge line VGH. The two cascaded N-type transistors are turned off (i.e., functioning as open circuit). When the conductive area VSS generates positive high-voltage electrostatic charge, the voltage on the left side of the two cascaded N-type transistors may instantaneously be higher than the voltage provided by the high-voltage electrostatic discharge line VGH. The two cascaded N-type transistors may be turned on such that the electrostatic charges generated in the conductive area VSS may be discharged through the high-voltage electrostatic circuit VGH.

[0050] Figure 6 illustrates a second electrostatic discharge structure ESD2 connected to a second switch module K2. ESD2 may include two cascaded N-type transistors. The two cascaded N-type transistors may be connected to a conductive area VSS on the left side and connected to the low-voltage electrostatic discharge line VGL on the right side. When no electrostatic charges is in the conductive area VSS, the voltage on the left side of the two cascaded N-type transistors may be higher than the voltage provided by the low-voltage electrostatic discharge line VGL. The two cascaded N-type transistors are turned off (i.e., functioning as open circuit). When the conductive area VSS generates negative high-voltage electrostatic charge, the voltage on the left side of the two cascaded N-type transistors may instantaneously be lower than the voltage provided by the low-voltage electrostatic discharge line VGL. The two cascaded N-type transistors may be turned on such that the electrostatic charges generated in the conductive area may be discharged through the low-voltage electrostatic circuit VGL.

[0051] Figures 3a and 3b show circuits of the first switch module K1 including N-type transistors and the second switch module K2 including N-type transistors. As shown in Figure 3a, the control terminal and the first terminal of the first switch module K1 may be connected to the conductive area VSS. The second terminal of the

first switch module K1 may be connected to the high-voltage electrostatic discharge line VGH. As shown in Figure 3b, the control terminal and the first terminal of the first switch module K2 may be connected to the low-voltage electrostatic discharge line VGL. The second terminal of the second switch module K2 may be connected to the conductive area VSS.

[0052] Figures 4a and 4b show circuits of the first switch module K1 including P-type transistors and the second switch module K2 including P-type transistors. As shown in Figures 4a, the control terminal and the first terminal of the first switch module K1 may be connected to the high-voltage electrostatic discharge line VGH. The second terminal of the first switch module K1 may be connected to the conductive area VSS. As shown in Figure 4b, the control terminal and the first terminal of the second switch module K2 may be connected to the conductive area VSS. The second terminal of the second switch module K2 may be connected to the low-voltage electrostatic discharge line VGL.

[0053] In the embodiments disclosed herein, the control terminal may be the gate of a transistor. The first terminal may be the source of a transistor and the second terminal may be the drain of the transistor. Alternatively, the first terminal may be the drain of a transistor and the second terminal may be the source of the transistor.

[0054] During the process of forming or depositing the cathode of the OLEDs, if positive high-voltage electrostatic charges are generated, the first switch modules K1 illustrated in Figures 3a and 4a may be turned on. The generated positive high-voltage electrostatic charges may be discharged through the high-voltage electrostatic line VGH. If negative high-voltage electrostatic charges are generated, the second switch modules K2 illustrated in Figures 3b or 4b may be turned on. The generated negative high-voltage electrostatic charges may be discharged through the low-voltage electrostatic line VGL. Accordingly, high-voltage electrostatic charges can be discharged and released, and damages to the array substrate can be reduced.

[0055] It should be noted that when positive high-voltage electrostatic charges and/or negative high-voltage electrostatic charges are generated by other processes, the first switch modules K1 and the second switch modules K2 may still be turned on or off under the same working principles. The high-voltage electrostatic charges may be discharged, and damages to the array substrate can be reduced.

[0056] The switch modules K1 and K2 illustrated in Figures 3a and 3b may each be arranged on the opposing side of each other on the display panel (e.g., left side and

right side). The switch modules K1 and K2 illustrated in Figures 4a and 4b may each be arranged on the opposing side of each other on the display panel (e.g., top side and bottom side). Alternatively, the first switch modules K1 illustrated in Figures 3a and 4a may each be arranged on the opposing side of each other on the display panel (e.g., left side and right side). The second switch modules K2 illustrated in Figures 3b and 4b may each be arranged on the opposing side on the display panel (e.g., top side and bottom side).

[0057] The disclosed OLED array substrate can also be exemplified in embodiment 3.

Figure 7a illustrates a circuit of gate lines/data lines, a conductive area, high-voltage electrostatic discharge lines, low-voltage electrostatic discharge lines, third switch modules, and fourth switch modules. Figure 7b illustrates another circuit of gate lines/data lines, a conductive area, high-voltage electrostatic discharge lines, low-voltage electrostatic discharge lines, third switch modules, and fourth switch modules.

[0058] Besides the features illustrated in embodiment 1, the OLED array substrate of embodiment 3 may further include gate lines and data lines. For illustrative purposes, in the figures provided by the present disclosure, gate lines and data lines may be arranged in similar configurations. In practice, gate lines may be parallel to each other and may be arranged to be perpendicular to the data lines (not shown). Each gate line may be electrically insulated from other gate lines and any data lines, and each data line may be electrically insulated from other data lines and any gate lines. A gate/data line may be connected to the low-voltage electrostatic discharge line VGL through the first electrostatic discharge structure ESD1, and may be connected to the high-voltage electrostatic discharge line VGH through the second electrostatic discharge structure ESD2.

[0059] For illustrative purposes, in embodiment 3, the third switch modules K3 and the fourth switch modules K4 both include N-type transistors.

[0060] In Figures 7a and 7b, G_{n-1} , G_n , and G_{n+1} may each represent the $(n-1)^{th}$ gate line, the n^{th} gate line, and the $(n+1)^{th}$ gate line, respectively. D_{n-1} , D_n and D_{n+1} may each represent the $(n-1)^{th}$ data line, the n^{th} data line, and the $(n+1)^{th}$ data line, respectively. Before the deposition process to form the cathode of the OLEDs, no voltage is applied on the circuit on the array substrate, and the transistors arranged in arrays are turned off. During the deposition process, if the conductive area VSS generates positive high-voltage electrostatic charges, the fourth switch modules K4 in Figure 7a may be turned on. The generated positive high-voltage electrostatic charges

may be discharged through the high-voltage electrostatic discharge line VGH. If the conductive area VSS generates negative high-voltage electrostatic charge, the third switch modules K3 may be turned on. The generated negative high-voltage electrostatic charges may be discharged through the low-voltage electrostatic discharge line VGL. Thus, high-voltage electrostatic charges can be discharged or released, and damages to the array substrate can be avoided or reduced.

[0061] The third switch module K3 and the fourth switch module K4 may have similar structures as the first switch module K1 and the second switch module K2. Detailed description of the structures are omitted herein. In Figure 7a, the portions circled in dashed lines may be the added switch modules K4, as compared to an existing OLED array substrate illustrated in Figure 8, which does not place a switch module between the conductive area VSS and the discharge lines VGH.

[0062] The design and arrangements described in Figures 7a and 7b may each be placed on two opposing sides of the display panel. For example, the design described in Figures 7a and 7b may each be arranged on the top side and on the bottom side of the display panel, or on the left side and on the right side of the display panel. Alternatively, the design described in Figure 7a may be arranged on two opposing sides of the display panel. The design described in Figure 7b may be arranged on the other two opposing sides of the display panel. For example, the design described in Figure 7a may be arranged on the left side and the right side of the display panel. The design described in Figure 7b may be arranged on the top side and the bottom side of the display panel, or vice versa. The specific arrangements of the circuit may be determined according to different applications and are thus not limited by the disclosed embodiments herein.

[0063] In various embodiments, the third switch module K3 and the fourth switch module K4 may both be used in the circuit to discharge positive high-voltage electrostatic charges and negative high-voltage electrostatic charges, as shown in Figure 9.

[0064] Another aspect of the present disclosure provides an OLED display apparatus.

[0065] The disclosed OLED display apparatus may be exemplified in embodiment 4. The OLED display apparatus illustrated by embodiment 4 may include any one of the OLED array substrates disclosed in embodiments 1 to 3. It should be noted that the display apparatus may be any suitable electronic device with display functions such as a TV, a monitor, a tablet, a video camera, a camera, or a navigator.

[0066] Another aspect of the present disclosure provides a method for manufacturing the disclosed OLED array substrate.

[0067] The disclosed method may be exemplified in embodiment 5. The OLED array substrate illustrated by embodiment 5 may include a display area and peripheral electrostatic discharge areas. The display area includes OLEDs arranged in arrays. The peripheral electrostatic discharge areas include conductive areas electrically connected to the cathode of the OLEDs. The OLED array substrate also includes electrostatic discharge lines.

[0068] The method for manufacturing the OLED array substrate includes the following steps. First, before forming the cathode of the OLEDs, the switch modules, configured to electrically connect the electrostatic discharge lines and the conductive areas of the display panel, may be formed. The conductive areas may be used to electrically connect the subsequently-formed cathode of the OLEDs on the display panel. Thus, when the cathode of the OLEDs is being formed, the electrostatic voltage, generated in the conductive areas, may turn on the switch modules. The generated electrostatic charges may be discharged through the electrostatic discharge lines.

[0069] In the method described above, switch modules, configured to electrically connect the electrostatic discharge lines and the conductive areas of the display panel, are formed before the formation of the cathode of the OLEDs. The conductive areas may be used to electrically connect the subsequently-formed cathode of the OLEDs on the display panel. Thus, the electrostatic voltage generated by the electrostatic charges may turn on the switch modules such that the electrostatic charges may be discharged through the electrostatic discharge lines. Thus, damages to the array substrate caused by the electrostatic charges generated during the deposition of the cathode of the OLEDs, can be avoided or reduced, which may improve manufacturing yield of the display panels.

[0070] It should be understood that the above embodiments disclosed herein are exemplary only and not limiting the scope of this disclosure. Without departing from the spirit and scope of this invention, other modifications, equivalents, or improvements to the disclosed embodiments are obvious to those skilled in the art and are intended to be encompassed within the scope of the present disclosure.

What is claimed is:

1. An organic light-emitting diode (OLED) array substrate, including:
a display area with OLEDs arranged in arrays;
electrostatic discharge lines; and
peripheral electrostatic discharge areas with conductive areas electrically connected to a cathode of the OLEDs and electrically connected to the electrostatic discharge lines through switch modules.
2. The OLED array substrate according to claim 1, wherein the switch modules are configured to form electrical connection between the conductive areas and the electrostatic discharge lines under an electrostatic voltage generated by electrostatic charges.
3. The OLED array substrate according to claim 1, wherein:
the electrostatic discharge lines include high-voltage electrostatic discharge lines and low-voltage electrostatic discharge lines; and
a conductive area is connected to a high-voltage electrostatic discharge line through first switch modules, and is connected to a low-voltage electrostatic discharge line through second switch modules.
4. The OLED array substrate according to claim 3, wherein:
when positive electrostatic charges are generated in the conductive area and create a positive electrostatic voltage, the first switch modules are turned on; and
when negative electrostatic charges are generated in the conductive area and create a negative electrostatic voltage, the second switch modules are turned on.
5. The OLED array substrate according to claim 3, wherein:
a control terminal and a first terminal of the first switch module are connected to the conductive area; and a second terminal of the first switch module is connected to the high-voltage electrostatic discharge line.
6. The OLED array substrate according to claim 3, wherein:
a control terminal and a first terminal of the second switch module are connected to the low-voltage electrostatic discharge line, and a second terminal of the second switch module is connected to the conductive area.
7. The OLED array substrate according to claim 5 or 6, wherein the first switch modules and the second switch modules are N-type transistors.
8. The OLED array substrate according to claim 3, wherein:

a control terminal and a first terminal of the first switch module are connected to the high-voltage electrostatic discharge line, and a second terminal of the first switch module is connected to the conductive area.

9. The OLED array substrate according to claim 3, wherein:

a control terminal and a first terminal of the second switch module are connected to the conductive area, and a second terminal of the second switch module is connected to the low-voltage electrostatic discharge line.

10. The OLED array substrate according to claim 9 or 10, wherein the first switch modules and the second switch modules are P-type transistors.

11. The OLED array substrate according to claim 1, wherein the switch module includes at least two cascaded transistors.

12. The OLED array substrate according to claim 1, further including gate lines and data lines arranged to be perpendicular to the gate lines, wherein:

gate lines and data lines are connected to the low-voltage electrostatic discharge line through a first electrostatic discharge structure and are connected to the high-voltage electrostatic discharge line through a second electrostatic discharge structure.

13. An OLED display apparatus, including the OLED array substrate in any one of claims 1 to 12.

14. A method for forming an OLED array substrate, including:

forming switch modules electrically connected to conductive areas and electrostatic discharge lines; and

forming, subsequently, a cathode of OLEDs in the array substrate,

wherein the conductive areas are connected to the cathode such that during a process for forming the cathode of the OLEDs, electrostatic voltages generated by electrostatic charges in the conductive areas turn on the switch modules and the electrostatic charges are discharged through the electrostatic discharge lines.

15. An electrostatic discharge circuit for discharging electrostatic charges generated during a formation process of a cathode layer of an organic light-emitting diode (OLED) array substrate, including:

electrostatic discharge lines;

peripheral electrostatic discharge areas with conductive areas, the conductive areas being electrically connected to the cathode layer; and

switch modules connecting the conductive areas and the electrostatic discharge lines; wherein the electrostatic charges in the conductive areas are discharged through the

switch modules and electrostatic discharge lines.

16. The electrostatic discharge circuit according to claim 15, wherein the switch modules are configured to be turned on by electrostatic voltages generated by electrostatic charges in the conductive areas such that the electrostatic charges are discharged through the electrostatic discharge lines.

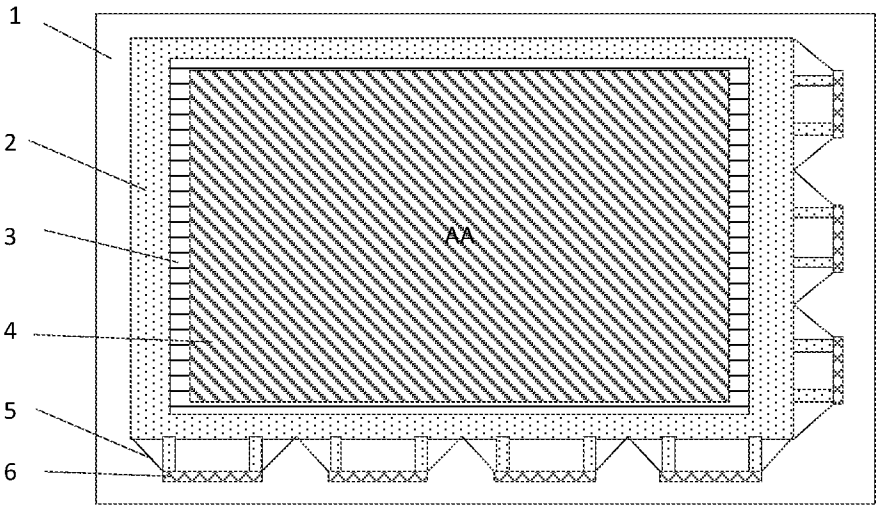


Figure 1

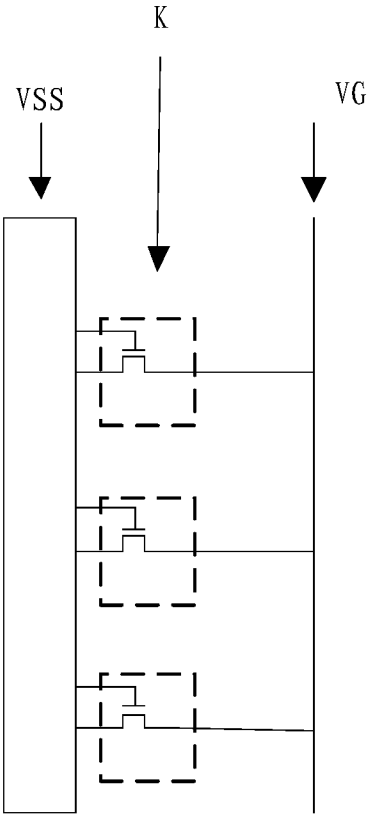


Figure 2

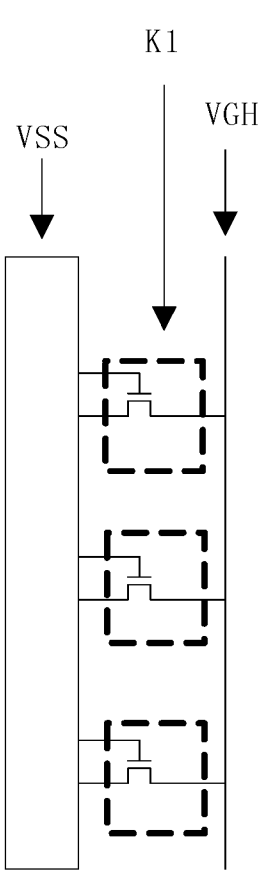


Figure 3a

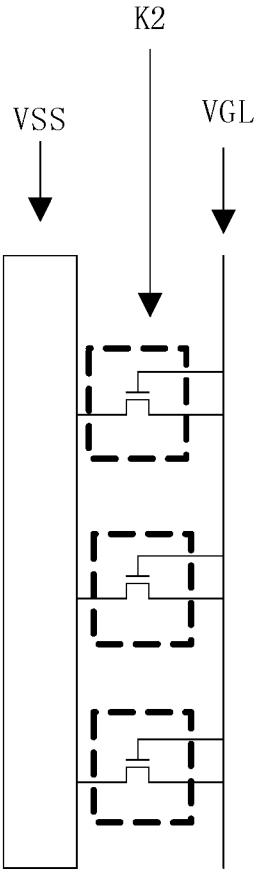


Figure 3b

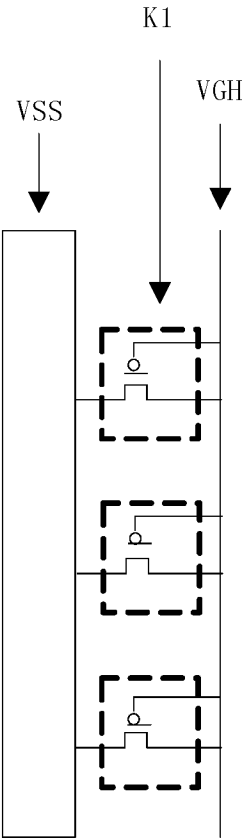


Figure 4a

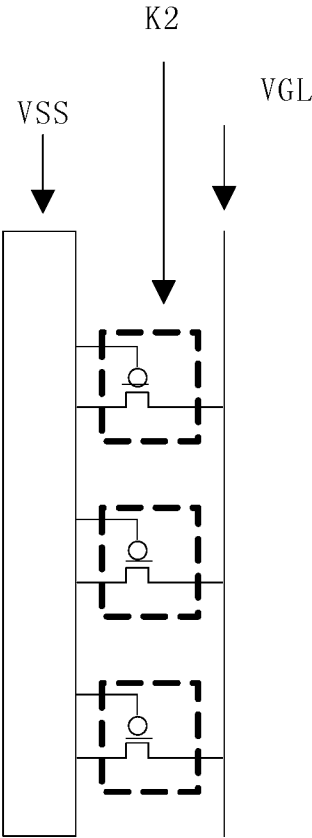


Figure 4b

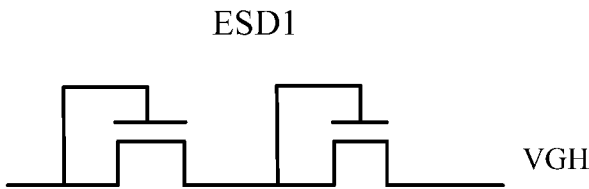


Figure 5

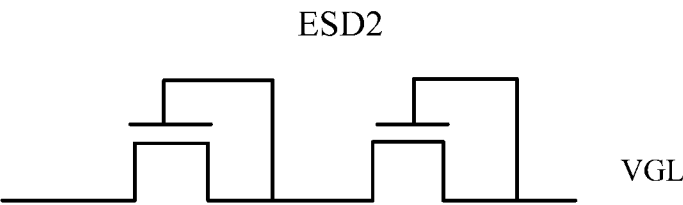


Figure 6

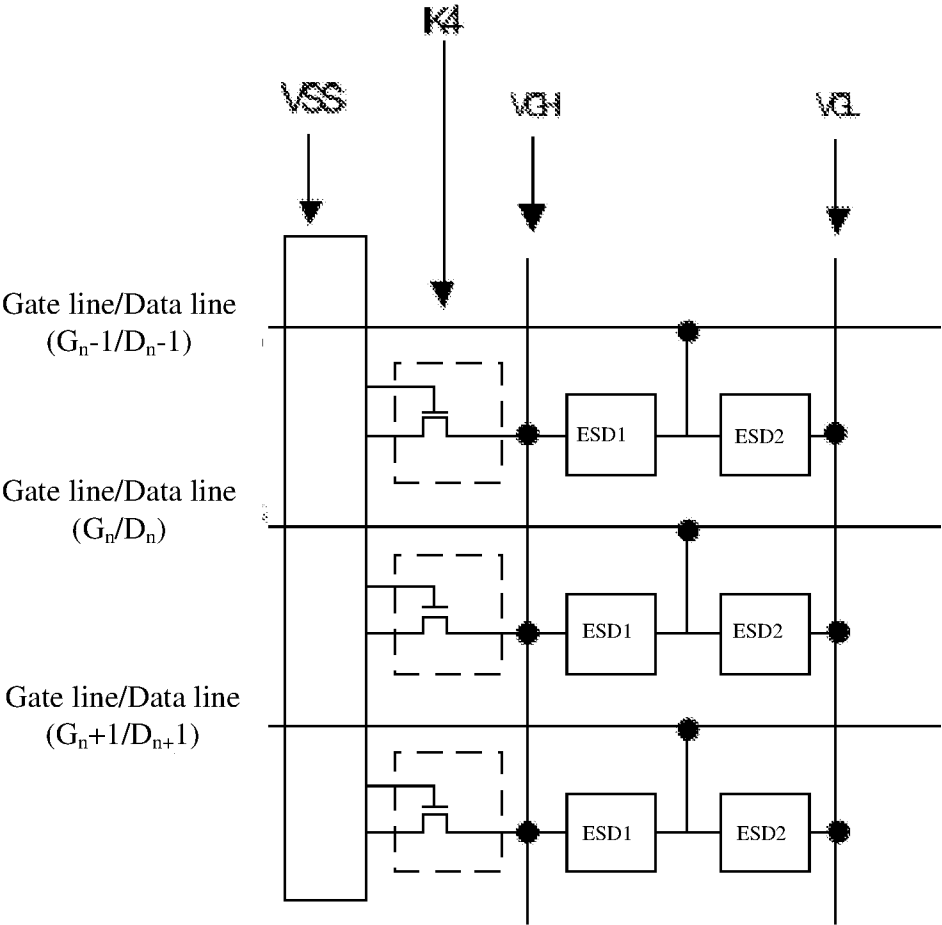


Figure 7a

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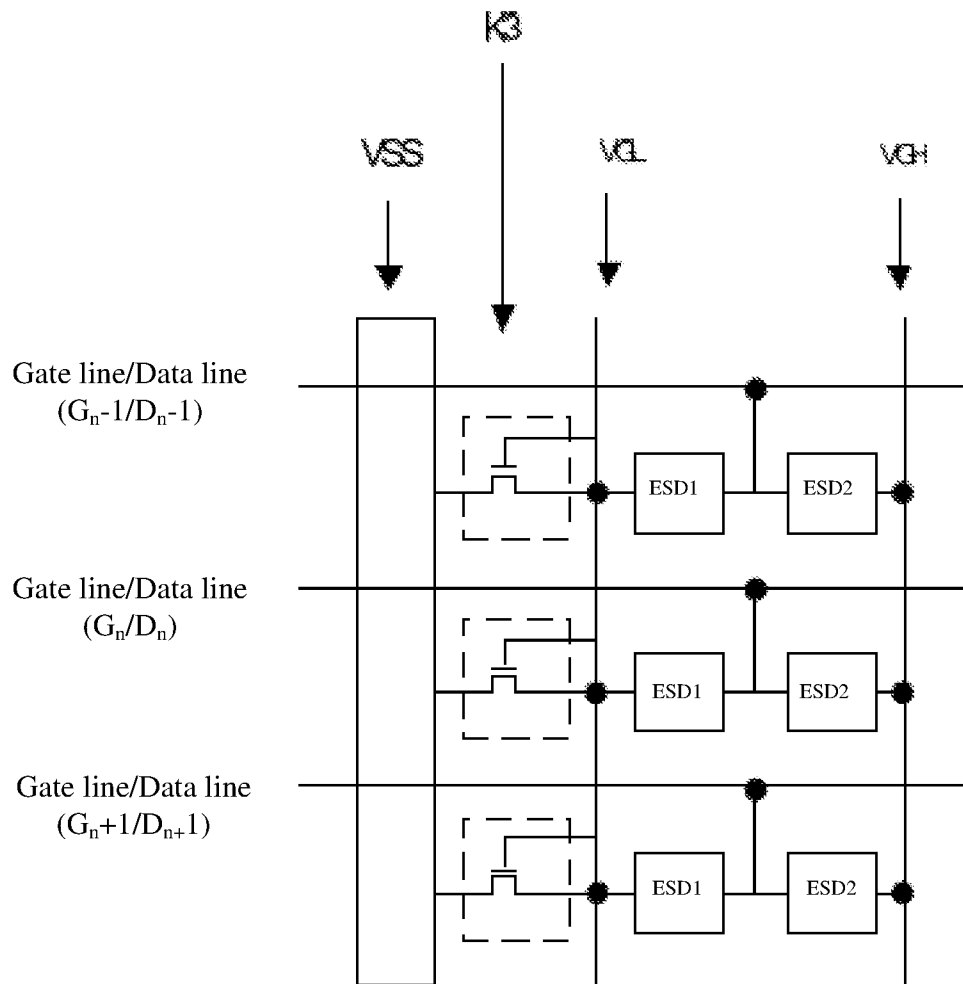


Figure 7b

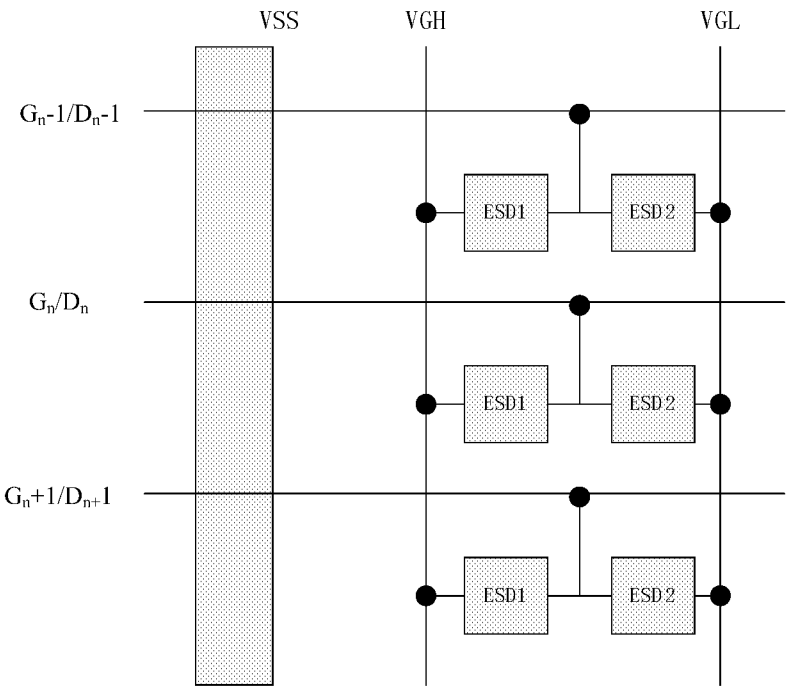


Figure 8 (Prior Art)

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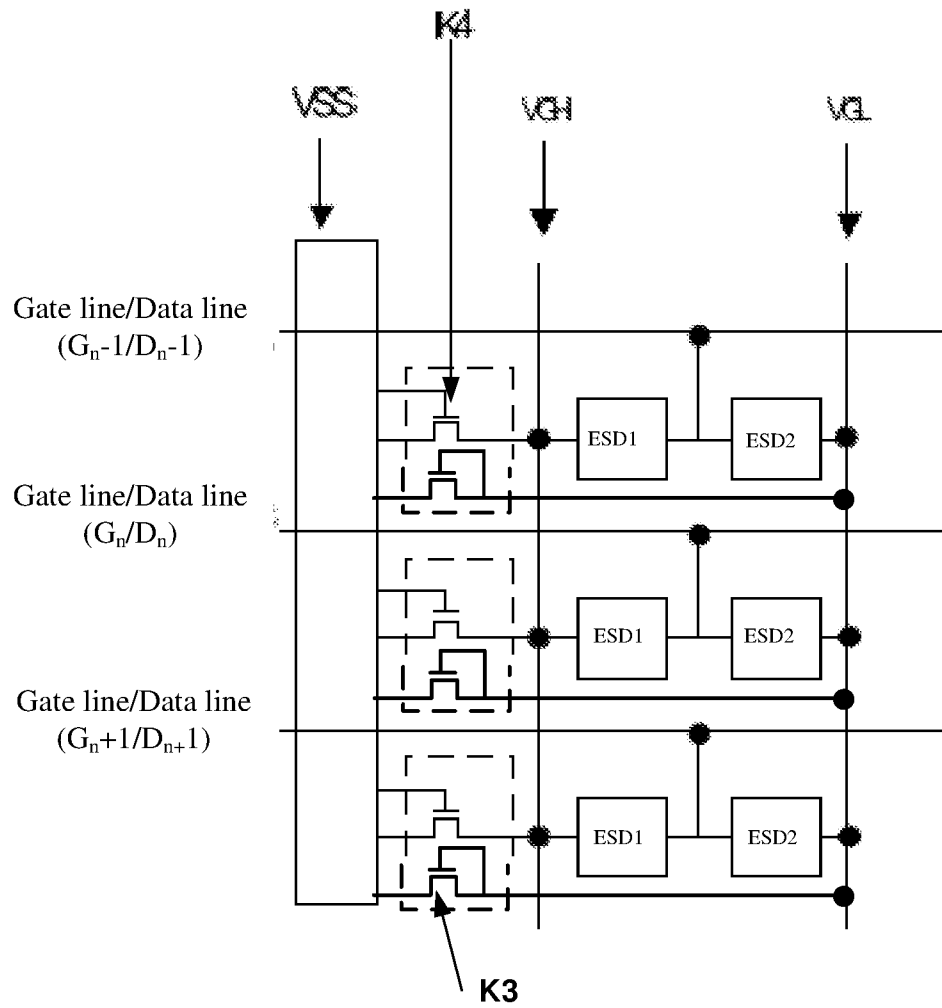


Figure 9

INTERNATIONAL SEARCH REPORT

International application No.

PCT/CN2015/089835

A. CLASSIFICATION OF SUBJECT MATTER

H01L 27/32(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNPAT, CNKI, WPI, EPODOC, IEEE: discharge, diode, electrode, ESD, light, cathode, organic, static, negative, emit+, electrostatic, OLED, anode, positive, prov+, proof, gate, data, high, low, VGH, VGL, transistor, TFT, deposit+, coat+, VSS, voltage, switch

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
PX	CN 104716165 A (BOE TECHNOLOGY GROUP CO., LTD.) 17 June 2015 (2015-06-17) description, paragraphs [0043] -[0077], Figs. 1-7	1-16
X	US 2008170013 A1 (JEONG SEONI ET AL.) 17 July 2008 (2008-07-17) description, paragraphs [0023] -[0075], [0097]-[0110], Figs. 1-8	1-2, 13-16
Y	US 2008170013 A1 (JEONG SEONI ET AL.) 17 July 2008 (2008-07-17) description, paragraphs [0023] -[0075], [0097]-[0110], Figs. 1-8	3-12
Y	US 2014185169 A1 (LG DISPLAY CO., LTD.) 03 July 2014 (2014-07-03) description, paragraphs [0008]-[0022], [0042]-[0057], [0076]-[0104], Figs. 1, 3-7	3-12
A	CN 102903733 A (SHENZHEN HUAXING OPTOELECT TECNOLOGY CO., LTD.) 30 January 2013 (2013-01-30) the whole document	1-16
A	CN 203338721 U (SHENZHEN HUAXING OPTOELECT TECNOLOGY CO., LTD.) 11 December 2013 (2013-12-11) the whole document	1-16



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

“A” document defining the general state of the art which is not considered to be of particular relevance	“T” later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
“E” earlier application or patent but published on or after the international filing date	“X” document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
“L” document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	“Y” document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
“O” document referring to an oral disclosure, use, exhibition or other means	“&” document member of the same patent family
“P” document published prior to the international filing date but later than the priority date claimed	

Date of the actual completion of the international search

02 November 2015

Date of mailing of the international search report

21 December 2015

Name and mailing address of the ISA/CN

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INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.

PCT/CN2015/089835

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				JP	4722866	B2	13 July 2011
				EP	1944803	A1	16 July 2008
				JP	2008170920	A	24 July 2008
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				US	8835912	B2	16 September 2014
				US	2014110673	A1	24 April 2014
CN	203338721	U	11 December 2013	None			