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(54) Title: APPARATUS AND METHOD FOR HIGH SPEED VOLTAGE REGULATION

(57) Abstract: A high-speed voltage regulating apparatus and a method for high-speed voltage regulation. The apparatus includes: (A) a regulator, adapted to provide a regulated voltage; (B) switching circuitry, connected to the regulator, adapted to either (i) connect the regulator to an output node or (ii) disconnect the regulator from the output node; whereas the output node is connected to a dynamic power consuming device and to a load capacitor; (C) control logic, connected to the regulator, adapted to receive at least an indication reflecting a voltage of the output node and to control the switching circuitry such that the regulator is disconnected from the output node to facilitate a decrease in the voltage of the output node. The method includes: (A) determining whether to (i) decrease a voltage of an output node, (ii) to maintain the voltage of the output node or to (iii) increase the voltage of the output node; (B) allowing a voltage of an output node to decrease by disconnecting a regulator from the output node; whereas the output node is coupled to a dynamic power consuming device and to a load capacitor; and (C) providing a regulated voltage corresponding to a required voltage of the output node, if determining to maintain the voltage of the output node or to increase the voltage of the output node.

APPARATUS AND METHOD FOR HIGH SPEED VOLTAGE REGULATION

FIELD OF THE INVENTION

The present invention relates to methods and systems for high-speed voltage regulation and especially relates to a high-speed regulator that supports dynamic voltage scaling.

BACKGROUND OF THE INVENTION

Mobile devices, such as but not limited to personal data appliances, cellular phones, radios, pagers, lap top computers, and the like are required to operate for relatively long periods before being recharged. These mobile devices usually include one or more processors as well as multiple memory modules and other peripheral devices.

In order to reduce the power consumption of mobile devices various power consumption control techniques were suggested. A first technique includes reducing the clock frequency of the mobile device. A second technique is known as dynamic voltage scaling (DVS) or alternatively is known as dynamic voltage and frequency scaling (DVFS) and includes altering the voltage that is supplied to a processor as well as altering the frequency of a clock signal that is provided to the processor in response to the computational load demands (also referred to as throughput) of the processor. Higher voltage levels are associated with higher operating frequencies and higher computational load but are also associated with higher energy consumption.

U.S. patent application 20040052098 of Burstein et al., titled "digital voltage using current control"; U.S. patent application 20030139927 of Gabara, et al., titled "Block processing in a maximum a posteriori processor for reduced power consumption"; U.S. patent application

20020000797 of Burstein et al., titled "Switching regulator with capacitance near load"; U.S. patent application 20040025068 of Gary et al., titled "Methodology for coordinating and tuning application power"; U.S. patent application 20010038277 of Burstein et al., titled "Digital voltage regulator using current control", and "A Dynamic Voltage Scaled Microprocessor System", T. D. Burd, T. A. Pering, A. J. Stratakos and R. W. Brodersen, IEEE Journal Journal of solid-state circuits, Vol. 35, No. 11, November 200, all being incorporated herein by reference, provide a brief review of some dynamic voltage scaling techniques.

FIG. 1 illustrates the supply voltage that is being supplied to a processor (such as the CPU of FIG. 2) during the execution of various tasks as well during an idle period. For simplicity of explanation the supply voltage is illustrated as a sequence of ramps, and the transition periods between voltage ramps are not illustrated. The transition periods are very short, and typically do not exceed few milliseconds.

During a first time period ΔT1 11 that starts at T0 and ends at T1, the processor executes a very high throughput task and accordingly receives a very high frequency clock signal and a very high level supply voltage Vvery_high.

During a second time period ΔT2 12 that starts at T1 and ends at T2, the processor executes a high throughput task and accordingly receives a high frequency clock signal and a high level supply voltage Vhigh.

During a third first time period ΔT3 13 that starts at T2 and ends at T3, the processor executes a medium throughput task and accordingly receives a medium frequency clock signal and a medium level supply voltage Vmedium.

During a fourth time period ΔT4 14 that starts at T3 and ends at T4, the processor is idle and accordingly receives a very low frequency clock signal (or alternatively does not receive a clock signal) and a very low (even zero) level supply voltage Vvery_low.

During a fifth time period ΔT5 15 that starts at T4 and ends at T5, the processor executes a high throughput task and accordingly receives a high frequency clock signal and a high level supply voltage Vhigh.

It is noted that the voltage supplied to the processor is decreased (usually during a very short time period) at about T1, T2 and T3 and is increased at about T4.

FIG. 2 illustrates a prior art device 20 that includes multiple power consuming devices such as a central processing unit (CPU), SRAM and I/O card, collectively denoted 30, a frequency regulator 40, a voltage regulator 50, an output inductor 34 and a load capacitor 32.

The voltage regulator 50 receives a desired frequency from the frequency regulator 40, a 1 Mhz clock signal and provides a frequency error signal to a digital filter that in turn sends control signals to a FET control and drivers unit 52 that applies a pulse-width/pulse frequency modulation scheme to control a pair of power FET transistors Mn 56 and Mp 54. The gates of Mn 56 and Mp 54 are connected to the FET control and drivers unit 52, that turns them on and off in response to said modulation scheme. The source of Mp 54 is connected to a battery 60 and the drain of Mp 54 is connected to the drain of Mn 56. The drain of Mn 56 is grounded.

The drains of Mn 56 and Mp 54 are connected at an output node of the regulator. This output node is connected to a first end of an inductor 34. The other end of the inductor 34 is connected to a first end of a load capacitor 32. The second end of the load capacitor 32 is

grounded. The second end of the inductor 34 is also connected to the frequency regulator 40 and to devices 30.

The load capacitor is relatively large (about 5.5 Microfarad). Typically, such as load capacitor 30 is used to smooth the voltage supplied to the processor. In various mobile devices the load capacitor is also used as a power reservoir that provides power during short supply power failure. Such a power reservoir is described at U.S. patent 6226556 of Itkin et al., which is incorporated herein by reference.

Referring back to the prior art device 20, the regulator 50 can increase or decrease the regulated voltage supplied to its output node, and thus may dynamically alter the voltage supplied to the CPU and other devices. In some prior art regulators a decrement in the regulated voltage involves decreasing the charge of the load capacitor 32 by draining said charge to the ground. Thus each voltage decrement involves power loss.

The prior art device 20 also loses energy as a result of removing charge from the load capacitor to a battery bypass capacitor (not shown in FIG. 2).

There is a need to provide an efficient method and apparatus for dynamically providing regulated voltage to a processor.

SUMMARY OF THE PRESENT INVENTION

Dynamically altering the voltage supplied to a processor in response to the computational load of the processor and operating frequency associated with said load. The supplied voltage is decreased by allowing a load capacitor to supply the required voltage and is increased by providing an appropriate regulated voltage.

A high-speed voltage regulating apparatus that includes: (A) a regulator, adapted to provide a regulated voltage; (B) switching circuitry, connected to the regulator, adapted to either (i) couple the regulator to an output node or (ii) disconnect the regulator from the output node; whereas the output node is connected to a dynamic power consuming device, such as but not limited to a processor, and to a load capacitor; and (C) control logic, connected to the regulator, adapted to receive at least an indication reflecting a voltage of the output node and to control the switching circuitry such that the regulator is disconnected from the output node to facilitate a decrease in the voltage of the output node.

A method for high-speed voltage regulation that includes: (A) determining whether to (i) decrease a voltage of an output node, (ii) to maintain the voltage of the output node or to (iii) increase the voltage of the output node; (B) allowing a voltage of an output node to decrease by disconnecting a regulator from the output node; whereas the output node is coupled to a dynamic power consuming device, such as but not limited to a processor, and to a load capacitor; and (C) providing a regulated voltage corresponding to a required voltage of the output node, if determining to maintain the voltage of the output node or to increase the voltage of the output node.

A mobile device that includes: (A) a battery; (B) a dynamic power consuming device, such as but not limited to a processor, that is connected to an output node; (C) a regulator, connected to the battery, whereas the regulator is adapted to provide a regulated voltage; (D) switching circuitry, connected to the regulator, adapted to either (i) couple the regulator to the output

node or (ii) disconnect the regulator from the output node; whereas the output node is further connected to a load capacitor; and a (E) control logic, connected to the regulator, adapted to receive at least an indication reflecting a voltage of the output node and to control the switching circuitry such that the regulator is disconnected from the output node to facilitate a decrease in the voltage of the output node.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be understood and appreciated more fully from the following detailed description taken in conjunction with the drawings in which:

FIG. 1 is a timing diagram illustrating the change of voltage supplied to a processor in response to the changing computational loads of the processor;

FIG. 2 illustrates a prior art device that includes a power supply unit;

FIG. 3 is a schematic diagram of a high-speed voltage regulating apparatus, according to an embodiment of the invention;

FIG. 4 is a timing diagram that illustrates an output voltage during transition periods and intermediate periods, according to an embodiment of the invention; and

FIG. 5 is a flow chart illustrating a method for high-speed voltage regulation, according to an embodiment of the invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

The following description related to supplying voltage to a processor. Those of skill in the art will appreciate that the disclosed systems and methods can be applied mutates mutandis to supplying voltage to other dynamic power consuming devices.

It is further noted that although the disclosed apparatus includes a buck switch that other switching elements and other configurations can be applied, including boost configurations and buck-boost configurations.

The term processor refers to an entity that is capable of performing various tasks that are associated with different computational loads. The processor can be a RISC processor, a general-purpose processor, a digital

signal processor, a controller, a scalar processor and the like.

It is noted that typically the voltage regulator provides a supply voltage to multiple devices such as memory banks, displays and the like but for simplicity of explanation the drawings and associated description refer to a processor.

The term "dynamic power consuming device" refers to a device that can operate at different power consuming modes, especially in response to throughput demands that can vary over time. Such a device can be a processor that can operate at different voltage levels and different operational frequencies, to support tasks associated with different computational loads.

FIG. 3 illustrates an apparatus 100 according to an embodiment of the invention. Apparatus 100 includes a voltage regulator 110, a switching circuitry such as switch 120 and a buck switch that in turn includes NMOS transistor 124 and PMOS transistor 122. Apparatus 100 further includes a load capacitor 140 and control logic 160.

Apparatus 100 includes an output node 102 that is connected to the load capacitor 140, to a processor 150 and to the output of the buck switch. The voltage of the output node is denoted Vout 130 and also referred to as "output voltage" of as the output voltage of apparatus 100.

Switch 120 is connected between the voltage regulator 110 and an input of the buck switch. The input of the buck switch is connected to the gates of transistors 124 and 122. The source of PMOS transistor 122 is connected to a battery 128 and its drain is connected to the drain of the NMOS transistor 124 to form an output node 102 of

apparatus 100. The drain of the NMOS transistor 124 is grounded.

The output node 102 is connected to a device such as processor 150 and also to one end of the load capacitor 140. The other end of the load capacitor is grounded. The output node 102 is also connected to voltage regulator 110 and optionally to the control unit 160 to provide one or more feedback signals to said latter devices.

The voltage regulator 110 can be any prior art device that is capable of providing a regulated voltage. It receives as inputs a signal representative of the voltage (Vout 200) of the output node 102 of apparatus 100, but may also receive Vout itself. The regulator further receives control signals such as but not limited to Vreq 204 that determines a desired Vout. The voltage regulator 110 or the control unit 160 may determine the relationship between a current value of Vout and a next value of Vout. For example, referring to the example set forth at FIG. 1, at T1 Vout has to be altered from Vvery_high to Vout.

Switch 120 is controlled by control logic 160 and can either connect the output of voltage regulator 110 to the buck switch or disconnect the buck switch from the voltage regulator 110. Switch 120 can be implemented by a transistor, although this is not necessarily so. Conveniently, when the buck switch is disconnected from the voltage regulator 110 the NMOS transistor 124 is OFF, thus preventing the load capacitor 140 to discharge through the NMOS transistor 124.

When switch 120 is closed the regulated voltage supplied by voltage regulator 110 is provided, via the buck switch, to the output node 102 of apparatus 100. When switch 120 is open the voltage regulator 110 is disconnected from the output node 102 and the voltage of

required voltage of the output node. Referring to FIG. 3, during this stage switch 120 is closed.

Stage 320 conveniently includes stage 340 of monitoring the decrement of the voltage of the output node and stage 350 of determining if the voltage of the output node decreases to substantially reach a voltage threshold. The voltage threshold can be dynamically set to a required voltage level in response to characteristics of dynamic power consuming device, such as computational load of a processor.

Stage 350 is followed by stage 360 of providing a regulated voltage that substantially equals a voltage threshold when the voltage of the output node decreases to substantially reach the voltage threshold. Stage 350 is followed by stage 340 while the voltage of the output node is above the voltage threshold.

Conveniently, stage 320 also includes controlling a rate of decrement of the voltage of the output node by supplying a charging current to at least the load capacitor. A portion of that current can flow through the processor 150 while another portion charges the capacitor 140.

Variations, modifications, and other implementations of what is described herein will occur to those of ordinary skill in the art without departing from the spirit and the scope of the invention as claimed. Accordingly, the invention is to be defined not by the preceding illustrative description but instead by the spirit and scope of the following claims.

WE CLAIM

1. A high-speed voltage regulating apparatus, the apparatus comprising:

a regulator, adapted to provide a regulated voltage;

switching circuitry, coupled to the regulator, adapted to either (i) couple the regulator to an output node or (ii) disconnect the regulator from the output node; whereas the output node is coupled to a dynamic power consuming device and to a load capacitor; and

control logic, coupled to the regulator, adapted to receive at least an indication reflecting a voltage of the output node and to control the switching circuitry such that the regulator is disconnected from the output node to facilitate a decrease in the voltage of the output node.

2. The apparatus of claim 1 adapted to prevent a decrement of the voltage of the output node below a voltage threshold by coupling the regulator to the output node.

3. The apparatus of claim 2 further adapted to prevent a decrement of the voltage of the output mode by configuring the regulator to provide a regulated voltage that substantially equals the voltage threshold.

4. The apparatus of claim 1 further adapted to control a rate of decrement of the voltage of the output node by supplying a charging current to at least the load capacitor.

5. The apparatus of claim 1 wherein the switching circuitry comprises a buck switch.

6. The apparatus of claim 1 wherein the regulated voltage is responsive to an operating frequency of the dynamic power consuming device.

7. The apparatus of claim 1 adapted to increase the regulated voltage in moderate steps when the control logic determines to increase the voltage of the output node.

8. The apparatus of claim 1 wherein the regulator is coupled to a battery.

9. A method for high-speed voltage regulation, the method comprises:

determining whether to (i) decrease a voltage of an output node, (ii) to maintain the voltage of the output node or to (iii) increase the voltage of the output node; whereas the output node is coupled to a dynamic power consuming device and to a load capacitor;

allowing a voltage of an output node to decrease by disconnecting a regulator from the output node; whereas the output node is coupled to a processor and to a load capacitor; and

providing a regulated voltage corresponding to a required voltage of the output node, if determining to maintain the voltage of the output node or to increase the voltage of the output node.

10. The method of claim 9 further comprising monitoring the decrement of the voltage of the output node and providing a regulated voltage that substantially equals a voltage threshold when the voltage of the output node decreases to substantially reach the voltage threshold.

11. The method of claim 9 further comprising controlling a rate of decrement of the voltage of the output node by supplying a charging current to at least the load capacitor.

12. The method of claim 11 wherein the required voltage of the output node is responsive to an operating frequency of the dynamic power consuming device.

13. A mobile device comprising:

a battery;

a dynamic power consuming device, coupled to an output node;

a regulator, adapted to provide a regulated voltage;

switching circuitry, coupled to the regulator, adapted to either (i) couple the regulator to the output node or (ii) disconnect the regulator from the output node; whereas the output node is further coupled to a load capacitor; and

control logic, coupled to the regulator, adapted to receive at least an indication reflecting a voltage of the output node and to control the switching circuitry such that the regulator is disconnected from the output node to facilitate a decrease in the voltage of the output node.

14. The mobile device of claim 13 further adapted to prevent a decrement of the voltage of the output node below a voltage threshold by coupling the regulator to the output node.

15. The mobile device of claim 14 further adapted to prevent a decrement of the voltage of the output mode by configuring the regulator to provide a regulated voltage that substantially equals the voltage threshold.

16. The mobile device of claim 13 further adapted to control a rate of decrement of the voltage of the output node by supplying a charging current to at least the load capacitor.

17. The mobile device of claim 13 wherein the switching circuitry comprises a buck switch.

18. The mobile device of claim 13 wherein the regulated voltage is responsive to an operating frequency of the dynamic power consuming device.

19. The mobile device of claim 13 further adapted to increase the regulated voltage in moderate steps when the control logic determines to increase the voltage of the output node.

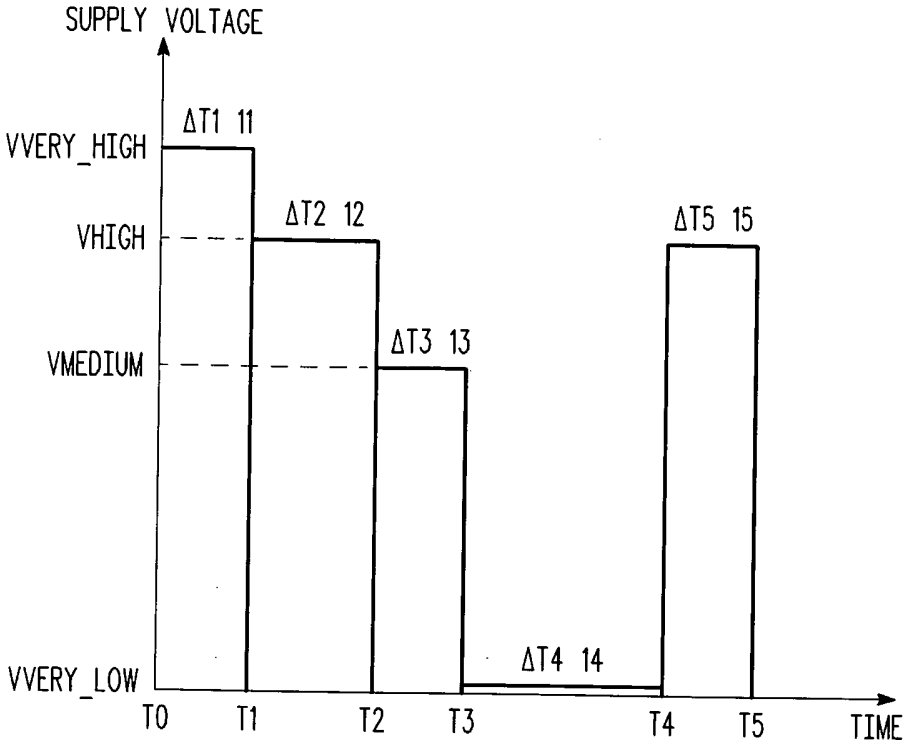

FIG. 1
-PRIOR ART-

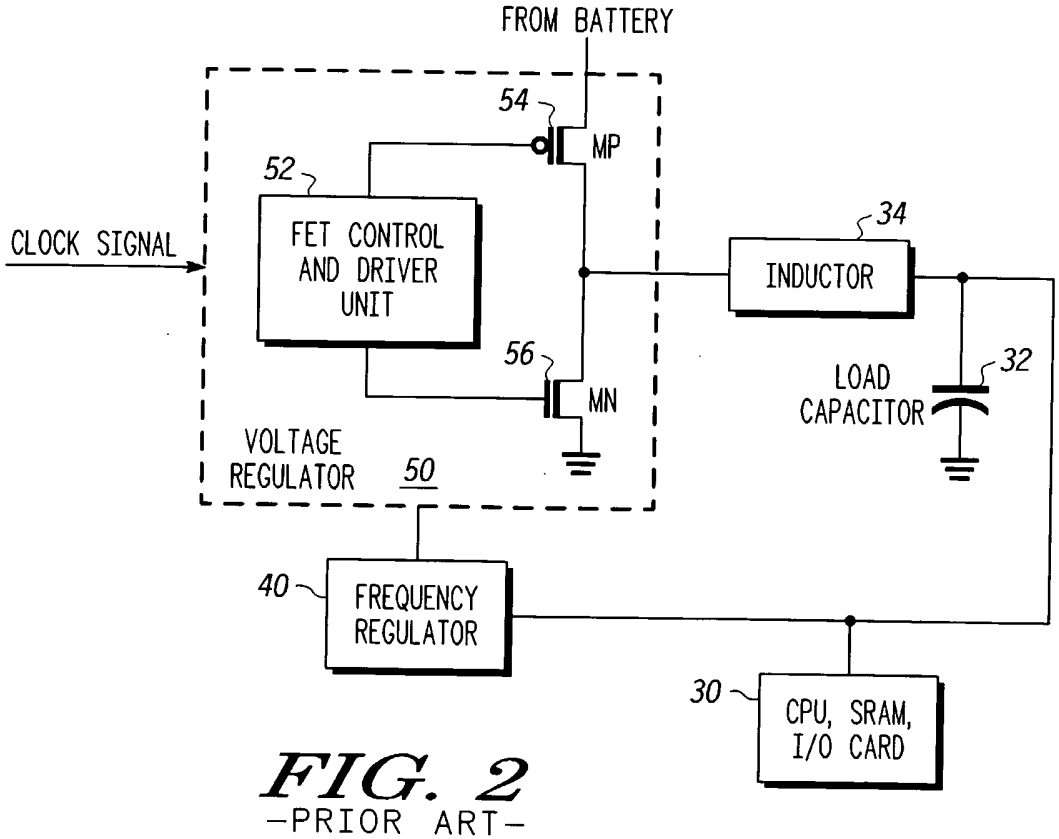

FIG. 2
-PRIOR ART-

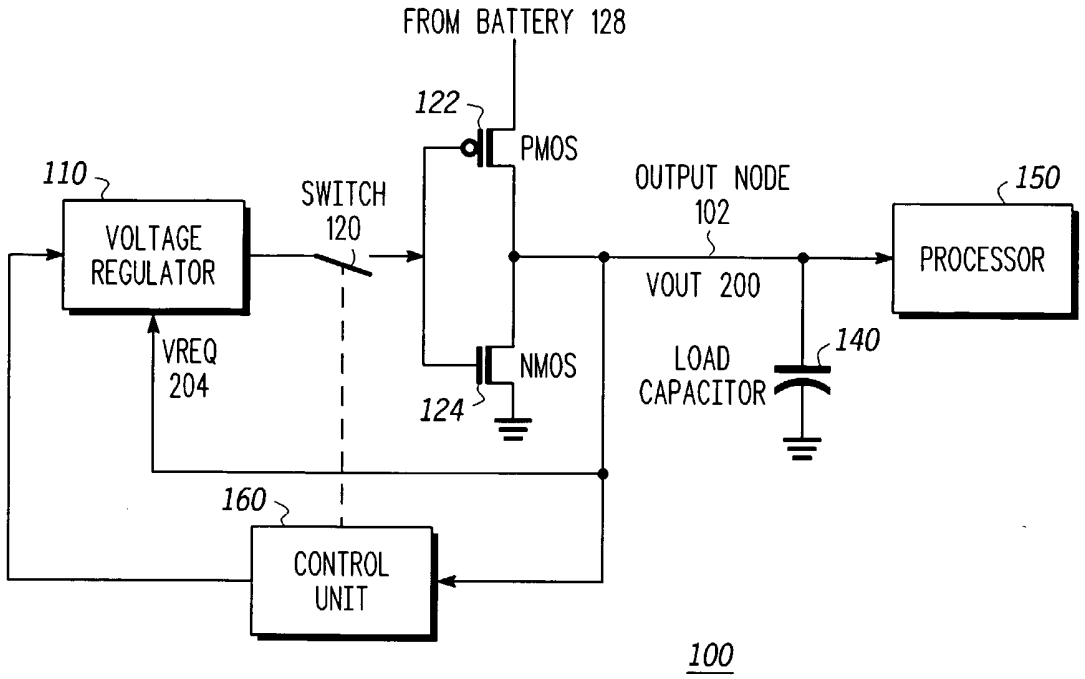
FROM BATTERY 128
122
PMOS
110
VOLTAGE REGULATOR
SWITCH 120
OUTPUT NODE 102
150
PROCESSOR
VOUT 200
VREQ 204
NMOS
124
LOAD CAPACITOR
140
160
CONTROL UNIT
100

FIG. 3

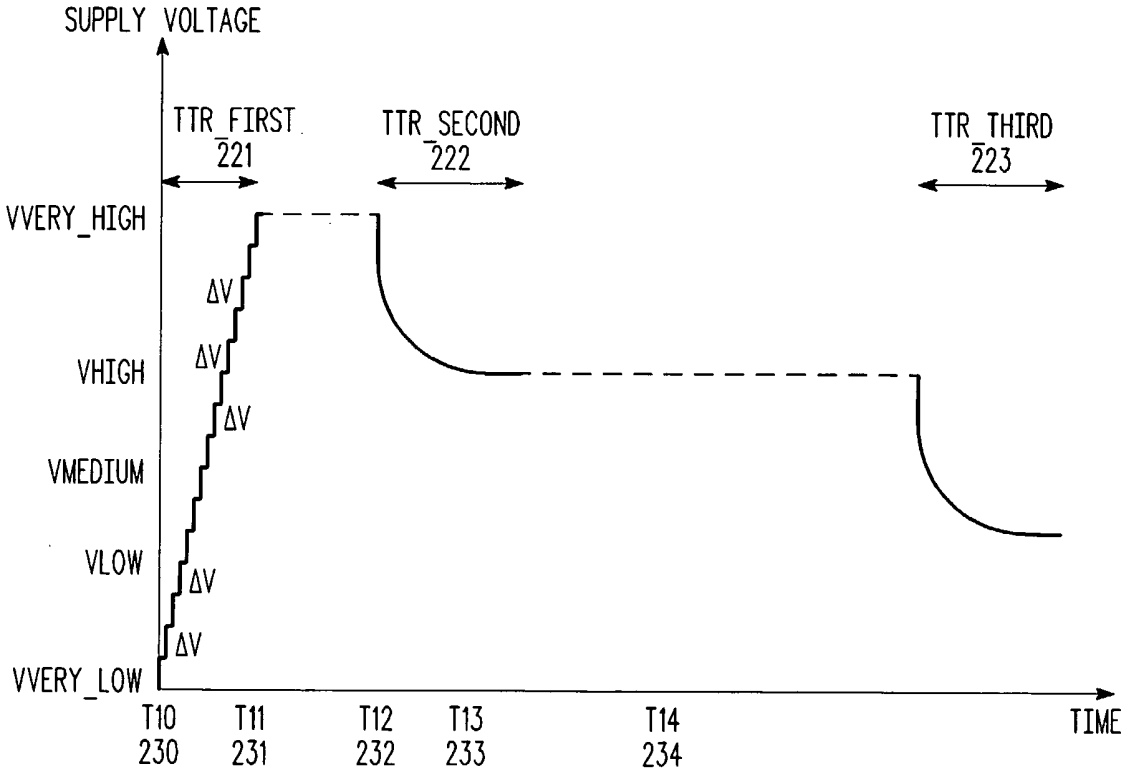
SUPPLY VOLTAGE
TTR_FIRST 221
TTR_SECOND 222
TTR_THIRD 223
VVERY_HIGH
VHIGH
VMEDIUM
VLOW
VVERY_LOW
ΔV
ΔV
ΔV
ΔV
ΔV
T10 230
T11 231
T12 232
T13 233
T14 234
TIME

FIG. 4

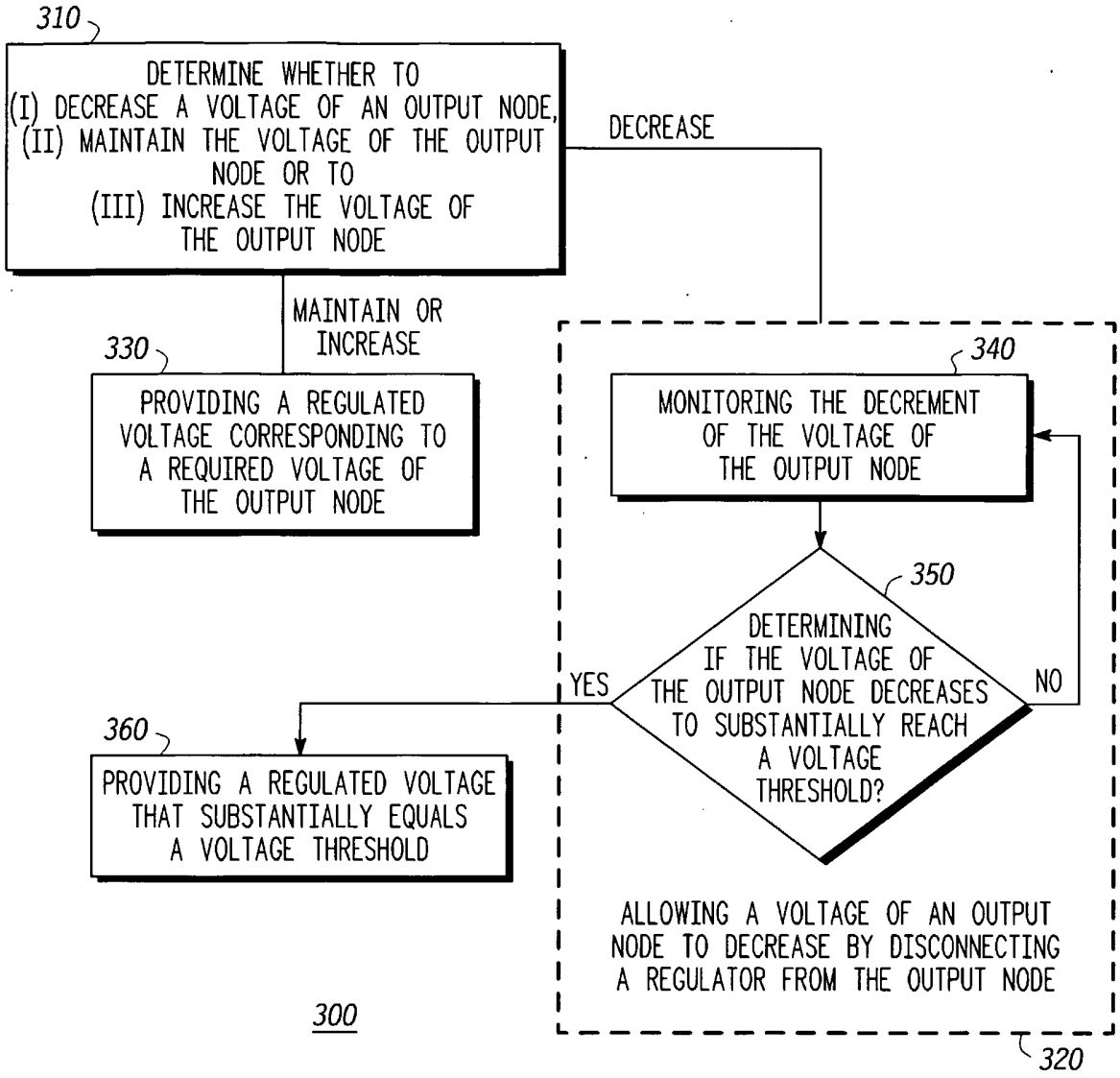
310
DETERMINE WHETHER TO
(I) DECREASE A VOLTAGE OF AN OUTPUT NODE,
(II) MAINTAIN THE VOLTAGE OF THE OUTPUT NODE OR TO
(III) INCREASE THE VOLTAGE OF THE OUTPUT NODE
DECREASE
MAINTAIN OR INCREASE
330
PROVIDING A REGULATED VOLTAGE CORRESPONDING TO A REQUIRED VOLTAGE OF THE OUTPUT NODE
340
MONITORING THE DECREMENT OF THE VOLTAGE OF THE OUTPUT NODE
350
DETERMINING IF THE VOLTAGE OF THE OUTPUT NODE DECREASES TO SUBSTANTIALLY REACH A VOLTAGE THRESHOLD?
YES
NO
360
PROVIDING A REGULATED VOLTAGE THAT SUBSTANTIALLY EQUALS A VOLTAGE THRESHOLD
ALLOWING A VOLTAGE OF AN OUTPUT NODE TO DECREASE BY DISCONNECTING A REGULATOR FROM THE OUTPUT NODE
320
300

FIG. 5