(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
30 October 2003 (30.10.2003)

PCT

(10) International Publication Number
WO 03/090356 A1

(51) International Patent Classification[7]: H03K 5/156

(21) International Application Number: PCT/US03/12292

(22) International Filing Date: 18 April 2003 (18.04.2003)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
10/126,036 18 April 2002 (18.04.2002) US

(71) Applicant: QUALCOMM INCORPORATED [US/US]; 5775 Morehouse Drive, San Diego, CA 92121 (US).

(72) Inventor: GOLDBLATT, Jeremy M.; 5136 Ellsworth Street, San Diego, CA 92110 (US).

(74) Agents: WADSWORTH, Philip R. et al.; QUALCOMM Incorporated, 5775 Morehouse Drive, San Diego, CA 92121 (US).

(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NI, NO, NZ, OM, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*
— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

WO 03/090356 A1

(54) Title: METHOD OF PERFORMING DUTY CYCLE CORRECTION

(57) Abstract: A method of performing duty cycle correction of an input signal having a non-uniform duty cycle is provided. A signal representative of the difference in duration between the positive and negative portions of the input signal duty cycle is formed. A switching level is derived from the signal. An output signal is then formed through a switching action, whereby durations of positive and negative portions of the output signal duty cycle are defined by crossover points between the input signal and the switching level. The signal (and switching level) are adjusted, if necessary, until the output signal duty cycle is at least substantially uniform.

METHOD OF PERFORMING DUTY CYCLE CORRECTION

1. Field of the Invention.

[0001] This invention relates to the fields of duty cycle correction and differential pair circuits, and, more specifically, to methods of performing duty cycle correction, including but not limited to methods of performing duty cycle correction using differential pair circuits.

2. Related Art.

[0002] Many non-linear systems introduce into a sinusoidal signal non-linearities in the form of high frequency harmonics, each at an integer multiple of the fundamental frequency. The harmonics may be odd harmonics, i.e., harmonics the frequency of which is an odd integer multiple of the fundamental frequency, even harmonics, i.e, harmonics the frequency of which is an even integer multiple of the fundamental frequency, or both.

[0003] The introduction of even harmonics to sinusoidal signals is problematic in differential or balanced applications where it is desired to maintain odd symmetry. The reason is the non-uniform group delay, i.e., a delay which varies with frequency, typically exhibited by many transmission media delays higher frequency components of a signal more than the fundamental frequency. Because of this non-uniform group delay, transmission of the signal through the media delays the even harmonics in the sinusoidal signal more than the fundamental frequency, thus destroying the odd symmetry exhibited by the signal.

[0004] Consider, for example, a sinusoidal signal at a particular fundamental frequency. Such a signal exhibits odd symmetry only if it has a uniform (about 50%) duty cycle, i.e., a duty cycle in which the portion of the period T during which the signal is positive is about equal to the portion of the period T the signal is negative. If even harmonics are introduced into such a signal, and the signal then transmitted over a transmission media with a non-constant group delay, the duty cycle of the resultant signal will no longer be uniform, i.e., at about 50%. Consequently, the signal will no

longer be suitable for differential or balanced applications where odd symmetry and a uniform duty cycle are required.

[0005] Consider, for example, the signal $x_y = 1.2 \sin(2\pi t_y)$, identified with numeral 100 in Figure 1. The signal $z_y = \sin(2\pi t_y) + .2\sin(4\pi t_y + \pi/2)$, identified in Figure 1 with numeral 102, is representative of the signal x_y to which has been added a second order harmonic with a phase shift of $\pi/2$. In addition, the signal $zz_y = \sin(2\pi t_y) + .2\sin(4\pi t_y + \pi/4)$, identified in Figure 1 with numeral 104, is representative of the signal x_y to which has been added a second order harmonic with a phase shift of $\pi/4$. Both the signals z_y and zz_y are representative of the signals that might result from introducing even harmonics into the signal x_y, and then passing the resultant signal through a transmission medium with a non-uniform group delay. While the signal x_y has a 50% duty cycle, it will be observed that both the signals z_y and zz_y have non-uniform duty cycles, i.e., signals at other that a 50% duty cycle. This can be seen most readily by comparing the zero-crossing for the signal x_y, identified with numeral 106, with that for the signals z_y and zz_y, identified with numeral 108, and observing that the latter zero crossings occur later in time that the former zero crossing, which occurs at $t_y = 0.5$.

[0006] As another example, consider again the signal $x_y = 1.2 \sin(2\pi t_y)$, identified with numeral 100 in Figure 2. The signal $z_y = \sin(2\pi t_y) + .2\sin(8\pi t_y + \pi/2)$, identified in Figure 2 with numeral 202, is representative of the signal x_y to which has been added a fourth order harmonic with a phase shift of $\pi/2$. In addition, the signal $zz_y = \sin(2\pi t_y) + .2\sin(8\pi t_y + \pi/4)$, identified in Figure 2 with numeral 204, is representative of the signal x_y to which has been added a fourth order harmonic with a phase shift of $\pi/4$. Again, both the signals z_y and zz_y are representative of the signals that might result from introducing even harmonics into the signal x_y, and then passing the resultant signal through a transmission medium with a non-uniform group delay. While the signal x_y has a 50% duty cycle, it will be observed that both the signals z_y and zz_y have non-uniform duty cycles. This can be seen most readily by comparing the zero-crossing for the signal x_y, identified with numeral 106, with that for the signals z_y and zz_y, identified with numeral 208, and observing that the latter zero crossings occur later in time that the former zero crossing. which occur at $t_y = 0.5$.

[0007] Other mechanisms exist for producing signals with non-uniform duty cycles when signals with uniform duty cycles are desired. Thus, what is needed is a method for performing duty cycle correction for signals having non-uniform duty cycles.

SUMMARY OF THE INVENTION

[0008] The invention provides a method of performing duty cycle correction of an input signal having a non-uniform duty cycle.

[0009] In this method, a signal is formed which is representative of the difference in duration between the positive and negative portions of the input signal duty cycle. A switching level is then derived from the signal. An output signal is formed through a switching action, whereby durations of positive and negative portions of the output signal duty cycle are defined by crossover points between the input signal and the switching level. The signal (and switching level) are then adjusted, if necessary, until the output signal duty cycle is substantially uniform.

[0010] In one embodiment, the signal representative of the difference in duration between the positive and negative portions of the input signal duty cycle is a DC voltage formed across one or more capacitors in a capacitor-degenerating differential pair circuit. A DC switching level is derived from the DC voltage. The output signal in this embodiment is formed through the switching actions of the differential pair circuit, whereby the durations of positive and negative portions of the output signal duty cycle are defined by crossover points between the input signal and the DC switching level. The DC voltage across the one or more capacitors (and the DC switching level) are automatically adjusted, if necessary, until the output signal duty cycle is at least substantially uniform.

[0011] Other systems, methods, features and advantages of the invention will be or will become apparent to one with skill in the art upon examination of the following figures and detailed description. It is intended that all such additional systems, methods, features and advantages be included within this description, be within the scope of the invention, and be protected by the accompanying claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] The components in the figures are not necessarily to scale, emphasis instead being placed upon illustrating the principles of the invention. In the figures, like reference numerals designate corresponding parts throughout the different views.

[0013] Figures 1 and 2 are examples illustrating how the addition to a sinusoidal signal having a uniform duty cycle of a delayed even harmonic introduces a non-uniform duty cycle.

[0014] Figure 3 illustrates a core portion of a bipolar implementation of a capacitor-degenerating differential pair circuit.

[0015] Figure 4A illustrates the operative portion of a capacitor-degenerating differential pair circuit during a first mode of operation when the input signal is above a switching level.

[0016] Figure 4B illustrates the operative portion of a capacitor-degenerating differential pair circuit during a second mode of operation when the input signal is below the switching level.

[0017] Figure 5A illustrates an example of an input signal having a non-uniform duty cycle, and Figure 5B illustrates the resultant output signal prior to adjustment of the switching level to substantially equalize the durations of the positive and negative portions of the output signal duty cycle.

[0018] Figure 6A illustrates an example of an input signal having a non-uniform duty cycle, and Figure 6B illustrates the resultant output signal after adjustment of the switching level to substantially equalize the durations of the positive and negative portions of the output signal duty cycle.

[0019] Figures 7A-7F illustrate alternate embodiments of a capacitor-degenerating differential pair circuit.

[0020] Figure 8 illustrates an example in which an increase in the switching level of a capacitor-degenerating differential pair circuit achieves a substantially uniform output signal duty cycle.

[0021] Figure 9 is a flowchart illustrating an embodiment of a method of performing duty cycle correction of an input signal having a non-uniform duty cycle.

DETAILED DESCRIPTION

[0022] As utilized herein, terms such as "about" and "substantially" are intended to allow some leeway in mathematical exactness to account for tolerances that are acceptable in the trade, e.g., any deviation upward or downward from the value modified by "about" or "substantially" by any value in the range(s) from 1% to 20% of such value.

[0023] Referring to Figure 3, an implementation of the core portion of a capacitor-degenerating differential pair circuit is illustrated. In this particular implementation, the circuit comprises a differential pair of NPN transistors, identified with numerals 302a and 302b, with a capacitor 310 coupled between the emitters of the two transistors. Each of the emitters is coupled to a current source, identified respectively with numerals 304a and 304b, which in turn is coupled to ground. Each of the current sources 304a and 304b source a current I_o. A voltage-mode differential input signal, V_{IN}^+ and V_{IN}^-, is input to the bases of the two transistors, identified respectively with numerals 306a and 306b (and with the labels 'A' and 'B'). In addition, a differential current mode output signal, I_{OUT}^+ and I_{OUT}^-, is produced on terminals 308a and 308b (identified respectively with labels 'C' and 'D').

[0024] While this particular implementation involves the use of bipolar NPN transistors, a differential voltage mode input signal, a differential current mode output signal, and a single capacitor between the emitters of the two transistors, it should be appreciated that the invention is not so limited and that embodiments of a capacitor degenerating differential pair circuit are possible for use in connection with the invention which involve the use of technologies other than bipolar, including but not limited to FET, MOS, or CMOS technology, that involve the use of PNP bipolar, FET, MOS, or CMOS transistors, that involves a single ended input signal or an input signal which is current mode rather than voltage mode, that involves a single ended output signal or an output signal which is voltage mode rather than current mode, or that involves more than one capacitor coupled between the emitters (or drains) of the differential pair of transistors.

[0025] When a periodic signal having a non-uniform duty cycle is input to the circuit at input terminals 306a and 306b, a DC voltage, V_{DC}, forms across the capacitor

310 in the circuit, which is representative of the difference in duration between the positive and negative portions of the input signal duty cycle.

[0026] To see this, observe that the circuit is configured to switch between two modes of operation. In the first mode, the transistor 302a is turned on, and the transistor 302b is turned off. This mode occurs during the positive portion of the input signal duty cycle, when the amplitude of the input signal at terminal 306a, V_{IN}^{+}, exceeds a switching level, equal to the sum of the threshold base to emitter voltage across the base to emitter junction of transistor 302a, V_{TH}, and the voltage at node 312a, and the amplitude of the input signal at terminal 306b, V_{IN}^{-}, is less than a switching level equal to the sum of the threshold base to emitter voltage across the base to emitter junction of transistor 302b, V_{TH}, plus the voltage at node 312b.

[0027] During this mode of operation, the circuit may be represented as shown in Figure 4A. As shown, due to application of Kirchoff's current law at node 312a, a current I_o flows through the capacitor 310 in the direction shown and charges it.

[0028] In the second mode of operation, transistor 302a is turned off, and transistor 302b is turned on. This mode occurs during the negative portion of the input signal duty cycle, when the amplitude of the input signal at terminal 306a, V_{IN}^{+}, is less than a switching level equal to the sum of the threshold base to emitter voltage across the base to emitter junction of transistor 302a, V_{TH}, and the voltage at node 312a, V_{312a}, and the amplitude of the input signal at terminal 306b, V_{IN}^{-}, is greater than a switching level equal to the sum of the threshold voltage across the base to emitter junction of transistor 302b, V_{TH}, and the voltage at node 312b, V_{312b}.

[0029] During this mode of operation, the circuit may be represented as shown in Figure 4B. As shown, the current I_o flows through capacitor 310 in the reverse direction and discharges it.

[0030] The charge q that will remain on the capacitor 310 upon the conclusion of the positive and negative portions of the input signal duty cycle can be expressed as $I_o \bullet (T_p - T_n)$, where T_p is the duration of the positive portion of the input signal duty cycle, and T_n is the duration of the negative portion of the input signal duty cycle. The DC voltage that forms across the capacitor, V_{DC}, can be expressed as $I_o \bullet (T_p - T_n)/C_p$. It can be

seen that this voltage is representative of the difference in duration between the positive and negative portions of the input signal duty cycle, T_p-T_n.

[0031] The DC voltage which forms across capacitor 310 modifies the switching action which occurs in the differential pair circuit so that the duty cycle of the output signal is substantially uniform.

[0032] To see this, observe that, prior to the formation of the DC voltage across the capacitor 310, an output signal is formed having a duty cycle which matches that of the input signal. Referring to Figure 5A, for example, a single-ended input signal is shown having a non-uniform duty cycle where the positive portion of the duty cycle, T_p, exceeds the negative portion of the duty cycle, T_n. Figure 5B illustrates the resultant output signal. As shown, the output signal also has a non-form duty cycle which matches that of the input signal. In particular, akin to the input signal, the positive portion of the output signal duty cycle, T_p, exceeds the negative portion of the output signal duty cycle, T_n.

[0033] Once the DC voltage has formed across the capacitor 310, referring to Figure 6A, the switching level for the input signal increases from the level identified with numeral 502 to the level identified by numeral 602, due to the DC voltage which forms across capacitor 310. Due to the change in the switching level of the input signal, the crossover points between the input signal and the switching level change from 502a, 502b, 502c, and 502d to 602a, 602b, 602c, and 602d. Consequently, the duration of the positive portion of the input signal duty cycle decreases from T_p to T_p^*, and the duration of the negative portion of the input signal duty cycle increases from T_n to T_n^*.

[0034] Referring to Figure 6B, the duration of the positive portion of the duty cycle of the resultant output signal which is formed, which is defined by the difference between successive crossover points between the input signal and the switching level, has also changed to T_p^*. Similarly, the duration of the negative portion of the duty cycle of the resultant output signal which is formed, which is also defined by the difference between successive crossover points between the input signal and the switching level, has also changed to T_n^*. If T_p^* is not equal to T_n^*, the DC voltage across the capacitor 310 will automatically adjust until the two are about equal. For example, if T_p^* exceeds T_n^*, the DC voltage across the capacitor 310 will increase, causing the switching level to

increase until T_p^* about equals T_n^*. Similarly, if T_p^* is less than T_n^*, the DC voltage across the capacitor 310 will decrease, causing the switching level to decrease until T_p^* about equals T_n^*. In either case, since T_p^* about equals to T_n^*, the output signal has a uniform duty cycle.

[0035] Figures 7A-7F illustrate some of the alternate embodiments of the core circuit of Figure 3 which are possible. Other embodiments are possible so these embodiments should not be construed as limiting.

[0036] Figures 7A and 7B illustrate embodiments where the input signal, V_{IN}, is a single-ended voltage mode signal, and the output signal is a differential current mode signal identified as I_{OUT}^+ and I_{OUT}^-.

[0037] Figures 7C illustrates an embodiment in which the input signal is a differential voltage mode signal identified as V_{IN}^+ and V_{IN}^-, and the output signal is a differential voltage mode signal identified as V_{OUT}^+ and V_{OUT}^-.

[0038] Figure 7D illustrates an embodiment in which the input signal is a differential voltage mode signal identified as V_{IN}^+ and V_{IN}^-, and the output signal is a single ended current mode signal identified as I_{OUT}.

[0039] Figure 7E illustrates an embodiment in which the input signal is a differential voltage mode signal identified as V_{IN}^+ and V_{IN}^-, and the output signal is fed into a current mode logic section.

[0040] Figure 7F illustrates an embodiment in which the input signal is a differential current mode signal identified as I_{IN}^+ and I_{IN}^-, and the output signal is a differential current mode signal identified as I_{OUT}^+ and I_{OUT}^-.

[0041] In one implementation example of the circuit illustrated in Figure 3, transistors 302a and 302b are matched bipolar NPN transistors each having the following physical parameters: emitter length = 3 microns, emitter width = 0.4 microns, and number of emitters = 6. Capacitor 310 in this example comprises four capacitors placed in parallel and having a combined capacitance of 1.0 pF. Each such capacitor has the following physical parameters: length = 10.4 microns, and width = 60.1 microns.

[0042] Figure 8 illustrates the operation of this implementation example in correcting the duty cycle of an input signal 802 having a non-uniform duty cycle with respect to the unadjusted switching level 804. As illustrated, the duration of the positive

portion of the duty cycle, represented by the horizontal distance between the markers M1 and M2, exceeds the duration of the negative portion of the duty cycle, represented by the horizontal distance between the markers M2 and M3. Due to operation of the circuit, the switching level is adjusted to the level identified with the marker M4. Relative to this adjusted switching level, the duty cycle of the input cycle is substantially uniform. This in turn causes the duty cycle of the output signal to be substantially uniform.

[0043] Referring to Figure 9, an embodiment of a method of performing duty cycle correction of an input signal having a non-uniform duty cycle is illustrated. The input signal may be a differential or single ended signal, and it may also be a current mode or voltage mode signal.

[0044] The method begins with step 902, which comprises forming a signal representative of the difference in duration between the positive portion of the input signal duty cycle and the negative portion of the input signal duty cycle. In one implementation, this signal is a DC voltage formed across one or more capacitors in a capacitor-degenerating differential pair circuit.

[0045] From step 902, the method proceeds to step 904, which comprises deriving a switching level from the signal resulting from step 902.

[0046] From step 904, the method proceeds to step 906, which comprises forming an output signal having a duty cycle, whereby durations of positive and negative portions of the output signal duty cycle are defined by crossover points between the input signal and the switching level resulting from step 904. The output signal may be differential or single-ended signal, and it may also be a current mode or a voltage mode signal. In one implementation example, the output signal is formed through the switching action of a capacitor-degenerating differential pair circuit.

[0047] From step 906, the method proceeds to step 908, which comprises adjusting, if necessary, the signal (and the resultant switching level) until the duty cycle of the output signal is uniform or at least substantially uniform. (In this embodiment, it is assumed that a switching level is possible which substantially equalizes the positive and negative portions of the output signal duty cycle.)

[0048] In "A 2.5-Gb/s 15-mW Clock Recovery Circuit," Behzad Razavi, IEEE Journal of Solid-State Circuits, Vol. 31, No. 4, April 1996, pp. 472-480, a capacitor-degenerating differential pair circuit is illustrated (see Figure 9(a)) and described for use in a particular application, i.e., clock recovery. However, this reference does not teach, describe or suggest the use of a capacitor-degenerating differential pair circuit for performing duty cycle correction.

[0049] While various embodiments of the invention have been described, it will be apparent to those of ordinary skill in the art that many more embodiments and implementations are possible that are within the scope of this invention.

CLAIMS

What is claimed is:

1. A method of performing duty cycle correction of an input signal having a non-uniform duty cycle using a capacitor-degenerating differential pair circuit comprising:

inputting to the circuit the input signal having the non-uniform duty cycle;

forming a DC voltage across one or more capacitors in the circuit which is representative of the difference in duration between positive and negative portions of the input signal duty cycle;

deriving a DC switching level from the DC voltage;

forming, through a switching action of the differential pair circuit, an output signal having a duty cycle, whereby durations of positive and negative portions of the output signal duty cycle are defined by crossover points between the input signal and the DC switching level; and

adjusting, if necessary, the DC voltage until the output signal duty cycle is at least substantially uniform.

2. The method of claim 1 wherein the circuit is implemented through bipolar technology.

3. The method of claim 1 wherein the circuit is implemented through FET technology.

4. The method of claim 1 wherein the circuit is implemented through MOS technology.

5. The method of claim 4 wherein the circuit is implemented through CMOS technology.

6. The method of claim 1 wherein the input signal is a single-ended signal.

7. The method of claim 1 wherein the input signal is a differential signal.

8. The method of claim 1 wherein the input signal is a voltage mode signal.

9. The method of claim 1 wherein the input signal is a current mode signal.

10. The method of claim 1 wherein the output signal is a single-ended signal.

11. The method of claim 1 wherein the output signal is a differential signal.

12. The method of claim 1 wherein the output signal is a voltage mode signal.

13. The method of claim 1 wherein the output signal is a current mode signal.

14. A method of performing duty cycle correction of an input signal having a non-uniform duty cycle using a capacitor-degenerating differential pair circuit comprising:

a step for inputting to the circuit the input signal having the non-uniform duty cycle;

a step for forming a DC voltage across one or more capacitors in the circuit which is representative of the difference in duration between positive and negative portions of the input signal duty cycle;

a step for deriving a DC switching level from the DC voltage;

a step for forming, through a switching action of the differential pair circuit, an output signal having a duty cycle, whereby durations of positive and negative portions of the output signal duty cycle are defined by crossover points between the input signal and the DC switching level; and

a step for adjusting, if necessary, the DC voltage until the output signal duty cycle is at least substantially uniform.

15. The method of claim 14 wherein the input signal comprises a sinusoidal signal to which has been introduced one or more delayed even harmonics.

16. The method of claim 14 wherein the capacitor-degenerating differential pair circuit comprises one or more capacitors coupled between the emitters of a differential pair of bipolar transistors.

17. The method of claim 14 wherein the capacitor-degenerating differential pair circuit comprises one or more capacitors coupled between the drains of a differential pair of field effect transistors.

18. A method of performing duty cycle correction of an input signal having a non-uniform duty cycle comprising:

forming a signal which is representative of the difference in duration between positive and negative portions of the input signal duty cycle;

deriving a switching level from the signal;

forming, through a switching action, an output signal having a duty cycle, whereby durations of positive and negative portions of the output signal duty cycle are defined by crossover points between the input signal and the switching level; and

adjusting, if necessary, the signal until the output signal duty cycle is at least substantially uniform.

19. The method of claim 18 wherein the signal is a DC signal.

20. The method of claim 19 wherein the DC signal is a DC voltage.

21. The method of claim 18 wherein the switching level is a DC switching level.

22. A method of performing duty cycle correction of an input signal having a non-uniform duty cycle comprising:

a step for forming a signal which is representative of the difference in duration between positive and negative portions of the input signal duty cycle;

a step for deriving a switching level from the signal;

a step for forming, through a switching action, an output signal having a duty cycle, whereby durations of positive and negative portions of the output signal duty cycle are defined by crossover points which occur between the input signal and the switching level; and

a step for adjusting, if necessary, the signal until the output signal duty cycle is at least substantially uniform.

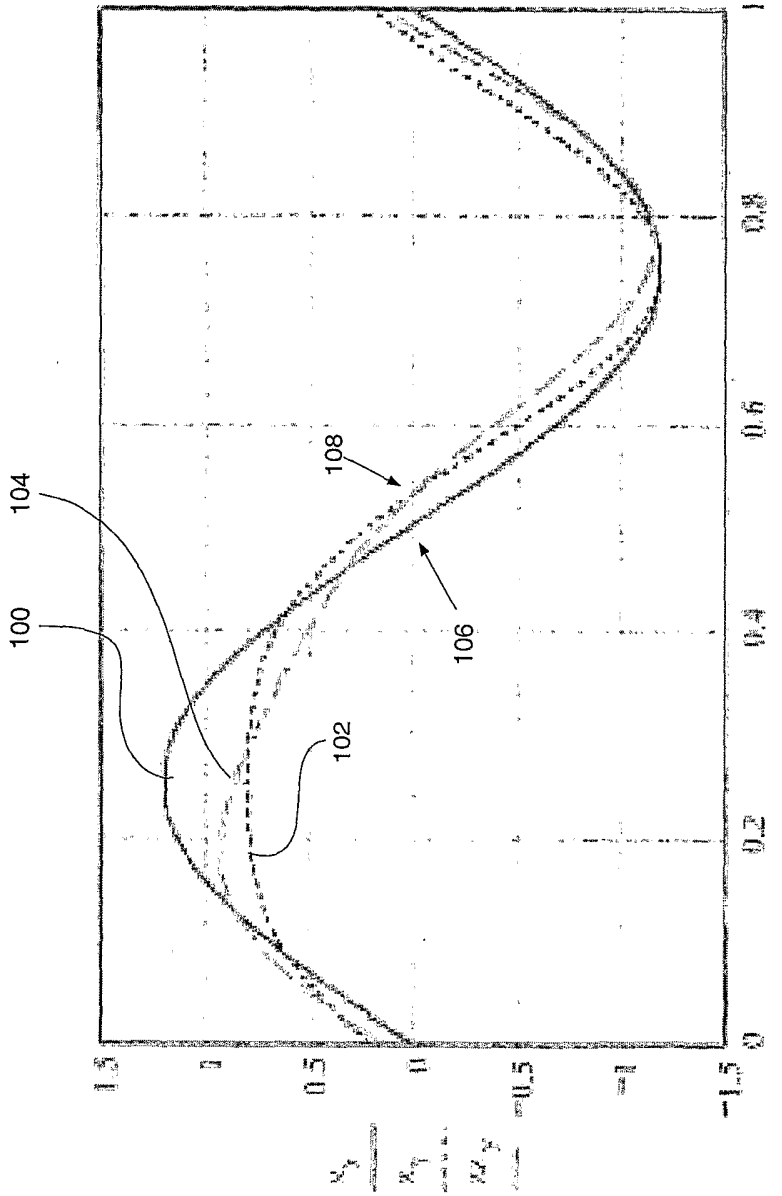


FIGURE 1

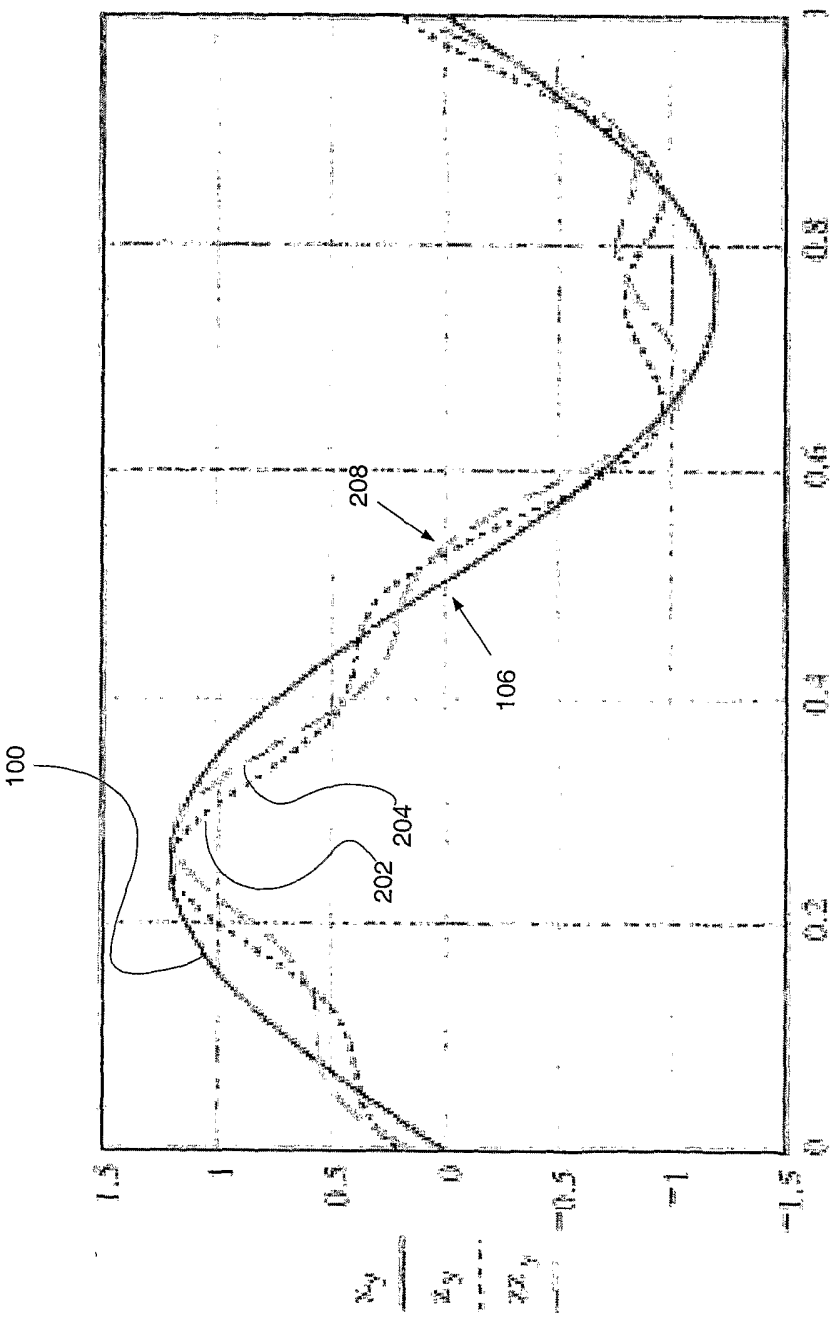


FIGURE 2

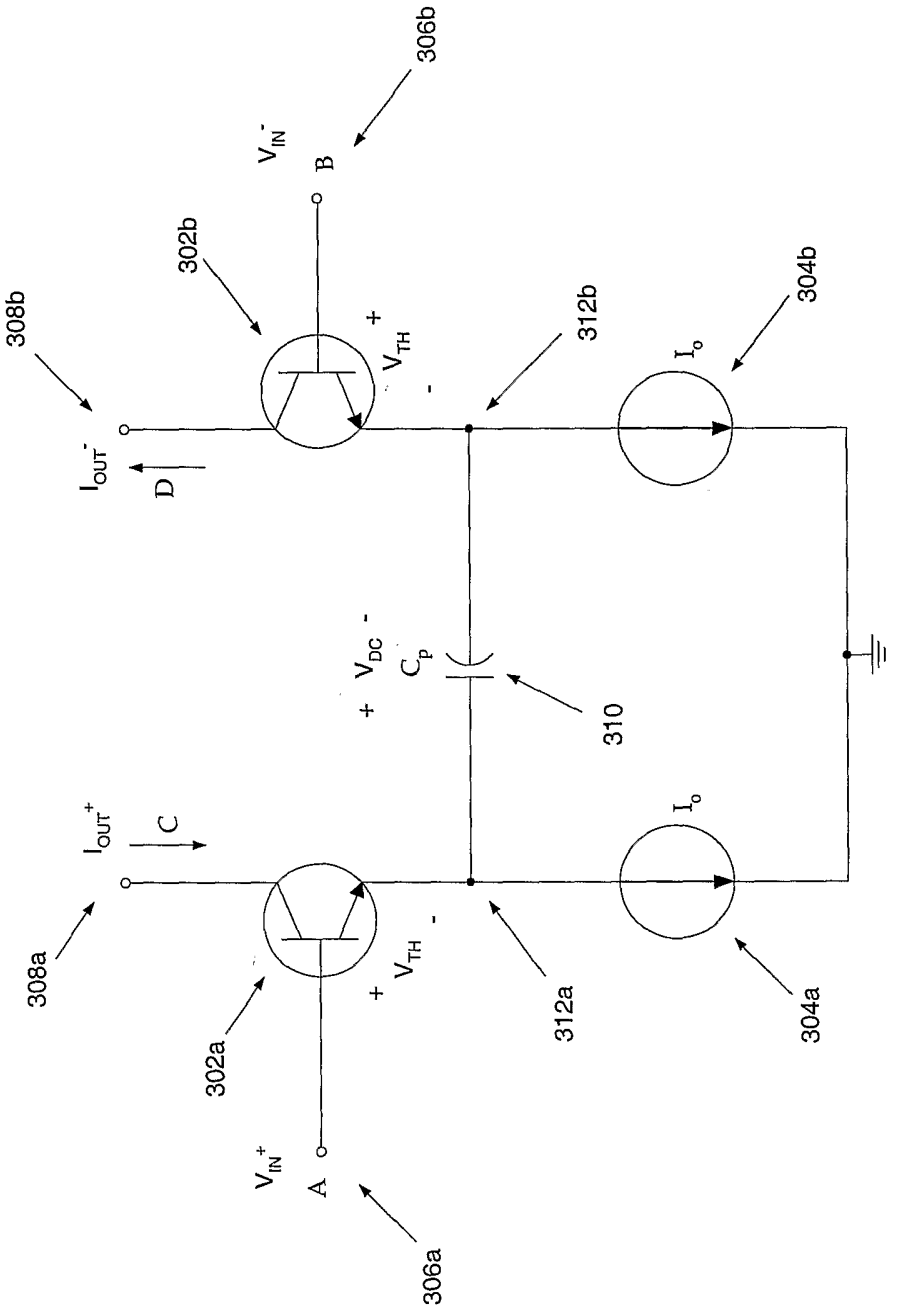

306b
V_{IN}^-
B
302b
308b
V_{TH}
312b
I_o
304b
I_{OUT}^-
D
V_{DC}
C_p
310
I_{OUT}^+
C
I_o
308a
V_{TH}
312a
304a
302a
V_{IN}^+
A
306a

FIGURE 3

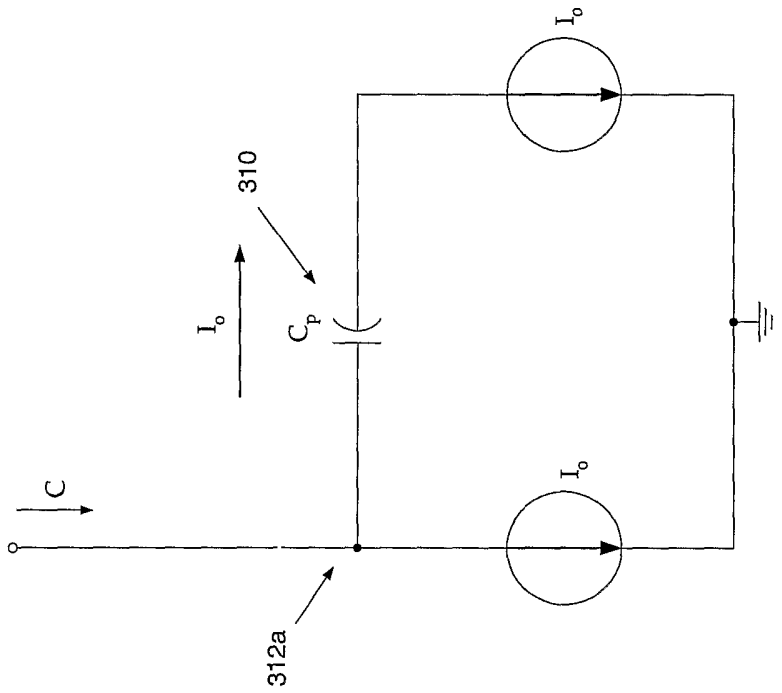


FIGURE 4A

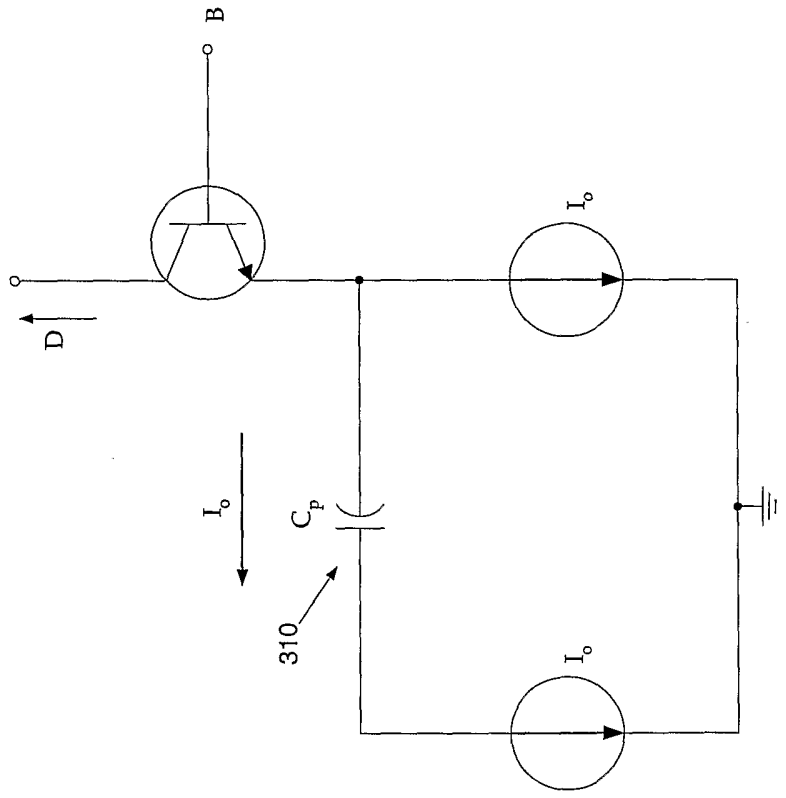


FIGURE 4B

FIG. 5A

FIG. 5B

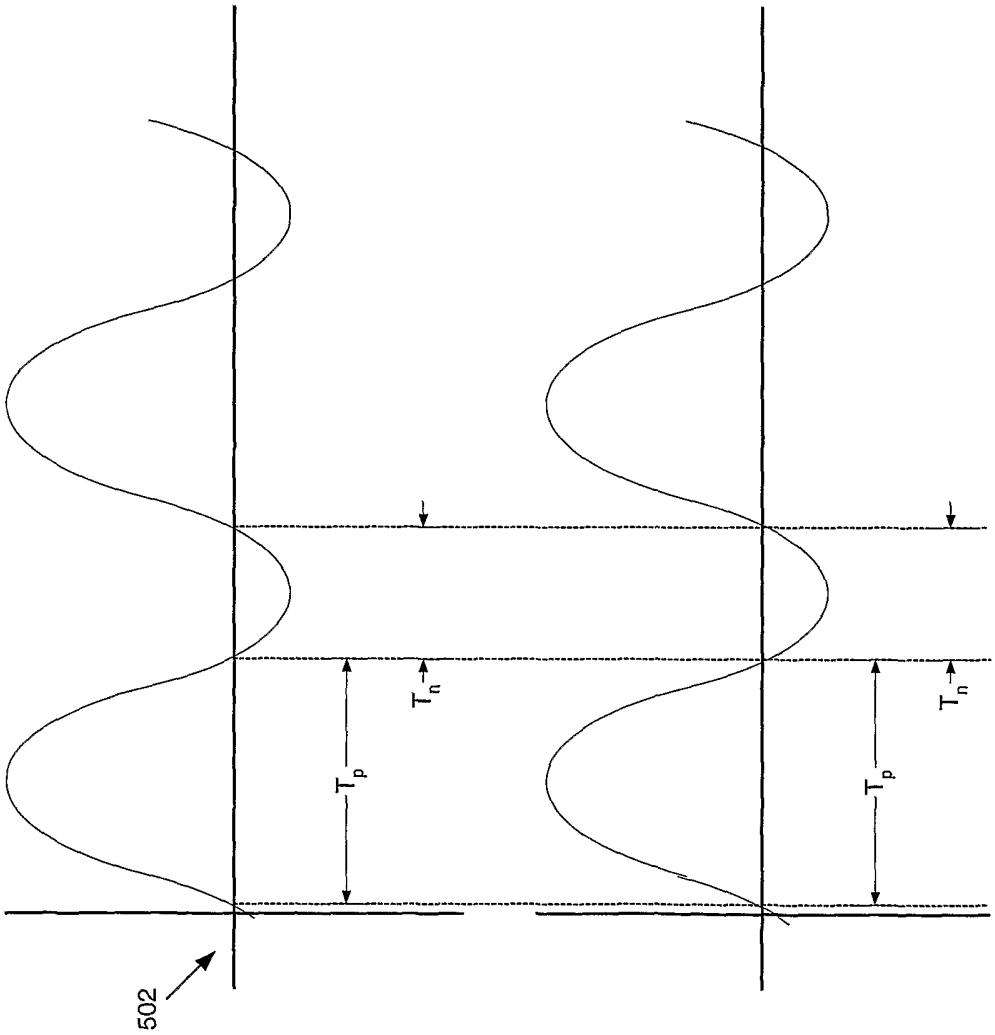
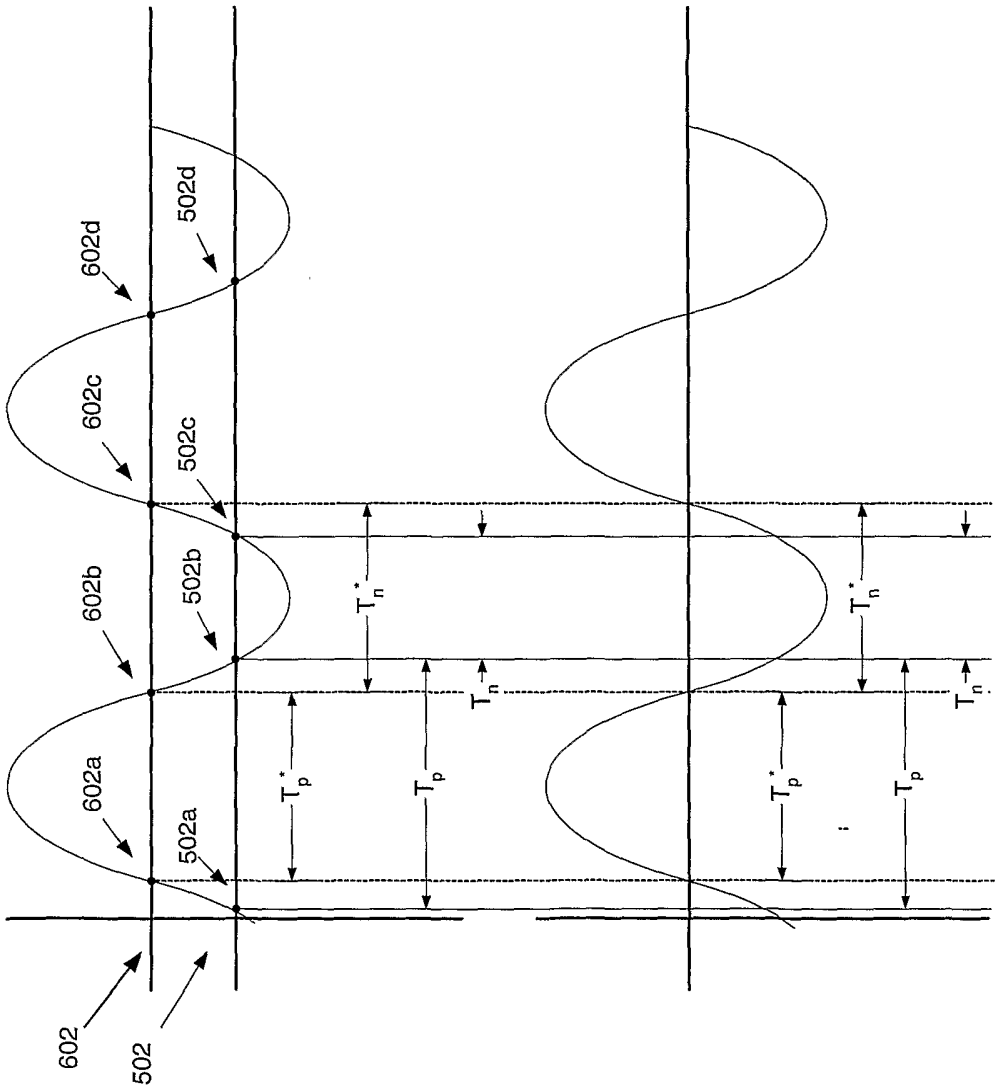


FIG. 6A

FIG. 6B



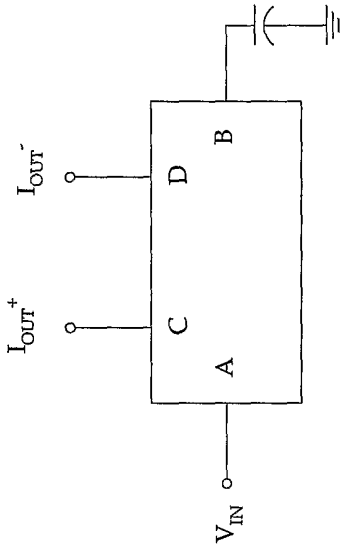


FIG. 7B

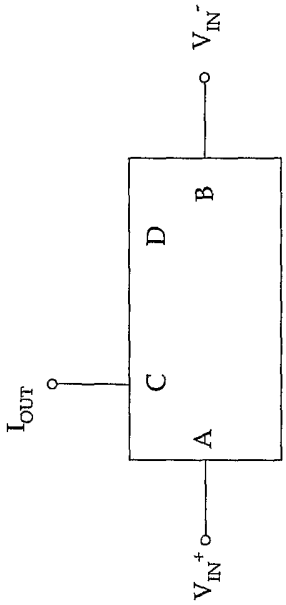


FIG. 7D

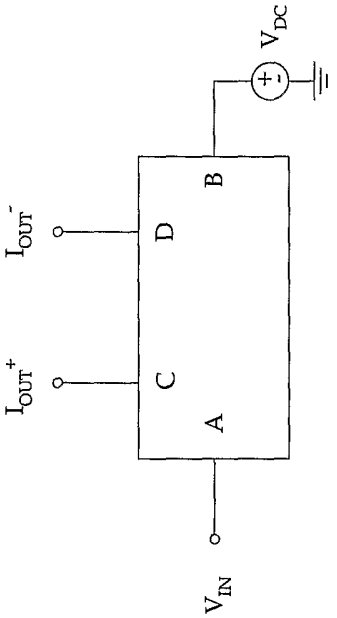


FIG. 7A

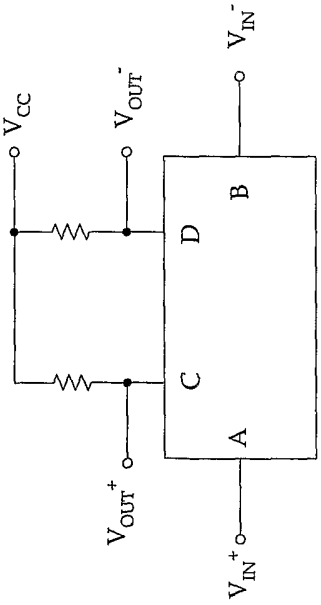


FIG. 7C

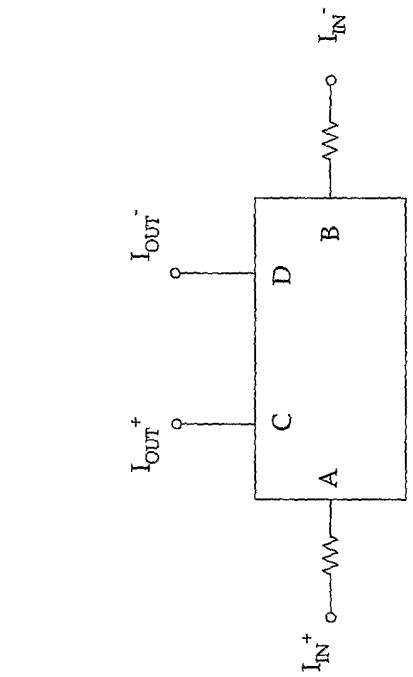


FIG. 7F

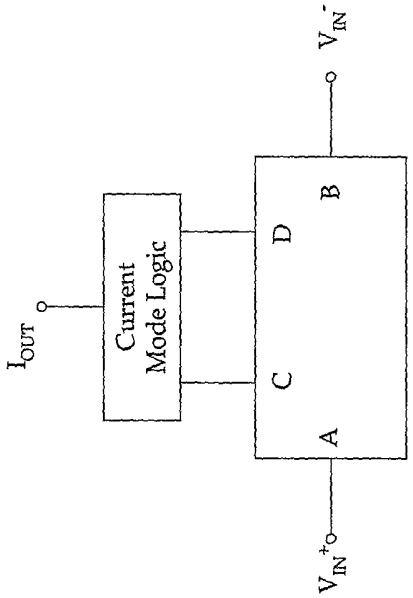


FIG. 7E

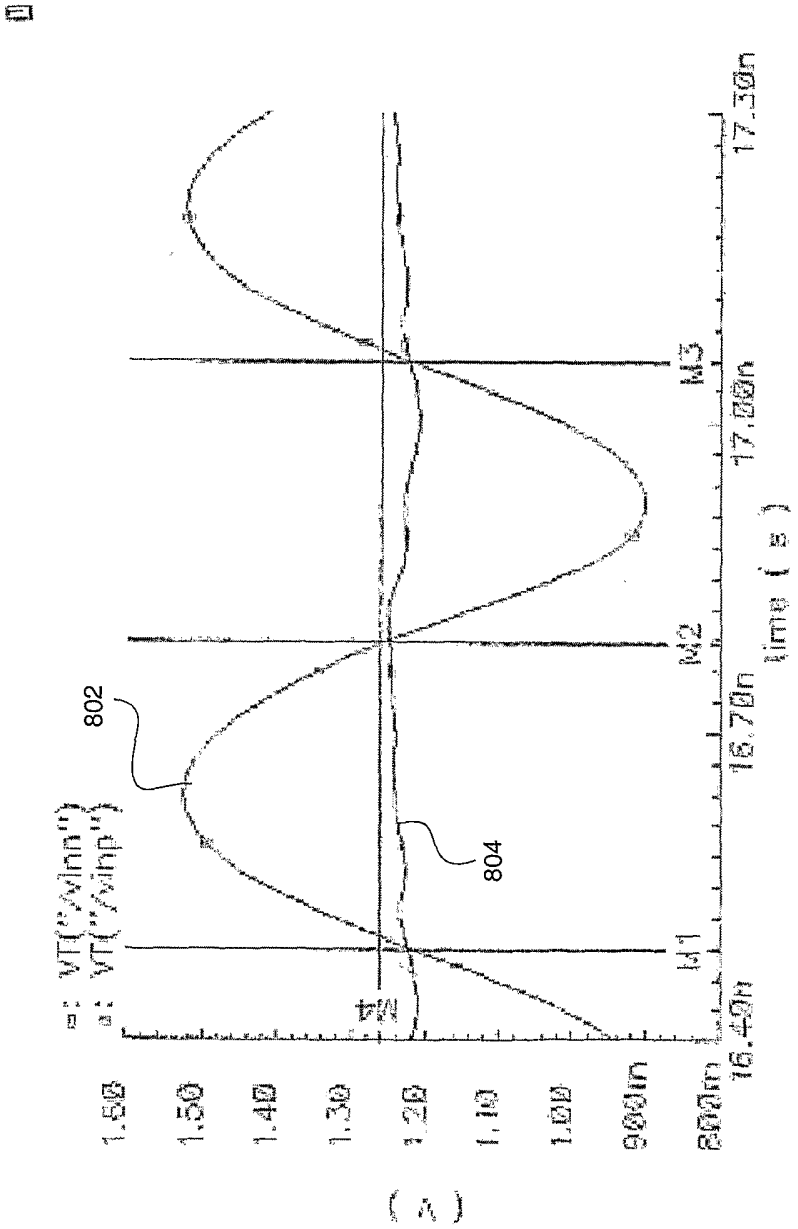

VT("/vinn")
VT("/vinp")
802
804
M1
M2
M3
16.40n
16.70n
17.00n
17.30n
Time (s)
1.60
1.50
1.40
1.30
1.20
1.10
1.00
900m
800m

FIGURE 8

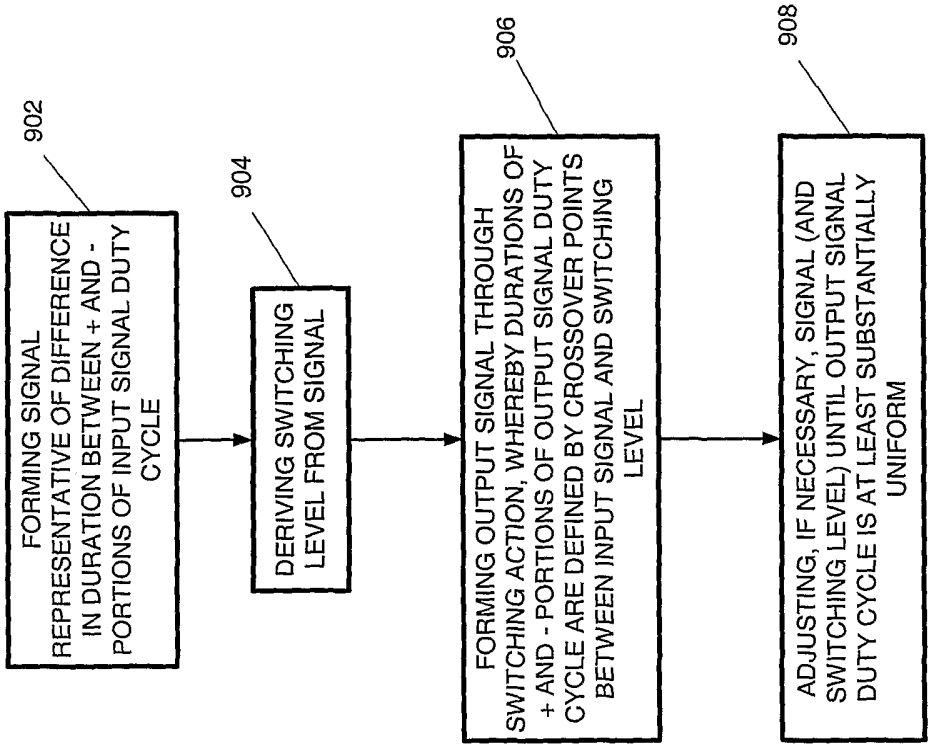

902
FORMING SIGNAL REPRESENTATIVE OF DIFFERENCE IN DURATION BETWEEN + AND - PORTIONS OF INPUT SIGNAL DUTY CYCLE
904
DERIVING SWITCHING LEVEL FROM SIGNAL
906
FORMING OUTPUT SIGNAL THROUGH SWITCHING ACTION, WHEREBY DURATIONS OF + AND - PORTIONS OF OUTPUT SIGNAL DUTY CYCLE ARE DEFINED BY CROSSOVER POINTS BETWEEN INPUT SIGNAL AND SWITCHING LEVEL
908
ADJUSTING, IF NECESSARY, SIGNAL (AND SWITCHING LEVEL) UNTIL OUTPUT SIGNAL DUTY CYCLE IS AT LEAST SUBSTANTIALLY UNIFORM

FIGURE 9

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 03/12292

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H03K5/156

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H03K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 572 158 A (LEE THOMAS H ET AL) 5 November 1996 (1996-11-05) column 2, line 20 -column 4, line 6; figures 1,2	1-15, 17-22
X	US 6 169 434 B1 (PORTMANN CLEMENZ L) 2 January 2001 (2001-01-02) column 2, line 29-65; figure 1 column 3, line 49 -column 4, line 51; figure 4	1-15, 17-22
X	US 6 169 765 B1 (HOLCOMBE WAYNE T) 2 January 2001 (2001-01-02) column 6, line 19 -column 8, line 65; figure 5	1,3-6, 8-10, 12-15, 18-22

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
11 August 2003	20/08/2003

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Moll, P

INTERNATIONAL SEARCH REPORT

Internati[redacted] Application No
PCT/US 03/12292

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 907 254 A (CHANG THEODORE H) 25 May 1999 (1999-05-25) column 2, line 20 -column 3, line 11; figure 1	18-22
X	EP 0 377 897 A (TOKYO SHIBAURA ELECTRIC CO) 18 July 1990 (1990-07-18) column 4, line 25 -column 9, line 4; figures 2,3	18-22

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/US 03/12292

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5572158 A	05-11-1996	AU 1726795 A	29-08-1995
		WO 9522202 A1	17-08-1995
US 6169434 B1	02-01-2001	TW 408259 B	11-10-2000
		WO 9912259 A2	11-03-1999
US 6169765 B1	02-01-2001	NONE	
US 5907254 A	25-05-1999	NONE	
EP 0377897 A	18-07-1990	EP 0377897 A2	18-07-1990
		JP 2085883 C	23-08-1996
		JP 2262714 A	25-10-1990
		JP 7114349 B	06-12-1995
		US 5057702 A	15-10-1991