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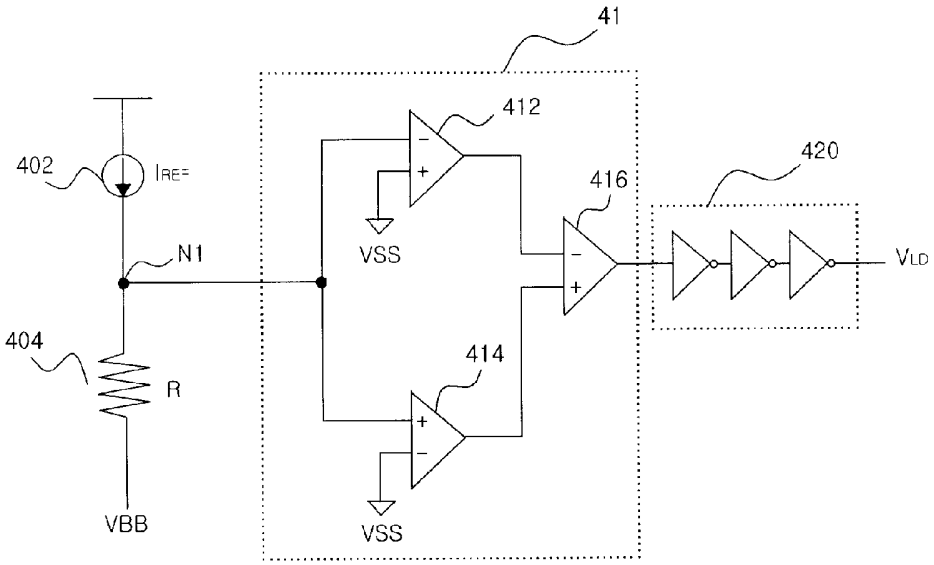
(54) Title: NEGATIVE VOLTAGE LEVEL DETECTOR




(57) Abstract: Provided is a negative voltage level detector for detecting a negative voltage level in a negative word-line driver to control oscillation for charge pumping, which includes a constant current source generated by a bandgap reference current generator, a resistor having one end connected to an output port of the constant current source to form a first node and the other end connected to VBB, and a differential amplification portion, in which a plurality of differential amplifiers are connected in cascade, having an input port connected to the first node and an output port connected to a control signal input port to control the oscillation of an oscillation portion. The differential amplification portion compares a voltage of the first node with VSS of a ground voltage level and outputs a signal of a ground voltage level if the voltage of the first node is lower than VSS and a signal of a VDD voltage level if the voltage of the first node is higher than VSS.

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*For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.*

# Description

# NEGATIVE VOLTAGE LEVEL DETECTOR

## Technical Field

[1] The present invention relates to a negative voltage level detector, and more particularly, to a negative voltage level detector which is stable and insensitive to a PVT.

## Background Art

[2] Recently, a low voltage of 1.5 V or less is widely used for a semiconductor circuit. Using a low voltage reduces storage charge and accordingly refresh time is shortened. To solve the problem, there is a conventional negative voltage word-line driving method in which the refresh characteristic is determined by junction leakage current and subthreshold leakage current at a DRAM cell transistor. A low VBB ( back bias voltage ) level lowers a threshold voltage of the DRAM cell transistor so that the threshold voltage increase in an OFF state. Thus, it is a problem that this current cannot be ignored.

[3] To solve the above problem, as another conventional driving method, a BSG (boosted sense-ground) method to restrict the subthreshold current of the DRAM cell transistor has been suggested. However, according to this method, since BL swing is smaller than VDD, a BL sense voltage is reduced so that the refresh characteristic is deteriorated, which is not suitable for a low voltage operation.

[4] FIG. 1 shows the structure of a negative voltage word-line driver to solve the above problem. Referring to FIG. 1, it is noted that a negative voltage word-line driver 10 is configured as shown in FIG. 1 to restrict the increase of subthreshold current due to the low VBB and that the voltage of a word-line WL that is not selected is -0.5 V that is a low VBB. That is, a superior refresh characteristic can be obtained by making the VGS (gate-to-source voltage) of the DRAM cell transistor for a tRAS cycle to reduce the subthreshold current. When the word-line WL is selected, the VT (threshold voltage) loss at a cell is removed by a VPP (boosted voltage) with the word-line driver.

[5] The negative word-line driver uses the same circuit as a VBB generator that is conventionally used. FIG. 2 is a block diagram of the general configuration of a back bias voltage generator. Referring to FIG. 2, a VBB generator 20 includes a VBB level detector 202, an oscillator 204, a charge pumping portion 206, and a capacitor 208. Since the VBB generator 20 uses a negative feedback mechanism, the VBB can maintain a target voltage. When the VBB does not reach the target voltage, the output voltage VLD of the VBB level detector 202 is VDD. The oscillator 204 continues to oscillate so that negative charge pumping continues toward the capacitor 208 that is a load capacitor CL. The VBB level continuously decreases in a negative direction toward the target voltage. When the VBB exceeds the target voltage, the output voltage

VLD becomes 0 and the oscillator 204 stops oscillation so that charge pumping does not continue any longer. Thus, the VBB maintains a voltage value that is the target voltage.

[6] When a gate-received scheme as shown in FIG. 3 is used as an example of the VBB level detector 202, since the change in the VBB level according to the change in PVT is great, a poly-silicon fuse is used so that laser repair is needed at the level of a wafer.

## Disclosure of Invention

### Technical Problem

[7] To solve the above and/or other problems, the present invention provides a negative voltage level detector which is not sensitive to PVT.

### Technical Solution

[8]

[9] According to an aspect of the present invention, a negative voltage level detector for detecting a negative voltage level in a negative word-line driver to control oscillation for charge pumping comprises a constant current source generated by a bandgap reference current generator, a resistor having one end connected to an output port of the constant current source to form a first node and the other end connected to VBB, and a differential amplification portion, in which a plurality of differential amplifiers are connected in cascade, having an input port connected to the first node and an output port connected to a control signal input port to control the oscillation of an oscillation portion, wherein the differential amplification portion compares a voltage of the first node with VSS of a ground voltage level and outputs a signal of a ground voltage level if the voltage of the first node is lower than VSS and a signal of a VDD voltage level if the voltage of the first node is higher than VSS.

[10] The differential amplification portion comprises a first differential amplifier having an inverted input port connected to the first node and a non-inverted input port connected to VSS, a second differential amplifier having an inverted input port connected to VSS and a non-inverted input port connected to the first node, and a third differential amplifier having an inverted input port connected to an output port of the first differential amplifier and a non-inverted input port connected to an output port of the second differential amplifier.

[11] The negative voltage level detector further comprises a level inversion portion having an input port connected to an output port of the differential amplification portion and inverts an output signal of the differential amplification portion to output the inverted signal.

### Description of Drawings

[12] FIG. 1 is a circuit diagram showing the configuration of the conventional negative voltage word-line driver;

[13] FIG. 2 is a block diagram showing the typical configuration of a conventional VBB generator;

[14] FIG. 3 is a circuit diagram showing the configuration of the conventional VBB detector using a gate-received scheme; and

[15] FIG. 4 is a circuit diagram showing the configuration of a negative voltage level detector according to an embodiment of the present invention.

## Best Mode

[16] Referring to FIG. 4, a negative voltage level detector according to an embodiment of the present invention for detecting a negative voltage level in a negative word-line driver (not shown) to control oscillation for charge pumping includes a constant current source $I_{REF}$ 402, a resistor R 404, and a differential amplification portion 41. The constant current source 402 is generated by a bandgap reference current generator (not shown). The resistor 404 has one end connected to an output end of the constant current source 402 to form a first node N1 and the other end connected to VBB.

[17] The differential amplification portion 41, in which a plurality of differential amplifiers are connected in cascade, has an input port connected to the first node N1 and an output port connected to a control signal input port to control the oscillation of the oscillator 204 (please refer to FIG. 2). The differential amplification portion 41 compares the voltage of the first node N1 with the VSS of a ground voltage level. If the voltage of the first node N1 is lower than VSS, the differential amplification portion 41 outputs a signal of a ground voltage level, for example, '0'. If the voltage of the first node N1 is higher than VSS, the differential amplification portion 41 outputs a signal of a VDD voltage level.

[18] In the present embodiment, the differential amplification portion 41 includes a first differential amplifier 412 having an inverted input port connected to the first node N1 and a non-inverted input port connected to VSS, a second differential amplifier 414 having an inverted input port connected to VSS and a non-inverted input port connected to the first node N1, and a third differential amplifier 416 having an inverted input port connected to the output port of the first differential amplifier 412 and a non-inverted input port connected to the output port of the second differential amplifier 414.

[19] Also, the negative voltage level detector includes a level inversion portion 420 having an input port connected to the output port of the differential amplification portion 41 and inverts the output signal of the differential amplification portion 41 to output the inverted signal.

[20] In the operation of the negative voltage level detector configured as above, IREF

402 that is constant current generated by the bandgap reference current generator (not shown) flows in the resister R 404. The voltage of the first node N1 is compared by the cascaded differential amplifiers with VSS that is a ground voltage level. If the voltage of the first node N1 is higher than VSS, the output voltage VLD becomes VDD so that negative charge pumping continues at the VBB generator 20. Accordingly, the VBB voltage decreases in the negative direction so that the voltage of the first node N1 drops.

[21] If the voltage of the first node N1 is lower than VSS, the output voltage VLD becomes '0' that is the ground voltage level so that charge pumping stops. At this time, the VBB becomes a target voltage of -R×IREF.

[22] The negative voltage level detector uses the constant current source generated by the bandgap reference current generator and the constant current source is obtuse to the change of PVT. Thus, as the negative voltage level is detected in the negative word-line driver, the oscillation for charge pumping is controlled so that a stable operation can be made.

[23] As described above, according to the present invention, the negative voltage level detector according to the present invention uses the constant current source generated by the bandgap reference current generator. Since the constant current source is obtuse to the change of PVT, as the negative voltage level is detected in the negative word-line driver, the oscillation for charge pumping is controlled so that a stable operation can be made.

# Claims

[1] 1. A negative voltage level detector for detecting a negative voltage level in a negative word-line driver to control oscillation for charge pumping, the detector comprising:

a constant current source generated by a bandgap reference current generator;

a resistor having one end connected to an output port of the constant current source to form a first node and the other end connected to VBB; and

a differential amplification portion, in which a plurality of differential amplifiers are connected in cascade, having an input port connected to the first node and an output port connected to a control signal input port to control the oscillation of an oscillation portion,

wherein the differential amplification portion compares a voltage of the first node with VSS of a ground voltage level and outputs a signal of a ground voltage level if the voltage of the first node is lower than VSS and a signal of a VDD voltage level if the voltage of the first node is higher than VSS.

2. The negative voltage level detector of claim 1, wherein the differential amplification portion comprises:

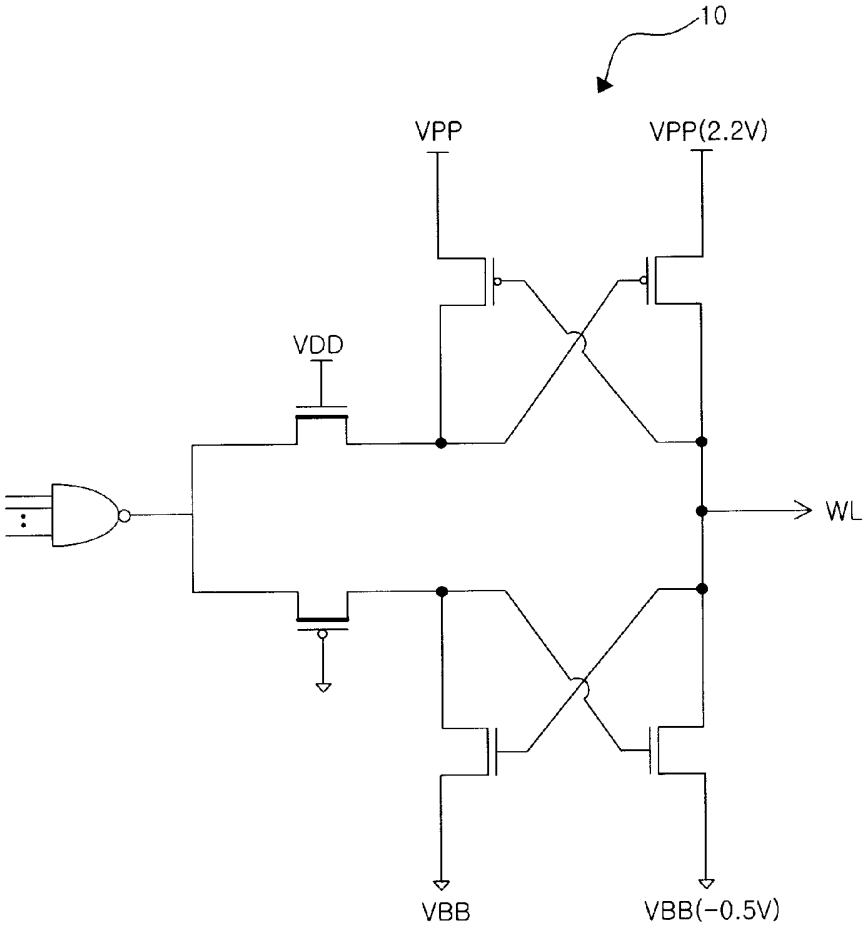
a first differential amplifier having an inverted input port connected to the first node and a non-inverted input port connected to VSS;

a second differential amplifier having an inverted input port connected to VSS and a non-inverted input port connected to the first node; and

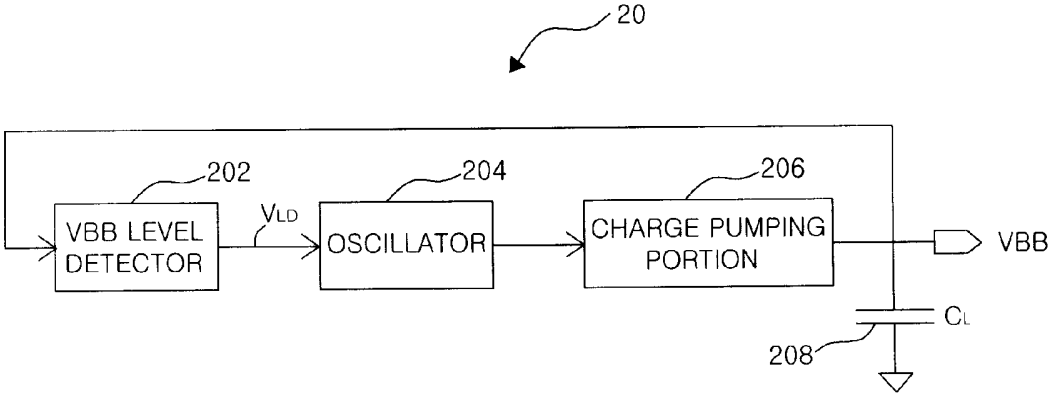
a third differential amplifier having an inverted input port connected to an output port of the first differential amplifier and a non-inverted input port connected to an output port of the second differential amplifier.

3. The negative voltage level detector of claim 2, further comprising a level inversion portion having an input port connected to an output port of the differential amplification portion and inverts an output signal of the differential amplification portion to output the inverted signal.

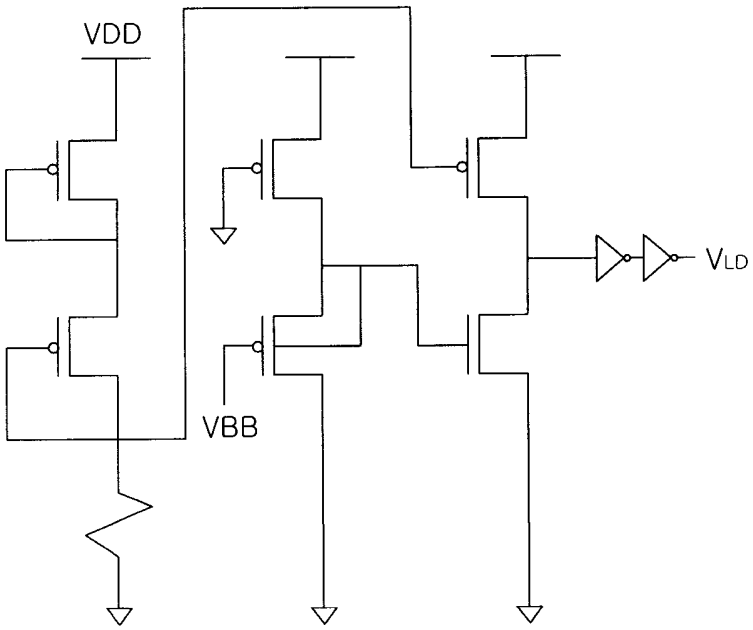
[Fig. 1]


10
VPP
VPP(2.2V)
VDD
WL
VBB
VBB(-0.5V)

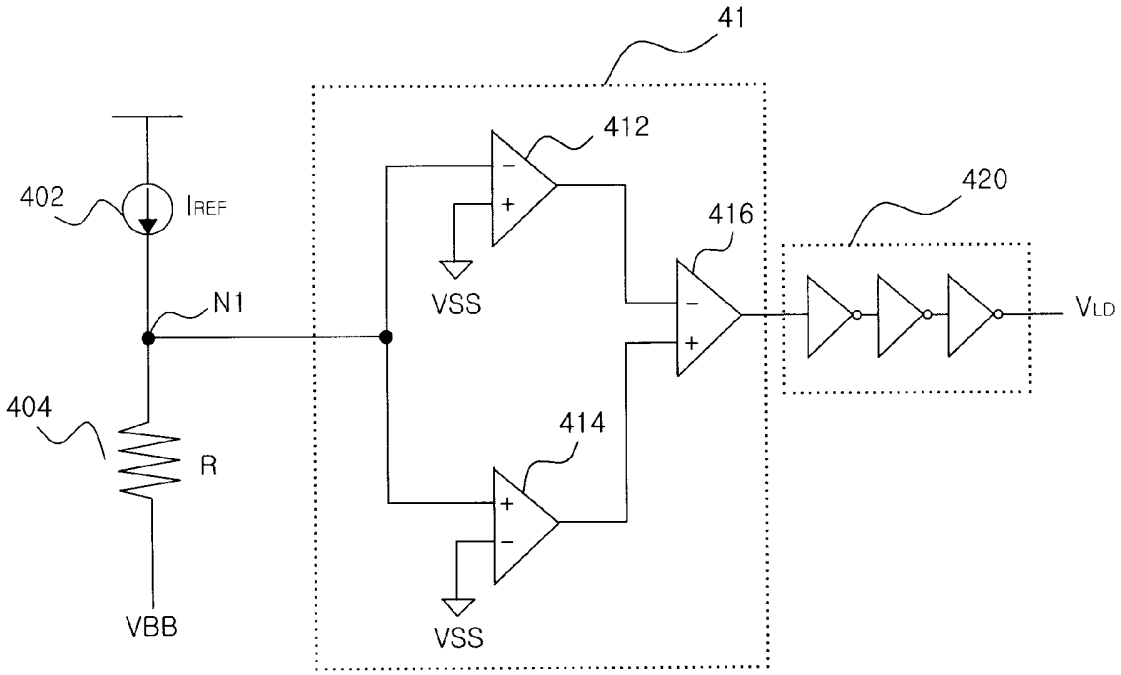
[Fig. 2]


20
202
204
206
VBB LEVEL DETECTOR
VLD
OSCILLATOR
CHARGE PUMPING PORTION
VBB
CL
208

[Fig. 3]




[Fig. 4]



**INTERNATIONAL SEARCH REPORT**

International application No.
PCT/KR2005/004626

**A. CLASSIFICATION OF SUBJECT MATTER**

*G11C 5/14(2006.01)i*

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)
IPC 8 G11C 5, G11C 7

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean Patents and applications for inventions since 1975

Electronic data base consulted during the intertnational search (name of data base and, where practicable, search terms used)
eKIPASS "charge pump", "level detect"

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

| Category* | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
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| A | US 6,240,033 B1 (HYUNDAI ELECTRONICS INDUSTRIES CO., LTD.) 29 MAY 2001<br>See [DESCRIPTION OF THE PRIOR ART] | 1-3 |
| A | US 6,600,690 B1 (MOTOROLA INC.) 29 JUL 2003<br>See the whole document | 1-3 |

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

| Date of the actual completion of the international search | Date of mailing of the international search report |
|---|---|
| 24 APRIL 2006 (24.04.2006) | **25 APRIL 2006 (25.04.2006)** |

| Name and mailing address of the ISA/KR | Authorized officer |
|---|---|
| Korean Intellectual Property Office<br>920 Dunsan-dong, Seo-gu, Daejeon 302-701,<br>Republic of Korea | HAN, Choong Hee |
| Facsimile No. 82-42-472-7140 | Telephone No. 82-42-481-8475 |

Form PCT/ISA/210 (second sheet) (April 2005)

**INTERNATIONAL SEARCH REPORT**

Information on patent family members

International application No.
PCT/KR2005/004626

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| | | EP 1576610 A2 | 21-09-2005 |