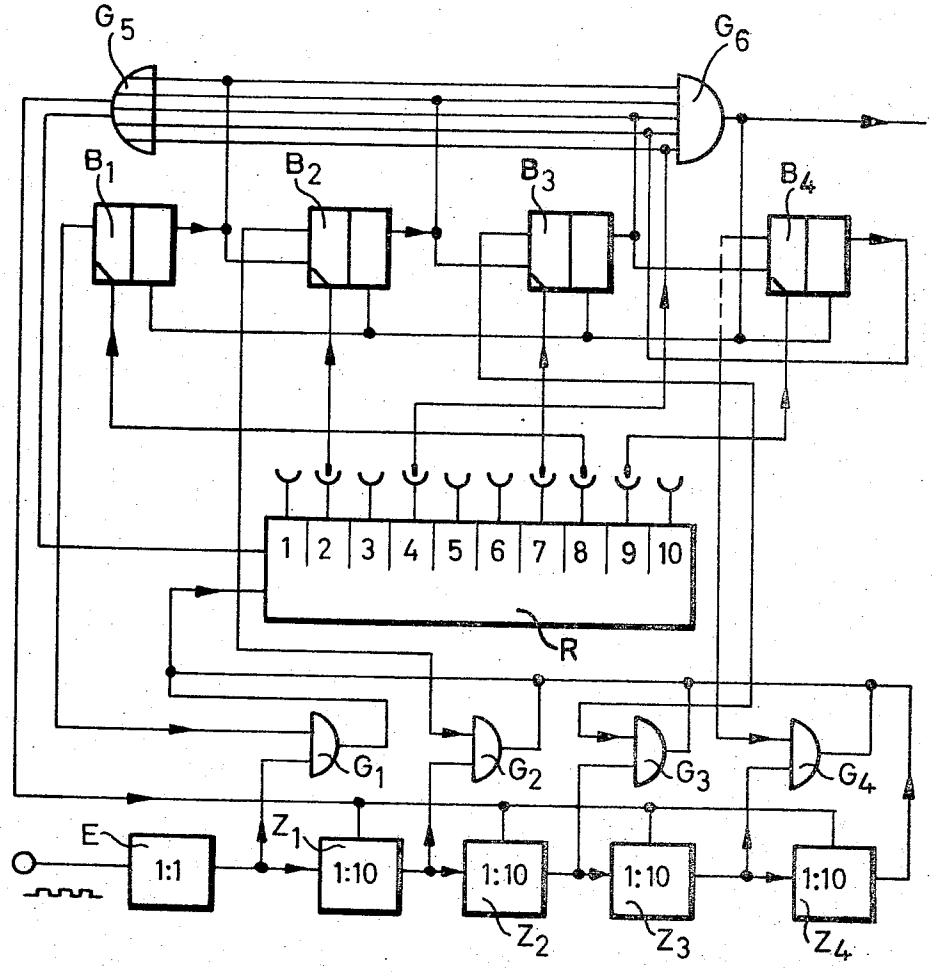
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SELECTABLE VALUE COUNTER

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SELECTABLE VALUE COUNTER

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The invention is generally directed to counting devices, and more particularly to the production of a counting device constructed of magnetic core storage members which delivers at selectable intermediate values an output impulse and which may be settable to arbitrary initial values.

Logical circuits built up of magnetic core storage members have various advantages. It is desired, if possible, to uniformly construct the entire apparatus, for example, a control device for measuring purposes, with magnetic core switching members, in order to economically utilize current supply components, timers, etc., which are necessary in the operation of magnetic core circuits. The known switching arrangements for counting chains which are built up of magnetic core storage members, however, have the drawback that they cannot be preset to arbitrarily determined values and likewise cannot be stopped at arbitrary intermediate values. In contrast thereto the problem is solved in this invention by the production of a counting device which is built up with the magnetic core storage members, and can be so switched over in a simple manner that it begins to run onward from any desired preset value, and/or may be stopped at will at any selectable value and which will release an output impulse for the initiation, for example, of another counting operation.

An important feature of the invention is the production of a magnetic core ring counter, for example, of ten-stages, in which the counting stage outputs thereof can be connected at will with bistable flip-flop stages and to which the input impulses to be counted are successively supplied over impulse reducers in such a way that following shifting over of a bistable flip-flop stage, in each case another impulse reducer, for example, in the ratio 1:10, is successively connected in series with the ring counter, with the outputs of the bistable flip-flop stages being operatively connected to an AND-gate which delivers the output impulse.

The invention is hereinafter described with the aid of the drawings, which represents a circuit embodying the invention.

The principal part of the apparatus is formed in the embodiment illustrated as a magnetic core ring counter R constructed in a known manner, whose ten outputs can be connected at will with any of four bistable flip-flop stages $B_1 \ldots B_4$, assuming the counting is to extend into the range of five-place numbers. The bistable flip-flop stages, which may likewise be constructed utilizing magnetic core technique, are in each case allocated to a place corresponding to the selected end result or to the number to be preset, with their output being collected over an OR-gate G_5 and an AND-gate G_6. The ring counter R is started and set at zero by means of the OR-gate G_5, while the output of the AND-fare G_6, upon reaching the preset initial or end value corresponding to the connection of the flip stages $B_1 \ldots B_4$ with the outputs of the counter R, delivers an output impulse.

In the embodiment of the invention illustrated, assuming for illustration that a counting up to the value 49728 is desired. The counting takes place backwards, that is, the first count is effected up to 8. The first figure does not require the use of a bistable flip-flop stage, but rather the corresponding output of the ring counter R is directly connected with one input of the OR-gate G_5 and one input of the AND-gate G_6. Accordingly there are provided four bistable flip-flop stages $B_1 \ldots B_4$, which in the illustrated example, are connected with the numerals 9728 of the counter. The arrangement further contains an impulse forming stage E, to which are directed input impulses, and similar impulse reducing stages $Z_1 \ldots Z_4$, which in each case effect a reduction in the ratio of 1:10, and can be formed, for example, by magnetic core circuits, in themselves known, which operate according to the principle of stagewise core magnetization. Further there are provided four AND-gates $G_1 \ldots G_4$, each with two inputs and one output.

The operation of the system described is as follows: The impulses to be counted are transformed in the impulse-former stage E in such a way that they are suitable for starting the impulse reducing stages $Z_1 \ldots Z_4$ formed, as aforementioned, of stagewise magnetizable cores.

Simultaneously these impulses are fed, first over gate G_1, and after its blocking over gate G_2, etc. to the input of the magnetic core ring counter R. As previously mentioned, in the example described, an output impulse is to be delivered as soon as the end value 49728 is reached. Therefore, the figure 8 is first counted, that is, when the magnetic core ring counter R delivers an impulse on its output allocated to 8 the bistable flip-flop stage B_1 is shifted over. The AND-gate G_1 is thereby blocked, and over the OR-gate G_5 of the magnetic core ring counter R is reset to 0. The impulse reducers $Z_1 \ldots Z_4$, insofar as they do not happen to be on 0 are similarly reset. As a result of the blocking of the AND-gate G_1, the impulse reducer Z_1, corresponding to each tenth input impulse, now feeds counting impulses over the AND-gate G_2 to the ring counter R. The switching over of the bistable flip stage B_1 further prepares the bistable flip-flop stage B_2, over a presetting input, for the switching thereof. Over the output allocated to the digit 2 of the ring counter R the bistable flip-flop stage B_2 is switched over, which has the consequence that, correspondingly the AND-gate G_2 is blocked and, in the above-described manner, the ring counter R and also possibly the impulse reducers $Z_1 \ldots Z_4$ are restored to 0. The output impulses of the impulse reducer Z_1 are thereby fed to the impulse reducer Z_2, whose output impulses are fed over the AND-gate G_3 to the input of the ring counter R. When the ring counter R reaches the digit 7, the bistable flip stage B_3 is similarly switched over. The subsequent operations proceed in a manner corresponding to that above described.

When the ring counter R corresponding to the first digit of the counting value, has energized the output allocated to the digit 4, an output impulse is delivered over the AND-gate G_6, since all the inputs of the AND-gate G_6 are energized as a result of the switching over of all of the bistable flip-flop stages $B_1 \ldots B_4$. Simultaneously therewith, from the output of the AND-gate G_6 a resetting impulse is delivered to the bistable flip stages $B_1 \ldots B_4$, while over the output of the OR-gate G_5 the magnetic core counter R and the impulse reducers $Z_1 \ldots Z_4$ are reset. The counting process as described can thereupon be repeated.

Changes may be made within the scope and spirit of the appended claims which define what is believed to be new and desired to have protected by Letters Patent.

I claim:

1. A counting device for delivering at selectable intermediate values an output impulse, and which may be settable to arbitrary starting values, comprising a magnetic core ring counter having a plurality of counting stages, each of which has an output, a plurality of bistable flip flop stages, means for selectively connecting outputs of said counting stages with flip flop stages, a plurality of

successively arranged impulse reducers, means operatively connected to said flip flop stages and said impulse reducers for successively connecting the respective impulse reducers to the counter in predetermined ratios following shifting over of the corresponding flip flop stage, means for feeding the impulses to be counted to said impulse reducers, and means operatively connected to the outputs of said flip-flop stages for receiving the impulses therefrom operative to supply an output impulse.

2. A counting device according to claim **1**, wherein said output means comprises an AND gate operatively connected to the respective flip flop stages.

3. A counting device according to claim **1**, comprising in further combination an OR gate operatively connected to the respective flip flop stages and to the ring counter and impulse reducers, operative to deliver resetting impulses to the ring counter and the impulse reducers.

4. A counting device according to claim **3**, wherein said means for connecting said impulse reducers to said counter comprise respective AND gates having their inputs connected to corresponding flip flop stages and impulse reducers, and their outputs connected to said counter.

5. A counting device according to claim **3**, wherein said impulse reducers are constructed in the form of stage-wise magnetizable magnetic cores.

6. A counting device as defined in claim **5**, wherein said magnetic core ring counter is provided with ten counting stages and each of said impulse reducers has an operative reduction ratio of 1:10.

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