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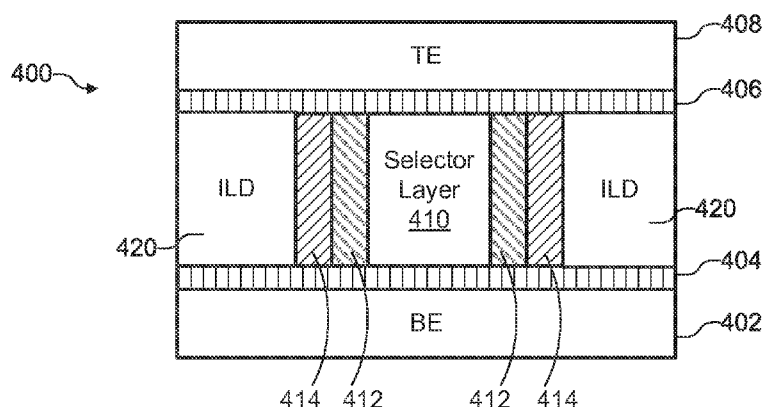
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(54) **Title:** SIDEWALL ANTI-CATION-DIFFUSION BARRIER

**FIG. 4A**

(57) **Abstract:** In one example, a device includes a first electrode, a second electrode, an insulator layer, and a sidewall anti-cation-diffusion barrier. The first electrode and the second electrode may each include a surface having an anti-cation diffusion barrier. The insulator layer is bounded by opposing electrode-facing surfaces and a sidewall surface. The insulator layer may be disposed between the first electrode and the second electrode such that each of the opposing electrode-facing surfaces of the insulator layer are situated along a respective one of the anti-cation-diffusion barriers of the first and second electrodes. The sidewall anti-cation-diffusion barrier may be situated along the sidewall surface of the insulator layer.

SIDEWALL ANTI-CATION-DIFFUSION BARRIER

BACKGROUND

[0001] Memory devices are used to store data. A memory device may be made up of multiple memory cells. In some cases, a memory cell may be a semiconductor device that can have two different states. The two different states can be associated with a respective binary logic value, such as 0 or 1. Data may be stored to a memory cell by assigning a logic value to that memory cell, and manipulating the memory cell to cause it to take the associated state. Further, the logic value of the memory cell may be queried by determining its state. Data assignment and query operations may be referred to as write and read operations, respectively. A group of memory cells can be used to store a binary dataset by assigning a respective logic value to each cell in the group such that each cell stores a bit of the dataset.

[0002] Various technologies have been used in the design and implementation of memory devices. In some cases, a chip includes multiple semiconductor memory cells that are connected to a set of driving and measurement lines that can be used to address individual memory cells or subsets of the memory cells. A control system can then use those lines to perform read and write operations by applying energy to the individual cells via the lines. For example, reading data from a memory cell may involve applying a read voltage to that memory cell while measuring current (or vice versa) to determine the state of the cell. Similarly, writing data to a memory cell may involve applying a write voltage (or current) to that memory cell which sets the memory cell's state.

BRIEF DESCRIPTION OF THE DRAWINGS

[0003] The following detailed description references the drawings, wherein:

[0004] FIG. 1A is a block diagram of an example memory cell including a selector in series with a memristor;

[0005] FIG. 1B is a chart of an example current and voltage for an example memory cell;

- [0006] FIG. 2 is a block diagram of an example crossbar array having multiple memory cells that each have a selector in series with a memristor;
- [0007] FIG. 3A is a flowchart of an example process for writing data to a memory cell;
- [0008] FIG. 3B is a flowchart of an example process for reading data from a memory cell;
- [0009] FIG. 4A is a side cross-sectional view of an example selector;
- [0010] FIG. 4B is a top cross-sectional view of the example selector shown in FIG. 4A;
- [0011] FIG. 5 is a flowchart of an example process for forming a selector; and
- [0012] FIGS. 6A, 6B, 6C, and 6D are a cross-sectional views of a selector during stages of an example fabrication process.

DETAILED DESCRIPTION

[0013] The following description makes reference to the accompanying drawings, in which similar symbols identify similar components, unless context dictates otherwise. The descriptions herein, as well as the drawings, present examples of the subject matter of the present disclosure and are in no way limiting in regard to the subject matter disclosed herein. Throughout the description, the singular forms of “a”, “an”, and “the” mean “one or more”. Thus, various examples in which a component is described in singular form also apply to examples having multiple of those components. Moreover, some aspects of the examples presented herein may be modified, re-arranged, re-ordered substituted, combined, and/or separated in a variety of different configurations without departing from the subject matter of the present disclosure.

[0014] A memory device may include an array of memory cells. A crossbar array of memory cells may include a grid of control lines arranged in rows and columns. Memory cells may be situated at the intersections of the row and column lines such that a given memory cell can be addressed by a combination of the row and column lines. One example of a memory cell that may be used in such a crossbar array is a memristor.

[0015] A memristor is a passive, non-volatile device with an electrical resistance that depends on the history of current conveyed through the memristor. A memristor may be used to store data using its resistance state. For example, a low-resistance state of the memristor may be associated with a first logical value and a high-resistance state of the memristor may be associated with a second logical value. Thus, a memristor may be used to store a bit of data (e.g., a logical 0 or 1). The resistance state may be modified to write data to the memristor by applying sufficient energy to the memristor. For example, applying a voltage pulse may place the memristor in a low-resistance state and applying a voltage pulse of a different polarity, or different value, may place the memristor in a high-resistance state. In some examples, applying a voltage between about 1-2 volts (V) may cause a memristor to switch its resistance state. The energy to change the state of the memristor may also be provided by a current source. To determine the resistance state of a memristor, a read voltage may be applied to the memristor. A current may be collected and used to determine the resistance state of the memristor. In some examples, the determination may involve comparing the measured current to a reference current. For example, if the output current is greater than the reference current, then the memristor may be determined to be in a low resistance state. On the other hand, if the output current is less than the reference current, then the memristor may be determined to be in a high resistance state.

[0016] Memristors may be implemented using a number of different materials and fabrication techniques. As used herein, the term “memristor” may refer to a passive two-terminal circuit element that changes its electrical resistance under sufficient electrical bias. A memristor may receive a read voltage to generate a current that can be measured to determine the resistance state of the memristor. A memristor may also receive a write voltage that sets the resistance state of the memristor. In one example, a memristor may have two layers: one that includes an electrically insulating material and one that includes an electrically conductive material. As used herein, the terms insulating and conductive are relative terms. That is, they refer to relative extents of electrical conductivity between the two materials. Thus, the two layers of the memristor include one that is more conductive than the other. In operation, a memristor may transition between

states of resistivity via drift of ions or holes between the two layers. For example, the two layers may be oxide films in which one is more conductive than the other due to oxygen vacancies providing a conductive channel through the depleted layer. Under sufficient bias, oxygen vacancies may form in the non-depleted layer so as to effectively decrease the thickness of the conductive layer relative to the insulating layer. The resistance of the memristor can then be approximated as the tunneling resistance through the non-depleted oxide layer, which decreases with the decreasing thickness of the insulating layer. Other examples of non-volatile, variable-resistance materials that transition between resistance states in response to application of an electrical bias or other transition energy may also be used to implement a memristor.

[0017] In a crossbar array of memristors, the term “target” may refer to a memristor that is to be written to or read from. A target row line and a target column line may be the row and column lines that correspond to the target memristor in a crossbar array. Non-target row lines and non-target column lines may be row lines and column lines that are not the target row or column line. The terms “row lines” and “column lines” may refer to distinct conductive lines, such as conductive traces, wires, etc., that are used to apply voltages to memristors in a crossbar array and/or to measure currents through memristors.

[0018] In some examples, row lines and column lines for non-selected memristors may be held at a fixed voltage, and the row and column lines for the target memristor can be set to apply a threshold voltage across the target memristor. However, in applying voltage(s) to the target row line and a target column line, other memristors coupled to the same row/column lines may also experience a voltage change. For example, a read voltage V_R may be applied to a target memristor by setting the target row and target column lines to $-\frac{1}{2} V_R$ and $+\frac{1}{2} V_R$, respectively, with the remaining lines set to 0. In such an example, the non-target memristors on the same column and row as the target may experience a bias of about half that applied to the target (e.g., about $\frac{1}{2} V_R$). While the voltage change is generally less than the voltage applied to the target memristor, the voltage across these partially-selected, non-target memristors may induce current that reaches the target column line. Such current paths that do not pass through

the target memristor are referred to as sneak currents. Sneak currents may lead to a number of issues such as inaccurate memristor queries due to sneak current contributions from neighboring low resistance state memristors, saturating the current of driving transistors and increasing power consumption. In some examples, noise from sneak currents may cause inaccurate or ineffective memory reading and writing operations.

[0019] In some examples, a selector may be coupled serially with a memristor. The selector may be a highly non-linear two-terminal circuit element that becomes conductive upon application of a threshold voltage. Below the threshold voltage, current flow through the selector, and the memristor, is minimal. To help mitigate the effect of sneak currents, the selector may have a threshold voltage that is not activated by the voltages applied to non-target memristors on the same row or column as a target memristor. As such, while some sneak current may be inevitable, series-coupled selectors may help mitigate the sneak current from non-target memristors described above. In some systems, a memory device includes a crossbar array of row and column lines arranged in a grid. A selector and a memristor coupled in series can be situated at intersections of the row and column lines.

[0020] The present disclosure relates to an arrangement for a selector that may be coupled in series with a memristor. The selector may be a metal-insulator-metal semiconductor device. For example, the selector may include conductive top and bottom electrodes that sandwich an insulator layer. The insulator layer may be an oxide film or another material that transitions between a non-conductive state and a conductive state. The insulator layer becomes conductive in response to a threshold voltage being applied across the top and bottom electrodes. When the applied voltage is less than the threshold voltage, the insulator layer does not allow current to flow between the top and bottom electrodes.

[0021] In some examples, the selector may include cation metal ions that can become arranged within the insulator layer so as to provide a current path upon application an activation energy via the electrodes. For instance, the insulator layer may include an oxide, nitride, or oxynitride having a lattice structure, and

cation metal ions may arrange themselves within the lattice to create a conductive path upon application of a threshold voltage across the electrodes. Such cation metal based selectors may provide fast switching and recovery times as well as a relatively high ratio between on and off currents. However, a variety of cation metals such as silver, copper, gold, nickel, etc., as well as their oxides, are highly diffusible into dielectric materials used along the sidewalls of such devices for electrical and/or thermal insulation. In such circumstances, the cation metal may diffuse out of the insulator layer and into the sidewall material, toward the top or bottom electrodes. Such diffusion may lead to reduced performance of the device due to reduced cation metal concentration within the insulator layer. In addition, upon cation metals reaching the electrodes via diffusion through the sidewall material, the cation metals may create connections (e.g., electrical shorts) between adjacent electrodes, conducting lines, etc. in a crossbar array.

[0022] To help mitigate such problems in the use of cation metal based selectors, the present disclosure presents an arrangement for a cation metal based selector in which the insulator layer including cations is confined by a sidewall structure that resists cation diffusion. The cation containment enclosure may include an anti-cation-diffusion barrier along the insulator-facing sides of the top and bottom electrodes. The electrode barriers may include layer(s) of cation barrier conductive material, such as cobalt, ruthenium, tantalum, tantalum nitride, indium oxide, tungsten nitride, tungsten silicon nitride, tantalum silicon carbide, tantalum carbide, and/or titanium nitride, for example. The insulator can be further enclosed by a sidewall anti-cation-diffusion barrier. The sidewall anti-cation-diffusion barrier may include layer(s) of a cation barrier dielectric material, such as boron carbonitride, silicon oxycarbide, silicon carbide, silicon nitride, and/or amorphous silicon carbide, for example.

[0023] FIG. 1A is a block diagram of an example memory cell 100 including a selector 110 electrically coupled in series with a memristor 120. In some examples, the memory cell 100 may be coupled between control lines at nodes 102 and 104. For example, the control lines may be lines in a crossbar array that includes many additional memory cells, such as at each intersection of the control lines.

[0024] The selector 110 includes a first electrode 112, a selector layer 114, and a second electrode 116. The memristor 120 includes a first electrode 122, a variable resistance layer 124, and a second electrode 126. In some examples, the first 112, 116 and second electrodes 122, 126 may be referred to as top and bottom electrodes, respectively. The selector 110 may exhibit a non-linear change in its conductivity in response to changing an applied voltage. For instance, the selector layer 114 may be characterized by a high-resistance state (low conductivity state) when the applied voltage is less than a threshold, and a low-resistance state (high conductivity state) when the applied voltage exceeds the threshold.

[0025] The selector layer 114 of the selector 110 includes cation metal ions that become arranged within the selector layer 114 to provide conductive channels through the selector layer 114 between the electrodes 112, 116 upon application of a threshold voltage. The selector layer 114 may also include an oxide, nitride, and/or oxynitride that forms a lattice structure. Cation metals may occupy defects within such lattice or otherwise become arranged within the material of the selector layer. In some cases, the selector layer 114 may be an insulating material that is doped with conductive material, for example. At voltages less than the threshold voltage, the cation metal ions are distributed throughout the selector layer and do not create significant conductive channels through the selector layer 114. Although in some examples, some current flow through the selector layer 114 may occur at voltages less than the threshold voltage of the selector 110, such sub-threshold current flow may be due to fewer conductive channels and/or channels with less current-carrying capacity than occurs above the threshold voltage. As a consequence, the selector 110 may be substantially non-conductive (e.g., have a high resistance) for voltages below its threshold voltage and be substantially conductive (e.g., have a low resistance) for voltages above its threshold voltage.

[0026] In addition, the cation metal based selector layer 114 may be encapsulated by anti-cation-diffusion barrier materials. As noted above, while the cation metals such as Cu, Au, Ag, Ni and/or their oxides may configure themselves within the selector layer 114 to cause the selector 110 to rapidly

switch between conductive and non-conductive states, these materials are also susceptible to diffusion into adjacent materials during operation. To keep the cation metal within the selector layer 114, the electrodes 112 and 116 may include an anti-cation-diffusion barrier at least along faces of those electrodes 112, 116 that are along the selector layer 114. Such an anti-cation-diffusion barrier for the electrodes 112, 116 may include Co, Ru, Ta, TaN, TiN, WN, WSiN, TaSiN, TaC, and/or InO, for example. In addition, the selector layer 114 may include a sidewall anti-cation-diffusion barrier adjacent the sidewall of the selector layer 114. For example, the anti-cation-diffusion barrier may be a conformal layer of anti-cation-diffusion material that extends between the two electrodes 112 and 116 so as to surround the sidewall surface of the selector layer 114. Such a sidewall anti-cation-diffusion barrier may include BCN, SiOC, SiC, and/or a-SiC, for example. Additional details of an example arrangement for a sidewall anti-cation-diffusion barrier are provided in connection with FIGS. 3A and 3B.

[0027] The memristor 120 may have a resistance that depends on the history of energy applied across its electrodes 122, 126. For instance, the variable resistance layer 124 may transition between a high-resistance state and a low-resistance state upon application of state-changing energy, such as a voltage pulse of sufficient magnitude and/or duration. Further, the variable resistance layer 124 may remain in its most-recently established resistance state until application of a subsequent state-changing voltage pulse. As such, the resistance state may be used as for non-volatile information storage with the two possible resistance states corresponding to a binary bit of information.

[0028] Both the selector 110 and the memristor 120 are two-terminal devices and they are coupled in series between nodes 102 and 104. As shown in the block diagram of FIG. 1A, node 102 is electrically coupled to the first electrode 112 of the selector 110. The second electrode 116 of the selector 110 is electrically coupled to the first electrode 122 of the memristor 120. The second electrode 126 of the memristor 120 is coupled to the node 104. FIG. 1A illustrates these electrical couplings schematically as wires, however the electrical couplings between electrodes and other components may be implemented in a various ways depending on fabrication, materials, and other factors. For instance, in some

examples, the electrodes 116 and 122 of the selector 110 and memristor 120 may be implemented as a single layer of conductive material situated between the selector layer 114 and the variable resistance layer 124. In some examples, the electrodes 112 and 126 proximate the nodes 102 and 104, respectively, may be implemented as control lines with multiple selector layers and/or variable resistance layers patterned thereon.

[0029] FIG. 1B is a chart of an example current and voltage for an example memory cell. The current-voltage chart of FIG. 1B schematically illustrates an example relationship between current passed through the memory cell 100 and the voltage applied across the memory cell 100. Referring to the positive voltage region of the chart, right of the axis, it can be seen that the current remains very low below a threshold voltage V_T . The threshold voltage V_T may be the threshold voltage of the selector 110, which exhibits a high electrical resistance for voltages below V_T , but transitions to a conductive state at voltages above V_T . Moreover, at sub-threshold voltages, the resistance of the selector 110 may be greater than the resistance of the memristor 120 such that the selector 110 dominates the resistance of the memory cell 100 for voltages below V_T . In some examples, the selector 110 may exhibit similar behavior at negative voltages: high resistance for voltages greater than $-V_T$ and conductive for voltages less than $-V_T$, which is portrayed in the example relationship shown in FIG. 1B. The region of the chart in which the behavior of the memory cell 100 is dominated by the selector is labelled as the "Selector Region."

[0030] For voltages above V_T (or less than $-V_T$) the selector 110 is conductive, and so the resistance of the memory cell is dominated by the memristor 120. As shown in FIG. 1B, above V_T , the I-V curve may proceed along two different paths, depending on whether the memristor 120 is in a high resistance state (HRS) or a low resistance state (LRS). To distinguish between the two paths in FIG. 1B, the paths are shown with dashed line for the HRS behavior and a solid line for the LRS behavior. Thus, if the memristor 120 is in the HRS, current through the memory cell 100 follows the dashed path at voltages above V_T . On the other hand, if the memristor 120 is in the LRS, current through the memory cell follows the solid path at voltages above V_T .

[0031] As noted above, to determine the state of the memristor 120, a read voltage V_R may be applied to the memory cell 100. As shown in FIG. 1B, if the memristor 120 is in HRS (dashed path), then applying V_R results in a first current I_1 . On the other hand, if the memristor 120 is in LRS (solid path), then applying V_R results in a second current I_2 . Reading the resistance state may be performed by measuring the current through the memory cell 100 while V_R is applied across the terminals 102, 104. For instance, the resulting current may be collected and compared to a threshold value, which threshold may be between I_1 and I_2 , and the state of the memory cell 100 may be determined based on the threshold comparison.

[0032] In some examples, V_R may be applied by setting one terminal of a target memory cell to about $\frac{1}{2} V_R$ and the other terminal to about $-\frac{1}{2} V_R$. In a crossbar array, applying V_R in this way using a target row line and target column line, with all other row/column lines set to 0 results in all non-target memory cells that share either the target row or target column receiving a voltage of $\frac{1}{2} V_R$. As such, many memory cells in a crossbar array will regularly receive a voltage of about $\frac{1}{2} V_R$. To help mitigate problems of sneak current, noise in the current measurement, and excess power consumption, the current at $\frac{1}{2} V_R$ should be at or near zero. In practice, this may be achieved by selecting V_R to be less than $2 V_T$, such that $\frac{1}{2} V_R$ is within the Selector Region shown in FIG. 1B. In addition, the value of V_R may be selected to be greater than V_T by some margin to ensure that the two currents I_1 and I_2 are measurable and distinguishable from one another. Balancing these concerns may result in selecting V_R to satisfy the following relation: $\frac{1}{2} V_R < V_T < V_R$.

[0033] Further, to set the resistance state of the memristor 120, a selection voltage V_S may be applied to the memory cell 100. The selection voltage V_S may be a voltage that causes the memristor to transition from HRS to LRS, as illustrated by the arrow in FIG. 1B from the HRS dashed path to the LRS solid path. For example, the transition between states may involve a change in distribution of ions, holes, and/or defects within the variable resistance layer 124 of the memristor 120. Applying a pulse at the selection voltage V_S may set the memristor 120 to LRS and applying a pulse at the negative selection voltage $-V_S$ may set the memristor 120 to

HRS. Other examples of hysteresis curves are possible in which a given memristor's resistance state may be set by application of suitable voltage pulses.

[0034] Note that the I-V chart described above in connection with FIG. 1B is provided for example purposes only to illustrate one example of behavior that may be exhibited by some memory cells. Other memristor devices may exhibit different hysteresis curves, including some in which the transition between resistance states may be initiated by voltages of the same polarity. The chart in FIG. 1B is therefore provided for example purposes only. Other examples applicable to the present disclosure may include memory cells that exhibit alternative hysteresis curves to that shown in FIG. 1B.

[0035] FIG. 2 is a block diagram of an example crossbar array 200 having multiple memory cells that each have a selector 110 in series with a memristor 120. Each of the selectors 110 include a selector layer 114 situated between two electrodes. The selector layers 114 of the selectors 110 may be similar to the selector layer described above in connection with FIGS. 1A-1B. For example, the selector layers 114 of the selectors 110 may each include cation metal ions that become arranged within the selector layer 114 to provide conductive channels through the selector layer 114 upon application of a threshold voltage. In addition, each selector layer 114 may include a sidewall anti-cation-diffusion barrier adjacent the sidewall of the selector layer 114. For example, the anti-cation-diffusion barrier may be a conformal layer of anti-cation-diffusion material that extends between the two electrodes so as to surround the sidewall surface of the selector layer 114.

[0036] The crossbar array 200 shown in FIG. 2 demonstrates a layout with two row lines 210, 212 and two column lines 220, 222. In some examples, the row lines 210, 212 may be parallel with one another and orthogonal to the conductive lines 220, 222, which are themselves parallel with one another. Memory cells are located at the intersections of the row lines and column lines such that a given memory cell is connected between one row line and one column line, which lines may be used to control that memory cell. As shown in FIG. 2, memory cell 202 is electrically coupled between row line 210 and column line 220; memory cell 204 is electrically coupled between row line 210 and column line 222; memory cell 206 is electrically

coupled between row line 212 and column line 220; and memory cell 208 is electrically coupled between row line 212 and column line 222. Each intersection of the memory cells 202-208 includes a selector 110 electrically coupled in series with a memristor 120. Example operations that may be performed using the crossbar array are described in connection with FIGS. 3A and 3B.

[0037] FIG. 3A is a flowchart of an example process 300 for writing data to a memory cell. FIG. 3B is a flowchart of an example process 310 for reading data from a memory cell. Processes 300 and 310 may be described below as being executed or performed by a system, for example, the crossbar array 200 of FIG. 2. Other suitable systems and/or computing devices may be used as well. Processes 300 and 310 may be implemented in the form of executable instructions stored on at least one machine-readable storage medium of the system and executed by at least one processor of the system. In some examples, processes 300 and 310 may be implemented in the form of electronic circuitry (e.g., hardware). The processes 300 and 310 are depicted with a series of blocks in the flowcharts of FIGS. 3A and 3B. In some cases, one or more blocks of processes 300 and/or 310 may be executed substantially concurrently or in a different order than shown in FIGS. 3A and 3B. In some cases, processes 300 and 310 may include more or less blocks than are shown in FIGS. 3A and 3B. In some examples, one or more of the blocks of processes 300 and/or 310 may, at certain times, be ongoing and/or may repeat.

[0038] Referring to FIG. 3A, at block 302, an indication may be received to write data to a target memory cell. For example, a control system associated with the crossbar array 200 of FIG. 2 may receive an indication that a data value should be written to memory cell 202.

[0039] At block 304, a write voltage pulse may be applied to the target memory cell. The write voltage pulse may cause the memory cell to transition to a resistance state associated with the data to be written to the target memory cell. For example, a control system associated with the crossbar array 200 of FIG. 2 may select the row and column line combination that corresponds to memory cell 202: row line 210 and column line 220, and apply a write voltage pulse across those lines 210, 220 so as to set to the resistance state of memory cell 202.

[0040] Referring to FIG. 3B, at block 312, an indication to read data from a target memory cell may be received. For example, a control system associated with the crossbar array 200 of FIG. 2 may receive an indication that a data value should be read from memory cell 202.

[0041] At block 314, a read voltage may be applied to the target memory cell. The read voltage may be greater than a threshold voltage of a selector in the memory cell to allow the resistance state of the memristor to be determined. For example, the row and column lines for the target memristor: row line 210 and column line 220 may be set to $+\frac{1}{2} V_R$ and $-\frac{1}{2} V_R$, respectively.

[0042] At block 316, the current that flows through the target memory cell may be measured while the read voltage is applied. For example, current may be collected along the column line 220.

[0043] At block 318, the data value of the target memory cell may be determined based on the measured current. For example, if the current exceeds a threshold, then the memory cell may be determined to be in a low resistance state and otherwise in a high resistance state.

[0044] FIG. 4A is a side cross-sectional view of an example selector 400. The selector 400 includes a bottom electrode 402, a bottom electrode anti-cation-diffusion barrier 404, a top electrode 408, a top electrode anti-cation-diffusion barrier 406, and a selector layer 410. The selector layer 410 may be an oxide, nitride, and/or oxynitride that includes cation metal such as Cu, Au, Ag, Ni, etc. Upon application of a threshold voltage, the cation metal may become arranged within a lattice structure of the selector layer 410 so as to create conductive channels therein. The selector layer 410 is sandwiched between the top and bottom electrodes 402, 408. The anti-cation-diffusion barriers 404, 406 may be situated along at least one face of the electrodes 402, 408 that face the selector layer 410. Thus, the selector layer 410 may have two electrode-facing surfaces that are each situated along one of the electrode anti-cation-diffusion barriers 404, 406. As described above, the electrode anti-cation-diffusion barriers 404, 406 may include a material that is electrically conductive and inhibits the diffusion of cation metals, such as Co, Ru, Ta, TaN, TiN, WN, WSiN, TaSiN, TaC, and/or InO, for example.

[0045] In addition to the electrode-facing surfaces of the selector layer 410, the selector layer 410 also includes a sidewall surface that extends between the top and bottom electrodes 402, 408. A sidewall anti-cation-diffusion barrier 412 may be situated along the sidewall surface of the selector layer 410. In some cases, the sidewall anti-cation-diffusion barrier 412 may entirely surround the sidewall surface of the selector layer 410 such that the selector layer 410 is entirely encapsulated by a combination of the sidewall anti-cation-diffusion barrier 412 and the electrode anti-cation-diffusion barriers 404, 406. The sidewall anti-cation-diffusion barrier may include a dielectric material that inhibits the diffusion of cation metals, such as BCN, SiC, SiOC, SiN, and/or a-SiOC, for example.

[0046] In some examples, the sidewall anti-cation-diffusion barrier 412 and/or the electrode anti-cation-diffusion barrier(s) 404, 406 may include multiple layers of barrier materials. For example, a sidewall anti-cation-diffusion barrier may include multiple layers of electrically insulating material(s) that inhibit diffusion of cation metals and/or cation metal oxides. Similarly, the electrode anti-cation-diffusion barrier(s) 404, 406 may include multiple layers of electrically conductive material(s) that inhibit diffusion of cation metals and/or cation metal oxides. Moreover, the multiple layers that form each barrier may be formed of similar or dissimilar materials. In some examples, the sidewall anti-cation-diffusion barrier 412 may include multiple layers formed of a common material (e.g., multiple layers of a-SiOC), and/or multiple layers in which one layer is formed of a first material (e.g., BCN) and another layer is formed of a second material (e.g., SiC). In some examples, the electrode anti-cation-diffusion barrier(s) 404, 406 may include multiple layers formed of a common material (e.g., multiple layers of TaN), and/or multiple layers in which one layer is formed of a first material (e.g., InO) and another layer is formed of a second material (e.g., WSiN).

[0047] An electrically insulating sidewall 414 may be disposed around the sidewall anti-cation-diffusion barrier 412. The electrically insulating sidewall 414 may include a material such as silicon nitride, for example, which provides an electrical and thermal barrier between the selector layer 410 and surrounding regions. In some examples, an inter-layer dielectric (ILD) 420 may be disposed

between the electrodes in regions not occupied by the selector and its adjacent sidewalls.

[0048] FIG. 4B is a top cross-sectional view of the example selector 400 shown in FIG. 4A. As shown in FIG. 4B, the selector layer 410 may be entirely surrounded by the sidewall anti-cation-diffusion barrier 412 along its sidewall surface. The sidewall anti-cation-diffusion barrier 412 thus confines cation metal within the selector layer 410 from diffusing out of the selector layer 410. The electrically insulating sidewall 414 may be situated to surround the outer sidewall surface of the sidewall anti-cation-diffusion barrier 412 to thereby insulate the selector layer 410 therein from electrical and/or thermal variations. In some examples, the electrically insulating sidewall 414 may also provide some structural stability to the sandwich structure of the selector device 400. In addition, the ILD 420 may be situated around the outer sidewall of the electrically insulating sidewall 414, which may separate the selector 400 from adjacent electronics, such as surrounding selectors in a crossbar array. In addition, the ILD 420 may help separate the top and bottom electrodes 402, 408 from one another. In some examples, the ILD 420 may be a dielectric material with a low relative permittivity (e.g., a low dielectric constant), which may help reduce capacitive coupling between the electrodes 402, 408.

[0049] FIG. 5 is a flowchart of an example process 500 for forming a selector. Process 500 may be described below as being executed or performed by a system, such as a fabrication system and/or computing device. Process 500 may be implemented in the form of executable instructions stored on at least one machine-readable storage medium of the system and executed by at least one processor of the system. In some examples, process 500 may be implemented in the form of electronic circuitry (e.g., hardware). The process 500 is depicted with a series of blocks in the flowchart of FIG. 5. In some cases, one or more blocks of process 500 may be executed substantially concurrently or in a different order than shown in FIG. 5. In some cases, process 500 may include more or less blocks than are shown in FIG. 5. In some examples, one or more of the blocks of process 500 may, at certain times, be ongoing and/or may repeat.

[0050] FIGS. 6A, 6B, 6C, and 6D are cross-sectional views of a selector during stages of an example fabrication process. For example purposes, FIGS. 6A-6D are referenced in the description of process 500 to illustrate fabrication stages.

[0051] At block 502, a cation metal based insulator layer is formed. The insulator layer is bounded by opposing electrode-facing surfaces and a sidewall surface. The insulator layer may be formed by patterning an insulator material over a first electrode via masking, photolithography, and/or another fabrication technique so as to form a layer of the insulator material at a desired thickness in a desired area. Moreover, the insulator layer may include cation metal ions. For example, as shown in FIG. 6A, an insulator layer 610 is formed over a first electrode 602. The first electrode 602 includes an electrode anti-cation-diffusion barrier 604 along its top surface – the same surface on which the insulator layer is formed. In some examples, the electrode anti-cation-diffusion barrier 604 may be a layer of conductive material that inhibits cation diffusion, such as those described above in connection with the electrode anti-cation-diffusion barriers 404, 406 of selector 400. The insulator layer 610 includes opposing electrode-facing surfaces 612, 614 and a sidewall surface 616. As shown in FIG. 6A, the electrode-facing surface 612 is situated along the electrode anti-cation-diffusion barrier 604 of the first electrode 602. The sidewall surface 616 is approximately orthogonal to the electrode-facing surfaces 612, 614 and extends around the perimeter of the insulator layer 610. The sidewall surface 616 may include exterior corners, depending on the layout of the insulator layer 610. In some cases, the insulator layer 610 may be approximately rectangular or square in shape, when viewed from the top (similar to the depiction of the selector 400 in FIG. 4B), in which case the sidewall surface 616 may extend around the rectangular shape. In some cases, the insulator layer 610 may be approximately circular or another closed shape, in which case the sidewall surface 616 may extend around the perimeter of that shape.

[0052] At block 504, an anti-cation-diffusion material may be deposited so as to be situated along the sidewall surface of the insulator layer. For example, the anti-cation-diffusion material may be deposited to form a conformal layer over the insulator layer formed in block 502. In some examples, a dielectric material that inhibits cation diffusion may be formed in a conformal layer via deposition

techniques. For example, the deposition process may involve physical vapor deposition (PVD), chemical vapor deposition (CVD), atomic layer deposition (ALD), plasma enhanced chemical vapor deposition (PECVD), and/or plasma assisted chemical vapor deposition (PACVD), etc. Such materials may include amorphous silicon carbide, a-SiC; boron carbonitride, BCN; silicon nitride, SiN; and/or silicon oxycarbide, SiOC; for example. As shown in FIG. 6B, a conformal layer of anti-cation-diffusion material 620 may be formed over the insulator layer 610 and electrode 602. As such, the anti-cation-diffusion material 620 is formed along the sidewall surface 616 as well as over the electrode-facing surface 614 that is still exposed. The opposing electrode-facing surface 612 of the insulator layer 610, which is disposed on the first electrode 602 is not covered by the anti-cation-diffusion material 620.

[0053] At block 506, a portion of the anti-cation-diffusion material may be removed so as to expose the insulator layer while leaving the anti-cation-diffusion material situated along the sidewall surface. The remaining anti-cation-diffusion barrier material forms a sidewall anti-cation-diffusion barrier. The exposed region of the insulator layer may then be coupled to a second electrode to complete the selector. Moreover, the second electrode may include an anti-cation-diffusion barrier situated along the insulator layer such that the insulator layer of the completed device is entirely encapsulated within anti-cation-diffusion barriers along its electrode-facing surfaces and its sidewall surface.

[0054] As shown in FIG. 6C, a portion of the anti-cation-diffusion material 620 is removed so as to expose the (top) electrode-facing surface 614. The sidewall surface 616 remains covered by anti-cation-diffusion material, which material forms the sidewall anti-cation-diffusion barrier 622. The removal of the anti-cation-diffusion material 620 so as to expose the electrode-facing surface 614 of the insulator layer 610 may be carried out via an anisotropic etching process, for example, so as to uniformly remove the thickness of the material 620 from the top down.

[0055] An example of an assembled selector device is shown in FIG. 6D. A second electrode 608 having an anti-cation-diffusion barrier 606 may be disposed over the electrode-facing surface 614 of the insulator layer 610. An electrically insulating sidewall 630 may be disposed adjacent the sidewall anti-cation-diffusion

barrier 622. The electrically insulating sidewall 630 may form a barrier that provides electrical and/or thermal insulation for the insulator layer 610. An inter-layer dielectric (ILD) 640 may be disposed between the electrodes 602, 608 adjacent the electrically insulating sidewall 630. Similar to the ILD 420 described in connection with FIGS. 4A and 4B, the ILD 640 may help to further isolate the insulator layer 610 from the effect of neighboring devices, such as neighboring selectors and/or memristors in a crossbar array. The ILD 640 may help to mitigate capacitive coupling between the opposing electrodes 602, 608. As shown in FIG. 6D, the insulator layer 610 may be encapsulated by a combination of the electrode anti-cation-diffusion barriers 606, 604 and the sidewall anti-cation-diffusion barrier 622. As such, cation metal within the insulator layer 610 may be contained within the insulator layer 610.

[0056] Some examples disclosed here relate to selector devices for being electrically coupled in series with a memristor device to form a memory cell. However, the selector devices described herein may be used in other contexts as well. For instance, in a crossbar array, selectors that include anti-cation-diffusion barriers may be electrically coupled in series with other two-terminal memory elements to help inhibit application of voltage below a threshold value to such memory elements. Moreover, selectors described herein may be applied in a variety of electrical contexts to help regulate voltage(s) applied to various components and/or current(s) through various components.

CLAIMS

1. A device comprising:
 - a first electrode having a surface including an anti-cation-diffusion barrier;
 - a second electrode having a surface including an anti-cation-diffusion barrier;
 - an insulator layer bounded by opposing electrode-facing surfaces and a sidewall surface, the insulator layer being disposed between the first electrode and the second electrode such that each of the opposing electrode-facing surfaces of the insulator layer are situated along a respective one of the anti-cation-diffusion barriers of the first and second electrodes; and
 - a sidewall anti-cation-diffusion barrier situated along the sidewall surface of the insulator layer.
2. The device of claim 1, wherein the insulator layer includes cation metal ions.
3. The device of claim 2, wherein the insulator layer is to transition from a high-resistance state to a low-resistance state responsive to application of a threshold voltage across the first and second electrodes, wherein the transition comprises the cation metal ions becoming arranged within the insulator layer so as to lower the electrical resistance between the first and second electrodes.
4. The device of claim 1, wherein the insulator layer is encapsulated by a combination of the sidewall anti-cation-diffusion barrier and the anti-cation-diffusion barriers of the first and second electrodes.
5. The device of claim 1, wherein the insulator layer comprises an oxide material.
6. The device of claim 1, further comprising a second sidewall situated adjacent the sidewall anti-cation-diffusion barrier, wherein the second sidewall comprises an electrical insulator.

7. The device of claim 1, wherein the sidewall anti-cation-diffusion barrier comprises a layer of amorphous silicon carbide.
8. A method comprising:
forming an insulator layer including cation metal ions, wherein the insulator layer is bounded by opposing electrode-facing surfaces and a sidewall surface;
forming, on the insulator layer, an anti-cation-diffusion barrier material such that the anti-cation-diffusion barrier material is disposed along the sidewall surface of the insulator layer; and
removing a portion of the anti-cation-diffusion barrier material so as to expose the insulator layer while the anti-cation-diffusion barrier material disposed on the sidewall surface of the insulator layer remains.
9. The method of claim 8, further comprising:
prior to forming the insulator layer, forming a first electrode, wherein the first insulator layer is formed on the first electrode;
forming a second electrode on the insulator layer such that the insulator layer is disposed between the first and second electrode; and
wherein each of the first and second electrodes include an anti-cation-diffusion barrier that is situated along a respective one of the electrode-facing surfaces of the insulator layer.
10. The method of claim 8, wherein the anti-cation-diffusion barrier material is formed as a conformal layer over the insulator layer via plasma enhanced chemical vapor deposition.
11. The method of claim 8, wherein the anti-cation-diffusion barrier comprises silicon oxycarbide.
12. A system comprising:

a memristor device having two terminals and a variable resistance layer disposed between the two terminals, the variable resistance layer to transition between resistance states responsive to application of a transition energy; and

a selector device electrically coupled in series with the memristor device, the selector device comprising:

- (i) a first electrode having a surface including an anti-cation-diffusion barrier;
- (ii) a second electrode having a surface including an anti-cation-diffusion barrier;
- (iii) an insulator layer bounded by opposing electrode-facing surfaces and a sidewall surface, the insulator layer being disposed between the first electrode and the second electrode such that each of the opposing electrode-facing surfaces of the insulator layer are situated along a respective one of the anti-cation-diffusion barriers of the first and second electrodes; and
- (iv) a sidewall anti-cation-diffusion barrier situated along the sidewall surface of the insulator layer.

12. The system of claim 11, wherein the insulator layer includes cation metal ions.

13. The system of claim 12, wherein the insulator layer is to transition from a high-resistance state to a low-resistance state responsive to application of a threshold voltage across the first and second electrodes, wherein the transition comprises the cation metal ions becoming arranged within the insulator layer so as to lower the electrical resistance between the first and second electrodes.

14. The system of claim 11, wherein the insulator layer is encapsulated by a combination of the sidewall anti-cation-diffusion barrier and the anti-cation-diffusion barriers of the first and second electrodes.

15. The system of claim 11, wherein the sidewall anti-cation-diffusion barrier comprises boron carbonitride.

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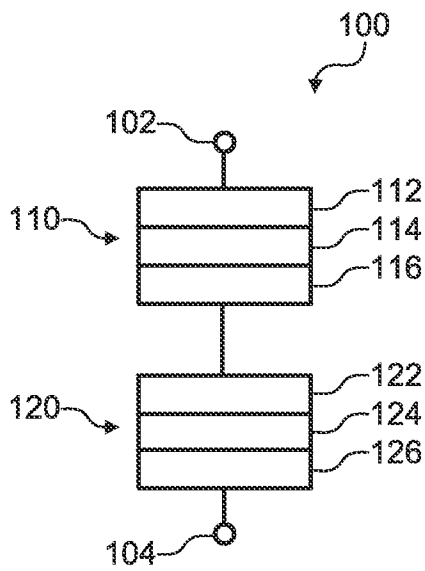


FIG. 1A

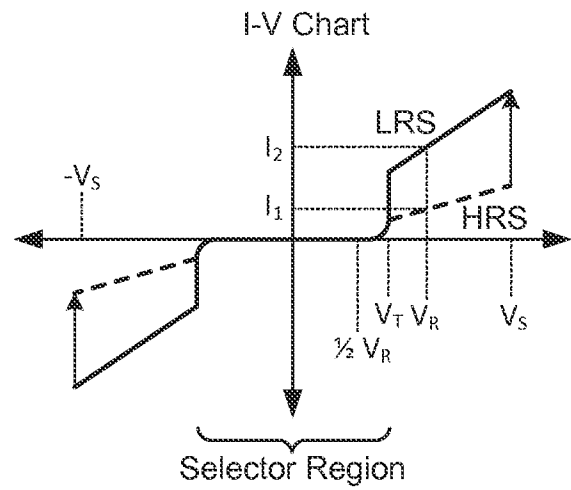


FIG. 1B

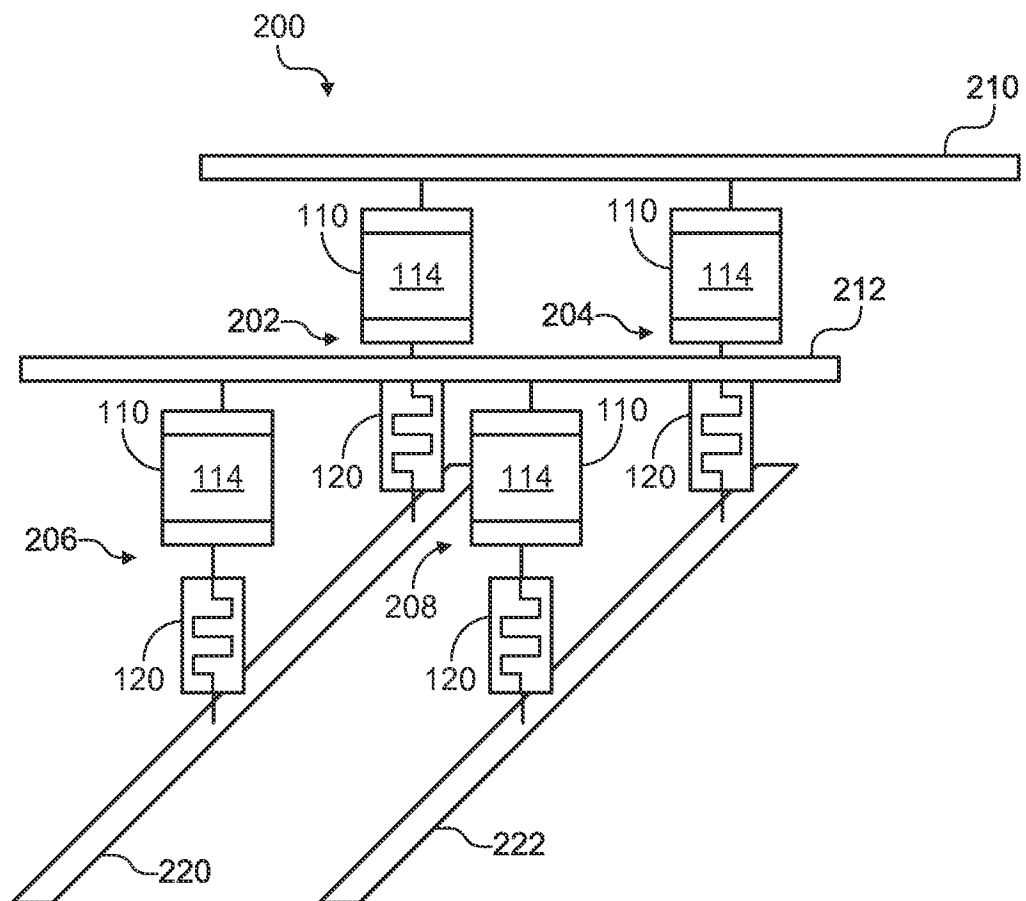


FIG. 2

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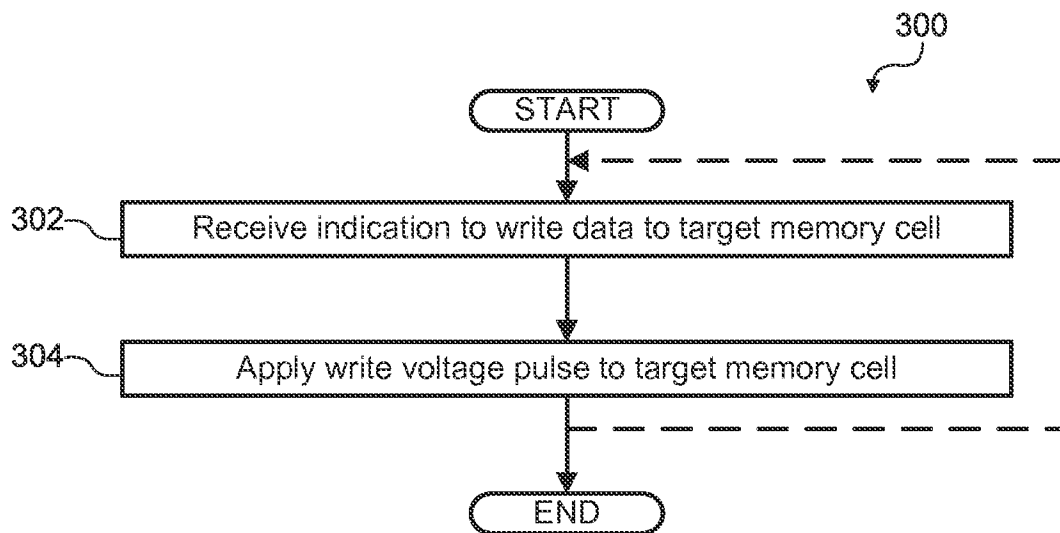


FIG. 3A

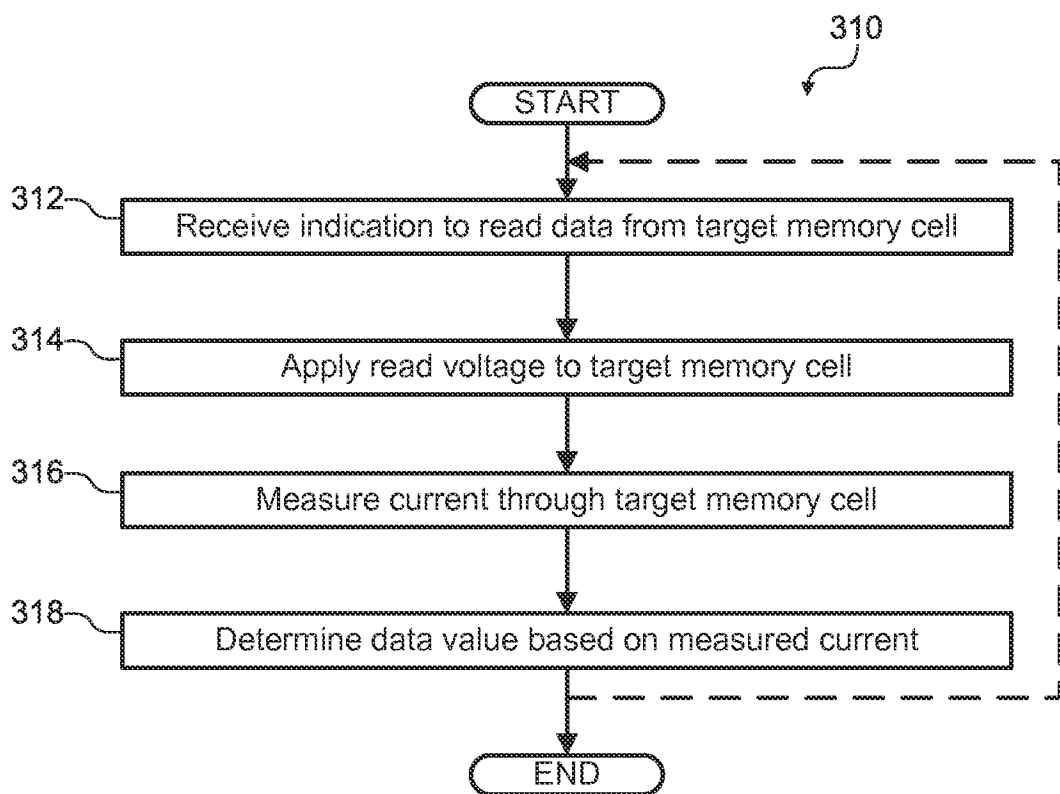


FIG. 3B

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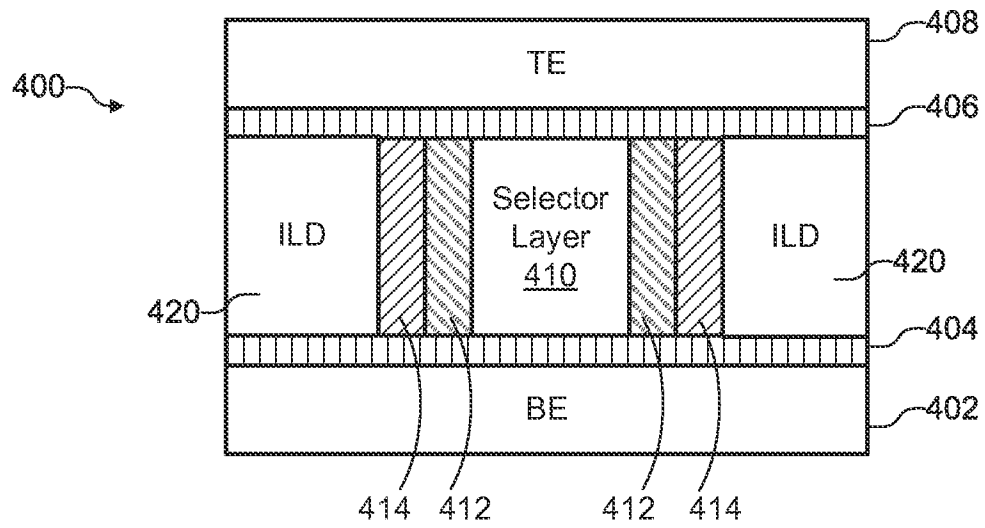


FIG. 4A

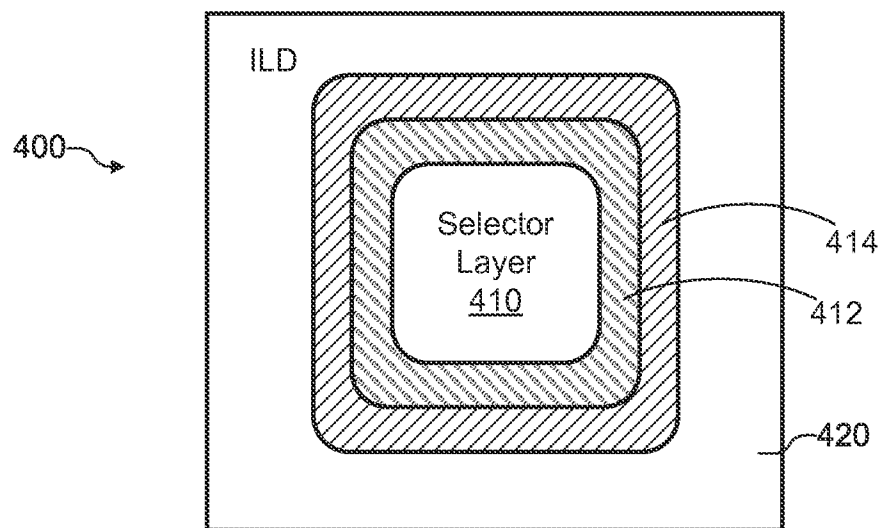


FIG. 4B

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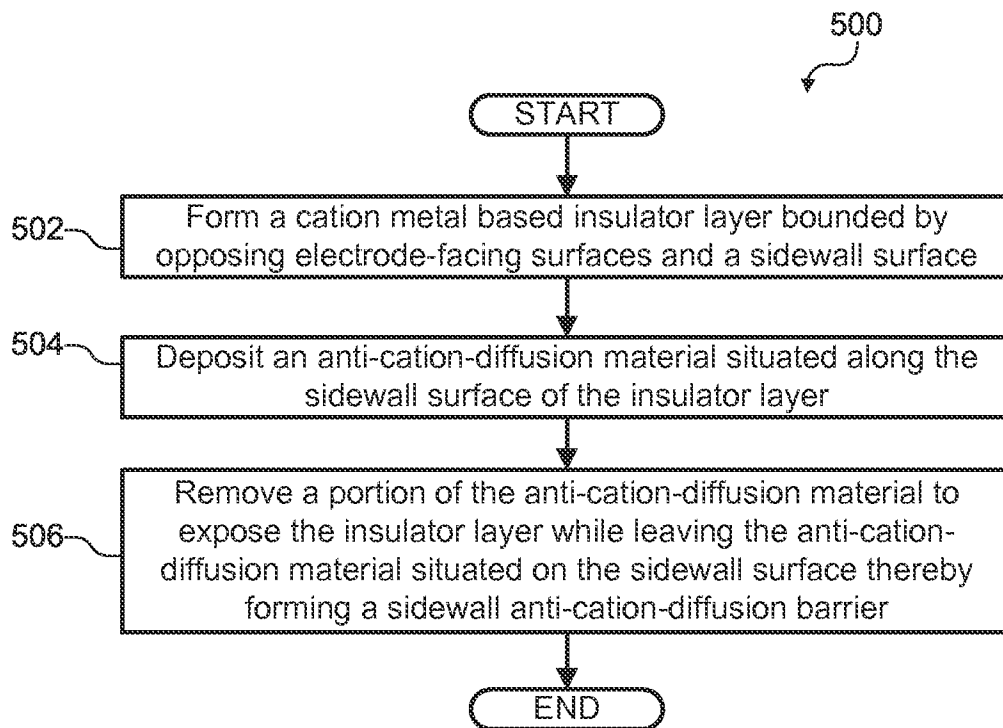


FIG. 5

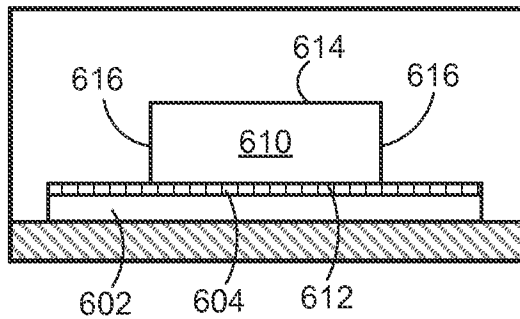


FIG. 6A

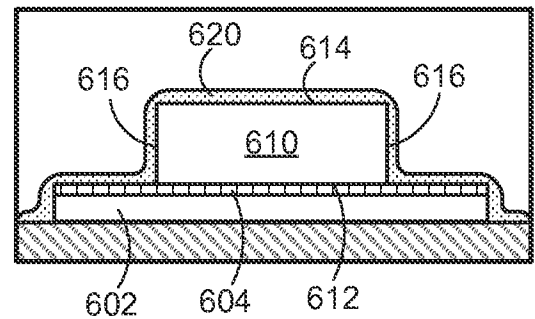


FIG. 6B

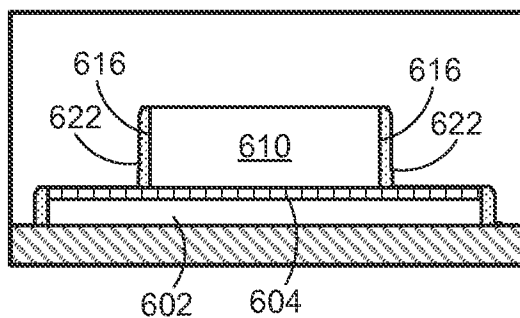


FIG. 6C

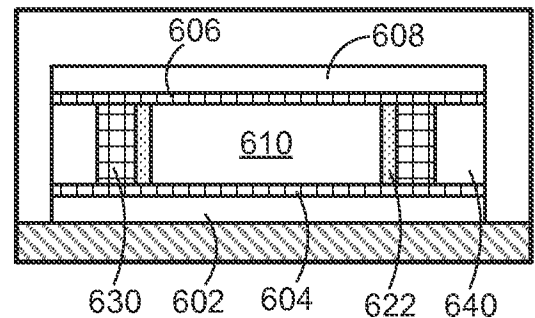


FIG. 6D

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2015/051612**A. CLASSIFICATION OF SUBJECT MATTER****H01L 27/115(2006.01)i, H01L 21/8247(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHEDMinimum documentation searched (classification system followed by classification symbols)
H01L 27/115; H01L 43/12; H01L 47/00; H01L 45/00; H01L 21/00; G11C 11/00; H01L 21/8247Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility modelsElectronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: selector, cation, diffusion, barrier**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2009-0121208 A1 (HIROYUKI NAGASHIMA et al.) 14 May 2009 See abstract, paragraphs [0036]-[0106] and figures 1-20B.	1, 4, 6-7
Y		2-3, 5, 8-15
Y	US 2012-0250395 A1 (JEAN-FRANCOIS NODIN) 04 October 2012 See abstract, paragraphs [0088]-[0159] and figures 8-16.	2-3, 5, 8-15
A	US 2013-0171741 A1 (SANG-MIN HWANG) 04 July 2013 See abstract, paragraphs [0026]-[0050] and figures 5-16B.	1-15
A	US 2013-0313508 A1 (KABUSHIKI KAISHA TOSHIBA) 28 November 2013 See abstract, paragraphs [0031]-[0048] and figures 1-8.	1-15
A	US 2014-0264237 A1 (MACRONIX INTERNATIONAL CO., LTD.) 18 September 2014 See abstract, paragraphs [0022]-[0031] and figures 2-6. Note: For claim 12(1), the claim was renumbered by this authority because claim 12 was found twice.	1-15



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

13 June 2016 (13.06.2016)

Date of mailing of the international search report

13 June 2016 (13.06.2016)

Name and mailing address of the ISA/KR

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

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