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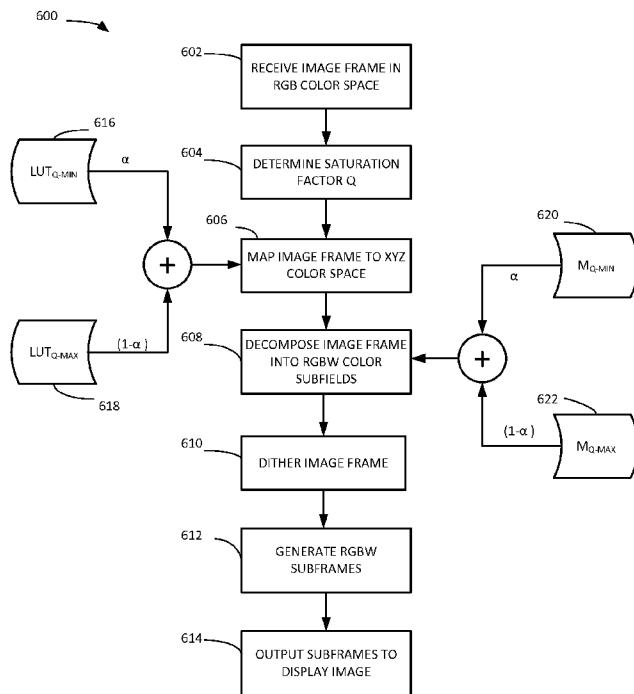
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*[Continued on next page]***(54) Title:** DISPLAY INCORPORATING DYNAMIC SATURATION COMPENSATING GAMUT MAPPING

(57) Abstract: This disclosure provides systems, methods, and apparatus for generating images on a display. A multi-primary display can include control logic that converts input image data into the multi-primary color space employed by the display by mapping the input pixel values into the XYZ color space according to a gamut mapping function and then decomposing the XYZ tristimulus values into color subfields associated with the displays primary colors. For example, such a process can be used to convert image frames encoded in an RGB color space into a RGBW color space. In some implementations, the control logic can adapt the gamut mapping and/or the decomposition processes based on a saturation level of the image being processed.

FIGURE 6



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DISPLAY INCORPORATING DYNAMIC SATURATION COMPENSATING GAMUT MAPPING

RELATED APPLICATIONS

[0001] The present Application claims priority to U.S. Patent Application No. 14/521,019, entitled “DISPLAY INCORPORATING DYNAMIC SATURATION COMPENSATING GAMUT MAPPING,” filed October 22, 2014, and assigned to the assignee hereof and hereby expressly incorporated by reference herein.

TECHNICAL FIELD

[0002] This disclosure relates to the field of imaging displays, and in particular to image formation processes for multi-primary displays.

DESCRIPTION OF THE RELATED TECHNOLOGY

[0003] Electromechanical systems (EMS) include devices having electrical and mechanical elements, actuators, transducers, sensors, optical components such as mirrors and optical films, and electronics. EMS devices or elements can be manufactured at a variety of scales including, but not limited to, microscales and nanoscales. For example, microelectromechanical systems (MEMS) devices can include structures having sizes ranging from about a micron to hundreds of microns or more. Nanoelectromechanical systems (NEMS) devices can include structures having sizes smaller than a micron including, for example, sizes smaller than several hundred nanometers. Electromechanical elements may be created using deposition, etching, lithography, and/or other micromachining processes that etch away parts of substrates and/or deposited material layers, or that add layers to form electrical and electromechanical devices.

[0004] EMS-based display apparatus have been proposed that include display elements that modulate light by selectively moving a light blocking component into and out of an optical path through an aperture defined through a light blocking layer. Doing so selectively passes light from a backlight or reflects light from the ambient or a front light to form an image.

SUMMARY

[0005] The systems, methods and devices of this disclosure each have several innovative aspects, no single one of which is solely responsible for the desirable attributes disclosed herein.

[0006] One innovative aspect of the subject matter described in this disclosure can be implemented in an apparatus that includes an array of display elements and control logic. The control logic is capable of receiving an input image frame, which includes, for each of a plurality of pixels, a first set of color parameter values. For each of the plurality of pixels, the control logic is further capable of applying a content adaptive gamut mapping process to the first set of color parameter values associated with the pixel. The content adaptive gamut mapping process is based at least in part on the content of the image frame and is configured to map the first set of color parameter values to a second set of color parameter values. The control logic decomposes the second set of color parameter values associated with the pixel to obtain pixel intensity values in respective color subfields associated with at least four different colors, and generates display element state information for the display elements based on the color subfields. The control logic is further capable of outputting display element state information associated with the at least four color subfields to the array of display elements.

[0007] In some implementations, the first set of color parameter values includes red, green, and blue pixel intensity values and the second set of color parameter values includes XYZ tristimulus values. In some implementations, the control logic is further configured to determine a saturation level parameter for the input image frame and adapt the gamut mapping process based on the determined color saturation parameter of the input image frame. The control logic can adapt the gamut mapping process by generating an image saturation level-dependent gamut mapping lookup table. In some implementations, the control logic can generate the image saturation level-dependent gamut mapping lookup table by interpolating between at least two stored gamut mapping lookup tables based on the determined image saturation parameter.

[0008] In some implementations, the control logic is further configured to decompose the second set of color parameter values associated with the plurality of pixels to form respective color subfields according to a content adaptive image decomposition process.

In some implementations, the control logic determines a saturation level parameter for the received image frame. The content adaptive image decomposition process can include applying a color decomposition matrix adjusted based on the determined saturation level parameter.

[0009] In some implementations, the apparatus further includes a backlight including light sources having colors associated with each of the respective color subfields. The control logic can, upon outputting a portion of the display element state information associated with a color subfield, illuminate a light source associated with the color subfield to illuminate the array of display elements. In some implementations, the control logic may, upon outputting the portion of the display element state information associated with the color subfield, further illuminate a light source associated with a different color subfield. The control logic may control the intensities with which the light source associated with the color subfield and the light source associated with the different color subfield are illuminated based in part on a value of a saturation level parameter determined for the received image frame.

[0010] In some implementations, the control logic is further configured to collectively dither the color subfields using a vector error diffusion process. In some implementations, the content adaptive gamut mapping process further maps, for each pixel, the first set of color parameter values to the second set of color parameter values based at least in part on a power management parameter. The power management parameter can include an inactivity period timer value, a target saturation parameter value or a battery level.

[0011] In some implementations, the apparatus further includes a display, a processor and a memory device. The display includes the array of display elements. The processor is capable of communicating with the display and processing image data. The memory device is capable of communicating with the processor. In some implementations, the display further includes a driver circuit capable of sending at least one signal to the display and a controller capable of sending at least a portion of the image data to the driver circuit. In some implementations, the apparatus further includes an image source module capable of sending the image data to the processor. The image source module includes at least one of a receiver, transceiver, and

transmitter. In some implementations, the apparatus further includes an input device capable of receiving input data and communicating the input data to the processor.

[0012] Another innovative aspect of the subject matter described in this disclosure can be implemented in a computer readable medium storing computer executable instructions, which when executed by a processor cause the processor to carry out a method of forming an image on a display. The method includes receiving an input image frame. The input image frame includes, for each of a plurality of pixels, a first set of color parameter values. The method also includes applying, for each of the plurality of pixels, a content adaptive gamut mapping process to the first set of color parameter values associated with the pixel. The content adaptive gamut mapping process is based at least in part on the content of the image frame and is configured to map the first set of color parameter values to a second set of color parameter values. The method further includes decomposing the second set of color parameter values associated with the pixel to obtain pixel intensity values in respective color subfields associated with at least four different colors. The method further includes generating display element state information for display elements in an array of display elements based on the color subfields, and outputting display element state information associated with the at least four color subfields to the array of display elements.

[0013] In some implementations, the first set of color parameter values includes red, green, and blue pixel intensity values and the second set of color parameter values includes XYZ tristimulus values. In some implementations, the method further includes determining a saturation level parameter for the input image frame and adapting the gamut mapping process based on the determined color saturation parameter of the input image frame. In some implementations, adapting the gamut mapping process includes generating an image saturation level-dependent gamut mapping lookup table. In some implementations, generating the image saturation level-dependent gamut mapping lookup table includes interpolating between at least two stored gamut mapping lookup tables based on the determined image saturation parameter.

[0014] In some implementations, decomposing the second set of color parameter values associated with each pixel includes decomposing the second set of color parameter values according to a content adaptive image decomposition process. In some implementations, the method further includes determining a saturation level

parameter for the received image frame. The content adaptive image decomposition process includes applying a color decomposition matrix adjusted based on the determined saturation level parameter.

[0015] In some implementations, the method further includes collectively dithering the color subfields using a vector error diffusion process. In some implementations, the content adaptive gamut mapping process further maps, for each pixel, the first set of color parameter values to the second set of color parameter values based at least in part on a power management parameter. The power management parameter can include an inactivity period timer value, a target saturation parameter value or a battery level.

[0016] Another innovative aspect of the subject matter described in this disclosure can be implemented in an apparatus that includes an array of display elements and control logic. The control logic is configured to receive an input image frame encoded in a first color space. The input image frame includes, for each of a plurality of pixels, a set of color intensity values. The control logic is further configured to determine a saturation parameter for the image frame. For each pixel in the image frame, the control logic applies a gamut mapping process to the color intensity values associated with the pixel in order to convert the color intensity values into corresponding tristimulus values in the XYZ color space based at least in part on the saturation parameter. The control logic also decomposes the XYZ tristimulus values associated with the pixel to obtain pixel intensity values associated with at least four different color subfields. The control logic is further configured to generate display element state information for the display elements in the array of display elements based on the color subfields, and output display element state information associated with the at least four color subfields to the array of display elements to form an image.

[0017] In some implementations, the control logic is further configured to derive a decomposition matrix based at least in part on the saturation parameter and apply the decomposition matrix in decomposing the XYZ tristimulus values.

[0018] Details of one or more implementations of the subject matter described in this disclosure are set forth in the accompanying drawings and the description below. Other features, aspects, and advantages will become apparent from the description, the

drawings and the claims. Note that the relative dimensions of the following figures may not be drawn to scale.

BRIEF DESCRIPTION OF THE DRAWINGS

[0019] Figure 1A shows a schematic diagram of an example direct-view microelectromechanical systems (MEMS) based display apparatus.

[0020] Figure 1B shows a block diagram of an example host device.

[0021] Figures 2A and 2B show views of an example dual actuator shutter assembly.

[0022] Figure 3 shows a block diagram of an example display apparatus.

[0023] Figure 4 shows a block diagram of example control logic suitable for use as, for example, the control logic in the display apparatus shown in Figure 3.

[0024] Figure 5 shows a flow diagram of an example process for generating an image on a display using the control logic shown in Figure 4.

[0025] Figure 6 shows a flow diagram of another example process for generating an image on a display using the control logic shown in Figure 4.

[0026] Figure 7 shows a flow diagram of an example process of forming an image on a display.

[0027] Figure 8 shows a flow diagram of an example process of reducing power consumption in a display.

[0028] Figure 9 shows a flow diagram of a second example process of reducing power consumption in a display.

[0029] Figure 10 shows a flow diagram of an example process of a display outputting images using a Q value that is selected in part based on a desired power consumption target.

[0030] Figures 11A and 11B show system block diagrams of an example display device that includes a plurality of display elements.

[0031] Like reference numbers and designations in the various drawings indicate like elements.

DETAILED DESCRIPTION

[0032] The following description is directed to certain implementations for the purposes of describing the innovative aspects of this disclosure. However, a person having ordinary skill in the art will readily recognize that the teachings herein can be applied in a multitude of different ways. The described implementations may be implemented in any device, apparatus, or system that is capable of displaying an image, whether in motion (such as video) or stationary (such as still images), and whether textual, graphical or pictorial. The concepts and examples provided in this disclosure may be applicable to a variety of displays, such as liquid crystal displays (LCDs), organic light-emitting diode (OLED) displays, field emission displays, and electromechanical systems (EMS) and microelectromechanical (MEMS)-based displays, in addition to displays incorporating features from one or more display technologies.

[0033] The described implementations may be included in or associated with a variety of electronic devices such as, but not limited to: mobile telephones, multimedia Internet enabled cellular telephones, mobile television receivers, wireless devices, smartphones, Bluetooth® devices, personal data assistants (PDAs), wireless electronic mail receivers, hand-held or portable computers, netbooks, notebooks, smartbooks, tablets, printers, copiers, scanners, facsimile devices, global positioning system (GPS) receivers/navigators, cameras, digital media players (such as MP3 players), camcorders, game consoles, wrist watches, wearable devices, clocks, calculators, television monitors, flat panel displays, electronic reading devices (such as e-readers), computer monitors, auto displays (such as odometer and speedometer displays), cockpit controls and/or displays, camera view displays (such as the display of a rear view camera in a vehicle), electronic photographs, electronic billboards or signs, projectors, architectural structures, microwaves, refrigerators, stereo systems, cassette recorders or players, DVD players, CD players, VCRs, radios, portable memory chips, washers, dryers, washer/dryers, parking meters, packaging (such as in electromechanical systems (EMS) applications including microelectromechanical systems (MEMS) applications, in addition to non-EMS applications), aesthetic structures (such as display of images on a piece of jewelry or clothing) and a variety of EMS devices.

[0034] The teachings herein also can be used in non-display applications such as, but not limited to, electronic switching devices, radio frequency filters, sensors, accelerometers, gyroscopes, motion-sensing devices, magnetometers, inertial

components for consumer electronics, parts of consumer electronics products, varactors, liquid crystal devices, electrophoretic devices, drive schemes, manufacturing processes and electronic test equipment. Thus, the teachings are not intended to be limited to the implementations depicted solely in the Figures, but instead have wide applicability as will be readily apparent to one having ordinary skill in the art.

[0035] A multi-primary display can include control logic that converts input image data into the multi-primary color spaces employed by the display by mapping the input pixel values into the XYZ color space according to a gamut mapping function and then decomposing the XYZ tristimulus values into color subfields associated with the display's primary colors. For example, such a process can be used to convert image frames encoded in an RGB color space into a RGBW color space.

[0036] In some implementations, to maintain color fidelity and improve power efficiency, the control logic can employ an image saturation dependent gamut mapping when converting input image pixel values into the XYZ color tristimulus space. In some implementations, the control logic can implement the image saturation dependent gamut mapping by generating a saturation level dependent gamut mapping lookup table (LUT). The saturation level is represented by a parameter Q. The saturation level dependent gamut mapping LUT can be formed by interpolating values between at least two stored saturation level dependent (i.e., Q-dependent) gamut mapping LUTs. In some implementations, the control logic can decompose the XYZ tristimulus values into the multi-primary color subfields using a saturation level dependent decomposition matrix.

[0037] In some implementations, the saturation based gamut mapping can be adapted to control the power consumption of the display. For example, images can be gamut mapped using a lower saturation (i.e., a higher Q value) in response to detecting device inactivity or in response to detecting a low battery condition. Similarly, the saturation level used for the gamut mapping can be adjusted to maintain a target power consumption or battery life.

[0038] Particular implementations of the subject matter described in this disclosure can be implemented to realize one or more of the following potential advantages. Significant power savings can be achieved while substantially maintaining color fidelity by converting input pixel values to output pixel values using a saturation dependent

gamut mapping process. By implementing the gamut mapping process such that input pixel values are mapped to XYZ tristimulus values in the XYZ color space, the display's control logic can more readily implement vector error diffusion processes before decomposing the resulting dithered pixel XYZ tristimulus values into RGBW intensity values. Vector error diffusion in the XYZ color space can significantly improve image quality relative to single color subfield dithering in a RGBW color space.

[0039] In some implementations, the gamut mapping process can be used to control the rate at which power is consumed by the display to maintain or extend the battery life of the device in which the display is incorporated. Additional power management features, such as subframe reduction, can also be employed based on the battery level of the display and/or the Q values selected for displaying an image frame.

[0040] Figure 1A shows a schematic diagram of an example direct-view MEMS-based display apparatus 100. The display apparatus 100 includes a plurality of light modulators 102a–102d (generally light modulators 102) arranged in rows and columns. In the display apparatus 100, the light modulators 102a and 102d are in the open state, allowing light to pass. The light modulators 102b and 102c are in the closed state, obstructing the passage of light. By selectively setting the states of the light modulators 102a–102d, the display apparatus 100 can be utilized to form an image 104 for a backlit display, if illuminated by a lamp or lamps 105. In another implementation, the apparatus 100 may form an image by reflection of ambient light originating from the front of the apparatus. In another implementation, the apparatus 100 may form an image by reflection of light from a lamp or lamps positioned in the front of the display, i.e., by use of a front light.

[0041] In some implementations, each light modulator 102 corresponds to a pixel 106 in the image 104. In some other implementations, the display apparatus 100 may utilize a plurality of light modulators to form a pixel 106 in the image 104. For example, the display apparatus 100 may include three color-specific light modulators 102. By selectively opening one or more of the color-specific light modulators 102 corresponding to a particular pixel 106, the display apparatus 100 can generate a color pixel 106 in the image 104. In another example, the display apparatus 100 includes two or more light modulators 102 per pixel 106 to provide a luminance level in an image 104. With respect to an image, a pixel corresponds to the smallest picture element

defined by the resolution of image. With respect to structural components of the display apparatus 100, the term pixel refers to the combined mechanical and electrical components utilized to modulate the light that forms a single pixel of the image.

[0042] The display apparatus 100 is a direct-view display in that it may not include imaging optics typically found in projection applications. In a projection display, the image formed on the surface of the display apparatus is projected onto a screen or onto a wall. The display apparatus is substantially smaller than the projected image. In a direct view display, the image can be seen by looking directly at the display apparatus, which contains the light modulators and optionally a backlight or front light for enhancing brightness and/or contrast seen on the display.

[0043] Direct-view displays may operate in either a transmissive or reflective mode. In a transmissive display, the light modulators filter or selectively block light which originates from a lamp or lamps positioned behind the display. The light from the lamps is optionally injected into a lightguide or backlight so that each pixel can be uniformly illuminated. Transmissive direct-view displays are often built onto transparent substrates to facilitate a sandwich assembly arrangement where one substrate, containing the light modulators, is positioned over the backlight. In some implementations, the transparent substrate can be a glass substrate (sometimes referred to as a glass plate or panel), or a plastic substrate. The glass substrate may be or include, for example, a borosilicate glass, wine glass, fused silica, a soda lime glass, quartz, artificial quartz, Pyrex, or other suitable glass material.

[0044] Each light modulator 102 can include a shutter 108 and an aperture 109. To illuminate a pixel 106 in the image 104, the shutter 108 is positioned such that it allows light to pass through the aperture 109. To keep a pixel 106 unlit, the shutter 108 is positioned such that it obstructs the passage of light through the aperture 109. The aperture 109 is defined by an opening patterned through a reflective or light-absorbing material in each light modulator 102.

[0045] The display apparatus also includes a control matrix coupled to the substrate and to the light modulators for controlling the movement of the shutters. The control matrix includes a series of electrical interconnects (such as interconnects 110, 112 and 114), including at least one write-enable interconnect 110 (also referred to as a scan line interconnect) per row of pixels, one data interconnect 112 for each column of pixels,

and one common interconnect 114 providing a common voltage to all pixels, or at least to pixels from both multiple columns and multiples rows in the display apparatus 100. In response to the application of an appropriate voltage (the write-enabling voltage, V_{WE}), the write-enable interconnect 110 for a given row of pixels prepares the pixels in the row to accept new shutter movement instructions. The data interconnects 112 communicate the new movement instructions in the form of data voltage pulses. The data voltage pulses applied to the data interconnects 112, in some implementations, directly contribute to an electrostatic movement of the shutters. In some other implementations, the data voltage pulses control switches, such as transistors or other non-linear circuit elements that control the application of separate drive voltages, which are typically higher in magnitude than the data voltages, to the light modulators 102. The application of these drive voltages results in the electrostatic driven movement of the shutters 108.

[0046] The control matrix also may include, without limitation, circuitry, such as a transistor and a capacitor associated with each shutter assembly. In some implementations, the gate of each transistor can be electrically connected to a scan line interconnect. In some implementations, the source of each transistor can be electrically connected to a corresponding data interconnect. In some implementations, the drain of each transistor may be electrically connected in parallel to an electrode of a corresponding capacitor and to an electrode of a corresponding actuator. In some implementations, the other electrode of the capacitor and the actuator associated with each shutter assembly may be connected to a common or ground potential. In some other implementations, the transistor can be replaced with a semiconducting diode, or a metal-insulator-metal switching element.

[0047] Figure 1B shows a block diagram of an example host device 120 (i.e., cell phone, smart phone, PDA, MP3 player, tablet, e-reader, netbook, notebook, watch, wearable device, laptop, television, or other electronic device). The host device 120 includes a display apparatus 128 (such as the display apparatus 100 shown in Figure 1A), a host processor 122, environmental sensors 124, a user input module 126, and a power source.

[0048] The display apparatus 128 includes a plurality of scan drivers 130 (also referred to as write enabling voltage sources), a plurality of data drivers 132 (also referred to as data voltage sources), a controller 134, common drivers 138, lamps

140–146, lamp drivers 148 and an array of display elements 150, such as the light modulators 102 shown in Figure 1A. The scan drivers 130 apply write enabling voltages to scan line interconnects 131. The data drivers 132 apply data voltages to the data interconnects 133.

[0049] In some implementations of the display apparatus, the data drivers 132 are capable of providing analog data voltages to the array of display elements 150, especially where the luminance level of the image is to be derived in analog fashion. In analog operation, the display elements are designed such that when a range of intermediate voltages is applied through the data interconnects 133, there results a range of intermediate illumination states or luminance levels in the resulting image. In some other implementations, the data drivers 132 are capable of applying a reduced set, such as 2, 3 or 4, of digital voltage levels to the data interconnects 133. In implementations in which the display elements are shutter-based light modulators, such as the light modulators 102 shown in Figure 1A, these voltage levels are designed to set, in digital fashion, an open state, a closed state, or other discrete state to each of the shutters 108. In some implementations, the drivers are capable of switching between analog and digital modes.

[0050] The scan drivers 130 and the data drivers 132 are connected to a digital controller circuit 134 (also referred to as the controller 134). The controller 134 sends data to the data drivers 132 in a mostly serial fashion, organized in sequences, which in some implementations may be predetermined, grouped by rows and by image frames. The data drivers 132 can include series-to-parallel data converters, level-shifting, and for some applications digital-to-analog voltage converters.

[0051] The display apparatus optionally includes a set of common drivers 138, also referred to as common voltage sources. In some implementations, the common drivers 138 provide a DC common potential to all display elements within the array 150 of display elements, for instance by supplying voltage to a series of common interconnects 139. In some other implementations, the common drivers 138, following commands from the controller 134, issue voltage pulses or signals to the array of display elements 150, for instance global actuation pulses which are capable of driving and/or initiating simultaneous actuation of all display elements in multiple rows and columns of the array.

[0052] Each of the drivers (such as scan drivers 130, data drivers 132 and common drivers 138) for different display functions can be time-synchronized by the controller 134. Timing commands from the controller 134 coordinate the illumination of red, green, blue and white lamps (140, 142, 144 and 146 respectively) via lamp drivers 148, the write-enabling and sequencing of specific rows within the array of display elements 150, the output of voltages from the data drivers 132, and the output of voltages that provide for display element actuation. In some implementations, the lamps are light emitting diodes (LEDs).

[0053] The controller 134 determines the sequencing or addressing scheme by which each of the display elements can be re-set to the illumination levels appropriate to a new image 104. New images 104 can be set at periodic intervals. For instance, for video displays, color images or frames of video are refreshed at frequencies ranging from 10 to 300 Hertz (Hz). In some implementations, the setting of an image frame to the array of display elements 150 is synchronized with the illumination of the lamps 140, 142, 144 and 146 such that alternate image frames are illuminated with an alternating series of colors, such as red, green, blue and white. The image frames for each respective color are referred to as color subframes. In this method, referred to as the field sequential color method, if the color subframes are alternated at frequencies in excess of 20 Hz, the human visual system (HVS) will average the alternating frame images into the perception of an image having a broad and continuous range of colors. In some other implementations, the lamps can employ primary colors other than red, green, blue and white. In some implementations, fewer than four, or more than four lamps with primary colors can be employed in the display apparatus 128.

[0054] In some implementations, where the display apparatus 128 is designed for the digital switching of shutters, such as the shutters 108 shown in Figure 1A, between open and closed states, the controller 134 forms an image by the method of time division gray scale. In some other implementations, the display apparatus 128 can provide gray scale through the use of multiple display elements per pixel.

[0055] In some implementations, the data for an image state is loaded by the controller 134 to the array of display elements 150 by a sequential addressing of individual rows, also referred to as scan lines. For each row or scan line in the sequence, the scan driver 130 applies a write-enable voltage to the write enable interconnect 131 for that row of the array of display elements 150, and subsequently the

data driver 132 supplies data voltages, corresponding to desired shutter states, for each column in the selected row of the array. This addressing process can repeat until data has been loaded for all rows in the array of display elements 150. In some implementations, the sequence of selected rows for data loading is linear, proceeding from top to bottom in the array of display elements 150. In some other implementations, the sequence of selected rows is pseudo-randomized, in order to mitigate potential visual artifacts. And in some other implementations, the sequencing is organized by blocks, where, for a block, the data for a certain fraction of the image is loaded to the array of display elements 150. For example, the sequence can be implemented to address every fifth row of the array of the display elements 150 in sequence.

[0056] In some implementations, the addressing process for loading image data to the array of display elements 150 is separated in time from the process of actuating the display elements. In such an implementation, the array of display elements 150 may include data memory elements for each display element, and the control matrix may include a global actuation interconnect for carrying trigger signals, from the common driver 138, to initiate simultaneous actuation of the display elements according to data stored in the memory elements.

[0057] In some implementations, the array of display elements 150 and the control matrix that controls the display elements may be arranged in configurations other than rectangular rows and columns. For example, the display elements can be arranged in hexagonal arrays or curvilinear rows and columns.

[0058] The host processor 122 generally controls the operations of the host device 120. For example, the host processor 122 may be a general or special purpose processor for controlling a portable electronic device. With respect to the display apparatus 128, included within the host device 120, the host processor 122 outputs image data as well as additional data about the host device 120. Such information may include data from environmental sensors 124, such as ambient light or temperature; information about the host device 120, including, for example, an operating mode of the host or the amount of power remaining in the host device's power source; information about the content of the image data; information about the type of image data; and/or instructions for the display apparatus 128 for use in selecting an imaging mode.

[0059] In some implementations, the user input module 126 enables the conveyance of personal preferences of a user to the controller 134, either directly, or via the host processor 122. In some implementations, the user input module 126 is controlled by software in which a user inputs personal preferences, for example, color, contrast, power, brightness, content, and other display settings and parameters preferences. In some other implementations, the user input module 126 is controlled by hardware in which a user inputs personal preferences. In some implementations, the user may input these preferences via voice commands, one or more buttons, switches or dials, or with touch-capability. The plurality of data inputs to the controller 134 direct the controller to provide data to the various drivers 130, 132, 138 and 148 which correspond to optimal imaging characteristics.

[0060] The environmental sensor module 124 also can be included as part of the host device 120. The environmental sensor module 124 can be capable of receiving data about the ambient environment, such as temperature and or ambient lighting conditions. The sensor module 124 can be programmed, for example, to distinguish whether the device is operating in an indoor or office environment versus an outdoor environment in bright daylight versus an outdoor environment at nighttime. The sensor module 124 communicates this information to the display controller 134, so that the controller 134 can optimize the viewing conditions in response to the ambient environment.

[0061] Figures 2A and 2B show views of an example dual actuator shutter assembly 200. The dual actuator shutter assembly 200, as depicted in Figure 2A, is in an open state. Figure 2B shows the dual actuator shutter assembly 200 in a closed state. The shutter assembly 200 includes actuators 202 and 204 on either side of a shutter 206. Each actuator 202 and 204 is independently controlled. A first actuator, a shutter-open actuator 202, serves to open the shutter 206. A second opposing actuator, the shutter-close actuator 204, serves to close the shutter 206. Each of the actuators 202 and 204 can be implemented as compliant beam electrode actuators. The actuators 202 and 204 open and close the shutter 206 by driving the shutter 206 substantially in a plane parallel to an aperture layer 207 over which the shutter is suspended. The shutter 206 is suspended a short distance over the aperture layer 207 by anchors 208 attached to the actuators 202 and 204. Having the actuators 202 and 204 attach to opposing ends of the shutter 206 along its axis of movement reduces out of plane motion of the shutter 206 and confines the motion substantially to a plane parallel to the substrate (not depicted).

[0062] In the depicted implementation, the shutter 206 includes two shutter apertures 212 through which light can pass. The aperture layer 207 includes a set of three apertures 209. In Figure 2A, the shutter assembly 200 is in the open state and, as such, the shutter-open actuator 202 has been actuated, the shutter-close actuator 204 is in its relaxed position, and the centerlines of the shutter apertures 212 coincide with the centerlines of two of the aperture layer apertures 209. In Figure 2B, the shutter assembly 200 has been moved to the closed state and, as such, the shutter-open actuator 202 is in its relaxed position, the shutter-close actuator 204 has been actuated, and the light blocking portions of the shutter 206 are now in position to block transmission of light through the apertures 209 (depicted as dotted lines).

[0063] Each aperture has at least one edge around its periphery. For example, the rectangular apertures 209 have four edges. In some implementations, in which circular, elliptical, oval, or other curved apertures are formed in the aperture layer 207, each aperture may have a single edge. In some other implementations, the apertures need not be separated or disjointed in the mathematical sense, but instead can be connected. That is to say, while portions or shaped sections of the aperture may maintain a correspondence to each shutter, several of these sections may be connected such that a single continuous perimeter of the aperture is shared by multiple shutters.

[0064] In order to allow light with a variety of exit angles to pass through the apertures 212 and 209 in the open state, the width or size of the shutter apertures 212 can be designed to be larger than a corresponding width or size of apertures 209 in the aperture layer 207. In order to effectively block light from escaping in the closed state, the light blocking portions of the shutter 206 can be designed to overlap the edges of the apertures 209. Figure 2B shows an overlap 216, which in some implementations can be predefined, between the edge of light blocking portions in the shutter 206 and one edge of the aperture 209 formed in the aperture layer 207.

[0065] The electrostatic actuators 202 and 204 are designed so that their voltage-displacement behavior provides a bi-stable characteristic to the shutter assembly 200. For each of the shutter-open and shutter-close actuators, there exists a range of voltages below the actuation voltage, which if applied while that actuator is in the closed state (with the shutter being either open or closed), will hold the actuator closed and the shutter in position, even after a drive voltage is applied to the opposing actuator. The

minimum voltage needed to maintain a shutter's position against such an opposing force is referred to as a maintenance voltage V_m .

[0066] Figure 3 shows a block diagram of an example display apparatus 300. The display apparatus 300 includes a host device 302 and a display module 304. The host device 302 can be an example of the host device 120 and the display module 304 can be an example of the display apparatus 128, both shown in Figure 1B. The host device 302 can be any of a number of electronic devices, such as a portable telephone, a smartphone, a watch, a tablet computer, a laptop computer, a desktop computer, a television, a set top box, a DVD or other media player, or any other device that provides graphical output to a display, similar to the display device 40 shown in Figures 11A and 11B below. In general, the host device 302 serves as a source for image data to be displayed on the display module 304.

[0067] The display module 304 further includes control logic 306, a frame buffer 308, an array of display elements 310, display drivers 312 and a backlight 314. In general, the control logic 306 serves to process image data received from the host device 302 and controls the display drivers 312, array of display elements 310 and backlight 314 to together produce the images encoded in the image data. The control logic 306, frame buffer 308, array of display elements 310, and display drivers 312 shown in Figure 3 can be similar, in some implementations, to the driver controller 29, frame buffer 28, display array 30, and array drivers 22 shown in Figures 11A and 11B, below. The functionality of the control logic 306 is described further below in relation to Figures 5–10.

[0068] In some implementations, as shown in Figure 3, the functionality of the control logic 306 is divided between a microprocessor 316 and an interface (I/F) chip 318. In some implementations, the interface chip 318 is implemented in an integrated circuit logic device, such as an application specific integrated circuit (ASIC). In some implementations, the microprocessor 316 is configured to carry out all or substantially all of the image processing functionality of the control logic 306. In addition, the microprocessor 316 can be configured to determine an appropriate output sequence for the display module 304 to use to generate received images. For example, the microprocessor 316 can be configured to convert image frames included in the received image data into a set of image subframes. Each image subframe can be associated with a color and a weight, and includes desired states of each of the display elements in the

array of display elements 310. The microprocessor 316 also can be configured to determine the number of image subframes to display to produce a given image frame, the order in which the image subframes are to be displayed, timing parameters associated with addressing the display elements in each subframe, and parameters associated with implementing the appropriate weight for each of the image subframes. These parameters may include, in various implementations, the duration for which each of the respective image subframes is to be illuminated and the intensity of such illumination. The collection of these parameters (i.e., the number of subframes, the order and timing of their output, and their weight implementation parameters for each subframe) can be referred to as an “output sequence.”

[0069] The interface chip 318 can be capable of carrying out more routine operations of the display module 304. The operations may include retrieving image subframes from the frame buffer 308 and outputting control signals to the display drivers 312 and the backlight 314 in response to the retrieved image subframe and the output sequence determined by the microprocessor 316. In some other implementations, the functionality of the microprocessor 316 and the interface chip 318 are combined into a single logic device, which may take the form of a microprocessor, an ASIC, a field programmable gate array (FPGA) or other programmable logic device. For example, the functionality of the microprocessor 316 and the interface chip 318 can be implemented by a processor 21 shown in Figure 11B. In some other implementations, the functionality of the microprocessor 316 and the interface chip 318 may be divided in other ways between multiple logic devices, including one or more microprocessors, ASICs, FPGAs, digital signal processors (DSPs) or other logic devices.

[0070] The frame buffer 308 can be any volatile or non-volatile integrated circuit memory, such as DRAM, high-speed cache memory, or flash memory (for example, the frame buffer 308 can be similar to the frame buffer 28 shown in Figure 11B). In some other implementations, the interface chip 318 causes the frame buffer 308 to output data signals directly to the display drivers 312. The frame buffer 308 has sufficient capacity to store color subfield data and subframe data associated with at least one image frame. In some implementations, the frame buffer 308 has sufficient capacity to store color subfield data and subframe data associated with a single image frame. In some other implementations, the frame buffer 308 has sufficient capacity to store color subfield data and subframe data associated with at least two image frames. Such extra memory

capacity allows for additional processing by the microprocessor 316 of image data associated with a more recently received image frame while a previously received image frame is being displayed via the array of display elements 310.

[0071] In some implementations, the display module 304 includes multiple memory devices. For example, the display module 304 may include one memory device, such as a memory directly associated with the microprocessor 316, for storing subfield data, and the frame buffer 308 is reserved for storage of subframe data.

[0072] The array of display elements 310 can include an array of any type of display elements that can be used for image formation. In some implementations, the display elements can be EMS light modulators. In some such implementations, the display elements can be MEMS shutter-based light modulators similar to those shown in Figures 2A or 2B. In some other implementations, the display elements can be other forms of light modulators, including liquid crystal light modulators, other types of EMS- or MEMS-based light modulators, or light emitters, such as OLED emitters, configured for use with a time division gray scale image formation process.

[0073] The display drivers 312 can include a variety of drivers depending on the specific control matrix used to control the display elements in the array of display elements 310. In some implementations, the display drivers 312 include a plurality of scan drivers similar to the scan drivers 130, a plurality of data drivers similar to the data drivers 132, and a set of common drivers similar to the common drivers 138, as shown in Figure 1B. As described above, the scan drivers output write enabling voltages to rows of display elements, while the data drivers output data signals along columns of display elements. The common drivers output signals to display elements in multiple rows and multiple columns of display elements.

[0074] In some implementations, particularly for larger display modules 304, the control matrix used to control the display elements in the array of display elements 310 is segmented into multiple regions. For example, the array of display elements 310 shown in Figure 3 is segmented into four quadrants. A separate set of display drivers 312 is coupled to each quadrant. Dividing a display into segments in this fashion can reduce the propagation time needed for signals output by the display drivers to reach the furthest display element coupled to a given driver, thereby decreasing the time needed

to address the display. Such segmentation also can reduce the power requirements of the drivers employed.

[0075] In some implementations, the display elements in the array of display elements can be utilized in a direct-view transmissive display. In direct-view transmissive displays, the display elements, such as EMS light modulators, selectively block light that originates from a backlight, such as the backlight 314, which is illuminated by one or more lamps. Such display elements can be fabricated on transparent substrates, made, for example, from glass. In some implementations, the display drivers 312 are coupled directly to the glass substrate on which the display elements are formed. In such implementations, the drivers are built using a chip-on-glass configuration. In some other implementations, the drivers are built on a separate circuit board and the outputs of the drivers are coupled to the substrate using, for example, flex cables or other wiring.

[0076] The backlight 314 can include a light guide, one or more light sources (such as LEDs), and light source drivers. The light sources can include light sources of multiple colors, such as red, green, blue, and in some implementations white. The light source drivers are capable of individually driving the light sources to a plurality of discrete light levels to enable illumination gray scale and/or content adaptive backlight control (CABC) in the backlight. In addition, lights of multiple colors can be illuminated simultaneously at various intensity levels to adjust the chromaticities of the component colors used by the display, for example to match a desired color gamut. Lights of multiple colors also can be illuminated to form composite colors. For displays employing red, green, and blue component colors, the display may utilize a composite color white, yellow, cyan, magenta, or any other color formed from a combination of two or more of the component colors.

[0077] The light guide distributes the light output by light sources substantially evenly beneath the array of display elements 310. In some other implementations, for example for displays including reflective display elements, the display apparatus 300 can include a front light or other form of lighting instead of a backlight. The illumination of such alternative light sources can likewise be controlled according to illumination gray scale processes that incorporate content adaptive control features. For ease of explanation, the display processes discussed herein are described with respect to the use of a backlight. However, it would be understood by a person of ordinary skill that such

processes also may be adapted for use with a front light or other similar form of display lighting.

[0078] Figure 4 shows a block diagram of example control logic 400 suitable for use as, for example, the control logic 306 in the display apparatus 300 shown in Figure 3. More particularly, Figure 4 shows a block diagram of functional modules executed by the microprocessor 316 and the I/F Chip 318 or by other integrated circuitry logic forming or included in the control logic 400. Each functional module can be implemented as software in the form of computer executable instructions stored on a tangible computer readable medium, which can be executed by the microprocessor 316 and/or as logic circuitry incorporated into the I/F Chip 318. In some implementations, the functionality of each module described below is designed to increase the amount of the functionality that can be implemented in integrated circuit logic, such as an ASIC, in some cases substantially eliminating or eliminating altogether the need for the microprocessor 316.

[0079] The control logic 400 includes input logic 402, subfield derivation logic 404, subframe generation logic 406, saturation compensation logic 408, and output logic 410. Generally, the input logic 402 receives input images for display. The subfield derivation logic 404 converts the received image frames into color subfields. The subframe generation logic 406 converts color subfields into a series of subframes that can be directly loaded into an array of display elements, such as the display elements 310 shown in Figure 3. The saturation compensation logic 408 evaluates the contents of a received image frame and provides image saturation-based conversion parameters to the subfield derivation logic 404 and the subfield generation logic 406 (as discussed further in relation to Figure 6). The output logic 410 controls the loading of the generated subframes into an array of display elements, such as the display elements 310 shown in Figure 3, and controls the illumination of a backlight, such as the backlight 314, also shown in Figure 3, to illuminate and display the subframes. While shown as separate functional modules in Figure 4, in some implementations, the functionality of two or more of the modules may be combined into one or more larger, more comprehensive modules, or divided into smaller, more discrete modules. Together the components of the control logic 400 function to carry out a method for generating an image on a display.

[0080] Figure 5 shows a flow diagram of an example process 500 for generating an image on a display using the control logic 400 shown in Figure 4. The process 500 includes receiving an image frame (stage 502), mapping the received image frame to the XYZ color space (stage 504), decomposing the image frame from the XYZ color space into red (R), green (G), blue (B), and white (W) color subfields (stage 506), dithering the image frame (stage 508), generating subframes for each of the color subfields (stage 510), and displaying the subframes to output the image (stage 512). In some implementations, the process 500 displays images without the use of the saturation compensation logic 408. A process using the saturation compensation logic 408 is shown in Figure 6.

[0081] Referring to Figures 4 and 5, the process 500 includes the input logic 402 receiving data associated with an image frame (stage 502). Typically, such image data is obtained as a stream of intensity values for the red, green, and blue components of each pixel in the image frame. The intensity values typically are received as binary numbers. The received data is stored as an input set of RGB color subfields. Each color subfield includes for each pixel in the display an intensity value indicating the amount of light to be transmitted by that pixel, for that color, to form the image frame. In some implementations, the input logic 402 and/or the subfield derivation logic 404 derives the input set of component color subfields by segregating the pixel intensity values for each primary color represented in the received image data (typically red, green, and blue) into respective subfields. In some implementations, one or more image pre-processing operations, such as gamma correction and dithering, also may be carried out by the input logic 402 and/or the subfield derivation logic 404 prior to, or in the process of, deriving the input set of color subfields.

[0082] The subfield derivation logic 404 converts the input set of color subfields into the XYZ color space (stage 504). To expedite the conversion process, the subfield derivation logic can employ a three-dimensional LUT, in which the intensity values of the respective input color subfields serve as the index into the LUT. Each triplet of {R,G,B} intensity values is mapped to a corresponding vector in the XYZ color space. The LUT is referred to as a RGB \rightarrow XYZ LUT 514. The RGB \rightarrow XYZ LUT 514 can be stored in memory incorporated into the control logic 400, or it can be stored in memory external to, but accessible by, the control logic 400. In some implementations, the subfield derivation logic 404 can separately calculate XYZ tristimulus values for each

pixel using a conversion matrix matched to the color gamut used to encode the image frame.

[0083] The subfield derivation logic 404 converts the pixel values in the XYZ tristimulus color space into red (R), green (G), blue (B), and white (W) subfields (or RGBW subfields) (stage 506). The subfield derivation logic applies a decomposition matrix M, which is defined as follows:

$$M = \begin{bmatrix} X_r^{\text{subfield}} & X_g^{\text{subfield}} & X_b^{\text{subfield}} & X_w^{\text{subfield}} \\ Y_r^{\text{subfield}} & Y_g^{\text{subfield}} & Y_b^{\text{subfield}} & Y_w^{\text{subfield}} \\ Z_r^{\text{subfield}} & Z_g^{\text{subfield}} & Z_b^{\text{subfield}} & Z_w^{\text{subfield}} \end{bmatrix},$$

where X_r^{subfield} , Y_r^{subfield} , and Z_r^{subfield} correspond to the XYZ tristimulus values of the color of the light used to illuminate subframes associated with the red subfield, X_g^{subfield} , Y_g^{subfield} , and Z_g^{subfield} correspond to the XYZ tristimulus values of the color of the light used to illuminate subframes associated with the green subfield, X_b^{subfield} , Y_b^{subfield} , and Z_b^{subfield} correspond to the XYZ tristimulus values of the color of the light used to illuminate subframes associated with the blue subfield, and X_w^{subfield} , Y_w^{subfield} , and Z_w^{subfield} correspond to the XYZ tristimulus values of the color of the light used to illuminate subframes associated with the white subfield.

Each pixel value in the RGBW space is equal to:

$$\begin{bmatrix} R \\ G \\ B \\ W \end{bmatrix} = f \left\{ \begin{bmatrix} X \\ Y \\ Z \end{bmatrix}, M \right\},$$

where f is some decomposition procedure involving the decomposition matrix M and the desired tristimulus value XYZ.

[0084] In some implementations, instead of applying a decomposition matrix, the subfield derivation logic 404 utilizes a XYZ→RGBW LUT 516, which is stored by or is accessible by the subfield derivation logic 404. The XYZ→RGBW LUT 516 maps each XYZ tristimulus value triplet to a set of RGBW pixel intensity values.

[0085] In some implementations, the control logic 400 displays images using what is referred to as a multi-primary display process. A multi-primary display process utilizes

more than three primary colors to form an image, and the sum of the XYZ tristimulus values of the primary colors equals the display XYZ tristimulus values of the gamut white point. This is in contrast to some other display processes that utilize more than three primary colors in which the sum of the primaries do not equal the white point. For example, in some display processes using red, green, blue, and white color subfields, the red, green, and blue color primaries sum to the display white point of the gamut, and the luminance provided through the white subfield is in addition to that combined luminance. That is if all RGBW primaries were illuminated at full strength, the total illumination would have twice the luminance of the gamut white point. As such, in some implementations, the XYZ values referred to above for each of the display primaries, red, green, blue and white, sum up to XYZ tristimulus values of the white point of the gamut being displayed.

[0086] In some implementations, the display outputs an image (stage 512) using a different number of subframes for each subfield. As such, the pixel intensity values within the RGBW subfields are adjusted such that the values can be displayed with the respective allocated number of subframes for each subfield. Such adjustments can introduce quantization errors which can reduce image quality. The subfield derivation logic 404 executes a dithering process to mitigate such quantization errors (stage 508).

[0087] In some implementations, each RGBW subfield is dithered separately in the RGBW color space. In some other implementations, the RGBW subfields are collectively processed by a vector error diffusion-based dithering algorithm. In some implementations, such vector error diffusion-based dithering is carried out in the XYZ color space. In some implementations, therefore, the dithering is carried out prior to conversion of the XYZ pixel values into the RGBW subfields. In vector error diffusion, since errors are diffused in the XYZ space, errors with respect to any one color can be diffused across all colors through direct adjustment to chromaticity or luminance values of the pixels. In contrast, dithering in the RGB or RGBW color space diffuses error in a color across other pixels within the same color subfield. In some implementations, the dithering (stage 508) and the conversion of the image frame into RGBW subfields (stage 506) can be combined into a unified process.

[0088] Referring back to Figures 4 and 5, the subframe generation logic 406 processes the RGBW subfields to generate sets of subframes (stage 510). Each subframe corresponds to a particular time slot in a time division gray scale image output

sequence. It includes a desired state of each display element in the display for that time slot. In each time slot, a display element can take either a non-transmissive state or one or more states that allow for varying degrees of light transmission. In some implementations, the generated subframes include a distinct state value for each display element in the array of display elements 310 shown in Figure 3.

[0089] In some implementations, the subframe generation logic 406 uses a code word LUT to generate the subframes (stage 510). In some implementations, the code word LUT stores a series of binary values referred to as code words that indicate corresponding series of display element states that result in given pixel intensity values. The value of each digit in the code word indicates a display element state (for example, light or dark, or open or close) and the position of the digit in the code word represents the weight that is to be attributed to the state. In some implementations, the weights are assigned to each digit in the code word such that each digit is assigned a weight that is twice the weight of a preceding digit. In some other implementations, multiple digits of a code word may be assigned the same weight. In some other implementations, each digit is assigned a different weight, but the weights may not all increase according to a fixed pattern, digit to digit.

[0090] To generate a set of subframes (stage 510), the subframe generation logic 406 obtains code words for all pixels in a color subfield. The subframe generation logic 406 can aggregate the digits in each of the respective positions in the code words for the set of pixels in the subfield together into subframes. For example, the digits in the first position of each code word for each pixel are aggregated into a first subframe. The digits in the second position of each code word for each pixel are aggregated into a second subframe, and so forth. The subframes, once generated, are stored in the frame buffer 308 shown in Figure 3.

[0091] In some other implementations, for example in implementations using light modulators capable of achieving one or more partially transmissive states, the code word LUT may store code words using base-3, base-4, base-10, or some other base number scheme.

[0092] The output logic 410 of the control logic 400 (shown in Figure 4) can output the generated subframes to display the received image frame (stage 512). Similar to as described above in relation to Figure 3 with respect to the I/F chip 318, the output logic

410 causes each subframe to be loaded into the array of display elements 310 (shown in Figure 3) and to be illuminated according to an output sequence. In some implementations, the output sequence is capable of being configured, and may be modified based on user preferences, the content of image data being displayed, external environmental factors, etc.

[0093] By displaying some amount of image luminance through a white subfield, which can be illuminated by a higher efficiency white light source, such as white LEDs (which tend to be more power efficient than red, green, or blue LEDs), the process 500 can improve the energy efficiency of a display. Given that the process 500 uses a single set of tristimulus values for each of the subfields being display, the process is computationally efficient, but image quality may be reduced when reproducing certain images. In some implementations, energy efficiency also may suffer. For example, assuming a non-negligible portion of image luminance is pushed to the white subfield, images with highly saturated colors may appear washed out.

[0094] Figure 6 shows a flow diagram of another example process 600 for generating an image on a display using the control logic 400 shown in Figure 4. The process 600 utilizes the saturation compensation logic 408 to mitigate the image quality issues that can arise with the display process 500 depicted in Figure 5. More particularly, the process 600 adjusts the manner in which input pixel values are converted to the XYZ color space and the manner in which pixel values in the XYZ color space are converted into pixel values in RGBW subfields based on a saturation metric, Q, which can be determined, in some implementations, for each image frame. In some implementations, such as for video images, a single Q value can be determined based on a first image frame in a scene and can be used for subsequent image frames until a scene change is detected. The process 600 includes receiving an image frame in the RGB color space (stage 602), determining a saturation factor, Q, for the image frame (stage 604), mapping the pixel values in the image frame to the XYZ color space based on Q (stage 606), decomposing the image frame in the XYZ color space into RGBW subfields (stage 608), dithering the image frame (stage 610), generating RGBW subframes (stage 612) and outputting the subframes to display the image (stage 614).

[0095] The process 600 includes receiving an image frame in the RGB color space (stage 602) in the form of a stream of RGB pixel values as described above in relation to stage 502 shown in Figure 5. As described with respect to stage 502, stage 602 can

include pre-processing the pixel values and storing the results in a set of input RGB color subfields.

[0096] The saturation compensation logic 408 shown in Figure 4 processes the image frame to determine a saturation factor Q for the image frame (stage 604). The Q parameter corresponds to the relative size of the output color gamut to the input color gamut. Viewed another way, Q represents the degree to which an image's luminance will be output by the display through the white subfield, relative to the red, green, and blue subfields. In general, as the Q value increases, the size of the color gamut output by the display shrinks. The shrinkage can be the result of the intensities of the subfield colors being reduced while their chromaticities remain fixed. For example, a Q value of 1.0 corresponds to a black and white image, as all display luminance is output in the white subfield. A Q value of 0.0 corresponds to a fully saturated color gamut formed purely by red, green, and blue color fields, without any luminance being transferred to a white subfield. Images including highly saturated colors can be more faithfully represented with low values of Q, whereas as images with large amounts of white content (for example, word processing documents and many web pages) can be displayed with higher values of Q without a perceptually significant decrease in quality, and while obtaining significant power savings. Accordingly Q is selected to be large for images that include largely unsaturated colors, whereas low Q values are selected for images that include highly saturated colors. In some implementations, the Q value can be obtained by taking histogram data associated with the input pixel values and using some or all of the histogram data as an index into a Q value LUT. In some implementations, the set of input RGB color subfields are analyzed to determine the maximum white intensity value that can be extracted from all pixels in the image frame without introducing color error. In some such implementations, Q is calculated as follows:

$$Q = \frac{\text{Min}_{\text{all pixels}}(\text{Min}_{\text{pixel}}(R, G, B))}{\text{MaxIntensity}},$$

where MaxIntensity corresponds to the maximum intensity value possible in a subfield (such as 255 in an 8-bit subfield).

[0097] In some other implementations, Q can be calculated in the XYZ color space. In such implementations, Q_s can be determined by identifying the size of a minimum bounding hexagon which can enclose all XYZ pixel values included in input image

projected to a common plane normal to an XYZ color space central axis connecting the XYZ values of black (at the origin) and pure white (such as XYZ values of 0.9502, 1.0, 1.0884). Q is set equal to the difference between 1.0 and the ratio of the size of the bounding hexagon and the hexagon that would result from capturing the full display color gamut (such as the sRGB, Adobe RGB color gamut, or the rec.2020 color gamut).

[0098] Based on the determined Q value, the pixel values stored in the input set of RGB color subfields are mapped to the XYZ color space (stage 606). As indicated above, as more image luminance is output through a white subfield as Q increases, rather than through the red, green, and blue subfields, the gamut of the output image is decreased. To maintain image quality, i.e., to maintain an appropriate color balance given the selected saturation level, pixel values are converted to the XYZ color space using gamut mapping algorithms tailored to the reduced output gamuts.

[0099] In some implementations, RGB values can be converted to the XYZ color space by multiplying a set of RGB pixel values by a Q-dependent color transform matrix. In some other implementations, to increase the speed of the conversion, three-dimensional Q-dependent RGB \rightarrow XYZ LUTs can be stored by (or may be accessible by) the saturation compensation logic 408, indexed by {R,G,B} triplet values. Storing a large number of such LUTs, may, for some implementations, become prohibitive from a memory capacity standpoint. To ameliorate the memory capacity concerns associated with storing a large number of Q-dependent RGB->XYZ LUTs, the saturation compensation logic 408 may store a relatively small number of Q-dependent RGB->XYZ LUTs, and use interpolation between the LUTs for Q values other than those associated with the stored LUTs.

[0100] Figure 6 shows one such implementation. The process 600 shown in Figure 6 utilizes two Q-dependent RGB \rightarrow XYZ LUTs, i.e., a Q_{\min} LUT 616 and a Q_{\max} LUT 618. The Q_{\min} LUT 616 is a RGB \rightarrow XYZ LUTs based on the lowest value of Q used by the control logic 400. The Q_{\max} LUT 618 is a RGB \rightarrow XYZ LUTs based on the highest value of Q used by the control logic 400. In some implementations, the minimum Q value ranges from about 0.01 to about 0.2, and the maximum Q value ranges from about 0.4 to about 0.8. In some implementations, the maximum Q value can range up to 1.0. In some implementations, more than two Q-dependent RGB \rightarrow XYZ LUTs can be employed for more accurate interpolation. For example, in some implementations, the process 600 can use RGB \rightarrow XYZ LUTs for Q values of 0.0, 0.5, and 1.0.

[0101] To carry out the interpolation, the saturation compensation logic 408 can calculate a scaling factor α , as follows:

$$\alpha = \frac{Q_{MAX} - Q}{Q_{MAX} - Q_{MIN}}$$

[0102] As the XYZ color space is linear, the XYZ tristimulus values for any RGB input pixel value with any Q values between Q_{min} and Q_{max} can be calculated to be equal to:

$$\alpha LUT_{Q-min}(RGB) + (1 - \alpha) LUT_{Q-max}(RGB),$$

where LUT(RGB) represents the output of an LUT for a given RGB input pixel value.

In some implementations, instead of carrying out two lookup functions for each pixel value, the saturation compensation logic 408 generates a new RGB \rightarrow XYZ LUTs for each image frame (or each time Q changes between image frames), combining the Q_{min} LUT and a Q_{max} LUT according to a similar equation for determining the XYZ tristimulus values for a given RGB input pixel value. That is:

$$LUT_Q = \alpha LUT_{Q-min} + (1 - \alpha) LUT_{Qmax}.$$

[0103] Once the image pixel values are in the XYZ tristimulus space, the subfield derivation logic 404 decomposes the pixel values into a set of RGBW color subfields (stage 608). Similar to the pixel decomposition stage (stage 506) shown in Figure 5, in stage 608, the subfield derivation logic 404 decomposes each pixel value using a decomposition matrix. In stage 608, however, the subfield derivation logic 404 uses a Q-dependent decomposition matrix M_Q . The Q-dependent decomposition matrix, M_Q , has the same form as the decomposition matrix M, other than the XYZ values associated with each subfield vary based on the value of Q selected.

[0104] In some implementations, the saturation compensation logic 408 stores, or has access to, a set of decomposition matrices for a large range of Q values. In some other implementations, to save memory, as with the RGB \rightarrow XYZ LUTs, the control logic 400 can store or access a more limited set of decomposition matrices, M_Q , with matrices for other values being calculated via interpolation. For example, the control logic may store or access a first decomposition matrix, M_{Q-min} 620 and a second decomposition matrix, M_{Q-max} 622. Decomposition matrices for values of Q between Q_{min} and Q_{max} can be calculated as follows:

$$M_Q = \alpha M_{Q-min} + (1 - \alpha) M_{Q-max}.$$

[0105] In some other implementations, instead of using a Q-dependent decomposition matrix in stage 608, the subfield derivation logic 404 instead utilizes a Q-dependent XYZ→RGBW LUT. As with the Q-dependent RGB→XYZ LUTs, the subfield derivation logic 404 can store or have access to a limited number of Q-dependent XYZ→RGBW LUTs. The subfield derivation logic 404 can then generate a frame-specific XYZ→RGBW LUT for the image frame based on its corresponding Q value through a similar interpolation process used to generate a Q-specific RGB→XYZ LUT.

[0106] In some other implementations, a LUT may not be used at all, and the XYZ to RGBW decomposition is derived directly first multiplying the XYZ pixel values by a matrix M' to obtain virtual primaries R' G' B' that enclose the display gamut for all Q. This matrix M' corresponds to M_{Q=0}, since the gamut for Q=0 encloses the gamut obtained for all Q>0. Intensity values for R,G,B and W are then obtained by calculating:

$$W = \min \left\{ \min \left\{ \frac{1-Q}{Q} (R', G', B') \right\}, 1 \right\}, \text{ and}$$

$$R, G, B = R', G', B' - \frac{1-Q}{Q} W.$$

[0107] The display process dithers the results of the pixel decomposition stage (stage 610) and generates a set of RGBW subframes from the results of the dithering (stage 612). The dithering stage (stage 610) and the subframe generation stage (stage 612) can be identical to the corresponding processing stages (stages 508 and 510) in the process 500 discussed in relation to Figure 5.

[0108] The generated RGBW subframes are output to display an image (stage 614). In contrast to the output stage 512 shown in Figure 5, the subframe output stage (stage 614) includes a light source intensity calculation process to adjust the intensities of the light sources based on the value of Q selected for the image frame. As indicated above, the selection of Q results in a modification to the display gamut, as such the light source intensities for each of the RGB subfields are adjusted to be less saturated as Q increases and the intensity of the white light source for the white subfield is increased as Q increases. In some implementations, the light source intensities are scaled linearly based on the value of Q. For example, with a Q of 0.5, the light source intensity values for each non-white subfield are multiplied by 0.5. If Q were 0.2, the light source intensity values for each non-white subfield would be multiplied by 0.8, and so forth. In

some implementations, the light source intensity calculation can be carried out earlier in the process 600.

[0109] Figure 7 shows a flow diagram of an example process 700 of forming an image on a display. The process 700 includes receiving an input image frame encoded in a first color space, in which the input image frame includes, for each of a plurality of pixels, a set of color intensity values (stage 702). Examples of such processing stages are discussed above as stages 502 and 602 shown in Figures 5 and 6, respectively. The process 700 includes applying a gamut mapping process to the color intensity values associated with the plurality of pixels in the received input image frame to convert the color intensity values associated with the respective pixels into corresponding tristimulus values in the XYZ color space (stage 704). Examples of this processing stage are discussed above as stages 504 and 606, also shown in Figures 5 and 6. The process 700 further includes decomposing the XYZ tristimulus values associated with the plurality of pixels to form respective color subfields associated with at least four different colors (stage 706). Each color subfield includes intensity values for a corresponding color for respective pixels from the input image. Examples of the processing stage 706 are discussed above in relation to stages 506 and 608 shown in Figures 5 and 6. Display element state information is generated for display elements in an array of display elements based on the color subfields (stage 708). The display element state information can include, in some implementations, subframes. Examples of generating subframes are discussed in relation to stages 510 and 612. The process 700 further includes outputting display element state information associated with the at least four color subfields to the array of display elements to form an image (stage 710). Examples of the processing stage 710 are described above in relation to stages 512 and 614, shown in Figures 5 and 6, respectively.

[0110] The process 700 is described above with respect to processing an entire image frame. A similar process can be implemented for segmented displays. In a segmented display, a backlight is divided into a set of independently controlled segments. As such, an image frame can be broken down into image frame segments. The image data corresponding to different segments can be broken down into subfields of different chromaticities and/or brightness levels. In some implementations, for a segmented display, the process 700 shown in Figure 7 is adapted such that each segment of an image frame is processed according to its own Q value. In some implementations, the

Q value for a segment is calculated independently from that of any other segment, treating the data associated with that segment as a distinct image frame using the process discussed above in relation to stage 604, shown in Figure 6. In some other implementations, Q values for the segments are determined collectively to ensure that the Q values of two adjacent segments do not differ too greatly from one another, thereby avoiding image artifacts that might result from a rapid change in color saturation between two adjacent segments. The collective Q value determination for the segments can be implemented using various constraint-based optimization algorithms known to a person of ordinary skill in the art.

[0111] Displays that vary the saturation level they employ in forming images by transferring image data into a white color subfield as described above can implement power management features that help extend battery life. For any given image, there exists a “lossless” or substantially lossless Q value, Q_{opt} , which corresponds to a level of image data that can be transferred to the white subfield without unduly impacting color fidelity. In some implementations, Q_{opt} corresponds to a Q value that introduces an amount of average color error into an output image that is approximately equal to a threshold color error beyond which the color error becomes noticeable to the human visual system (i.e., an acceptably low loss). As more data is presented through the white color subfield, which is illuminated by a higher efficiency white light source, the power consumption of the display decreases. At the extreme, outputting an image in black and white with a Q value of 1.0 saves the maximum amount of power, as non-white light sources need not be illuminated at all. Power also can be saved by forgoing addressing the display with subframes corresponding to the non-white subfields.

[0112] Figure 8 shows a flow diagram of an example process 800 of reducing power consumption in a display. In the process 800, the power savings possible through varying saturation level by varying the value of Q used to display an image can be leveraged to provide a de-saturation based time out function for a display. That is, instead of a display dimming, and then shutting off after periods of time of inactivity as many current smartphones and tablet displays are configured to do, a display can progressively reduce its saturation level (by increasing the Q value) in response to such inactivity.

[0113] The process can include displaying images using Q_{opt} (stage 802). While activity, such as an interaction with the display device or a host device incorporating the

display device, is detected (decision block 804), the display device resets an inactivity period timer (stage 806) and displays images using Q_{opt} (stage 802). If no activity is detected (decision block 804) an inactivity period timer is incremented (stage 808). If the inactivity period timer remains below a first threshold $T1$ (decision block 810), the process 800 continues to display images using Q_{opt} (stage 802). If the inactivity period timer exceeds $T1$ but remains below a second threshold $T2$ (decision block 812), the display device displays images at an increased value of Q , Q_{high} (stage 814). Q_{high} can be a function of Q_{opt} , such as a multiple of Q_{opt} , or it can be a fixed higher Q value, such as a value between about 0.6 and about 0.8. If the inactivity period timer exceeds $T1$, the display outputs images in black and white using a Q value of 1.0 (stage 816). In some implementations, the display device transitions directly to displaying images using the 1.0 Q value. In some implementations, the display device smoothly transitions from using the Q_{high} value to a 1.0 Q value over a series of frames. The display continues to output images using a Q value of 1.0 until activity is detected at decision block 804. That is, upon a user re-engaging with the device incorporating the display, the inactivity period can be reset (stage 806) and the display can return to outputting images using the lossless (or the acceptably low loss) Q value, i.e., Q_{opt} (stage 802).

[0114] Figure 9 shows a flow diagram of a second example process 900 of reducing power consumption in a display. The process 900 adjusts the value of Q used to display an image based on a remaining battery level of a host device in which the display is included. The process 900 includes displaying images using Q_{opt} (stage 902). The process 900 checks the host device battery level (904) and compares the battery level to a first threshold $P1$, such as 25% of the battery life remaining (decision block 906). If the battery level is above $P1$, the display device continues to display images using Q_{opt} (stage 902). If the battery level is between $P1$ and a second threshold $P2$ (decision block 907), such as about 5% of the battery life remaining, the display displays images using a Q value that is scaled relative to the remaining battery life, referred to as Q_{scaled} (stage 908). For example, while the battery has between about 25% and about 5% of its life remaining, the display device can output images using a Q value that is determined via a linear interpolation (or other suitable ramping function) between two Q values, such as about 0.25, and about 1.0. If the battery life falls below $P2$ (decision block 909), the display outputs images in black and white, using a Q value of 1.0 (stage 910). In the

above example, the threshold percentages are merely illustrative in nature and other percentage thresholds can be used in other implementations.

[0115] Figure 10 shows a flow diagram of an example process 1000 of a display outputting images using a Q value that is selected in part based on a desired power consumption target. For some electronic devices, it is desirable to be able to identify an average power consumption level for a display included in the device so that a given battery life can be guaranteed. For displays whose power consumption is heavily dependent on the content of the images being displayed, providing an accurate power consumption level can be challenging. The process 1000 shown in Figure 10 allows a display device to adjust the Q value it uses to display images (and therefore adjust its power consumption) in order to meet a desired or specified power consumption target.

[0116] The process 1000 includes receiving an image frame (stage 1002) and determining Q_{opt} (stage 1004). The display device compares the difference between the average Q value it had been using to display images in the past, Q_{avg} , to a Q value, Q_{target} , that corresponds to the specified power consumption target. If the absolute value of that difference falls below a threshold (decision block 1006), the display device outputs the image using the Q_{opt} value determined for the image (stage 1008), updates Q_{avg} (stage 1010), and processes the next image frame. If the absolute value of the difference exceeds the threshold (decision block 1006), the display device determines if Q_{avg} is greater than Q_{target} (decision block 1012). If Q_{avg} is less than Q_{target} , then the image is displayed with an increased value of Q (stage 1014), Q_{avg} is updated (stage 1010), and a next image frame is received (stage 1002). In some implementations, the increased value of Q is selected to be greater than Q_{target} to begin moving Q_{avg} closer to Q_{target} . In some implementations, a limit is placed on the amount Q is increased above Q_{opt} to avoid excessive deterioration in image fidelity. If Q_{avg} is greater than Q_{target} the image can be displayed with Q_{opt} . The display updates Q_{avg} (stage 1010) and processes the next image frame upon receipt (stage 1002).

[0117] In some implementations of the process 1000, Q_{opt} can be selected based on data other than the color content of the image being displayed. For example, Q_{opt} can be selected based on an application or content type associated with an image in conjunction with a selected battery life setting. For example, in general, images output by word processing or e-reader applications can be displayed using relatively high Q values without much deterioration in image fidelity, whereas images generated by photography

or video applications often suffer from image deterioration when output with higher Q values. The battery life settings can be adjusted, for example, by a graphical user interface provided by the display device or by a host device in which the display device is incorporated.

[0118] In such implementations, the display apparatus can maintain a two dimensional LUT. The LUT is keyed to the application or content type of the image and to possible battery life settings. The LUT stores a corresponding Q value for each application/content type-battery life setting. An example of such a LUT is shown below as Table 1.

	User Selected Battery Life Setting			
	Maximize Color Performance	5 Hours	10 Hours	Maximize Battery Life
<u>Application</u>				
Photo Gallery	$Q = Q_{opt}$	$Q = Q_{opt}$	$Q = 0.5$	$Q = 0.8$
Video Player	$Q = Q_{opt}$	$Q = Q_{opt}$	$Q = 0.8$	$Q = 0.8$
Word Game	$Q = Q_{opt}$	$Q = 0.5$	$Q = 0.8$	$Q = 1$
Email Client	$Q = Q_{opt}$	$Q = 0.8$	$Q = 0.9$	$Q = 1$
eReader	$Q = Q_{opt}$	$Q = 0.9$	$Q = 1$	$Q = 1$

TABLE 1

[0119] As shown in Table 1, Q values for each application generally increase as the desired battery life setting increases. In some implementations, Q_{target} can also be varied based on the battery life setting. In some such implementations, the Q values in the above table can be constant for all battery life settings.

[0120] In some implementations of the processes 800, 900, and 1000 shown in Figures 8–10, one or more additional power management features may be implemented. For example, in some implementations, as the battery level of a display apparatus decreases over time, in addition to the saturation level changes discussed above, the control logic (such as the control logic 306 shown in Figure 3) of a display apparatus can reduce the number of subframes the display apparatus uses to output each image frame. Reducing the number of subframes reduces the amount of power consumed by reducing the amount of power expended in loading data into the display for the subframes that will no longer be displayed. It also allows the remaining subframes that are displayed to be illuminated for longer at a lower intensity, allowing the display light sources to operate more efficiently.

[0121] For example, at full power, the display apparatus may display an image frame using between four and eight subframes for each of the red, green, and blue color subfields and using between three and five subframes for the white color subfield. As the battery level decreases, the display apparatus can reduce the number of red, green, and blue subfields used to between three and five -- unless the display switches to a monochrome mode, as discussed in relation to stages 816 and 910 in Figures 8 and 9, in which case, the display does not output any red, green, or blue subframes at all. In some implementations, the same number of white subframes can be displayed regardless of battery level. In some implementations, the number of subframes used to display the white color subfield can increase as Q increases. In some implementations, the number of subframes used to display the red, green, and blue subfields can be generally inversely proportional to the value of Q used to display the image frame, regardless of the battery level of the display apparatus.

[0122] In some implementations, when the number of subframes used to display an image frame is reduced, the control logic causes the display to omit display of lower weighted subframes before omitting higher weighted subframes. In some other implementations, the control logic can implement different subframe weighting schemes for a color subfield depending on the number of subframes used to display the color subfield. In addition, the control logic may implement additional or different dithering operations in response to a reduction in the number of subframes used to display a color subfield to account for quantization errors the reduction might introduce.

[0123] In some implementations in which fewer subframes are displayed responsive to a decrease in display apparatus battery level, additional power savings can be obtained by selectively powering down portions of the display apparatus's frame buffer when fewer subframes are used, as less image data needs to be stored. When the display is operated in monochrome mode, additional display hardware can be powered down to save additional power. For example, the drivers and logic associated with the red, green, and blue light sources can be powered down, if they will not be used for a given image frame.

[0124] In some implementations, the control logic can be capable of adjusting the complexity of the image processing operations it executes based on the battery level of the display apparatus. For example, the control logic can vary the number of pixels in an image frame it takes into account during its dithering operations. To determine a

value of a pixel, a dithering algorithm takes into account the values of pixels within a configurable distance around the pixel in question. For example, a dithering algorithm may take into account only the values of immediately adjacent pixels, or it may take into account the values of all pixels two, three, four, or more pixels away. A dithering process that takes into account a greater number of pixels requires more processor cycles to execute than a process that takes into account fewer pixels. As such, the control logic can be configured, responsive to a decrease in battery level, to reduce the number of pixels it takes into account in its dithering operations to reduce the number of processor cycles needed to complete the operation, thereby saving power.

[0125] While the above power management techniques are described above for use in conjunction with the processes 800, 900, and 1000 shown in Figures 8–10, in some implementations, a display controller can employ these techniques independently of such processes.

[0126] Figures 11A and 11B show system block diagrams of an example display device 40 that includes a plurality of display elements. The display device 40 can be, for example, a smart phone, a cellular or mobile telephone. However, the same components of the display device 40 or slight variations thereof are also illustrative of various types of display devices such as televisions, computers, tablets, e-readers, hand-held devices and portable media devices.

[0127] The display device 40 includes a housing 41, a display 30, an antenna 43, a speaker 45, an input device 48 and a microphone 46. The housing 41 can be formed from any of a variety of manufacturing processes, including injection molding, and vacuum forming. In addition, the housing 41 may be made from any of a variety of materials, including, but not limited to: plastic, metal, glass, rubber and ceramic, or a combination thereof. The housing 41 can include removable portions (not shown) that may be interchanged with other removable portions of different color, or containing different logos, pictures, or symbols.

[0128] The display 30 may be any of a variety of displays, including a bi-stable or analog display, as described herein. The display 30 also can be capable of including a flat-panel display, such as plasma, electroluminescent (EL) displays, OLED, super twisted nematic (STN) display, LCD, or thin-film transistor (TFT) LCD, or a non-flat-

panel display, such as a cathode ray tube (CRT) or other tube device. In addition, the display 30 can include a mechanical light modulator-based display, as described herein.

[0129] The components of the display device 40 are schematically illustrated in Figure 11B. The display device 40 includes a housing 41 and can include additional components at least partially enclosed therein. For example, the display device 40 includes a network interface 27 that includes an antenna 43 which can be coupled to a transceiver 47. The network interface 27 may be a source for image data that could be displayed on the display device 40. Accordingly, the network interface 27 is one example of an image source module, but the processor 21 and the input device 48 also may serve as an image source module. The transceiver 47 is connected to a processor 21, which is connected to conditioning hardware 52. The conditioning hardware 52 may be configured to condition a signal (such as filter or otherwise manipulate a signal). The conditioning hardware 52 can be connected to a speaker 45 and a microphone 46. The processor 21 also can be connected to an input device 48 and a driver controller 29. The driver controller 29 can be coupled to a frame buffer 28, and to an array driver 22, which in turn can be coupled to a display array 30. One or more elements in the display device 40, including elements not specifically depicted in Figure 11A, can be capable of functioning as a memory device and be capable of communicating with the processor 21. In some implementations, a power supply 50 can provide power to substantially all components in the particular display device 40 design.

[0130] The network interface 27 includes the antenna 43 and the transceiver 47 so that the display device 40 can communicate with one or more devices over a network. The network interface 27 also may have some processing capabilities to relieve, for example, data processing requirements of the processor 21. The antenna 43 can transmit and receive signals. In some implementations, the antenna 43 transmits and receives RF signals according to any of the IEEE 16.11 standards, or any of the IEEE 802.11 standards. In some other implementations, the antenna 43 transmits and receives RF signals according to the Bluetooth® standard. In the case of a cellular telephone, the antenna 43 can be designed to receive code division multiple access (CDMA), frequency division multiple access (FDMA), time division multiple access (TDMA), Global System for Mobile communications (GSM), GSM/General Packet Radio Service (GPRS), Enhanced Data GSM Environment (EDGE), Terrestrial Trunked Radio (TETRA), Wideband-CDMA (W-CDMA), Evolution Data Optimized (EV-DO), 1xEV-

DO, EV-DO Rev A, EV-DO Rev B, High Speed Packet Access (HSPA), High Speed Downlink Packet Access (HSDPA), High Speed Uplink Packet Access (HSUPA), Evolved High Speed Packet Access (HSPA+), Long Term Evolution (LTE), AMPS, or other known signals that are used to communicate within a wireless network, such as a system utilizing 3G, 4G or 5G, or further implementations thereof, technology. The transceiver 47 can pre-process the signals received from the antenna 43 so that they may be received by and further manipulated by the processor 21. The transceiver 47 also can process signals received from the processor 21 so that they may be transmitted from the display device 40 via the antenna 43.

[0131] In some implementations, the transceiver 47 can be replaced by a receiver. In addition, in some implementations, the network interface 27 can be replaced by an image source, which can store or generate image data to be sent to the processor 21. The processor 21 can control the overall operation of the display device 40. The processor 21 receives data, such as compressed image data from the network interface 27 or an image source, and processes the data into raw image data or into a format that can be readily processed into raw image data. The processor 21 can send the processed data to the driver controller 29 or to the frame buffer 28 for storage. Raw data typically refers to the information that identifies the image characteristics at each location within an image. For example, such image characteristics can include color, saturation and gray-scale level.

[0132] The processor 21 can include a microcontroller, CPU, or logic unit to control operation of the display device 40. The conditioning hardware 52 may include amplifiers and filters for transmitting signals to the speaker 45, and for receiving signals from the microphone 46. The conditioning hardware 52 may be discrete components within the display device 40, or may be incorporated within the processor 21 or other components.

[0133] The driver controller 29 can take the raw image data generated by the processor 21 either directly from the processor 21 or from the frame buffer 28 and can re-format the raw image data appropriately for high speed transmission to the array driver 22. In some implementations, the driver controller 29 can re-format the raw image data into a data flow having a raster-like format, such that it has a time order suitable for scanning across the display array 30. Then the driver controller 29 sends the formatted information to the array driver 22. Although a driver controller 29 is

often associated with the system processor 21 as a stand-alone Integrated Circuit (IC), such controllers may be implemented in many ways. For example, controllers may be embedded in the processor 21 as hardware, embedded in the processor 21 as software, or fully integrated in hardware with the array driver 22.

[0134] The array driver 22 can receive the formatted information from the driver controller 29 and can re-format the video data into a parallel set of waveforms that are applied many times per second to the hundreds, and sometimes thousands (or more), of leads coming from the display's x-y matrix of display elements. In some implementations, the array driver 22 and the display array 30 are a part of a display module. In some implementations, the driver controller 29, the array driver 22, and the display array 30 are a part of the display module.

[0135] In some implementations, the driver controller 29, the array driver 22, and the display array 30 are appropriate for any of the types of displays described herein. For example, the driver controller 29 can be a conventional display controller or a bi-stable display controller (such as a mechanical light modulator display element controller). Additionally, the array driver 22 can be a conventional driver or a bi-stable display driver (such as a mechanical light modulator display element controller). Moreover, the display array 30 can be a conventional display array or a bi-stable display array (such as a display including an array of mechanical light modulator display elements). In some implementations, the driver controller 29 can be integrated with the array driver 22. Such an implementation can be useful in highly integrated systems, for example, mobile phones, portable-electronic devices, watches or small-area displays.

[0136] In some implementations, the input device 48 can be configured to allow, for example, a user to control the operation of the display device 40. The input device 48 can include a keypad, such as a QWERTY keyboard or a telephone keypad, a button, a switch, a rocker, a touch-sensitive screen, a touch-sensitive screen integrated with the display array 30, or a pressure- or heat-sensitive membrane. The microphone 46 can be configured as an input device for the display device 40. In some implementations, voice commands through the microphone 46 can be used for controlling operations of the display device 40. Additionally, in some implementations, voice commands can be used for controlling display parameters and settings.

[0137] The power supply 50 can include a variety of energy storage devices. For example, the power supply 50 can be a rechargeable battery, such as a nickel-cadmium battery or a lithium-ion battery. In implementations using a rechargeable battery, the rechargeable battery may be chargeable using power coming from, for example, a wall socket or a photovoltaic device or array. Alternatively, the rechargeable battery can be wirelessly chargeable. The power supply 50 also can be a renewable energy source, a capacitor, or a solar cell, including a plastic solar cell or solar-cell paint. The power supply 50 also can be configured to receive power from a wall outlet.

[0138] In some implementations, control programmability resides in the driver controller 29 which can be located in several places in the electronic display system. In some other implementations, control programmability resides in the array driver 22. The above-described optimization may be implemented in any number of hardware and/or software components and in various configurations.

[0139] As used herein, a phrase referring to “at least one of” a list of items refers to any combination of those items, including single members. As an example, “at least one of: a, b, or c” is intended to cover: a, b, c, a-b, a-c, b-c, and a-b-c.

[0140] The various illustrative logics, logical blocks, modules, circuits and algorithm processes described in connection with the implementations disclosed herein may be implemented as electronic hardware, computer software, or combinations of both. The interchangeability of hardware and software has been described generally, in terms of functionality, and illustrated in the various illustrative components, blocks, modules, circuits and processes described above. Whether such functionality is implemented in hardware or software depends upon the particular application and design constraints imposed on the overall system.

[0141] The hardware and data processing apparatus used to implement the various illustrative logics, logical blocks, modules and circuits described in connection with the aspects disclosed herein may be implemented or performed with a general purpose single- or multi-chip processor, a digital signal processor (DSP), an application specific integrated circuit (ASIC), a field programmable gate array (FPGA) or other programmable logic device, discrete gate or transistor logic, discrete hardware components, or any combination thereof designed to perform the functions described herein. A general purpose processor may be a microprocessor, or, any conventional

processor, controller, microcontroller, or state machine. A processor also may be implemented as a combination of computing devices, e.g., a combination of a DSP and a microprocessor, a plurality of microprocessors, one or more microprocessors in conjunction with a DSP core, or any other such configuration. In some implementations, particular processes and methods may be performed by circuitry that is specific to a given function.

[0142] In one or more aspects, the functions described may be implemented in hardware, digital electronic circuitry, computer software, firmware, including the structures disclosed in this specification and their structural equivalents thereof, or in any combination thereof. Implementations of the subject matter described in this specification also can be implemented as one or more computer programs, i.e., one or more modules of computer program instructions, encoded on a computer storage media for execution by, or to control the operation of, data processing apparatus.

[0143] If implemented in software, the functions may be stored on or transmitted over as one or more instructions or code on a computer-readable medium. The processes of a method or algorithm disclosed herein may be implemented in a processor-executable software module which may reside on a computer-readable medium. Computer-readable media includes both computer storage media and communication media including any medium that can be enabled to transfer a computer program from one place to another. A storage media may be any available media that may be accessed by a computer. By way of example, and not limitation, such computer-readable media may include RAM, ROM, EEPROM, CD-ROM or other optical disk storage, magnetic disk storage or other magnetic storage devices, or any other medium that may be used to store desired program code in the form of instructions or data structures and that may be accessed by a computer. Also, any connection can be properly termed a computer-readable medium. Disk and disc, as used herein, includes compact disc (CD), laser disc, optical disc, digital versatile disc (DVD), floppy disk, and blu-ray disc where disks usually reproduce data magnetically, while discs reproduce data optically with lasers. Combinations of the above should also be included within the scope of computer-readable media. Additionally, the operations of a method or algorithm may reside as one or any combination or set of codes and instructions on a machine readable medium and computer-readable medium, which may be incorporated into a computer program product.

[0144] Various modifications to the implementations described in this disclosure may be readily apparent to those skilled in the art, and the generic principles defined herein may be applied to other implementations without departing from the spirit or scope of this disclosure. Thus, the claims are not intended to be limited to the implementations shown herein, but are to be accorded the widest scope consistent with this disclosure, the principles and the novel features disclosed herein.

[0145] Additionally, a person having ordinary skill in the art will readily appreciate, the terms “upper” and “lower” are sometimes used for ease of describing the figures, and indicate relative positions corresponding to the orientation of the figure on a properly oriented page, and may not reflect the proper orientation of any device as implemented.

[0146] Certain features that are described in this specification in the context of separate implementations also can be implemented in combination in a single implementation. Conversely, various features that are described in the context of a single implementation also can be implemented in multiple implementations separately or in any suitable subcombination. Moreover, although features may be described above as acting in certain combinations and even initially claimed as such, one or more features from a claimed combination can in some cases be excised from the combination, and the claimed combination may be directed to a subcombination or variation of a subcombination.

[0147] Similarly, while operations are depicted in the drawings in a particular order, this should not be understood as requiring that such operations be performed in the particular order shown or in sequential order, or that all illustrated operations be performed, to achieve desirable results. Further, the drawings may schematically depict one or more example processes in the form of a flow diagram. However, other operations that are not depicted can be incorporated in the example processes that are schematically illustrated. For example, one or more additional operations can be performed before, after, simultaneously, or between any of the illustrated operations. In certain circumstances, multitasking and parallel processing may be advantageous. Moreover, the separation of various system components in the implementations described above should not be understood as requiring such separation in all implementations, and it should be understood that the described program components and systems can generally

be integrated together in a single software product or packaged into multiple software products. Additionally, other implementations are within the scope of the following claims. In some cases, the actions recited in the claims can be performed in a different order and still achieve desirable results.

CLAIMS

What is claimed is:

1. An apparatus comprising:
 - an array of display elements;
 - control logic configured to:
 - receive an input image frame, wherein the input image frame includes, for each of a plurality of pixels, a first set of color parameter values;
 - apply a content adaptive gamut mapping process to the first set of color parameter values associated with the pixel to map the first set of color parameter values to a second set of color parameter values, wherein the content adaptive gamut mapping process is based at least in part on the content of the image frame; and
 - decompose the second set of color parameter values associated with the pixel to obtain pixel intensity values in respective color subfields associated with at least four different colors;
 - generate display element state information for the display elements based on the color subfields; and
 - output display element state information associated with the at least four color subfields to the array of display elements.
2. The apparatus of claim 1, wherein the first set of color parameter values include red, green, and blue pixel intensity values and the second set of color parameter values include XYZ tristimulus values.
3. The apparatus of claim 1, wherein:
 - the control logic is further configured to determine a saturation level parameter for the image and adapt the gamut mapping process based on the determined color saturation parameter of the input image frame.
4. The apparatus of claim 3, wherein the control logic is further configured to adapt the gamut mapping process by generating an image saturation level-dependent gamut mapping lookup table.

5. The apparatus of claim 4, wherein the control logic is further configured to generate the image saturation level-dependent gamut mapping lookup table by interpolating between at least two stored gamut mapping lookup tables based on the determined image saturation parameter.
6. The apparatus of claim 1, wherein the control logic is further configured to decompose the second set of color parameter values associated with the plurality of pixels to form respective color subfields according to a content adaptive image decomposition process.
7. The apparatus of claim 6, wherein:
 - the control logic is further configured to determine a saturation level parameter for the received image frame; and
 - the content adaptive image decomposition process includes applying a color decomposition matrix adjusted based on the determined saturation level parameter.
8. The apparatus of claim 1, further comprising a backlight including light sources having colors associated with each of the respective color subfields, and wherein the control logic is configured, upon outputting a portion of the display element state information associated with a color subfield, to illuminate a light source associated with the color subfield to illuminate the array of display elements.
9. The apparatus of claim 8, wherein the control logic is configured, upon outputting the portion of the display element state information associated with the color subfield, to illuminate a light source associated with a different color subfield, and wherein the control logic is configured to control the intensities with which the light source associated with the color subfield and the light source associated with the different color subfield are illuminated based in part on a value of a saturation level parameter determined for the received image frame.
10. The apparatus of claim 1, wherein the control logic is further configured to collectively dither the color subfields using a vector error diffusion process.
11. The apparatus of claim 1, wherein the content adaptive gamut mapping process further maps, for each pixel, the first set of color parameter values to the second set of color parameter values based at least in part on a power management parameter.

12. The apparatus of claim 12, wherein the power management parameter comprises one of an inactivity period timer value, a target saturation parameter value, and a battery level.
13. The apparatus of claim 1, further comprising:
 - a display including:
 - the array of display elements,
 - a processor capable of communicating with the display, the processor being capable of processing image data; and
 - a memory device capable of communicating with the processor.
14. The apparatus of claim 13, the display further including:
 - a driver circuit capable of sending at least one signal to the display; and
 - a controller capable of sending at least a portion of the image data to the driver circuit.
15. The apparatus of claim 13, further including:
 - an image source module capable of sending the image data to the processor, wherein the image source module includes at least one of a receiver, transceiver, and transmitter.
16. The apparatus of claim 13, further including:
 - an input device capable of receiving input data and to communicate the input data to the processor.
17. A computer readable medium storing computer executable instructions, which when executed by a processor cause the processor to carry out a method of forming an image on a display, the method comprising:
 - receiving an input image frame, wherein the input image frame includes, for each of a plurality of pixels, a first set of color parameter values;
 - applying a content adaptive gamut mapping process to the first set of color parameter values associated with the pixel to map the first set of color parameter values associated with the pixel to a second set of color parameter values, wherein the content adaptive gamut mapping process is based at least in part on the content of the image frame; and

decomposing the second set of color parameter values associated with the pixel to obtain pixel intensity values in respective color subfields associated with at least four different colors;

generating display element state information for display elements in an array of display elements based on the color subfields; and

outputting display element state information associated with the at least four color subfields to the array of display elements.

18. The computer readable medium of claim 17, wherein the first set of color parameter values include red, green, and blue pixel intensity values and the second set of color parameter values include XYZ tristimulus values.
19. The computer readable medium of claim 17, wherein the method further includes determining a saturation level parameter for the image and adapting the gamut mapping process based on the determined color saturation parameter of the input image frame.
20. The computer readable medium of claim 17, wherein adapting the gamut mapping process includes generating an image saturation level-dependent gamut mapping lookup table.
21. The computer readable medium of claim 20, wherein generating the image saturation level-dependent gamut mapping lookup table includes interpolating between at least two stored gamut mapping lookup tables based on the determined image saturation parameter.
22. The computer readable medium of claim 17, wherein decomposing the second set of color parameter values associated with the each pixel includes decomposing the seconds set of color parameter values according to a content adaptive image decomposition process.
23. The computer readable medium of claim 22, wherein the method further comprises determining a saturation level parameter for the received image frame, and wherein the content adaptive image decomposition process comprises applying a color decomposition matrix adjusted based on the determined saturation level parameter.

24. The computer readable medium of claim 17, wherein the method further comprises collectively dithering the color subfields using a vector error diffusion process.
25. The computer readable medium of claim 17, wherein the content adaptive gamut mapping process further maps, for each pixel, the first set of color parameter values to the second set of color parameter values based at least in part on a power management parameter.
26. The computer readable medium of claim 25, wherein the power management parameter includes at least one of an inactivity period timer value, target saturation parameter value, and a battery level.
27. An apparatus comprising:
 - an array of display elements;
 - control logic configured to:
 - receive an input image frame encoded in a first color space, wherein the input image frame includes, for each of a plurality of pixels, a set of color intensity values;
 - determine a saturation parameter for the image frame;
 - for each pixel in the received image frame:
 - apply a gamut mapping process to the color intensity values associated with the pixel in order to convert the color intensity values into corresponding tristimulus values in the XYZ color space based at least in part on saturation parameter; and
 - decompose the XYZ tristimulus values associated with the pixel to obtain pixel intensity values associated with at least four different color subfields;
 - generate display element state information for the display elements in the array of display elements based on the color subfields; and
 - output display element state information associated with the at least four color subfields to the array of display elements to form an image.
28. The apparatus of claim 27, wherein the control logic is further configured to derive a decomposition matrix based at least in part on the saturation parameter and decomposing the XYZ tristimulus values comprises applying the decomposition matrix.

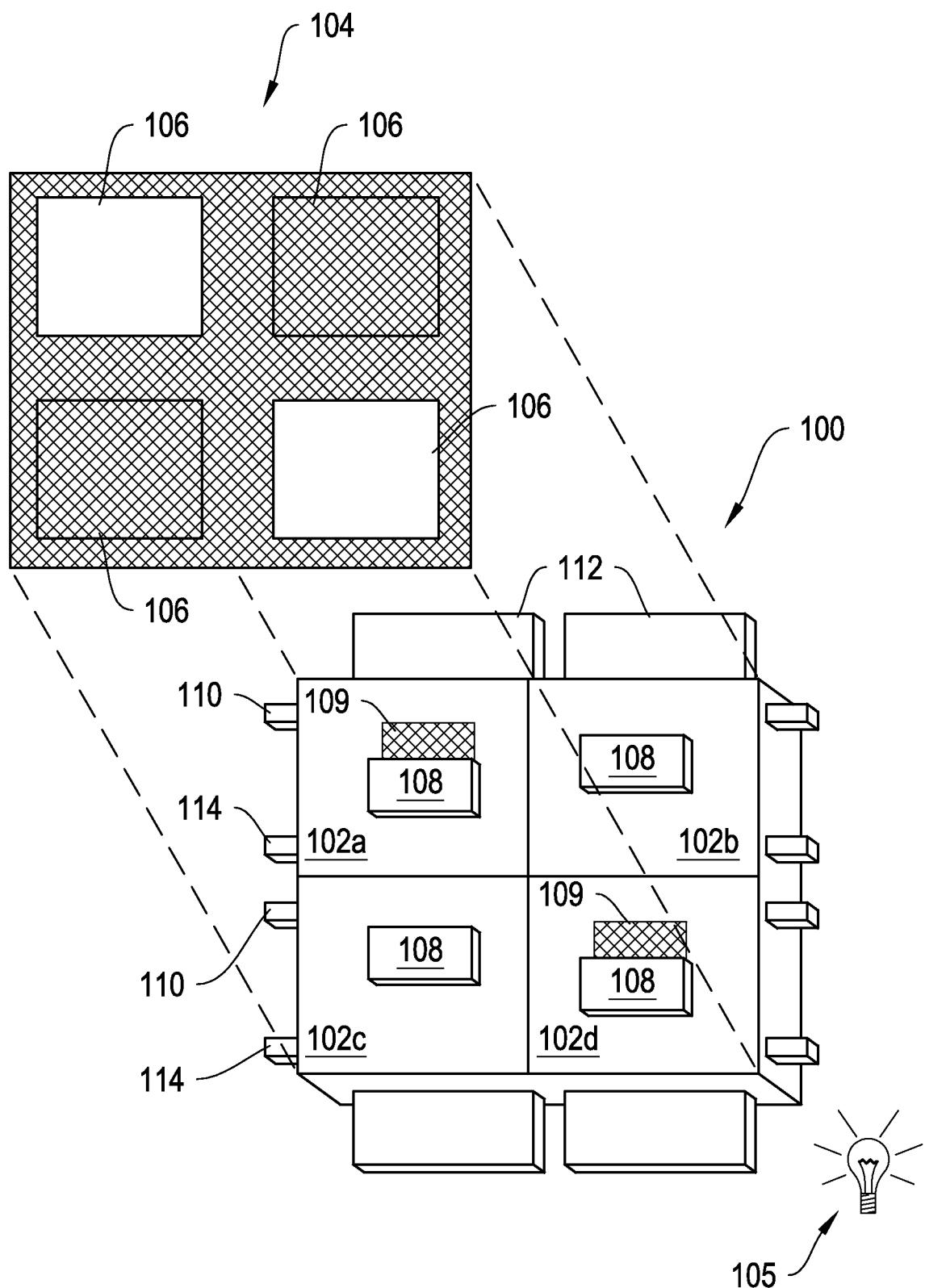


Figure 1A

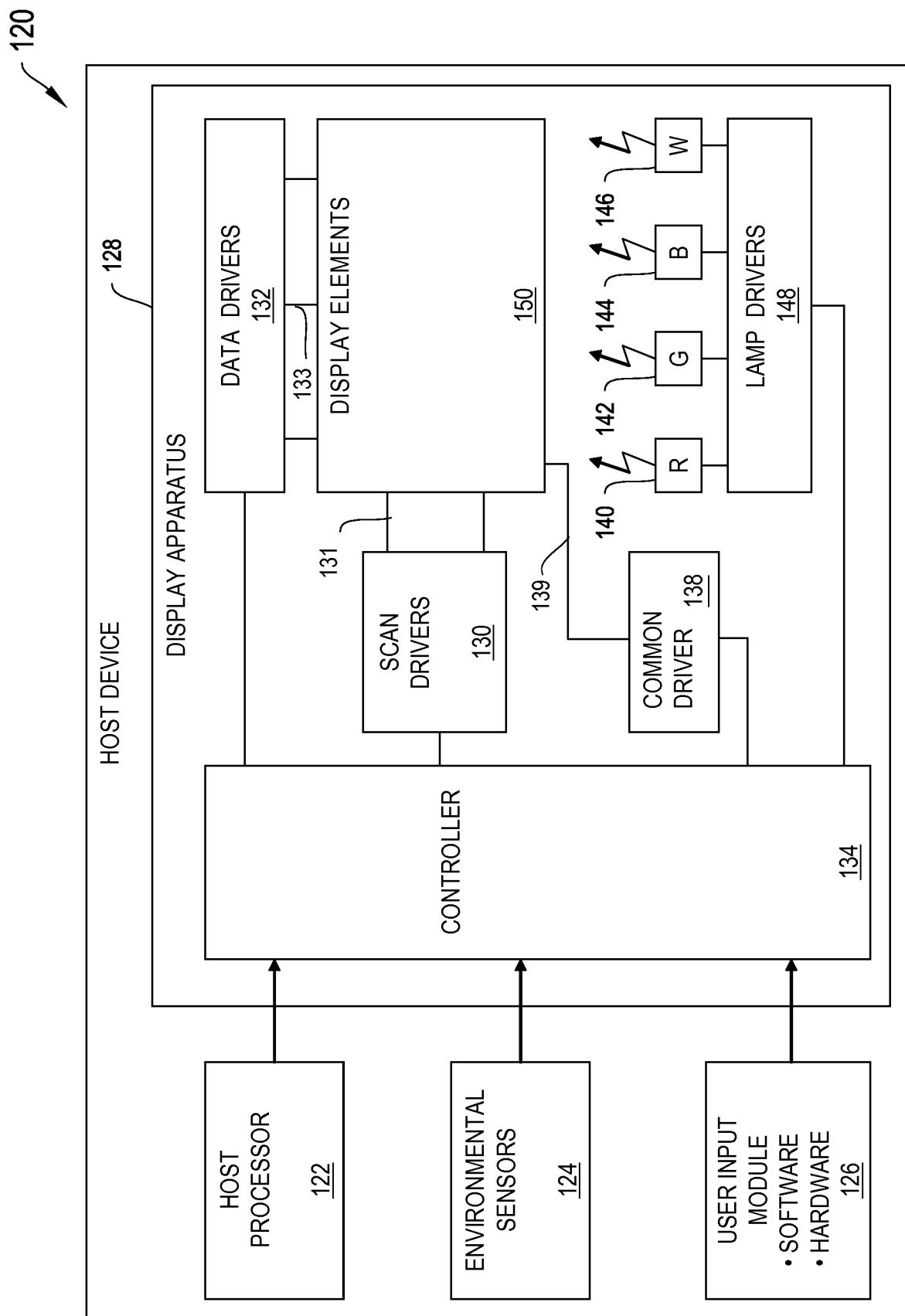
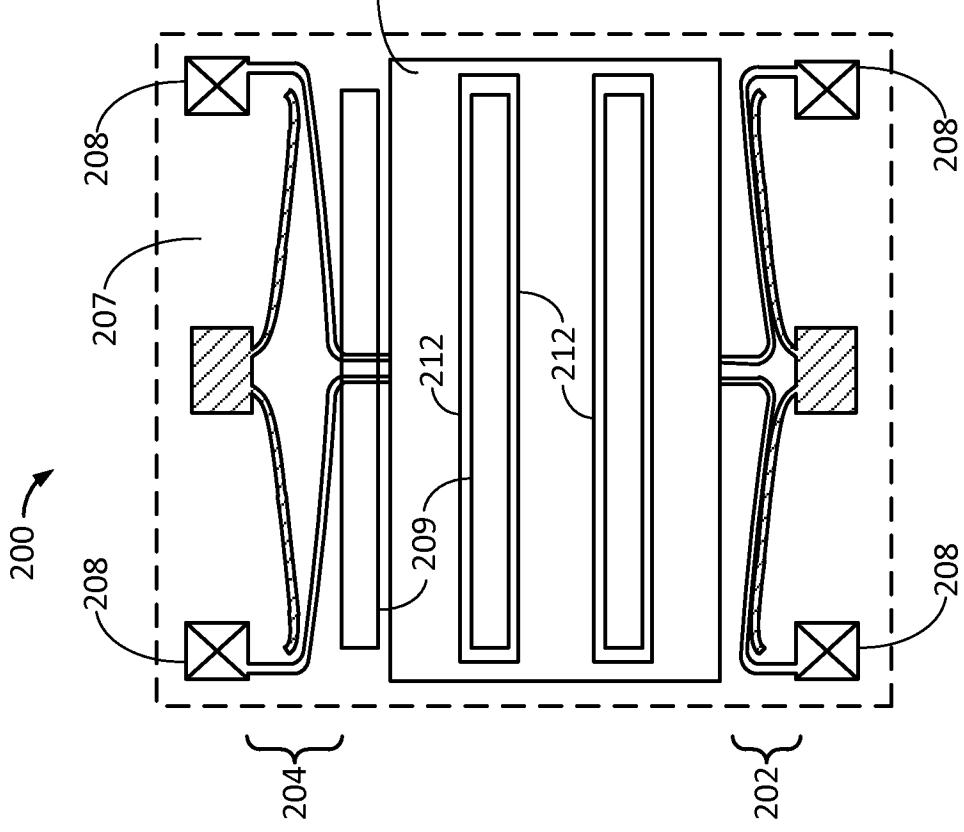
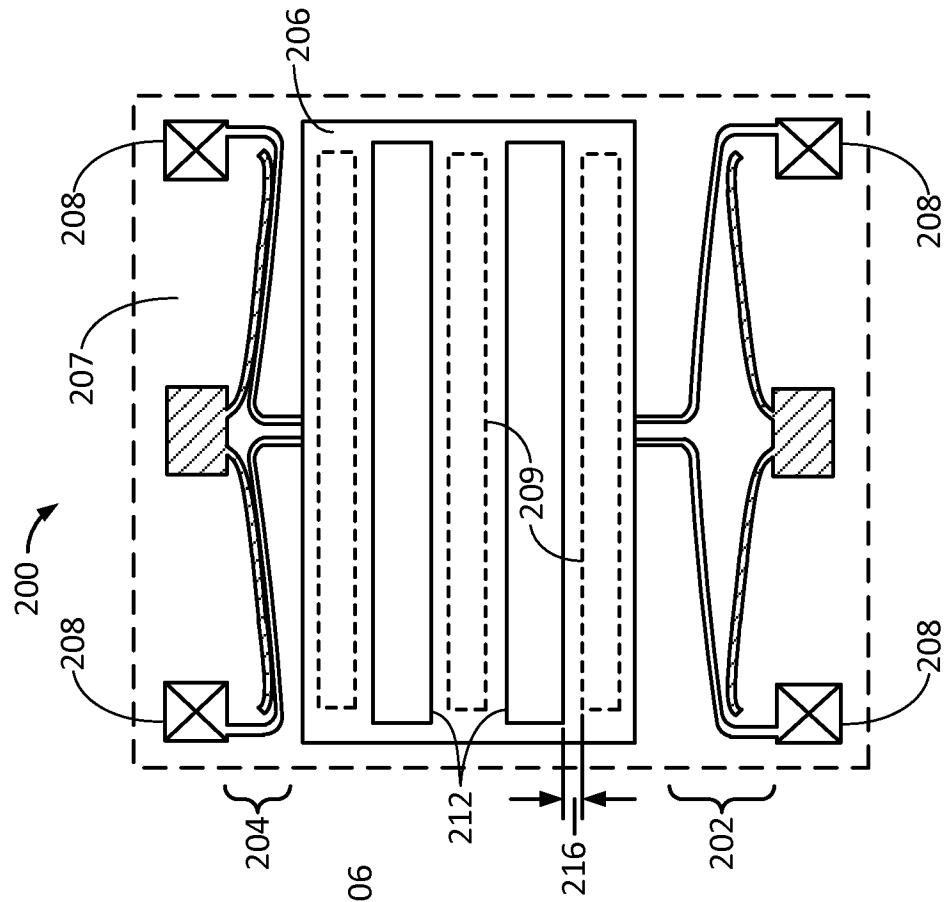


Figure 1B

FIGURE 2A**FIGURE 2B**

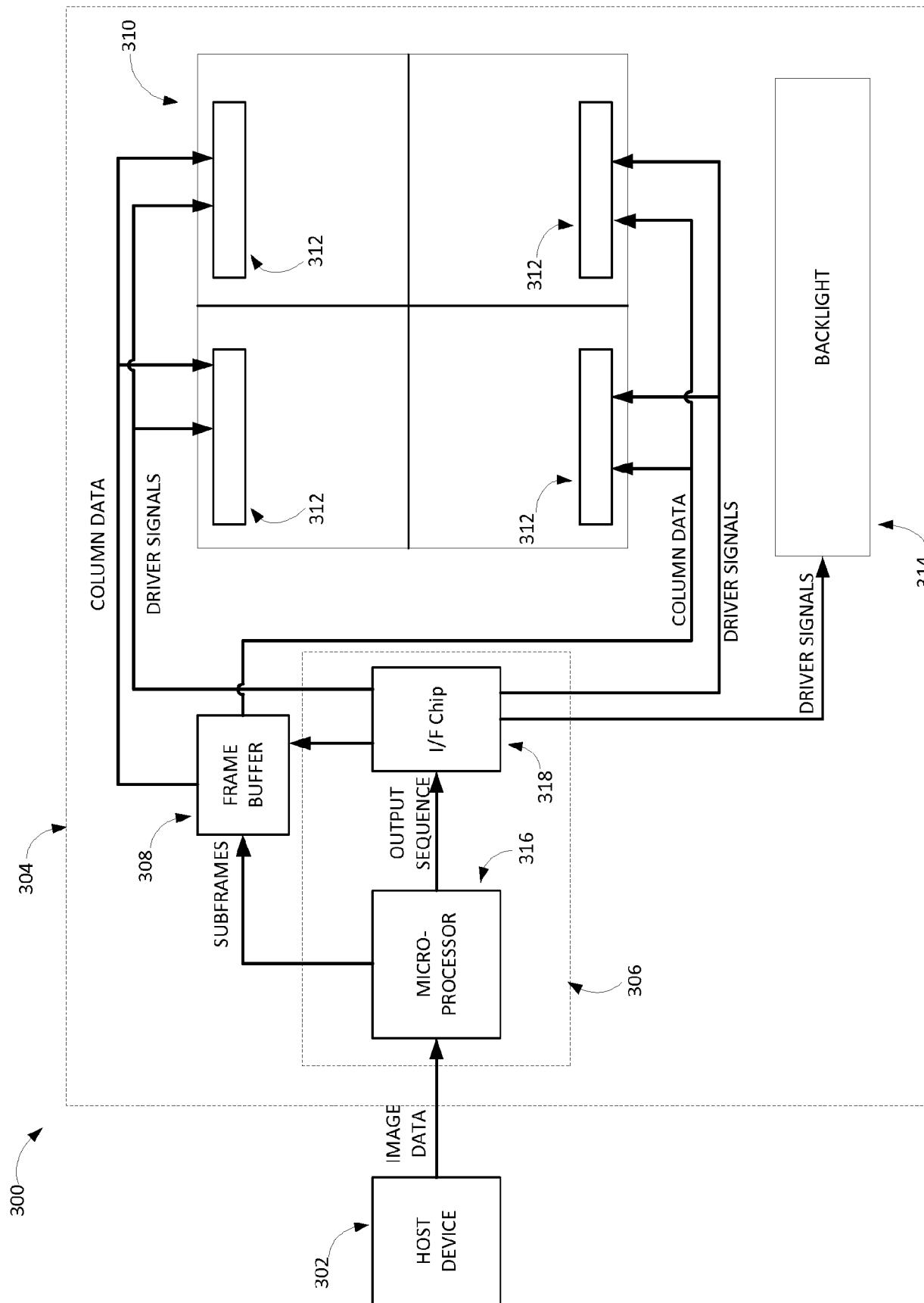


FIGURE 3

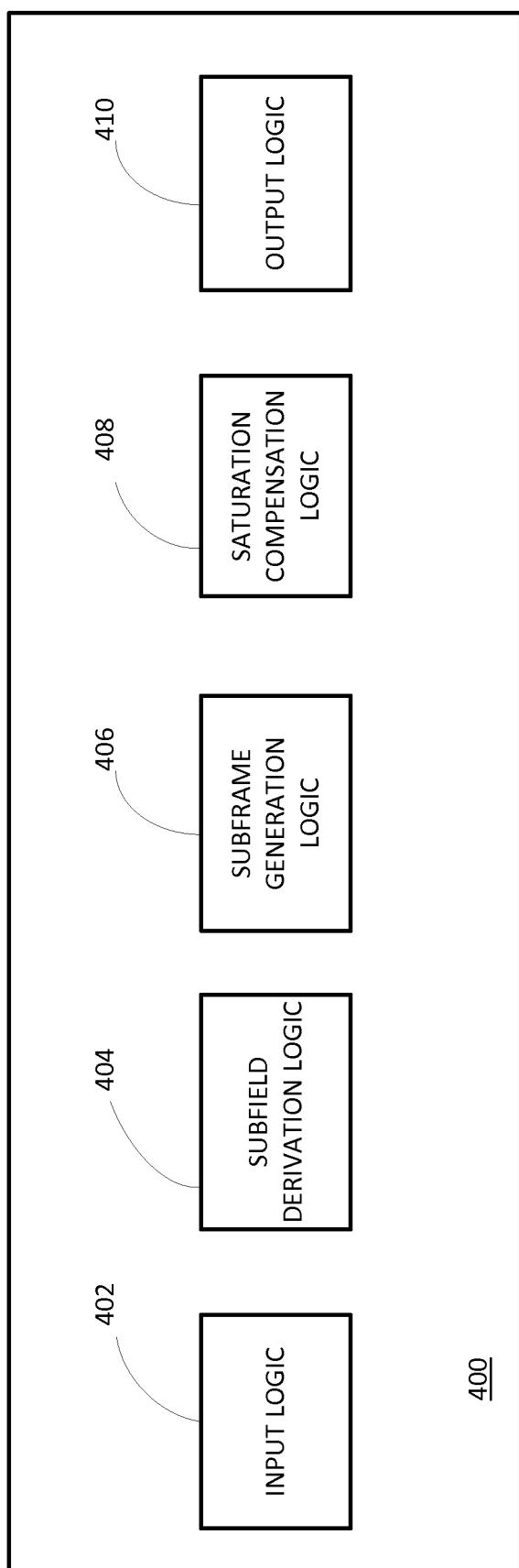


FIGURE 4

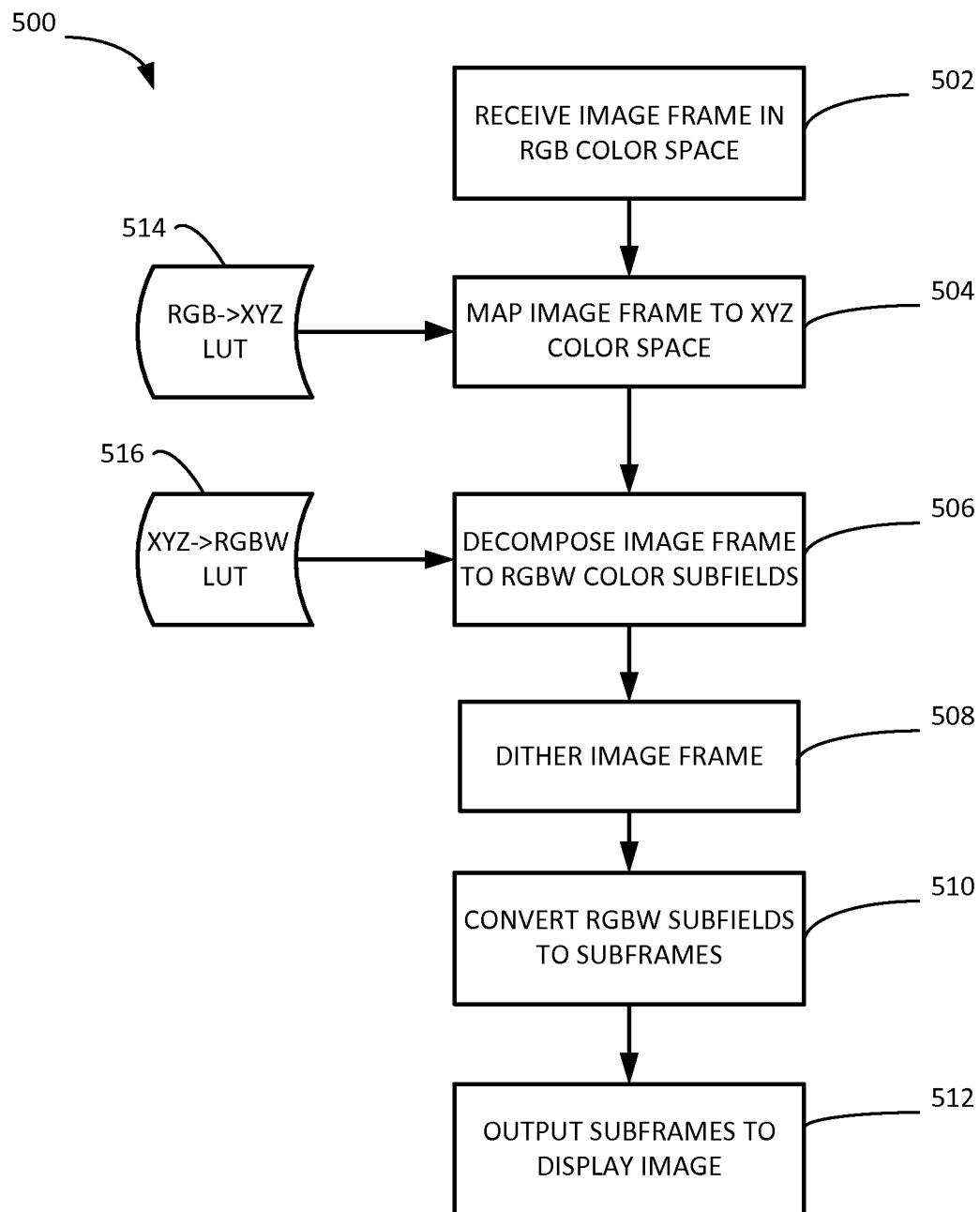


FIGURE 5

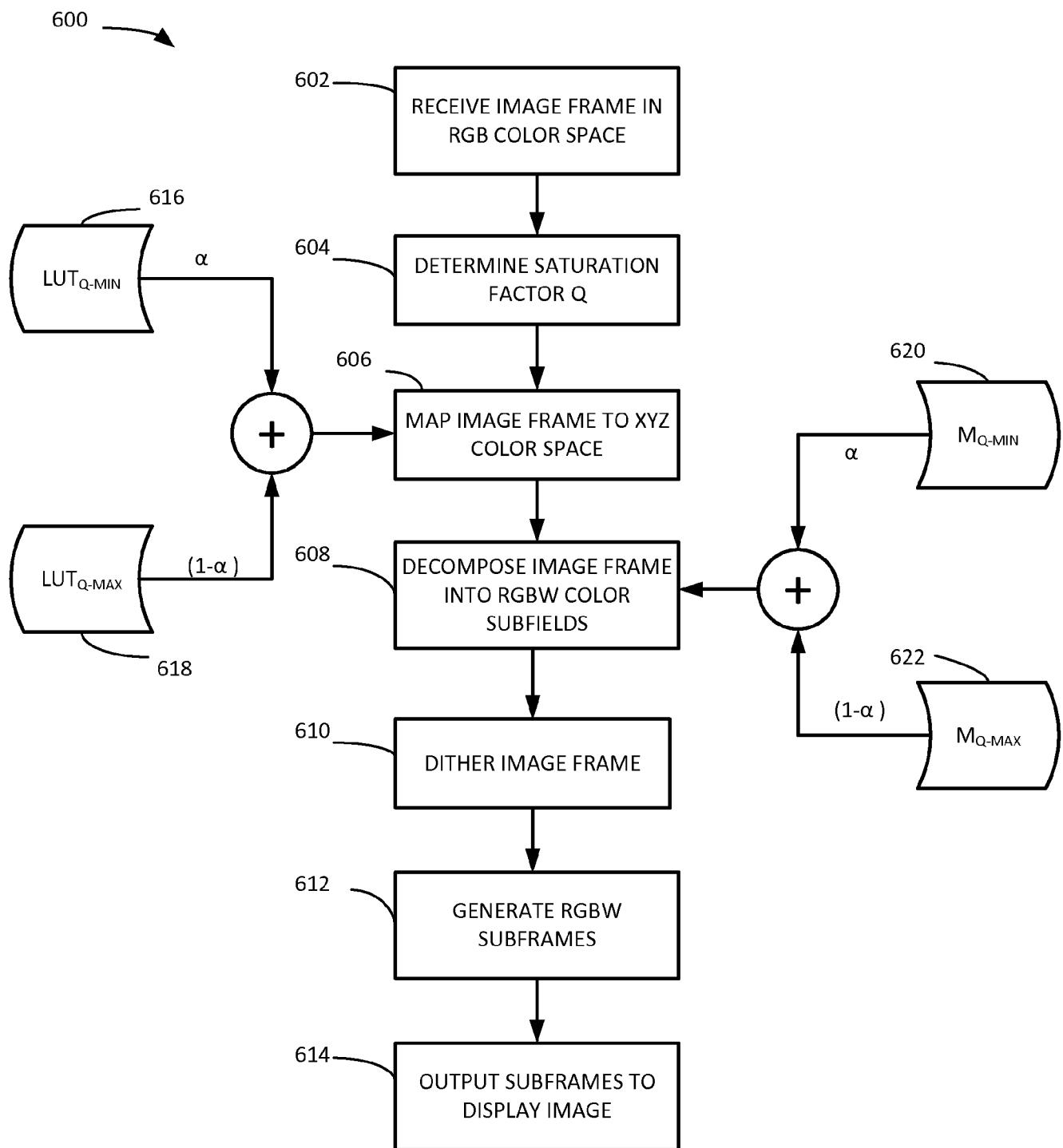


FIGURE 6

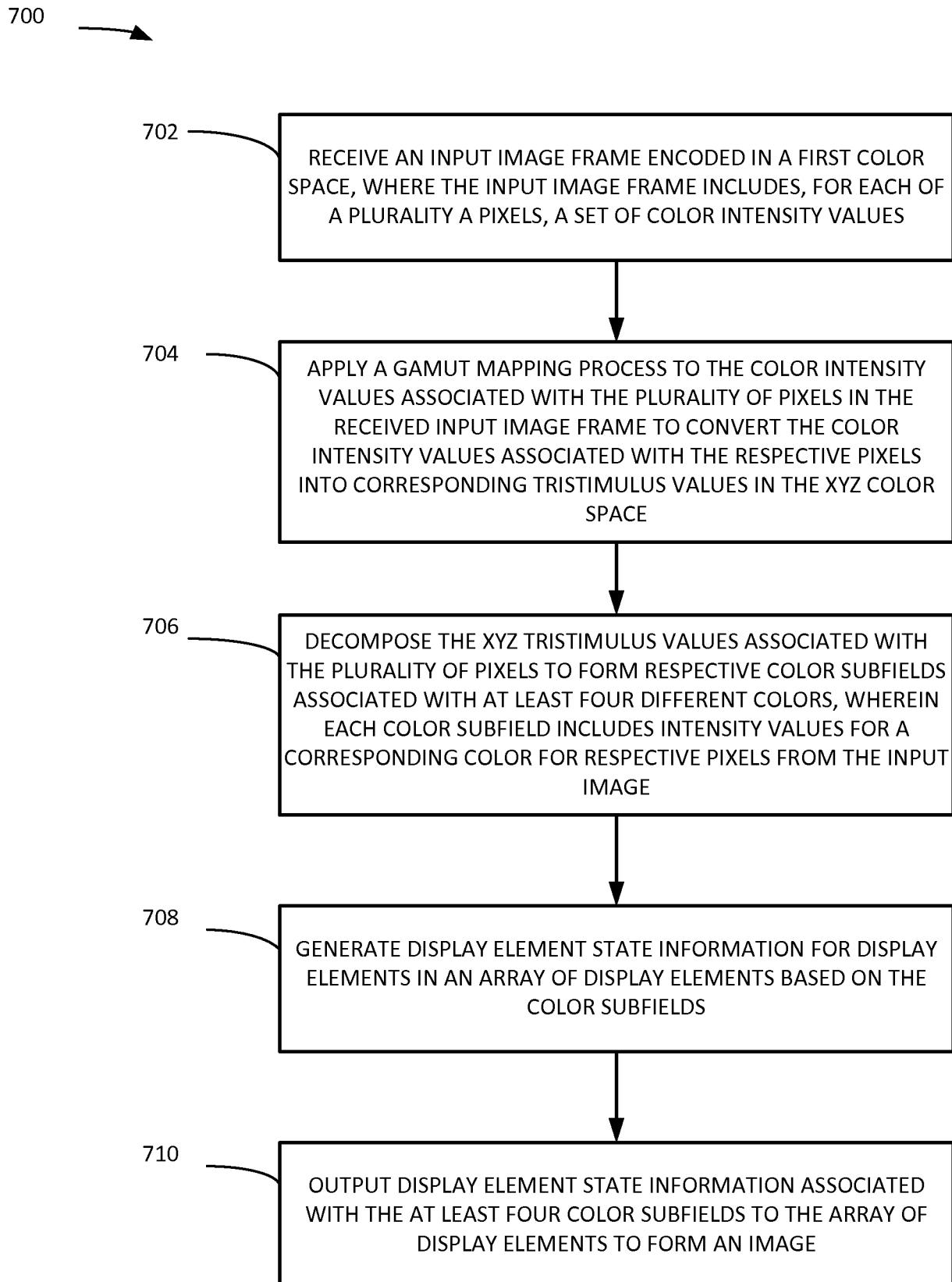


FIGURE 7

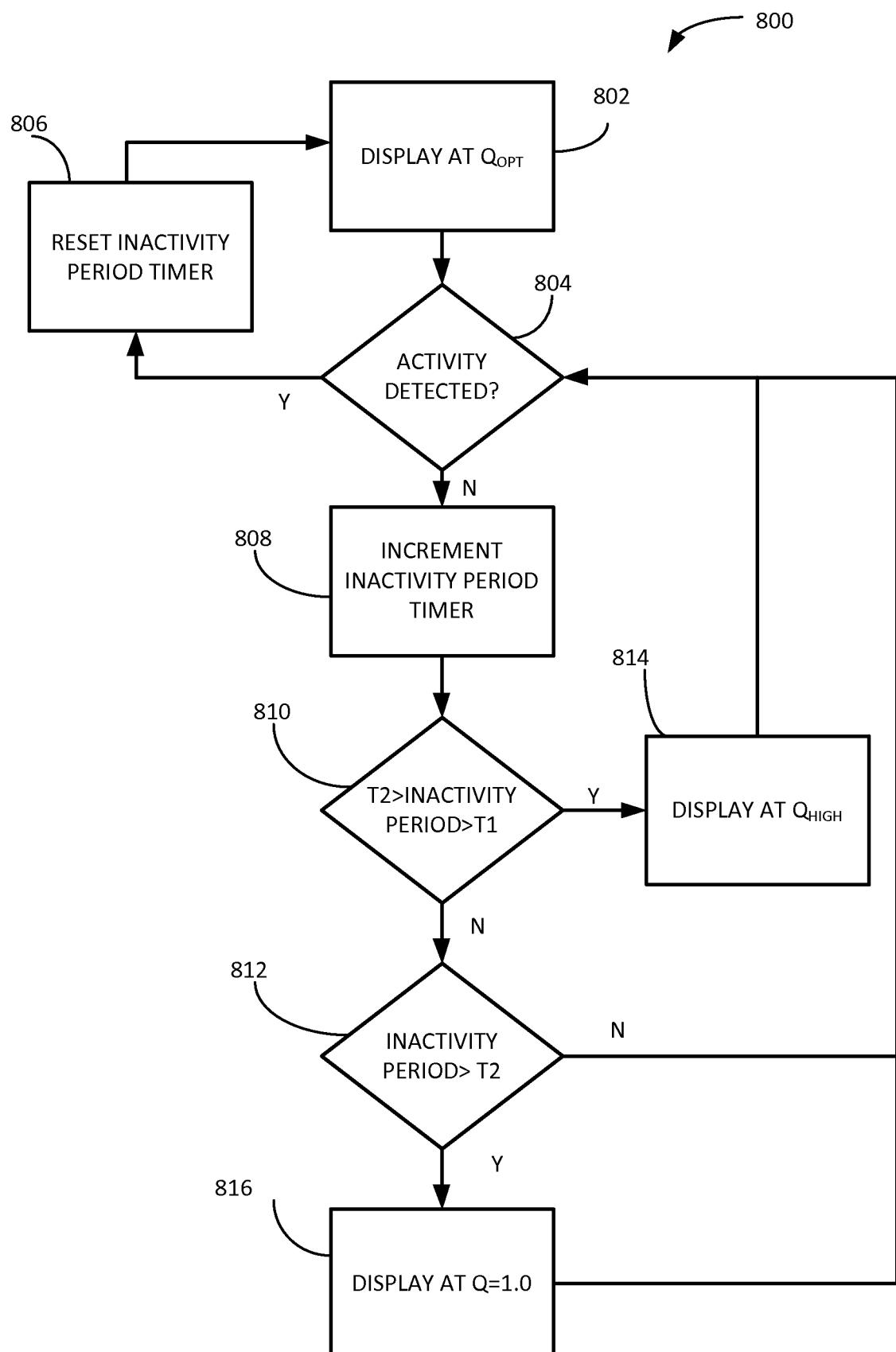


FIGURE 8

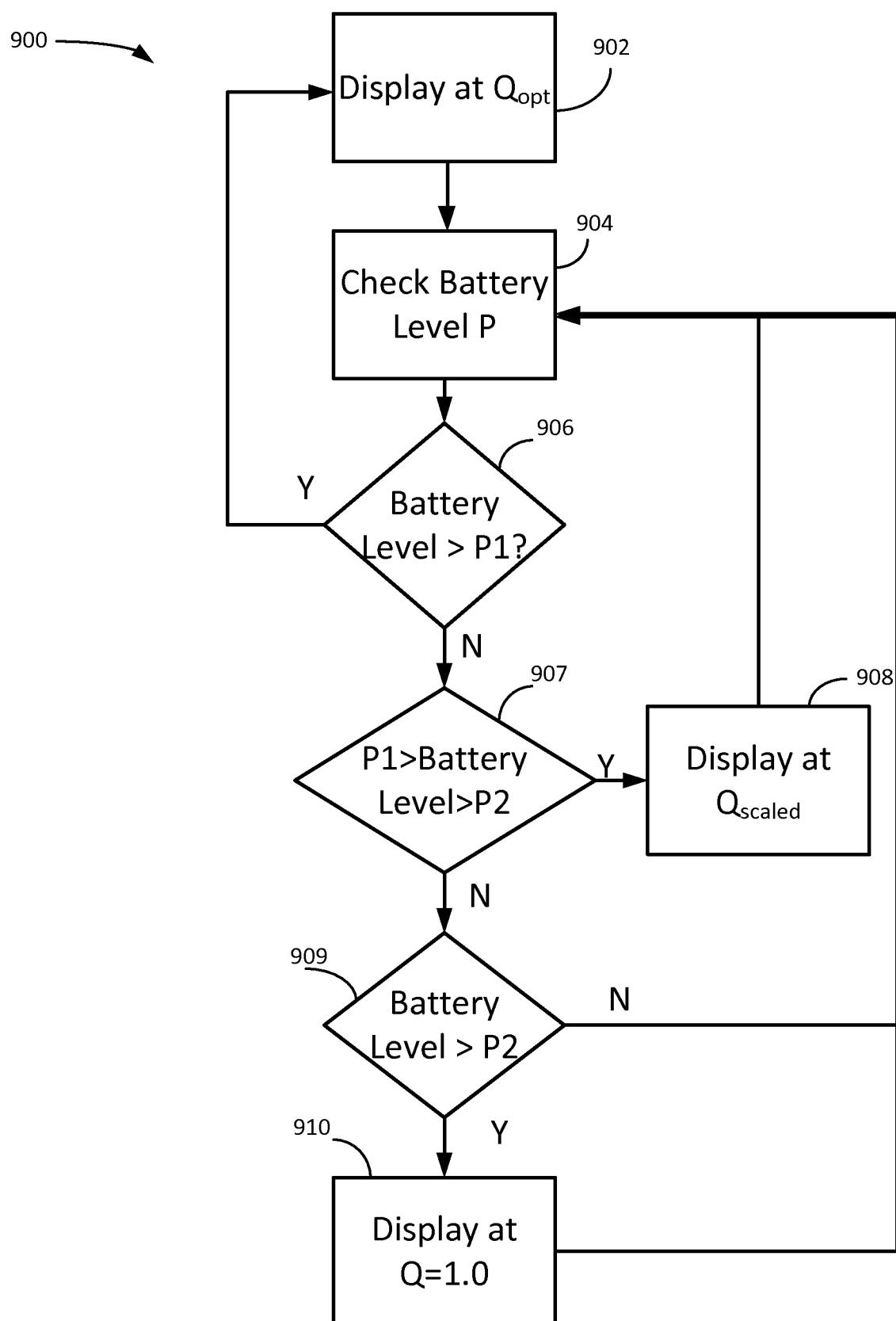


FIGURE 9

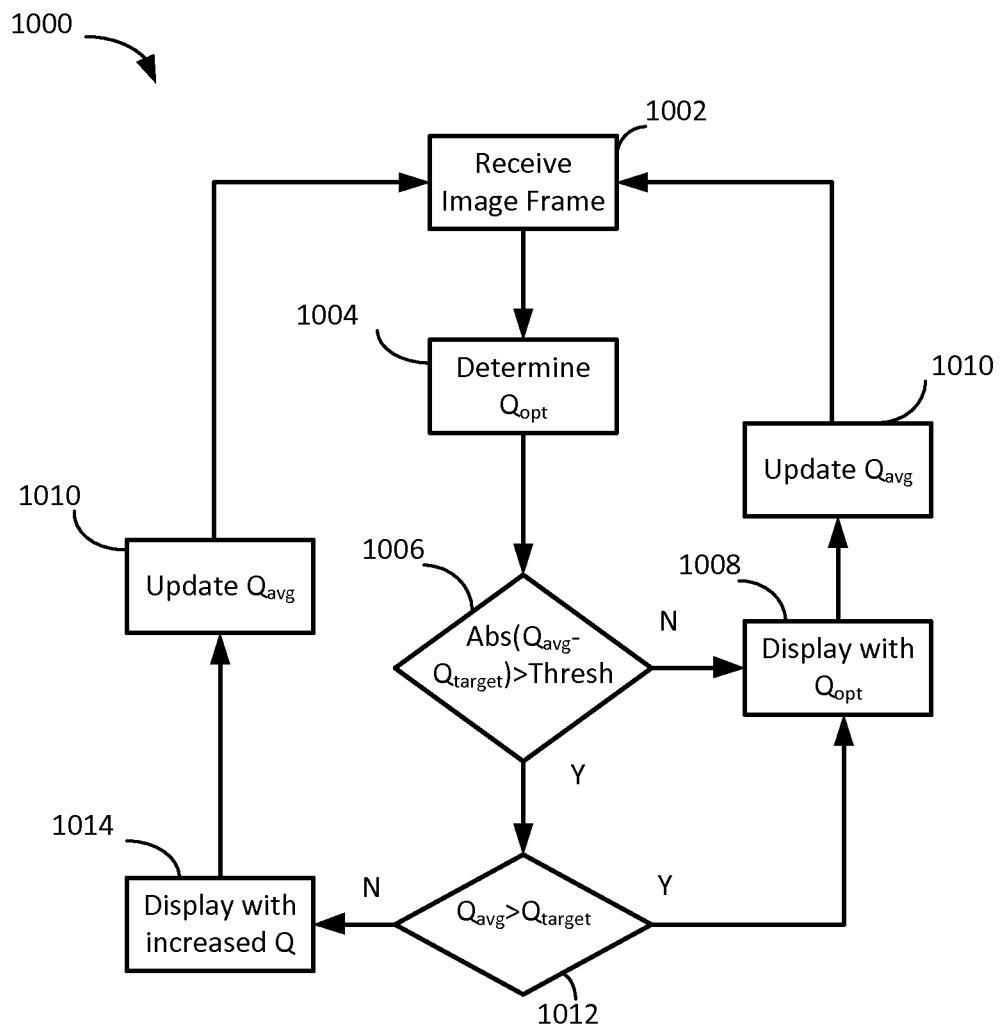


FIGURE 10

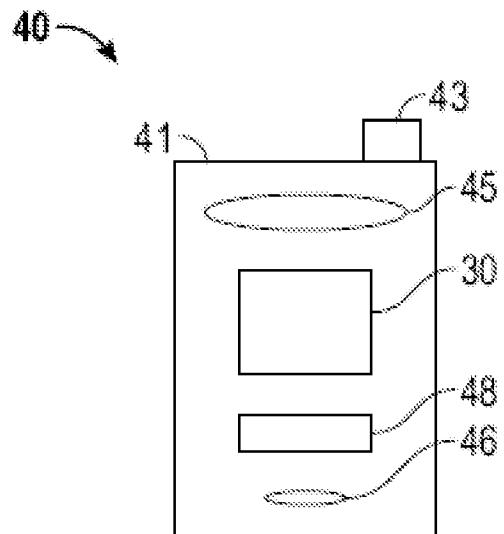


FIGURE 11A

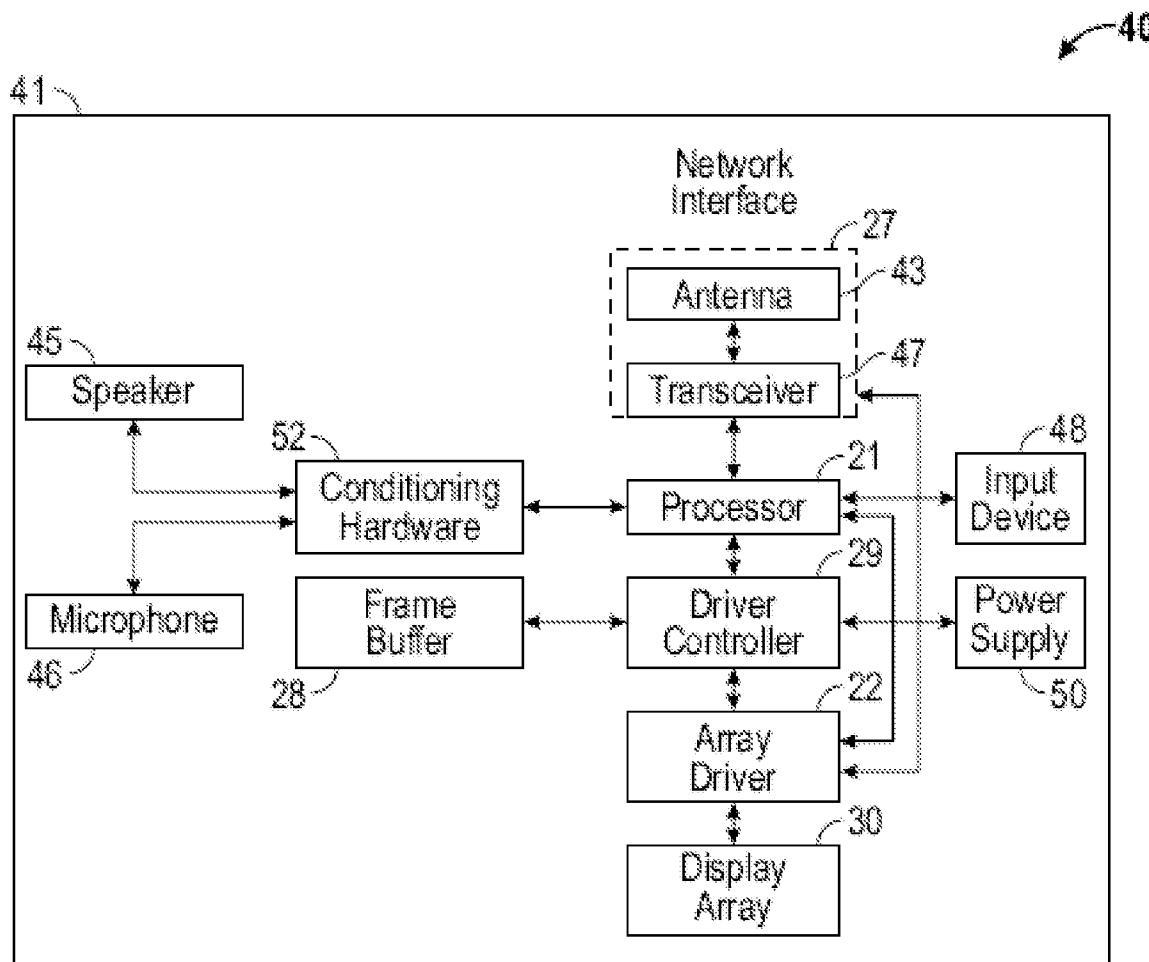


FIGURE 11B

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2015/054006

A. CLASSIFICATION OF SUBJECT MATTER

INV. G09G3/20

ADD. G09G5/06

H04N1/52

H04N1/54

H04N9/31

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G09G H04N

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2014/118388 A1 (BUCKLEY EDWARD [US] ET AL) 1 May 2014 (2014-05-01) paragraphs [0141], [0198], [0202]; figures 1,6,7,10 -----	1-28
Y	JP 2007 108249 A (SONY CORP) 26 April 2007 (2007-04-26) paragraphs [0036], [0037]; figure 5 -----	1-28



Further documents are listed in the continuation of Box C.



See patent family annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

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"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

Date of mailing of the international search report

16 December 2015

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/US2015/054006

Patent document cited in search report	Publication date	Patent family member(s)		Publication date
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JP 2007108249	A	26-04-2007	NONE	