

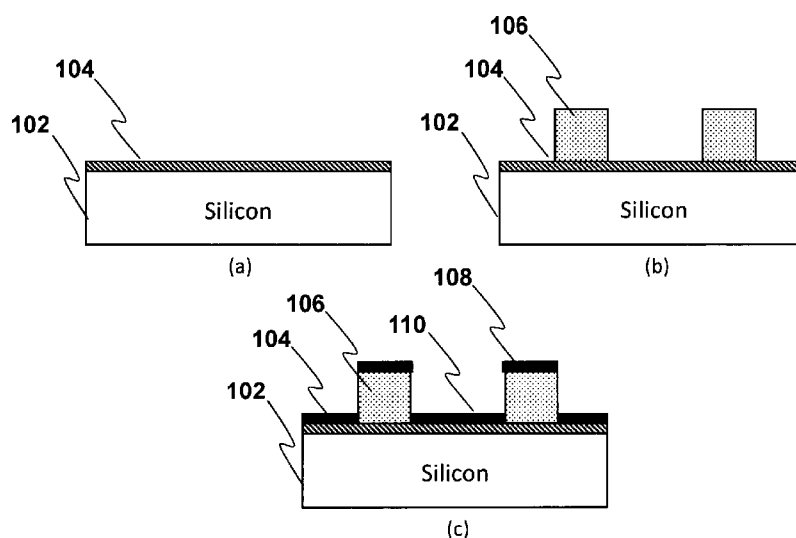


- (51) **International Patent Classification:**
H01L 21/027 (2006.01)
- (21) **International Application Number:**
PCT/MY2015/000026
- (22) **International Filing Date:**
29 April 2015 (29.04.2015)
- (25) **Filing Language:** English
- (26) **Publication Language:** English
- (30) **Priority Data:**
PI 2014701169 7 May 2014 (07.05.2014) MY
- (71) **Applicant:** MIMOS BERHAD [MY/MY]; Technology Park Malaysia, 57000 Kuala Lumpur (MY).
- (72) **Inventors:** LEE, Hing Wah; c/o MIMOS BERHAD, Technology Park Malaysia, 57000 Kuala Lumpur (MY). BIEN, Daniel Chia Sheng; c/o MIMOS BERHAD, Technology Park Malaysia, 57000 Kuala Lumpur (MY). ABD WAHID, Khairul Anuar; c/o MIMOS BERHAD, Technology Park Malaysia, 57000 Kuala Lumpur (MY). ATAN@MOHAM, Khairom Nizam; c/o MIMOS BERHAD, Technology Park Malaysia, 57000 Kuala Lumpur (MY). ZAKARIA, Anifah; c/o MIMOS BERHAD, Technology Park Malaysia, 57000 Kuala Lumpur (MY).
- (74) **Agent:** CHEW, Kherk Ying; Wong & Partners, Level 21, The Gardens South Tower, Mid Valley City, Lingkaran Syed Putra, 59200 Kuala Lumpur (MY).
- (81) **Designated States** (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.
- (84) **Designated States** (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

- as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))

[Continued on next page]

(54) **Title:** AN ETCH-FREE METHOD FOR CONDUCTIVE ELECTRODE FORMATION**FIGURE 1**

(57) **Abstract:** The present invention provides an etch-free method for conductive electrode formation. The method comprises depositing an insulating layer (104) on a substrate (102), spin coating a first polymer layer (106) on the substrate (102), patterning the first polymer layer (106) by photo-lithography and depositing a conductive metal layer by physical deposition to form a top metallic layer (108) and a bottom metallic layer (110).



— *of inventorship (Rule 4.17(iv))*

Published:

— *with international search report (Art. 21(3))*

— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments (Rule 48.2(h))*

AN ETCH-FREE METHOD FOR CONDUCTIVE ELECTRODE FORMATION

FIELD OF INVENTION

5 The present invention relates generally to an etch-free method for conductive electrode formation, more particularly a fabrication method for conductive electrode structure comprising the formation of high aspect ratio polymer structures by lithographic techniques, followed by self-aligning of a conductive metal layer onto the formed polymer by physical metal deposition to define the conductive electrode
10 structures.

BACKGROUND ART

15 In semiconductor device fabrication, formation of conductive metal electrodes is essential when creating device platforms for MEMS and NEMS sensors and actuators applications. At present, these conductive metal electrode structures are typically formed by either etching a deposited metal layer in a wet chemical etchant or gaseous plasma, lifting off the metallic layer at unwanted areas by chemically etching a polymer resist material or self-aligning the metal onto plasma etched
20 substrate.

All these methods involved an etching process by either wet chemical or gaseous plasma at certain stages to form the final electrode structures. These methods would typically utilise high powered plasma, heated acid or solvents and ultrasonic agitation. This sometimes makes finding a robust masking material difficult as it
25 needs to withstand the harsh etching conditions mentioned above.

Methods such as lift-off which is used to form noble metal electrodes create other potential process issues such as "ear-effect" and surface contamination as the metal in the etch solution re-deposits onto the substrate surface while etching of the
30 substrate may also cause unintentional damage or fracture to the substrate itself, hence making it more fragile. Also, when forming a high aspect ratio structure on a conducting or semiconducting substrate such as silicon, coating of an insulating

layer is required to isolate the electrical effect from the substrate. This limits the type of insulating material and fabrication process that can be used.

SUMMARY OF INVENTION

5

The present invention provides an etch-free method for conductive electrode formation. The present invention proposes a method to fabricate conductive electrodes, the method being independent of any masking material as it does not require any chemical or gaseous plasma etching.

10

In one aspect of the present invention is an etch-free method for conductive electrode formation that comprises depositing an insulating layer on a substrate, spin coating a first polymer layer on the substrate, patterning the first polymer layer by photo-lithography and depositing a conductive metal layer by physical deposition to form a top metallic layer and a bottom metallic layer.

15

In another aspect of the present invention, the method further comprises spin coating a second polymer layer on the top metallic layer and the bottom metallic layer and patterning the second polymer layer by photo-lithography to selectively expose the top metallic layer and the bottom metallic layer.

20

The first polymer layer has high aspect ratio of at least 10:1. The first polymer layer is of non-conductive material to electrically isolate the top metallic layer and the bottom metallic layer. The second polymer layer (116) is of non-conductive material.

25

The first polymer layer and second polymer layer is of polyimide, SU-8 or polymethyl methacrylate (PMMA) material. The depositing the conductive metal layer is by metal evaporation.

In one embodiment of the present invention, patterning the first polymer layer by photo-lithography defines the first polymer layer with a vertical sidewall with a minimum aspect ratio of 15.

30

In another embodiment of the present invention, patterning the first polymer layer by photo-lithography defines the first polymer layer with an undercut sidewall with a minimum aspect ratio of 5.

- 5 The present invention consists of features and a combination of parts hereinafter fully described and illustrated in the accompanying drawings, it is being understood that various changes in the details may be made without departing from the scope of the invention or sacrificing any of the advantages of the present invention.

BRIEF DESCRIPTION OF THE ACCOMPANYING DRAWINGS

To further clarify various aspects of some embodiments of the present invention, a more particular description of the invention will be rendered by references to specific
5 embodiments thereof, which are illustrated, in the appended drawings. It is appreciated that these drawings depict only typical embodiments of the invention and are therefore not to be considered limiting of its scope. The invention will be described and explained with additional specificity and detail through the accompanying drawings in which:

10

FIGURES 1 (a), (b) & (c) illustrate an etch-free method for conductive electrode formation.

15

FIGURE 2 illustrates a device with conductive electrodes fabricated by an etch-free method.

FIGURE 3 (a) illustrates a photo-lithographically patterned polymer layer with vertical sidewalls.

20

FIGURE 3 (b) illustrates a photo-lithographically patterned polymer layer with undercut sidewalls.

25

FIGURE 4 illustrates a device with a top metallic layer embedded by a second polymer layer.

FIGURE 5 illustrates a device with a bottom metallic layer embedded by a second polymer layer.

30

FIGURE 6 illustrates a device with a combination of exposed and embedded top and bottom metallic layers.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention relates to an etch-free method for conductive electrode formation. Hereinafter, this specification will describe the present invention according to the preferred embodiments of the present invention. However, it is to be understood that limiting the description to the preferred embodiments of the invention is merely to facilitate discussion of the present invention and it is envisioned that those skilled in the art may devise various modifications and equivalents without departing from the scope of the appended claims.

The present invention more particularly relates a fabrication method for conductive electrode structure comprising the formation of high aspect ratio polymer structures by lithographic techniques, followed by self-aligning of a conductive metal layer onto the formed polymer by physical metal deposition to define the conductive electrode structures. The present invention proposes a method to fabricate conductive electrodes, the method being independent of any masking material as it does not require any chemical or gaseous plasma etching. The number of electrode structures formed may be of single, dual or in an array type with potential applications as electrical conductivity sensor, gas sensor, pressure sensor and electrochemical sensor.

Reference is now made collectively to FIGURES 1(a), (b) & (c) as well as FIGURE 2. FIGURES 1 (a), (b) & (c) illustrate an etch-free method for conductive electrode formation. FIGURE 2 illustrates a device with conductive electrodes fabricated by an etch-free method.

The method according to the present invention begins with the step of depositing an insulating layer (104) on a substrate (102) as shown in FIGURE 1(a). The substrate is a silicon based substrate and the insulating layer serves as an isolation layer between the metal electrodes and the silicon substrate. The method is followed by spin coating a first polymer layer (106) on the substrate (102) and patterning the first polymer layer (106) by photo-lithography as shown in FIGURE 1 (b). The first polymer layer (106) patterned by photo-lithography has a high aspect ratio of at least

10:1. The first polymer layer (106) is of a non-conductive material and highly chemical resistant, for instance of polyimide, SU-8 or poly-methyl methacrylate (PMMA) material, to electrically isolate the top metallic layer (108) and the bottom metallic layer (110). Thereafter, a conductive metal layer is deposited by physical
5 deposition such as metal evaporation to form a top metallic layer (108) and a bottom metallic layer (110) as shown in FIGURE 1 (c).

Reference is now made collectively to FIGURES 3(a) & 3(b). FIGURE 3 (a) illustrates a photo-lithographically patterned polymer layer with vertical sidewalls.
10 FIGURE 3 (b) illustrates a photo-lithographically patterned polymer layer with undercut sidewalls. With photo-lithography, the high aspect ratio first polymer layer (106) comprises of a vertical sidewall as shown in FIGURE 3(a) or an undercut sidewall as shown in FIGURE 3(b). The undercut sidewall is typically achieved when using a negative type photo-polymer. With vertical sidewall structure, a minimum
15 aspect ratio of 15 is required where the height of the polymer needs to be at least 15 times higher than the conductive metal thickness while with an undercut sidewall type structure a minimum aspect ratio of 5 is sufficient. The lower aspect ratio is an advantage where a more planar device structure is required. Another advantage of having an undercut sidewall structure is that both the physical evaporation and
20 sputtering methods can be used for metal deposition, whereas with vertical sidewall structures the metal deposition process is limited to physical evaporation where vertical directionality during metal deposition process is important.

Depending on the required application, all the metal electrode structures can be
25 exposed as shown in FIGURE 1 or selectively exposed by spin coating a second polymer layer (116) on the top metallic layer (108) and the bottom metallic layer (110) and patterning the second polymer layer (116) by photo-lithography to selectively expose the top metallic layer (108) and the bottom metallic layer (110). The second polymer layer (116) is of non-conductive material and highly chemical
30 resistant, for instance of polyimide, SU-8 or poly-methyl methacrylate (PMMA) material. Both the first polymer layer (106) and second polymer layer (116) can be of the same type of material or different types of material with typical thickness in the range of 5 μm to 50 μm . Similar to the first polymer layer (106), the second polymer

layer (116) is formed by photo-lithographic method without any chemical or plasma etching.

Reference is now made collectively to FIGURE 3, FIGURE 4 and FIGURE 5.

5 FIGURE 4 illustrates a device with a top metallic layer embedded by a second polymer layer. FIGURE 5 illustrates a device with a bottom metallic layer embedded by a second polymer layer. FIGURE 6 illustrates a device with a combination of exposed and embedded top and bottom metallic layers.

10 With reference to FIGURE 4, to expose the bottom electrodes (120) the second polymer layer (116) is coated and patterned to enclose and embed the top electrodes (119). With reference to FIGURE 5, the similar process is used to enclose and embed the bottom electrodes (117) with the second polymer layer (116) leaving the top electrode structure (122) exposed. With reference to FIGURE 6, it is also
15 possible to expose or embed selected top (122, 119) and bottom (120,117) electrodes by photo-lithographically defining the second polymer layer (116). This is done by designing the lithographic reticule accordingly.

CLAIMS

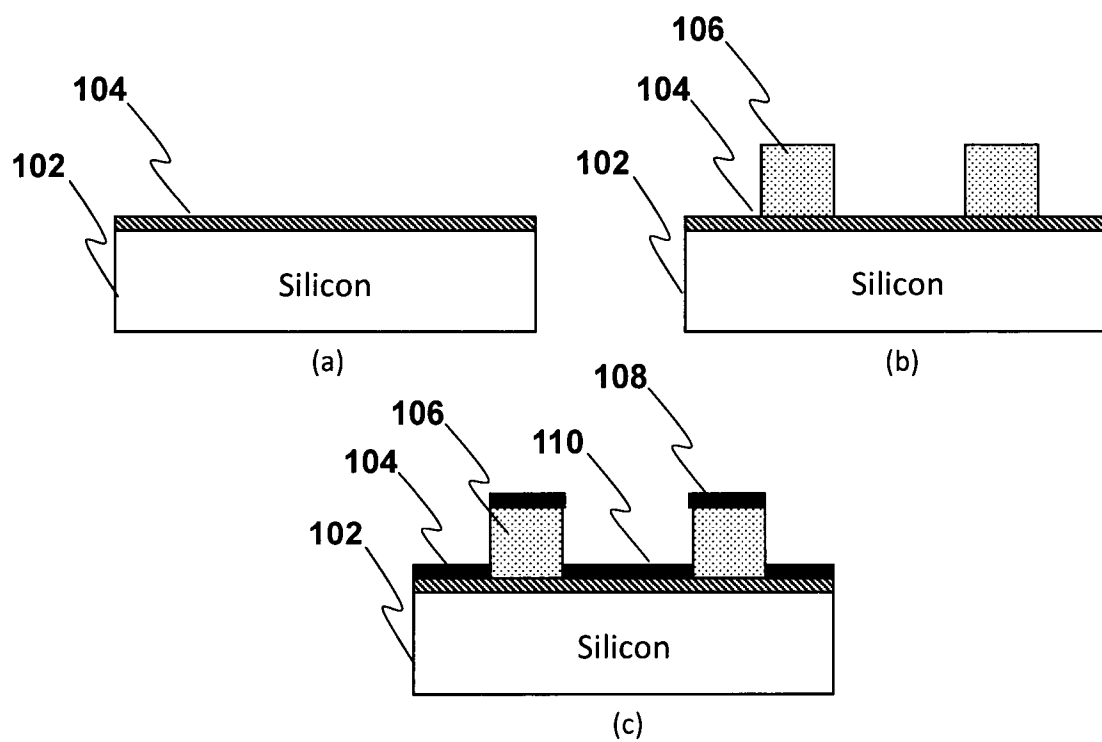
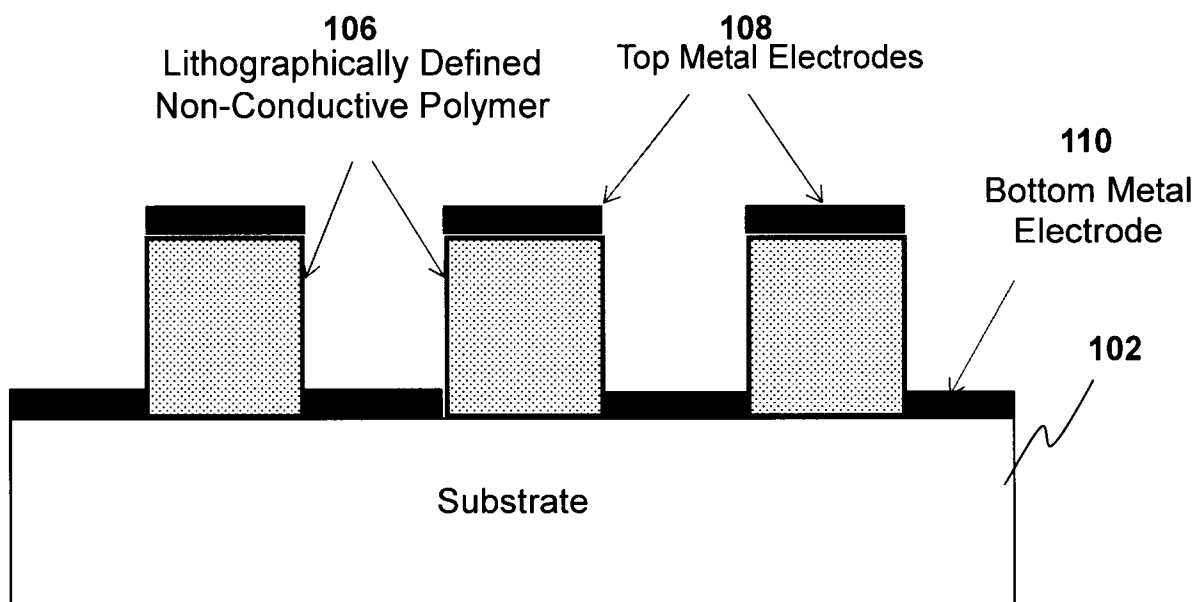
1. An etch-free method for conductive electrode formation, the method comprises
 - 5 depositing an insulating layer (104) on a substrate (102);
 - spin coating a first polymer layer (106) on the substrate (102);
 - patterning the first polymer layer (106) by photo-lithography; and
 - depositing a conductive metal layer by physical deposition to form a top metallic layer (108) and a bottom metallic layer (110).
- 10 2. A method according to claim 1 wherein the method further comprises
 - spin coating a second polymer layer (116) on the top metallic layer (108) and the bottom metallic layer (110); and
 - 15 patterning the second polymer layer (116) by photo-lithography to selectively expose the top metallic layer (108) and the bottom metallic layer (110).
3. A method according to claim 1 wherein the first polymer layer (106) has high aspect ratio of at least 10:1.
- 20 4. A method according to claim 1 wherein the first polymer layer (106) is of non-conductive material to electrically isolate the top metallic layer (108) and the bottom metallic layer (110).
- 25 5. A method according to claim 2 wherein the second polymer layer (116) is of non-conductive material.
6. A method according to claims 1 and 2 wherein the first polymer layer (106) and second polymer layer (116) is of polyimide, SU-8 or poly-methyl methacrylate (PMMA) material.
- 30 7. A method according to claim 1 wherein patterning the first polymer layer (106) by photo-lithography defines the first polymer layer (106) with a vertical sidewall (112) with a minimum aspect ratio of 15.
- 35

8. A method according to claim 1 wherein patterning the first polymer layer (106) by photo-lithography defines the first polymer layer (106) with an undercut sidewall (114) with a minimum aspect ratio of 5.

5

9. A method according to claim 1 wherein the depositing the conductive metal layer is by metal evaporation.

10

**FIGURE 1****FIGURE 2**

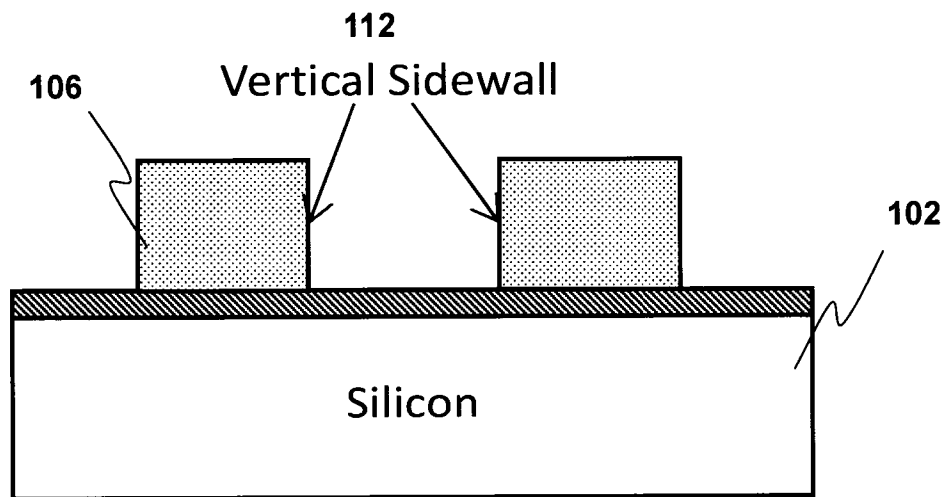


FIGURE 3 (a)

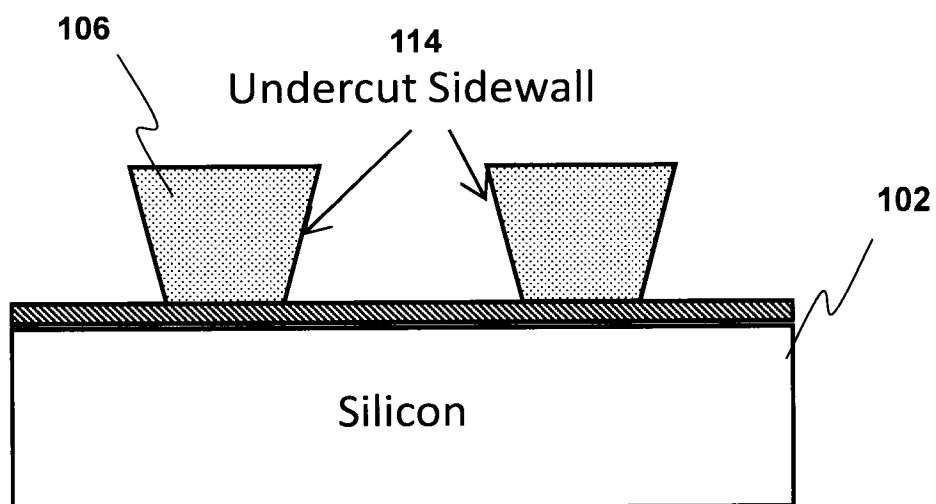


FIGURE 3 (b)

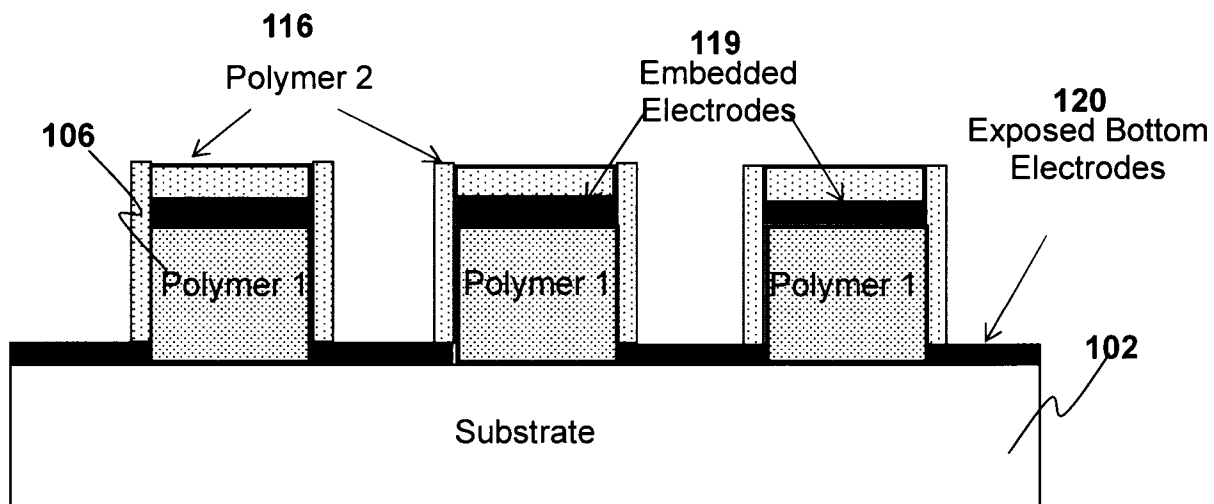


FIGURE 4

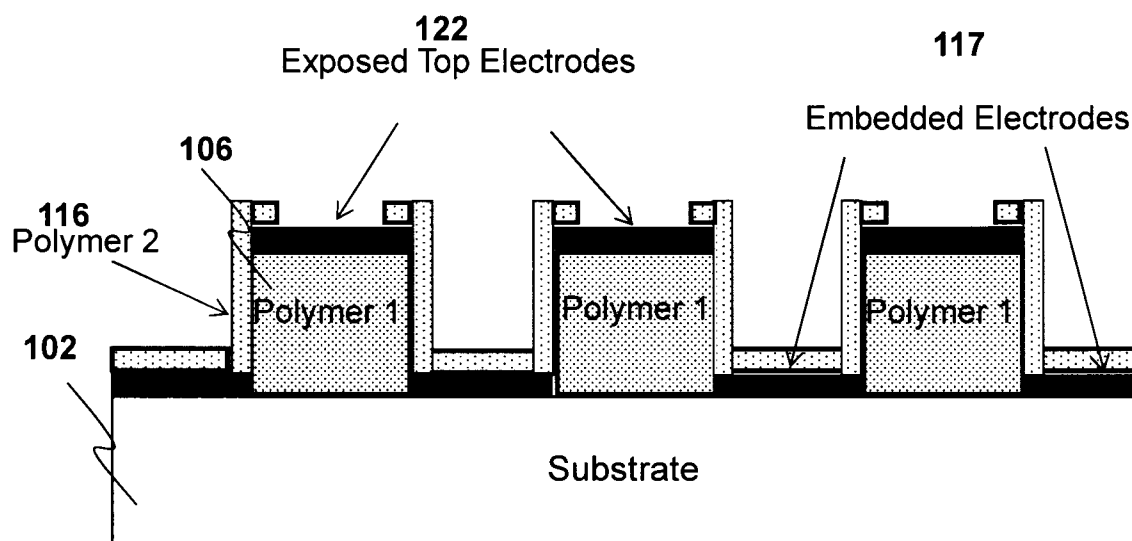


FIGURE 5

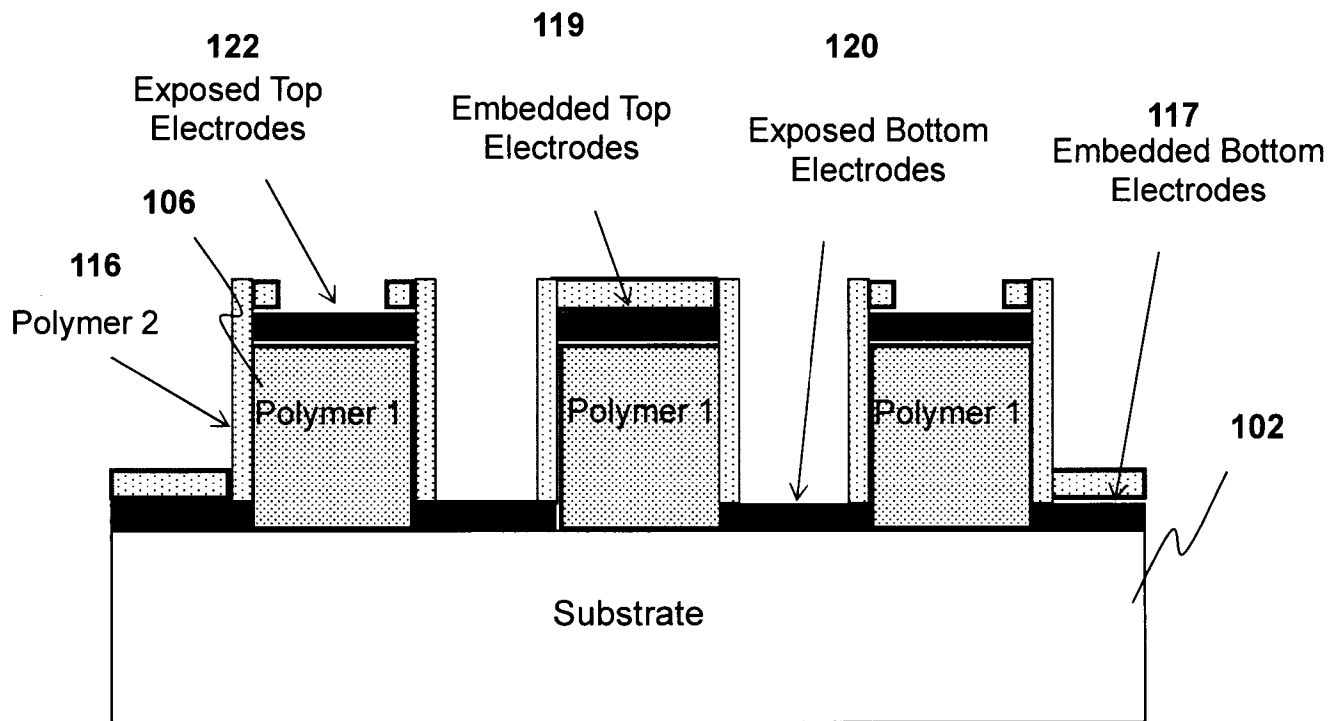


FIGURE 6

A. CLASSIFICATION OF SUBJECT MATTER**H01L 21/027(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 21/027; H01L 21/768; H01L 21/306; H01L 31/0352; G03F 7/20; H01L 21/00; H01L 41/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: metal electrode, etch-free, polymer, patterning, photolithography, spin, insulating, sensor and high aspect ratio

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2009-0023288 A1 (MI HEE JEONG et al.) 22 January 2009 See abstract, paragraphs [0020]-[0034], claim 1 and figures 1-2H.	1-9
A	US 2010-0143848 A1 (KANTI JAIN et al.) 10 June 2010 See abstract, paragraph [0068], claim 1 and figure 5.	1-9
A	US 7094622 B1 (TIANHONG CUI et al.) 22 August 2006 See column 4, line 13 - column 5, line 48, claim 1 and figures 1(E)(1)-1(G)(1).	1-9
A	US 2007-0013266 A1 (MING-WEI CHANG et al.) 18 January 2007 See abstract, paragraphs [0038]-[0040], claim 1 and figures 1-28.	1-9
A	US 2010-0065819 A1 (YONGXIAN WU) 18 March 2010 See abstract, paragraph [0057], claim 1 and figure 9.	1-9



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

31 August 2015 (31.08.2015)

Date of mailing of the international search report

31 August 2015 (31.08.2015)

Name and mailing address of the ISA/KR

International Application Division
Korean Intellectual Property Office
189 Cheongsu-ro, Seo-gu, Daejeon Metropolitan City, 35208,
Republic of Korea

Facsimile No. +82-42-472-7140

Authorized officer

CHOI, Sang Won

Telephone No. +82-42-481-8291



INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/MY2015/000026

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2009-0023288 A1	22/01/2009	KR 10-0843552 B1 US 7811934 B2	04/07/2008 12/10/2010
US 2010-0143848 A1	10/06/2010	US 8187795 B2 WO 2010-068695 A1	29/05/2012 17/06/2010
US 7094622 B1	22/08/2006	None	
US 2007-0013266 A1	18/01/2007	DE 102005051604 A1 FR 2887242 A1 GB 2427321 A GB 2427321 B JP 2006-352823 A JP 4142040 B2 KR 10-0634994 B1 TW I260940 B US 2009-0126183 A1 US 7673375 B2	23/11/2006 22/12/2006 20/12/2006 16/05/2007 28/12/2006 27/08/2008 10/10/2006 21/08/2006 21/05/2009 09/03/2010
US 2010-0065819 A1	18/03/2010	CN 101536187 A EP 2082425 A1 EP 2082425 A4 JP 2010-505728 A US 8044379 B2 WO 2008-045301 A1	16/09/2009 29/07/2009 13/07/2011 25/02/2010 25/10/2011 17/04/2008