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(72) Inventors LUCIANO GANDOLFI
RUDOLF ROCAK

(19)

(54) IMPROVEMENTS IN OR RELATING TO THE MANUFACTURE OF SEMICONDUCTOR DEVICES

(71) We, SGS-ATES COMPONENTI ELETTRONICI S.p.A., an Italian Company, of 2 Via C. Olivetti, 20041 Agrate Brianza, Milan, Italy, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

The present invention relates to the manufacture of p-n. junction semiconductor devices, and in particular a method of passivating the p-n. junctions of a multiplicity of semiconducting elements.

The "mesa" technique is already known in the production of power semiconductor devices having junctions adapted to withstand very high reverse bias. In this technique, a wafer of semicondutor material, usually silicon or germanium in a microcrystalline state, after having been treated with conventional diffusion and photoengraving techniques to form one or more p-n junctions parallel to its faces, is subjected to an etching operation according to a predetermined pattern. The etched areas divide the wafer into a plurality of semiconducting elements or chips which have lateral surfaces intersecting one or more junctions between zones having opposite conductivity types. The engraving or etching angle is determined during the design of the device in accordance with the principle of minimizing the electrostatic fields which, owing to the difference in polarity and resistivity of the semiconductor layers are formed on the lateral surface of the semiconducting element. The bevel or inclination is usually termed positive bevel when, considering two superimposed layers having different resistivity and forming a junction, the layer having lower resistivity projects beyond the layer having higher resistivity, and negative bevel (standard mesa) when the higher resistivity layer projects from the layer having lower resistivity.

As known the electrical properties of the semiconductor devices can be affected by even small amounts of impurities deposited on the surfaces of the semiconductor material when the surfaces remain uncovered during the various operational processing steps, and thus in direct contact with the air or other substances. Particularly sensitive to contamination are the zones immediately adjacent to the p-n junctions. which in the case of devices manufactured in accordance with the "mesa" technique are the lateral surfaces of the semiconducting element. This problem requires a great deal of care especially when junctions withstanding reverse voltages higher than 1000 volt are to be produced. In that case, it is necessary to provide working conditions characterized by meticulous cleanliness throughout the successive operations following the engraving operation, while taking care that the wafers should be manipulated to the smallest possible extent until they are mounted on their supports and passivated, i.e. completely insulated from the effects of any foreign contaminating agent by being clad in suitable materials.

Working costs for high reverse bias devices, which costs are already large owing to the specific measures required in handling wafers with unprotected p-n junctions, are further increased by the impossibility of testing the individual semiconducting elements on the still uncut wafer, e.g. by using suitable automatic measuring apparatus, since passivation of the lateral surfaces is a determining factor for the purposes of measuring maximum reverse bias values to which the p-n junctions may be subjected. Consequently, the overall cost of the finished product is relatively high because the already faulty elements owing to inevitable defects in the crystalline struc-

ture of the starting material or possible damage caused in the various working steps can be rejected only after mounting during the final test.

To avoid the above described disadvantages, it is necessary to effect passivation immediately after the engraving operation. In this way not only the risk of surface contamination is reduced to a minimum but it is also possible to test the entire wafer, thereby considerably reducing wastage of material and labour.

A method of passivating in a single operation all the semiconducting elements in a wafer is already known, in which a wafer of semiconductor material is fixed at one face thereof to a metal substrate by means of an electrically conductive adhesive. The wafer is then subdivided into chips without detaching it from the substrate and is then subjected to glass deposition by electrophoresis, whereby the lateral surfaces of the chips and the parts of the substrate between adjacent chips are covered by a glass layer. This method has some drawbacks which make it difficult to carry it out. First, the adheive used for fixing the wafer to the substrate can contaminate the chips because it is electrically conductive. In practice, it is rarely sufficently effective to prevent the chips from being prematurely detached during mechanical cutting of the wafer. Furthermore, the parts of the metal substrate which remain free after subdivision are covered by a glass layer which is thicker than that covering the lateral parts of the chips, and thus subsequent separation of the chips is rather critical since there is a great risk of cracking, during this operation, the glass covering the junctions, thereby giving access to contaminating agents.

According to one aspect of the present invention, there is provided a method of passivating junction semiconductor elements which are formed from a wafer of semiconductor material, and which comprises at least two zones having opposite conductivity types defining one or more p-n junctions substantially parallel to the faces of the wafer and which elements are separated from one another by grooves formed in one face of the semiconductor wafer which grooves intersect and expose at least one p-n junction, and which grooves are defined by a layer shielding material which is undercut by the grooves, in which method a thin and uniform layer of passivating organic substance is applied to the shielding layer and the surfaces of the grooves at a temperature at which the shielding material is not affected, the parts of the shielding layer and the thin passivating layer overhanging the grooves are mechanically removed, and the remaining portion of the shielding layer and the thin passivating layer superimposed on it are removed by a process effected at a temperature which does not adversely affect the organic substance covering the surfaces of the grooves.

According to a second aspect of the present invention there is provided a method of manufacturing semiconductor chips in which p-n junction intersect lateral surfaces of the chips, which method comprises mounting one face of a wafer from which the chips are to be divided on a supporting structure, forming a mask of shielding material on the opposite face of the wafer, cutting grooves in the wafer along lines defined by the mask to undercut the mask and to divide the wafer into chips, depositing a passivating organic substance in the grooves and over the mask of shielding material at a temperature which does not adversely affect the shielding material, mechanically removing the shielding material overhanging the grooves and dissolving the shielding material to provide a plurality of individual chips attached to one another by means of the deposited layer of passivating organic substance.

The invention will be further described by way of example with reference to the accompanying drawings, in which Figs. 1 to 7 depict various stages on the manufacture of high-voltage power transistors of positive bevel "mesa" type.

In the accompanying drawings, a wafer of monocrystalline silicon doped with N-type impurities constituting the starting material is subjected to conventional diffusion, masking and photoengraving operations so as to obtain the structure illustrated in Fig. 1. This structure comprises a layer 1 the conductivity of which has remained the same as that of the starting material, and an N^+ conductivity layer 2 obtained by diffusing into the wafer N-type impurities, e.g. phosphorus. The N^+ layer has the function of creating a relatively low resistivity zone at the collector of the individual transistors which will be obtained from the wafer and its thickness is determined on the basis of design considerations mainly regarding the collector saturation voltage.

Subsequently, to form the bases of the transistors, a P-type impurity, e.g. boron, is diffused onto the face of the wafer opposite to that doped with N-type impurities (N^+ layer 2) to obtain a relatively high impurity concentration. A P layer 3 is thus obtained which has resistivity lower than that of the layer 1 disposed below it. Diffusion depth is adjusted so that the distance between the outer collector layer 2 and the base layer 3 is sufficient to withstand the required reverse collector voltage and

penetration of the corresponding space charge into the inner collector layer 1, while avoiding both excessive increase in the V_{CE}sat and excessive reduction in the maximum collector current of the transistors thus obtained.

The drawings show emitter zones 4 of the individual transistors. These zones are obtained by diffusing N-type impurities in predetermined zones of the surface of the layer 3 by using conventional masking and diffusion techniques. The distance between adjacent emitter zones depends on the dimensions and current characteristics of the transistors one wishes to obtain from the silicon wafer. Once the structure shown in Fig 1 has been obtained in the described manner, one proceeds to the formation of the metal contact zones for the terminals of the transistors on both faces of the wafer. For clarity such zones have not been shown in the drawings.

The successive working steps relate to the provision of a support structure for the wafer, subdivision of the wafer into chips, and passivation of the individual chips in accordance with the method of the present invention.

In the first step, the wafer is covered on both faces thereof with a layer of material surfaces of the wafer from acids which will surfaces of the wafer from acids which yill be subsequently used for etching the silicon. A suitable shielding material is a mixture of carnauba wax and paraffin (for simplicity this material is termed wax below). A layered structure comprising wax and a support film, e.g. filter paper, is prepared separately. The structure is then applied onto the face of the wafer, which has emitter zones, by causing first adhesion and then fusion and resoldification of the adjacent wax layers. A structure is thus obtained, generally indicated by 6 in Fig. 2, which comprises a support film 5 and two wax layers 6*a* and 6*b*. Its function is to permit subdivision of the wafer while maintaining the relative position of the chips unaltered, and to protect the upper surface of the transistors formed on the chips, the bottom of the wafer, i.e. the face opposite to that covered by the support structure is also covered with a wax layer 6*c* and is then mechanically cut to delimit the individual chips, as shown in Fig. 3. The cuts in the bottom of the wafer define a network of channels 7 which extend throughout the wax layer 6*c* and penetrate to a small extent into the silicon surface.

The wafer is then subjected to etching, *viz.* by using a nitric, hydrofluoric and acetic acid solution so as to increase the depth of the channels 7. Etching continues until the individual semiconducting chips are completely separated from one another, thereby obtaining transistors spaced from one another as shown in Fig. 4. The chips keep their mutual position owing to the support structure 6 to which they adhere. As is shown, acids act also beneath the protecting layer 6*c* and form undercuts partially closed by the protection layer and having inclined surfaces 8 as shown in the drawings. As mentioned above, the inclination of the lateral surfaces influences the electrical characteristics of the transistors. In the case of a high-voltage power transisitor, the inclination is estimated while designing the device so as to maximize the collector reverse bias voltage and minimize electrostatic fields on the lateral surfaces by taking into account the charge concentrations and the thicknesses of the various layers of the semiconductor structure. By varying the composition and/or the concentration of the etching acid solution, it is possible to obtain inclined surfaces in accordance with optimum design values.

Although in the application some steps of which have been described above etching has been used to form the lateral surfaces of the devices, it is known that to obtain the same result or a similar result mechanical engraving can be used instead of etching, or a combination of the two.

The grooves in the wafer, i.e., the lateral surfaces of the chips are passivated by being covered with a thin and uniform layer 9 consisting of an insulating organic substance of high purity (Figure 5). It has been found to be advantageous to use a polymer available under the Trade Mark "Parylene" which can be used at ambient temperature. In particular, the method of applying a thin layer of Parylene comprises heating a solid dimer under vacuum to obtain a gaseous double radical. When the molecules of the double radical are deposited on the cold surface of the wafer, they combine together to form a solid polymer having a high molecular weight. A complete and uniform covering of the surface subjected to the treatment is thus obtained owing to the penetration capacity of the vapour into each recess in the surface. The coating thus obtained is porefree and is extremely pure because it is obtained from a single starting material. This latter characteristic is very important for passivating the lateral surfaces of the chips since it eliminates the risk of surface contamination due to the passivating material itself which could impair the possibility of obtaining the electrical characteristics required in the transistor, especially the possibility of attaining high reverse collector voltages.

The parts of the protective layer 6*c* projecting over the grooves as a consequence of the undercutting and also coated with a thin layer of Parylene are removed by a

suitable mechanical procedure, such as by using conventional engraving and cutting apparatus, thereby obtaining the structure illustrated in Fig. 6. The wax layers are removed at ambient temperature by means of a suitable solvent. Together with the wax layers there are also removed the layer of filter paper 5 and the Parylene layer formed on the wax layer 6_C. The chips remain united by the Parylene layer formed on the bottom of the grooves, as shown in Fig. 7, and the transistors contained therein can be subjected to automatic or manual measurement of all their electrical parameters.

The subsequent operations comprising separation of the chips and their mounting in suitable containers are not described in detail here since they do not form part of the method of the present invention. It should be noted, however, that in order to weld the chips to the respective substrates use must be made of low-melting point alloys of the type usually adopted in the manufacture of power devices since at high temperatures the chemical and physical characteristics of the Parylene layer could be adversely affected.

The invention has been described with reference to its application to a "mesa" type transistor having positive bevel, but it should be understood that it could be used in the same way in the manufacture of "mesa" type transistor having a negative bevel. In that case the upper face of the wafer instead of the lower face would be etched, while inverting the positions of the support structure 6 and the wax layer 6c.

Although only one embodiment of the invention has been described and illustrated, many variants and modifications may be made within the scope of the present invention as set out in the appended claims. For example, the metal zones for the contacts of the transistor terminals could be formed after passivation by using methods and alloys which do not involve temperatures which might damage the Parylene layer. Furthermore, during passivation instead of the thin Parylene layer obtained by an evaporation under vacuum process, a suitable plastics material, such as polytetrafluorethylene could be deposited on the bottom of the wafer and in the grooves by means of an ion sputtering process.

WHAT WE CLAIM IS:—

1. A method of passivating junction semiconductor elements which are formed from a wafer of semiconductor material and which comprise at least two zones having opposite conductivity types defining one or more p-n junctions substantially parallel to the faces of the wafer and which elements are separated from one another by grooves formed in one face of the semiconductor wafer which grooves intersect and expose at least one p-n junction, and which grooves are defined by a layer shielding material which is undercut by the grooves, in which method a thin and uniform layer of passivating organic substance is applied to the shielding layer the surfaces of the grooves at a temperature at which the shielding material is not affected, the parts of the shielding layer and the thin passivating layer overhanging the grooves are mechanically removed, and the remaining portion of the shielding layer and the thin passivating layer superimposed on it are removed by a process effected at a temperature which does not adversely affect the organic substance covering the surfaces of the grooves.

2. A method as claimed in claim 1, in which at least one face of the wafer has one or more zones coated with a metal layer.

3. A method as claimed in claim 1 or 2, in which the thin layer of passivating substance is applied by depositing on the face of the wafer formed with grooves the vapour of an organic substance which polymerizes at ambient temperature.

4. A semiconductor device when obtained by the method as claimed in any one of the preceding claims.

5. A method of manufacturing semiconductor chips in which p-n junctions intersect lateral surfaces of the chips, which method comprises mounting one face of a wafer from which the chips are to be divided on a supporting structure, forming a mask of shielding material on the opposite face of the wafer, cutting grooves in the wafer along lines defined by the mask to undercut the mask and to divide the wafer into chips, depositing a passivating organic substance in the grooves and over the mask of shielding material at a temperature which does not adversely affect the shielding material, mechanically removing the shielding material overhanging the grooves and dissolving the shielding material to provide a plurality of individual chips attached to one another by means of the deposited layer of passivating organic substance.

6. A method as claimed in claim 5, in which the grooves are mechanically cut and are then etched.

7. A method as claimed in claim 5 or 6 in which the organic substance is deposited by heating a solid dimer under vacuum to produce a gas the molecules of which are

deposited and polymerize on the surface of the wafer.

8. A method of manufacturing semiconductor chips substantially as herein described with reference to and as illustrated in the accompanying drawings.

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Chartered Patent Agents

57-60 Lincolns Inn Fields,
London, WC2A 3LS.
Agent for the Applicant(s)

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1569931 COMPLETE SPECIFICATION

1 SHEET

This drawing is a reproduction of the Original on a reduced scale

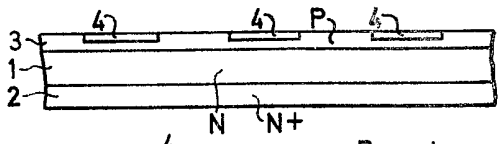

FIG. 1.

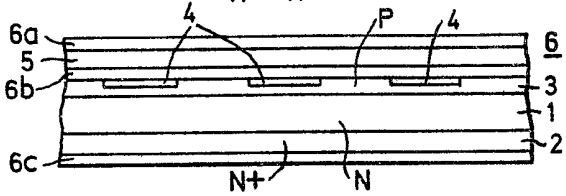

FIG. 2.

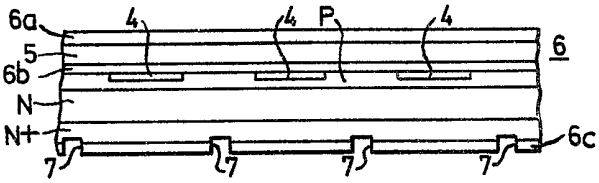

FIG. 3.

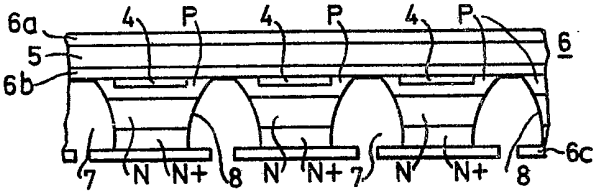

FIG. 4.

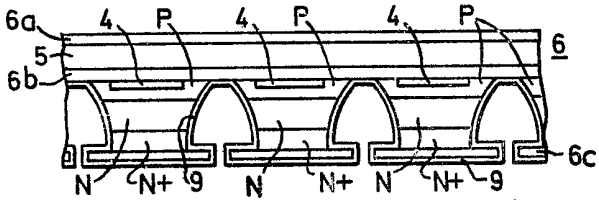

FIG. 5.

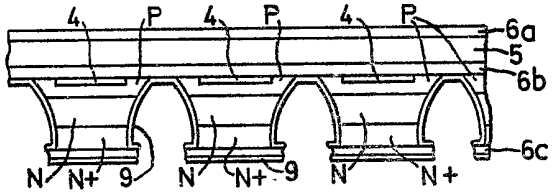

FIG. 6.

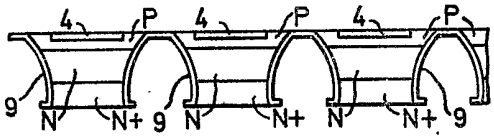

FIG. 7.