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MURATA MANUFACTURING CO., LTD. [JP/JP]; 10-1, Higashikotari 1-chome, Nagaokakyo-shi, Kyoto 617-8555 (JP).

(72) Inventor; and

(75) Inventor/Applicant (for US only): **GONSALVES, Joseph** [US/US]; c/o Murata Power Solutions, 11 Cabot Boulevard, Mansfield, MA 02048 (US).(74) Agent: **MEDLEY, Peter**; c/o Keating & Bennett, LLP, 1800 Alexander Bell Drive, Suite 200, Reston, VA 20191-5465 (US).

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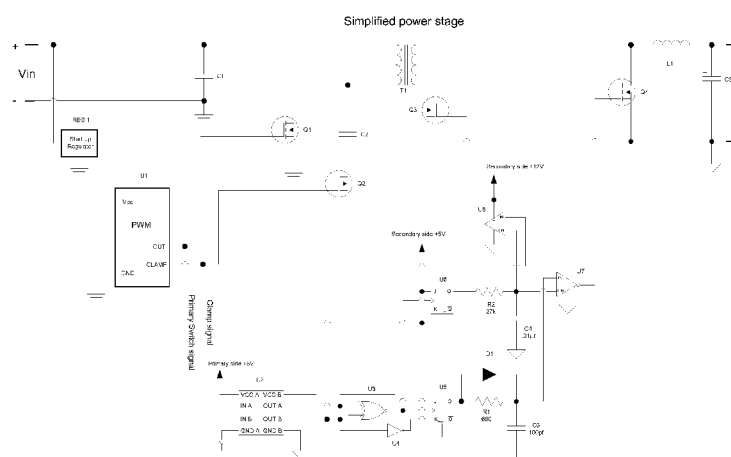


FIG. 2

(57) Abstract: A synchronous rectification circuit includes a transformer receiving an input voltage at a primary side and outputting an output voltage at a secondary side and a controller arranged and programmed to operate independently from the input and output voltages. The controller preferably outputs control signals to switching logic devices, the switching logic devices being arranged to output timing signals to drive individual synchronous rectifiers included in the secondary side of the transformer. The synchronous rectification circuit includes at least one logic gate which receives the control signals output from the controller and supplies clock signals to the switching logic devices, the clock signals being generated by the at least one logic gate based on the control signal and driving devices arranged to receive the timing signals from a respective one of the switching logic devices, the driving devices driving the synchronous rectifiers in accordance with the timing signals.

A CONTROL DRIVEN SYNCHRONOUS RECTIFIER SCHEME FOR ISOLATED ACTIVE CLAMP FORWARD POWER CONVERTERS

BACKGROUND OF THE INVENTION

1. Field of the Invention.

[0001] The present invention relates to power conversion, and in particular, to circuits that provide secondary control over synchronous rectifiers with load pre-bias, monotonic start-up, and dead time control.

2. Description of the Related Art

[0002] In a conventional power conversion system including an Active Clamp Pulse Width Modification controller that does not provide synchronous rectifier control signals (which is typically the most common arrangement), a self driven control scheme is often chosen. In a self driven control scheme, a self driven rectifier gate voltage varies with an input line voltage such that the self driven rectifier gate voltage may drop to a point where full enhancement of the self driven rectifier is no longer possible which thus impacts efficiency and/or exceeds safe operating limits. For example, in a self driven control scheme, when a needed output voltage is 12 volts or greater, the self driven rectifier gate voltage which is provided by a main transformer secondary winding will be at a level that is beyond safe operating limits of the self driven rectifiers.

[0003] In self driven or control driven schemes, i.e., driven with a Pulse Width Modulation (PWM) controller with secondary control outputs, a pre-bias condition on the output has the potential of creating a short circuit condition forcing the PWM controller into a current limiting protection scheme that the PWM controller will enter into to thereby make it impossible for the output of the power conversion system to ever develop. Additionally, in self driven or control driven schemes, there are no provisions for a monotonic startup. Finally, in a self driven control scheme, there is no dead time control of synchronous rectifiers such that, as an operating temperature of the power conversion system increases, the possibility of cross conduction also increases.

[0004] In an attempt to overcome the above problems, it has been proposed to use a main transformer secondary winding or an additional winding to provide a control signal/drive voltage (i.e., a self driven scheme). However, such an arrangement has a major drawback in which the control signal/drive voltage will vary with an input line voltage, which thereby leads to a possible reduction in efficiency or even a device failure unless specific safeguards are put in place.

[0005] In order to overcome the problems described above, it has also been proposed to keep an input voltage range small, such as a ratio of 2:1, so that the secondary voltage does not vary widely such that the secondary voltage will not exceed the safe operating limit of the synchronous rectifiers or drop below the enhancement level of the synchronous rectifiers. However, such a proposal significantly limits the number and type of applications in which such a power conversion system effectively operates.

[0006] Similarly, using shunt regulators to limit the drive voltage to be maintained within the safe operating limits of the synchronous rectifiers or using an additional winding on the main transformer which has a different turns ratio such that a scaled down drive voltage can be provided have also been proposed. However, both of these proposed arrangements result in an undesirable reduction in overall operating efficiency of the power conversion system.

[0007] Using a secondary controller that includes its own additional bias supply voltage or controlling a rate at which feedback begins its control of the power conversion system has also been proposed. However, this arrangement leads to more complex circuitry and also a corresponding increase in cost. Also, carefully choosing synchronous rectifiers with very fast turn off and very stable temperature characteristics has been proposed. The drawback with this is that it requires more exotic and expensive components with the potential for long lead times.

SUMMARY OF THE INVENTION

[0008] In order to overcome the problems described above, preferred embodiments of the present invention provide a control driven synchronous rectifier in which a controller is arranged to output control signals to at least two switching logic devices, the at least two switching logic devices each being arranged to output timing signals used to drive individual

ones of at least two synchronous rectifiers. The control driven synchronous rectifier makes it possible to provide more system control with predictable delays and also to prevent an input range of the voltage input into the control driven synchronous rectifier from influencing the output voltage of the control driven synchronous rectifier.

[0009] A synchronous rectification circuit according to a preferred embodiment of the present invention preferably includes a transformer arranged to receive an input voltage at a primary side and output an output voltage at a secondary side and a controller arranged and programmed to operate independently from the input voltage and the output voltage. The controller is preferably arranged to output control signals to at least two switching logic devices, each of the at least two switching logic devices being arranged to output timing signals used to drive individual ones of at least two synchronous rectifiers included in the secondary side of the transformer.

[0010] The synchronous rectification circuit according to the above described preferred embodiment also preferably includes at least one logic gate arranged to receive the control signals output from the controller and to supply clock signals to the at least two switching logic devices, the clock signals being generated by the at least one logic gate based on the control signal and at least two driving devices arranged to receive the timing signals from a respective one of the at least switching logic devices, the at least two driving devices being arranged to drive the individual ones of the at least two synchronous rectifiers in accordance with the timing signals. The at least two driving devices being, for example, MOSFET drivers.

[0011] Each of the at least two driving devices are preferably arranged to receive timing signals from a same one of the at least two switching logic devices. One of the at least two driving devices is preferably arranged to receive one of the control signals output from the controller. A synchronous rectification circuit according to another preferred embodiment preferably includes a digital isolator arranged between the controller and the two at least switching logic devices, the at least one logic gate, and the at least two driving devices. The digital isolator is arranged to receive the control signals from the controller and then to output the control signals.

[0012] The control signals of a synchronous rectification circuit according to a preferred embodiment of the present invention preferably include a first control signal and a second control signal, the at least one logic gate being arranged to generate one of the clock signals based on the first control signal and the second control signal. Here, at least one logic gate is arranged to generate the one of the clock signals such that a rising edge of the first control signal corresponds to a rising edge of the one of the clock signals and a rising edge of the second control signal corresponds to a falling edge of the one of the clock signals on a first pulse of the one of the clock signals; and on a next clock pulse of the one of the clock signals, falling edges of the first control signal and the second control signal correspond to the next clock pulse. It is preferable that the first control signal is a clamp signal and the second control signal is a primary switching signal, for example.

[0013] Preferably, one of the at least two switching logic devices is arranged to generate a freewheeling signal based on the one of the clock signals, the freewheeling signal being input into one of the at least two driving devices. The one of the at least two switching logic devices which is arranged to generate the freewheeling signal is preferably arranged to generate the freewheeling signal based on one of the first control signal and the second control signal and also based on signals output from the at least one logic gate. The freewheeling signal supplied to the one of the at least two driving devices is preferably delayed due to, for example, a resistor, a diode, and a capacitor connected to an output of the same one of the at least two switching logic devices. Also, the timing signals received by each of the at least two driving devices from the same one of the at least switching logic devices are preferably delayed, this delay preferably being caused by a resistor and a capacitor connected to an output of the same one of the at least two switching logic devices.

[0014] The synchronous rectification circuit according to a preferred embodiment of the present invention may also include a start-up regulator arranged to supply power to the controller.

[0015] Preferably, in various preferred embodiments of the present invention, the at least two switching logic devices are flip-flops, the at least one logic gate includes an exclusive OR gate, and the at least two driving devices are op-amps, for example.

[0016] The above and other features, elements, characteristics, steps and advantages of the present invention will become more apparent from the following detailed description of preferred embodiments of the present invention with reference to the attached drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0017] Fig. 1 is a circuit diagram showing a power converter in accordance with a preferred embodiment of the present invention.

[0018] Fig. 2 is a circuit diagram showing a power converter in accordance with another preferred embodiment of the present invention.

[0019] Fig. 3 is a timing diagram in accordance with a preferred embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0020] Preferred embodiments of the present invention will be described below with reference to the accompanying drawing.

[0021] A preferred embodiment of a power conversion system in accordance with the present invention preferably includes a synchronous rectifier with an active clamp forward converter. Fig. 1 shows a simplified circuit of an output section of a synchronous rectifier in accordance with a preferred embodiment of the present invention. The synchronous rectifier preferably includes a transformer T1, an output filter inductor L1, and an output filter capacitor C3. The synchronous rectifier also preferably includes a digital isolator U2 arranged to receive control signals from a host PWM controller (not shown in Fig. 1), the control signals preferably including a Clamp signal and a Primary Switch signal. The digital isolator U2 is arranged to output signals OUT A and OUT B that are needed to create the synchronous rectifier's control signals.

[0022] The output signals OUT A and OUT B of the digital isolator U2 are input into an exclusive NOR gate U3 and an inverter U4. The exclusive NOR gate U3 is arranged to create a clock signal for a flip-flop U5 and the inverter U4 is arranged to invert the Primary Switch signal output from OUT B of the digital isolator U2 and then input this inverted signal into the K input

of the flip-flop U5. The output of the flip-flop U5 is arranged to provide a secondary control signal used for the synchronous rectifier, where a resistor R1, a diode D1, and a capacitor C5 are arranged to provide additional dead time delay to the output of the flip-flop U5.

[0023] The power conversion system shown in Fig. 1 further includes a forward synchronous rectifier Q3 and a freewheeling synchronous rectifier Q4. The forward synchronous rectifier Q3 is preferably driven by a non-inverting driver U8 which is controlled in part by being connected to the OUT B signal of the digital isolator U2. The freewheeling synchronous rectifier Q4 is preferably driven by an inverting driver U7 which is controlled in part by being connected to the output of the flip-flop U5. Additionally, both of the non-inverting driver U8 and the inverting driver U7 are arranged to receive an output from a flip-flop U6. The output of the flip-flop U6 is arranged to slowly charge a capacitor C4 through a resistor R2 such that a pre-bias startup delay will occur before the non-inverting driver U8 and the inverting driver U7 are enabled. The inverting driver U7 and the non-inverting driver preferably being provided by, for example, MOSFET drivers.

[0024] Accordingly, by using the above described arrangement, the synchronous rectifier control signals used to drive the forward synchronous rectifier Q3 and the freewheeling synchronous rectifier Q4 are created by the Primary Switch control signal from the host PWM controller (not shown in Fig. 1) and not from a main transformer, such as transformer T1. Thus, it is possible to thereby provide more system control with predictable delays and with far less development effort. Additionally, because the synchronous rectifier drive voltage of the forward synchronous rectifier Q3 and the freewheeling synchronous rectifier Q4 is derived from an auxiliary bias supply and not from the main transformer, an input range of the voltage input into the power conversion system does not have any influence over the output of the forward synchronous rectifier Q3 and the freewheeling synchronous rectifier Q4.

[0025] In addition, both of the forward synchronous rectifier Q3 and the freewheeling synchronous rectifier Q4 have their outputs fully enhanced such that the synchronous rectifier Q3 and the freewheeling synchronous rectifier Q4 will be fully on (which is a state similar to when a transistor becomes saturated), thereby keeping overall efficiency high across the input

range of the voltage input into the power conversion system which thereby results in a wider input range that can be used economically. Further, the synchronous rectifier drive voltage is fixed, is derived from an auxiliary bias supply, and is chosen to be in the safe operating range of the synchronous rectifiers to thereby avoid a possibility that the forward synchronous rectifier Q3 and the freewheeling synchronous rectifier Q4 will be operated beyond their safe operating limits.

[0026] Finally, because the control signals of the non-inverting driver U8 and the inverting driver U7 are delayed for a small amount of time because the output of the flip-flop U6 is arranged to slowly charge a capacitor C4 through a resistor R2, the resulting pre-bias startup delay to both of the forward synchronous rectifier Q3 and the freewheeling synchronous rectifier Q4 allow the body diodes of the forward synchronous rectifier Q3 and the freewheeling synchronous rectifier Q4 to conduct and develop output voltages prior to full synchronous operation. Thus works to prevent the pre-bias voltage from creating a short circuit situation. Similarly, because the control signals of the non-inverting driver U8 and the inverting driver U7 have delays introduced, a body diode conduction of the synchronous rectifiers provides a smooth rise of the desired output voltage before enabling full synchronous rectification. The required dead time provided by diode D1, resistor R1, and capacitor C1 is added to prevent cross conduction during higher temperatures.

[0027] Another preferred embodiment of a power conversion system in accordance with the present invention will now be described with reference to Fig. 2. Fig. 2 shows a simplified circuit of a power stage of a power conversion system including a synchronous rectifier with an active clamp forward converter. The preferred embodiment shown in Fig. 2 includes elements similar to those described above with reference to Fig. 1. For the sake of simplicity, these similar elements include the same reference characters as those described above with reference to Fig. 1.

[0028] The preferred embodiment of the synchronous rectifier shown in Fig. 2 preferably includes a transformer T1, primary side transistors Q1 and Q2, an input filter capacitor C1, a capacitor C2 connected to the collectors of the primary side transistors Q1 and Q2, an output filter inductor L1, and an output filter capacitor C3. The synchronous rectifier also

preferably includes a digital isolator U2 arranged to receive control signals from a host PWM controller U1, which receives power from a Start up Regulator REG 1. The Start Up Regulator REG 1 is arranged to provide a bias voltage to the host PWM controller U1. Start up Regulator REG 1 is preferably a series type regulator that regulates input voltage for the PWM. Once the converter is up and running, an auxiliary voltage is created that will provide slightly higher operating voltage that in a sense shuts off the Start Up Regulator REG 1. The control signals from the host PWM controller U1 preferably include a Clamp signal and a Primary Switch signal. The digital isolator U2 is arranged to output signals OUT A and OUT B that are needed to create the synchronous rectifier's control signals.

[0029] The output signals OUT A and OUT B of the digital isolator U2 are inputs into an exclusive NOR gate U3 and an inverter U4. The exclusive NOR gate U3 is arranged to create a clock signal for a flip-flop U5 and the inverter U4 is arranged to invert the Primary Switch signal output from OUT B of the digital isolator U2 and then input this inverted signal into the K input of the flip-flop U5. The output of the flip-flop U5 is arranged to provide a secondary control signal used for the freewheeling synchronous rectifier, where a resistor R1, a diode D1, and a capacitor C5 are arranged to provide additional dead time delay to the output of the flip-flop U5.

[0030] The power conversion system shown in Fig. 2 further includes a forward synchronous rectifier Q3 and a freewheeling synchronous rectifier Q4. The forward synchronous rectifier Q3 is preferably driven by a non-inverting driver U8 which is controlled in part by being connected to the OUT B signal of the digital isolator U2. As shown in Fig. 2, this signal is the isolated Primary Switch control signal, the Primary Switch control signal also controls the primary side transistor Q1. The freewheeling synchronous rectifier Q4 is preferably driven by an inverting driver U7 which is controlled in part by being connected to the output of the flip-flop U5. Additionally, both of the non-inverting driver U8 and the inverting driver U7 are arranged to receive an output from a flip-flop U6. The output of the flip-flop U6 is arranged to slowly charge a capacitor C4 through a resistor R2 such that a pre-bias startup delay will occur before the non-inverting driver U8 and the inverting driver U7 are enabled. The inverting driver U7 and the non-inverting driver preferably being provided by, for example, MOSFET drivers.

[0031] As discussed above, both of the isolated Primary Switch signal and the isolated Clamp signal from the digital isolator U2 are sent to the exclusive NOR gate U3. The exclusive NOR gate U3 is arranged to generate a clock signal needed by both the flip-flop U5 and the flip-flop U6 as follows; the rising edge of the Clamp signal 1 defines the rising edge of the Clock signal 3. The rising edge of the Primary Switch signal 2 defines the falling edge of the Clock signal 3. On the next pulse of the Clock signal 3, the falling edges of the isolated Clamp signal 1 and the Primary Switch signal 2 are used to create the clock pulse of the Clock signal 3. This Clock signal 3 is then used to extract the SR freewheeling signal 4. See the timing diagram shown in Fig. 3.

[0032] The SR freewheeling signal 4 is extracted as follows: the isolated Clamp signal 1 is supplied to the J input of the flip-flop U5 and an inverted version of the isolated Primary Switch signal 2 generated by the inverter U4 is supplied to the K input of the flip-flop U5. The flip-flop U5 processes the signal needed for freewheeling synchronous rectifier Q4. The flip-flop U5's input clock pin uses the rising edges of the isolated Clamp signal 1 and the Primary Switch signal 2 to extract the necessary edges from both the J and K pins to thereby create the SR freewheel signal 4. As can be seen in the timing diagram of Fig. 3, the SR freewheel signal 4 is never on when the Primary Switch signal 2 is on and is in fact delayed by a small amount by the circuit defined by the diode D1, the resistor R1, and the capacitor C5. This small amount of delay is needed to prevent cross conduction between primary and secondary conduction times of the synchronous rectifier.

[0033] The Pre-bias startup delay enable signal 5 is also shown in the timing diagram of Fig. 3. The Pre-bias startup delay enable signal 5 requires a few cycles from the flip-flop U6 to charge the capacitor C4 through the resistor R2. This delay holds the enable pins of both non-inverting driver U8 and the inverting driver U7 at a low voltage level for a short time, allowing body diode conduction time of the synchronous rectifiers Q3 and Q4 to freewheel and thereby preventing any voltage present at the output from creating a short circuit condition on startup. This delay also provides monotonic startup of the output voltage should no Pre-bias condition be present. The Pre-bias startup delay is preferably set to be long enough for body diode

conduction of the synchronous rectifiers to provide a smooth rise of the desired output voltage before enabling full synchronous rectification.

[0034] Accordingly, by using the above described arrangement, the synchronous rectifier control signals used to drive the forward synchronous rectifier Q3 and the freewheeling synchronous rectifier Q4 are created by the Primary Switch control signal from the host PWM controller (not shown in Fig. 1) and not from a main transformer, such as transformer T1. Thus, it is possible to thereby provide more system control with predictable delays and with far less development effort. Additionally, because the synchronous rectifier drive voltage of the forward synchronous rectifier Q3 and the freewheeling synchronous rectifier Q4 is derived from an auxiliary bias supply and not from the main transformer, an input range of the voltage input into the power conversion system does not have any influence over the output of the forward synchronous rectifier Q3 and the freewheeling synchronous rectifier Q4.

[0035] Furthermore, both of the forward synchronous rectifier Q3 and the freewheeling synchronous rectifier Q4 have their outputs fully enhanced such that the synchronous rectifier Q3 and the freewheeling synchronous rectifier Q4 will be fully on (which is a state similar to when a transistor becomes saturated), thereby keeping overall efficiency high across the input range of the voltage input into the power conversion system which thereby results in a wider input range that can be used economically. Further, the synchronous rectifier drive voltage is fixed, is derived from an auxiliary bias supply, and is chosen to be in the safe operating range of the synchronous rectifiers to thereby avoiding a possibility that the forward synchronous rectifier Q3 and the freewheeling synchronous rectifier Q4 will be operated beyond their safe operating limits.

[0036] Finally, because the control signals of the non-inverting driver U8 and the inverting driver U7 are delayed for a small amount of time because the output of the flip-flop U6 is arranged to slowly charge a capacitor C4 through a resistor R2, the resulting pre-bias startup delay to both of the forward synchronous rectifier Q3 and the freewheeling synchronous rectifier Q4 allow the body diodes of the forward synchronous rectifier Q3 and the freewheeling synchronous rectifier Q4 to conduct and develop output voltages prior to full

synchronous operation. This works to block and prevent the pre-bias voltage from creating a short circuit situation. Similarly, because the control signals of the non-inverting driver U8 and the inverting driver U7 have delays introduced, body diode conduction of the synchronous rectifiers provide a smooth rise of the desired output voltage before enabling full synchronous rectification. The required dead time provided by the diode D1, the resistor R1, and the capacitor C1 is added to prevent cross conduction during higher temperatures.

[0037] It should be understood that the foregoing description is only illustrative of the present invention. Various alternatives and modifications can be devised by those skilled in the art without departing from the present invention. Accordingly, the present invention is intended to embrace all such alternatives, modifications, and variances that fall within the scope of the appended claims.

[0038] For example, it would be possible to use a signal transformer instead of the digital isolator U2 described above. Additionally, for non-isolated designs, the digital isolator could be eliminated all together.

[0039] While preferred embodiments of the present invention have been described above, it is to be understood that variations and modifications will be apparent to those skilled in the art without departing from the scope and spirit of the present invention. The scope of the present invention, therefore, is to be determined solely by the following claims.

WHAT IS CLAIMED IS:

1. A synchronous rectification circuit, comprising:
 - a transformer arranged to receive an input voltage at a primary side and output an output voltage at a secondary side;
 - a controller arranged and programmed to operate independently from the input voltage and the output voltage, the controller arranged to output control signals;
 - at least two switching logic devices each being arranged to output timing signals used to drive individual ones of at least two synchronous rectifiers included in the secondary side of the transformer;
 - at least one logic gate arranged to receive the control signals output from the controller and to supply clock signals to the at least two switching logic devices, the clock signals being generated by the at least one logic gate based on the control signals; and
 - at least two driving devices arranged to receive the timing signals from a respective one of the at least switching logic devices, the at least two driving devices being arranged to drive the individual ones of the at least two synchronous rectifiers in accordance with the timing signals.
2. The synchronous rectification circuit according to Claim 1, wherein each of the at least two driving devices are arranged to receive timing signals from a same one of the at least two switching logic devices.
3. The synchronous rectification circuit according to Claim 2, wherein one of the at least two driving devices is arranged to receive one of the control signals output from the controller.
4. The synchronous rectification circuit according to Claim 1, further comprising a digital isolator arranged between the controller and the two at least switching logic devices, the at least one logic gate, and the at least two driving devices; wherein

the digital isolator is arranged to receive the control signals from the controller and then to output the control signals.

5. The synchronous rectification circuit according to Claim 1, wherein the control signals include a first control signal and a second control signal, the at least one logic gate being arranged to generate one of the clock signals based on the first control signal and the second control signal.

6. The synchronous rectification circuit according to Claim 5, wherein the at least one logic gate is arranged to generate the one of the clock signals such that:

on a first pulse of the one of the clock signals, a rising edge of the first control signal corresponds to a rising edge of the one of the clock signals and a rising edge of the second control signal corresponds to a falling edge of the one of the clock signals; and

on a next clock pulse of the one of the clock signals, falling edges of the first control signal and the second control signal correspond to the next clock pulse.

7. The synchronous rectification circuit according to Claim 5, wherein the first control signal is a clamp signal and the second control signal is a primary switching signal.

8. The synchronous rectification circuit according to Claim 6, wherein one of the at least two switching logic devices is arranged to generate a freewheeling signal based on the one of the clock signals, the freewheeling signal being input into one of the at least two driving devices.

9. The synchronous rectification circuit according to Claim 8, wherein the one of the at least two switching logic devices is arranged to generate the freewheeling signal based on one of the first control signal and the second control signal and also based on signals output from the at least one logic gate.

10. The synchronous rectification circuit according to Claim 2, wherein the timing signals received by each of the at least two driving devices from the same one of the at least switching logic devices are delayed.

11. The synchronous rectification circuit according to Claim 10, wherein the delay in the timing signals is caused by a resistor and a capacitor connected to an output of the same one of the at least two switching logic devices.

12. The synchronous rectification circuit according to Claim 8, wherein the freewheeling signal supplied to the one of the at least two driving devices is delayed.

13. The synchronous rectification circuit according to Claim 12, wherein the delay in the freewheeling signal is caused by a resistor, a diode, and a capacitor connected to an output of the same one of the at least two switching logic devices.

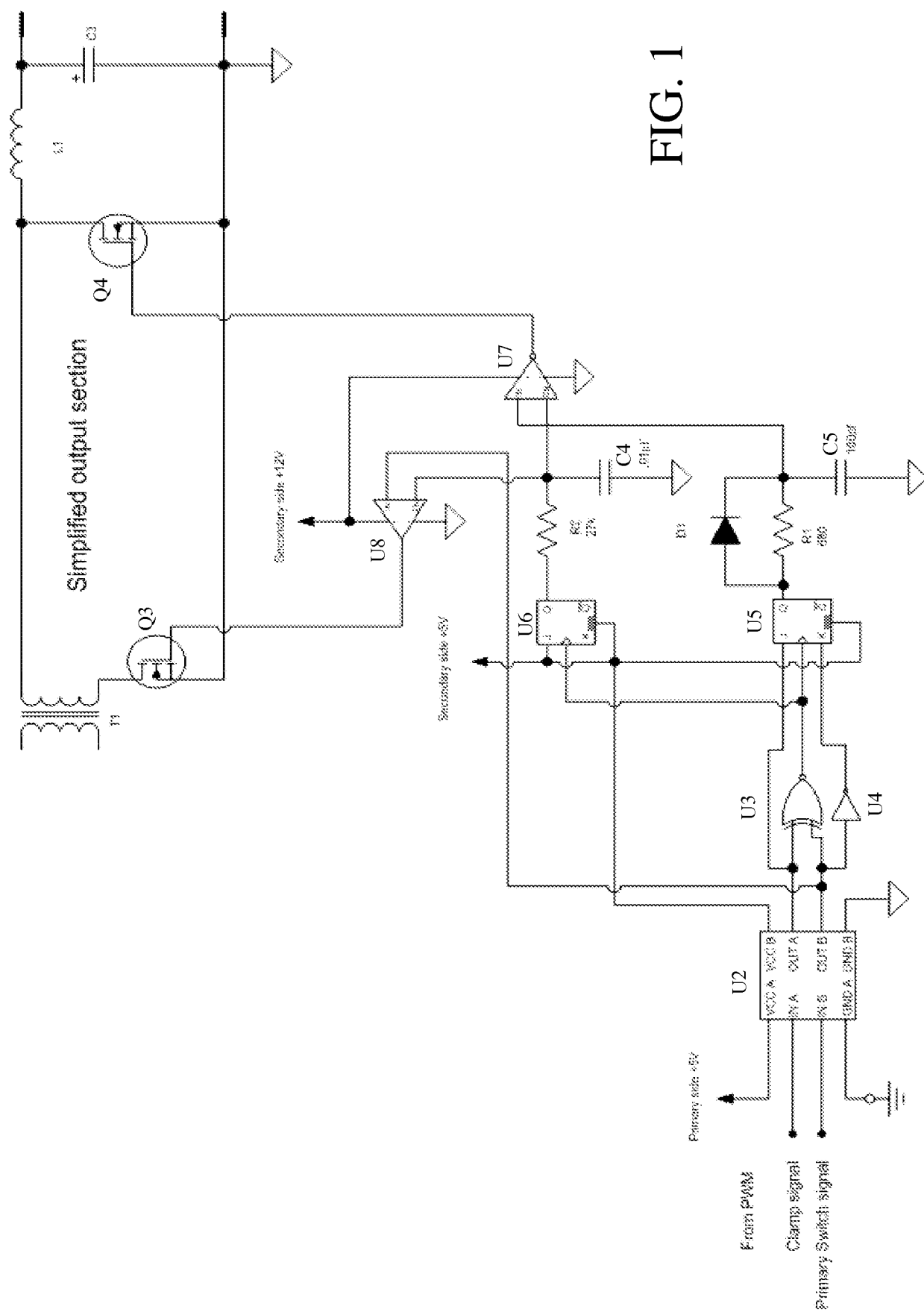
14. The synchronous rectification circuit according to Claim 1, further comprising a start up regulator arranged to supply power to the controller.

15. The synchronous rectification circuit according to Claim 1, wherein the at least two switching logic devices are flip-flops.

16. The synchronous rectification circuit according to Claim 1, wherein the at least one logic gate includes an exclusive OR gate.

17. The synchronous rectification circuit according to Claim 1, wherein the at least two driving devices are MOSFET drivers.

18. The synchronous rectification circuit according to Claim 1, wherein the synchronous rectification circuit is arranged to define an active clamp forward converter.



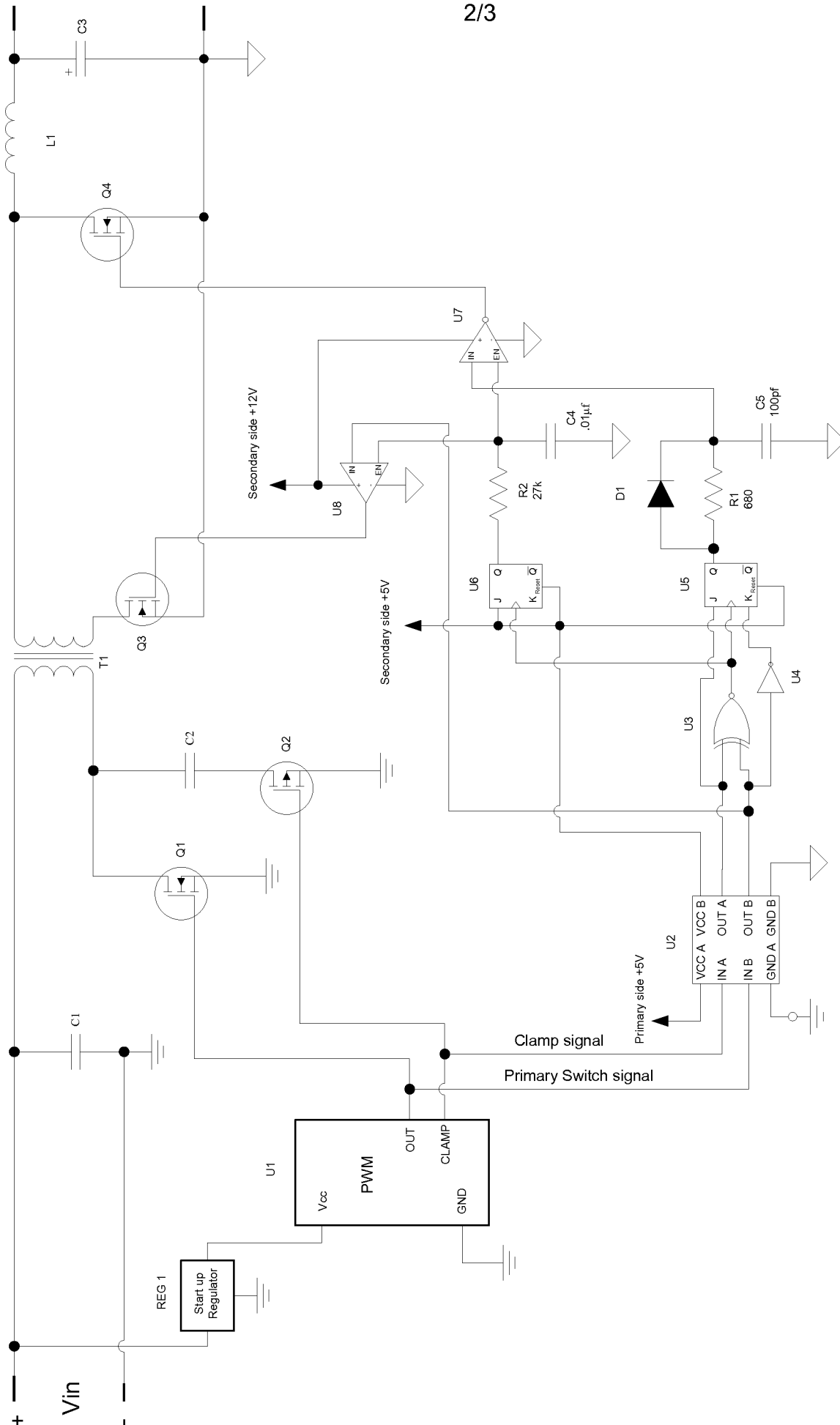


FIG. 2

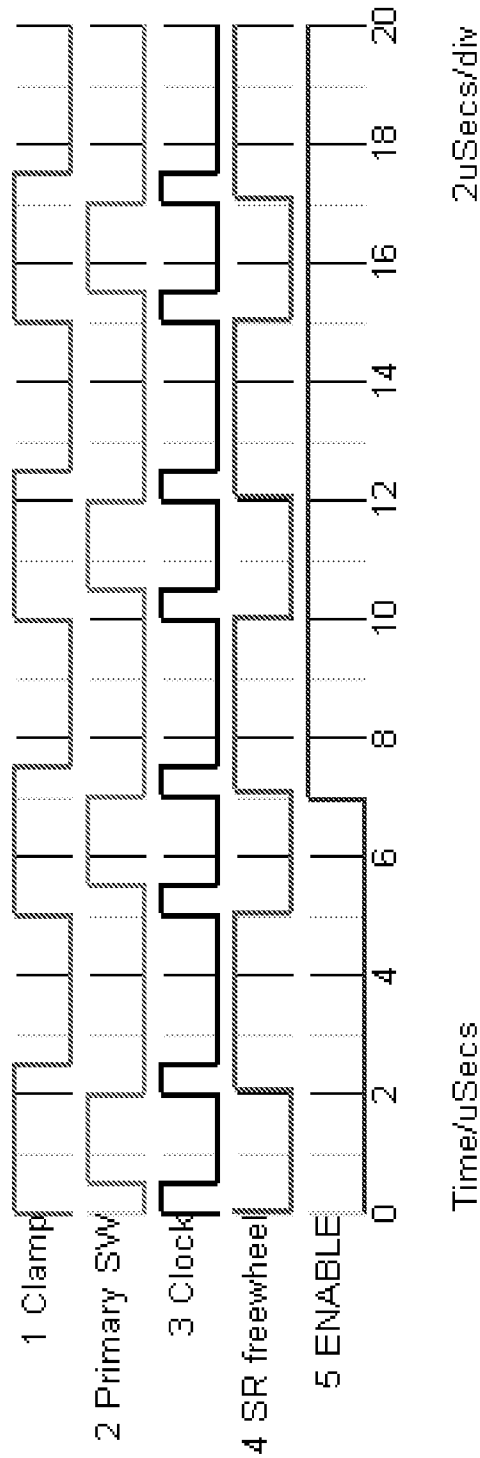


FIG. 3