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[Continued on next page]

(54) Title: AMPLIFIER OFFSET AND NOISE REDUCTION IN A MULTISTAGE SYSTEM

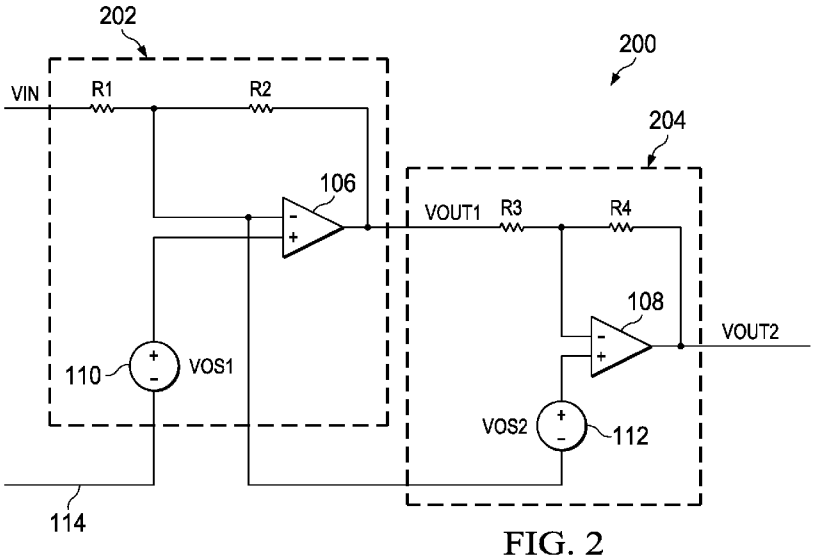

FIG. 2

(57) Abstract: A system, method and graphical user interface display for validating, monitoring and otherwise reviewing the sales and distribution of medicines, to reduce the instances of counterfeit medicines. A pharmaceutical company provides medicines to users, either directly or through representatives for the pharmaceutical company. The products have associated identifying codes that are used to track the sales of the products. The system provides verifications of the medicines, as well as statistical analysis of the sales and distribution. The verifications and comparisons of the distribution and sales of the medicines can be reviewed by the user or on a dashboard user interface. The system further allows pharmaceutical companies provided the medicines to provide response messages to users.

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— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

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AMPLIFIER OFFSET AND NOISE REDUCTION IN A MULTISTAGE SYSTEM

[0001] The invention relates generally to multistage amplifier system and, more particularly, to multistage amplifier system having reduced noise and offset.

BACKGROUND

[0002] FIG. 1 shows a conventional two-stage amplifier system 100 can be seen. System 100 generally comprise a first stage 102 and a second stage 104 (which are each generally inverting amplifiers). As can be seen, resistor networks (resistors R1/R1 and resistors R3/R4) are coupled between the negative input terminals and output terminals of operational amplifiers 106 and 108, respectively, so that stage 102 can receive the input signal VIN and that stage 104 can receive output signal VOUT1. Additionally, offset voltage source 110 and 112 provide offset voltages VOS1 and VOS2 to operational amplifiers 106 and 108, respectively. Each of the voltage sources 110 and 112 (which include the internal offsets of amplifiers 106 and 108) are also coupled to supply rail 114 (which is generally at ground).

[0003] Because of the configuration of system 100 offset and noise contributions from voltage source 110 can significantly affect the output signal VOUT2. For the amplifier stage 102, output signal VOUT1 can be represented as follows:

$$VOUT1 = \frac{-R2}{R1}(VIN - VOS1) + VOS1 \quad (1)$$

Additional, amplifier stage 104, output signal VOUT2 can be represented as follows:

$$VOUT2 = \frac{-R4}{R3}(VOUT1 - VOS2) + VOS2 \quad (2)$$

Now, substituting equation (1) into equation (2), output signal VOUT2 becomes:

$$\begin{aligned} VOUT2 &= \frac{-R4}{R3}\left(\frac{-R2}{R1}(VIN - VOS1) + VOS1 - VOS2\right) + VOS2 \\ &= \frac{R4 \cdot R2}{R3 \cdot R1}VIN + \frac{-R4}{R3}\left(\left(\frac{R2}{R1} + 1\right)VOS1 - VOS2\right) + VOS2 \end{aligned} \quad (3)$$

Equation (3) can also be expressed as a function of offset voltage VOS1 (where offset voltage VOS2 is about 0):

$$VOUT2 = \frac{R4 \cdot R2}{R3 \cdot R1} VIN + \frac{-R4}{R3}\left(\frac{R2}{R1} + 1\right) VOS1 \quad (4)$$

When resistor R1 is coupled to a block capacitor (AC coupled), the input signal VIN is equal to offset voltage VOS1, reducing equation (3) as follows:

$$\begin{aligned} VOUT2 &= \frac{-R4}{R3}(VOS1 - VOS2) + VOS2 \\ &= \left(1 + \frac{R4}{R3}\right) VOS2 - \frac{R4}{R3} VOS1 \end{aligned} \quad (5)$$

So, it can clearly be see from the DC coupled and AC coupled cases of equations (3) through (5), respectively, that noise and offset contributions in output voltage VOUT2 from offset voltage VOS1 can be significant. Thus, system 100 may require the use of trim circuit or better device matching to reduce the noise and offset contributions from offset voltage VOS1.

[0004] Some other conventional designs are described in: U.S. Patent Nos. 3,899,743; 5,257,285; 6,642,783; 7,132,882; and U.S. Patent Publ. No. 2006/0279344.

SUMMARY

[0005] An example embodiment of the invention provides an comprising a first amplifier stage having an input terminal and an output terminal, wherein the first amplifier receives an input signal at its input terminal, and wherein the first amplifier stage includes a first offset voltage source that provide a first offset voltage to the first amplifier stage and that is coupled to a supply rail; and a second amplifier stage having an input terminal and an output terminal, wherein the input terminal of the second amplifier stage is coupled to the output terminal of the first amplifier stage, and wherein the second amplifier offset includes a second offset voltage source that provides a second offset voltage to the second amplifier stage, and wherein the second offset voltage source is coupled to the first amplifier stage so as to substantially reduce noise contribution from the first offset voltage.

[0006] In accordance with an example embodiment of the invention, the first and second amplifiers stages further comprise a first inverting amplifier and a second inverting amplifier, respectively.

[0007] In accordance with an example embodiment of the invention, the first inverting amplifier further comprises: an operational amplifier having a first input terminal, a second input terminal, and an output terminal, wherein the second offset voltage source is coupled to the first input terminal of the operational amplifier, and wherein the first voltage offset source is coupled to the second input terminal of the operational amplifier; and a resistor network coupled to the input terminal of the first inverting amplifier, the first input terminal of the operational amplifier, and the output terminal of the operational amplifier.

[0008] In accordance with an example embodiment of the invention, the resistor network further comprises a plurality of resistors coupled in series with one another.

[0009] In accordance with an example embodiment of the invention, the first input terminal of the operational amplifier is a negative input terminal, and wherein the second input terminal of the operational amplifier is a positive input terminal.

[0010] In accordance with an example embodiment of the invention, the second inverting amplifier further comprises: an operational amplifier having a first input terminal, a second input terminal, and an output terminal, wherein the second voltage offset source is coupled to the second input terminal of the operational amplifier; and a resistor network coupled to the output terminal of the first inverting amplifier, the first input terminal of the operational amplifier, and the output terminal of the operational amplifier.

[0011] In accordance with an example embodiment of the invention, the first input terminal of the operational amplifier is a negative input terminal, and wherein the second input terminal of the operational amplifier is a positive input terminal.

[0012] In accordance with an example embodiment of the invention, an apparatus is provided. The apparatus comprises a first inverting amplifier having: a first resistor that receives an input signal; a first operational amplifier having a positive input terminal, an negative input terminal, and an output terminal, wherein the negative input terminal is coupled to the first resistor; a second resistor that is coupled between the output terminal of the first operational amplifier and the negative input terminal of the first operational amplifier; and a first offset voltage source that is coupled between the positive input terminal of the first operational

amplifier and ground; and a second inverting amplifier having: a third resistor that is coupled to the output terminal of the first operational amplifier; a second operational amplifier having a negative input terminal, a positive input terminal, and an output terminal, wherein the negative input terminal of the second operational amplifier is coupled to the third resistor; a fourth resistor that is coupled between the output terminal of the second operational amplifier and the negative input terminal of second operational amplifier; and a second offset voltage source that is coupled between the positive input terminal of the second operational amplifier and the negative input terminal of the first operational amplifier.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] Example embodiments are described with reference to accompanying drawings, wherein:

[0014] FIG. 1 is an example of a conventional multistage system; and

[0015] FIG. 2 is an example of a multistage system in accordance with an example embodiment of the invention.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0016] FIG. 2 illustrates a multistage system 200 in accordance with an example embodiment of the invention. System 200 generally comprises amplifiers stages 202 and 204 (which are generally inverting amplifiers). When compared to system 100, system 200 has the same general components. One difference, however, is the coupled to voltage source 112 and the negative input terminal of operational amplifier 106 instead of supply rail 114. By making this change, the output voltage VOUT1 is represented as follows:

$$VOUT2 = \frac{-R4}{R3}\left(VOUT1 - (VOS1 + VOS2)\right) + (VOS1 + VOS2) \tag{6}$$

If equation (1) is substituted into equation (6), it becomes:

$$\begin{aligned} VOUT2 = & \\ & \frac{-R4}{R3}\left(\frac{-R2}{R1}\left(VIN - VOS1\right) + VOS1 - (VOS1 + VOS2)\right) + (VOS1 + VOS2) \\ & = \frac{-R4}{R3}\left(\frac{-R2}{R1}\left(VIN - VOS1\right) - VOS2\right) + (VOS1 + VOS2) \\ & = \frac{R4 \cdot R2}{R3 \cdot R1} VIN + \frac{-R4}{R3}\left(\frac{R2}{R1} VOS1 - VOS2\right) + (VOS1 + VOS2) \end{aligned} \tag{7}$$

Equation (7) can also be expressed as a function of offset voltage VOS1 (where offset voltage VOS2 is about 0):

$$(8)\quad \begin{aligned} VOUT2 &= \frac{R4\cdot R2}{R3\cdot R1}VIN + \frac{-R4}{R3}\left(\frac{R2}{R1}VOS1\right) + VOS1 \\ &= \frac{R4\cdot R2}{R3\cdot R1}VIN + \left(1-\frac{R4\cdot R2}{R3\cdot R1}\right)VOS1 \end{aligned}$$

Additionally, when resistor R1 is coupled to a block capacitor (AC coupled), the input signal VIN is equal to offset voltage VOS1, reducing equation (7) as follows:

$$(9)\quad VOUT2 = \frac{R4}{R3}VOS2 + (VOS1 + VOS2) = \left(\frac{R4}{R3}+1\right)VOS2 + VOS1$$

As can clearly be seen by comparing equation (5) to equation (9) and equation (4) to equation (8), offset contributions from offset voltage VOS1 in output signal VOUT2 can be significantly reduced. Additionally, for noise contributions, the same analysis would apply to a noise analysis, leading a reduced noise in system 200 as compared to system 100.

[0017] As an example, these types of cascaded arrangements are typically used for single ended to differential conversion, where the differential output voltage $V_{OUTDiff}$ is:

$$(10)\quad V_{OUTDiff} = VOUT1 - VOUT2$$

One can substitute equation (1) and (2) (for the conventional system 100) into equation (10) to arrive at the differential output voltage $V_{OUTDiff}$, which becomes:

$$(11)\quad \begin{aligned} V_{OUTDiff} &= VOUT1 - VOUT2 = VOU1 + \frac{R4}{R3}(VOUT1 - VOS2) - VOS2 \\ &= \left(1+\frac{R4}{R3}\right)VOUT1 - \left(1+\frac{R4}{R3}\right)VOS2 \\ &= \left(1+\frac{R4}{R3}\right)\left(\frac{-R2}{R1}(VIN - VOS1) + VOS1\right) - \left(1+\frac{R4}{R3}\right)VOS2 \\ &= \frac{-R2}{R1}\left(1+\frac{R4}{R3}\right)VIN + \frac{R2}{R1}\left(1+\frac{R4}{R3}\right)VOS1 + \left(1+\frac{R4}{R3}\right)VOS1 - \left(1+\frac{R4}{R3}\right)VOS2 \\ &= \frac{-R2}{R1}\left(1+\frac{R4}{R3}\right)VIN + \left(1+\frac{R2}{R1}\right)\left(1+\frac{R4}{R3}\right)VOS1 - \left(1+\frac{R4}{R3}\right)VOS2 \end{aligned}$$

Alternatively, one can substitute equation (1) and (6) (for the system 200) into equation (10) to arrive at the differential output voltage $V_{OUTDiff}$, which becomes:

$$
\begin{aligned}
V_{OUTDiff} &= VOUT1 - VOUT2 = VOUT1 + \frac{R4}{R3}\left(VOUT1 - (VOS1 + VOS2)\right) - (VOS1 + VOS2) \\
&= \left(1 + \frac{R4}{R3}\right) VOUT1 - \left(1 + \frac{R4}{R3}\right)(VOS1 + VOS2) \\
&= \left(1 + \frac{R4}{R3}\right)\left(\frac{-R2}{R1}(VIN - VOS1) + VOS1\right) - \left(1 + \frac{R4}{R3}\right)(VOS1 + VOS2) \\
&= \frac{-R2}{R1}\left(1 + \frac{R4}{R3}\right) VIN + \left(1 + \frac{R4}{R3}\right)\left(1 + \frac{R2}{R1}\right) VOS1 - \left(1 + \frac{R4}{R3}\right)(VOS1 + VOS2) \\
&= \frac{-R2}{R1}\left(1 + \frac{R4}{R3}\right) VIN + \frac{R2}{R1}\left(1 + \frac{R4}{R3}\right) VOS1 + \left(1 + \frac{R4}{R3}\right) VOS1 - \left(1 + \frac{R4}{R3}\right) VOS1 - \left(1 + \frac{R4}{R3}\right) VOS2 \\
&= \frac{-R2}{R1}\left(1 + \frac{R4}{R3}\right) VIN + \frac{R2}{R1}\left(1 + \frac{R4}{R3}\right) VOS1 - \left(1 + \frac{R4}{R3}\right) VOS2
\end{aligned}
\tag{12}
$$

Comparing equations (11) and (12), the input signal VIN and offset voltage VOS2 contributions are clearly the same for both, whereas the offset voltage VOS1 contribution is significantly reduced. Additionally, because (in a differential to single ended conversion) the ratio of resistors R4/R3 is generally 1. Equations (11) and (12) can be rewritten as follows (where the input signal VIN and offset voltage VOS2 contributions have been dropped):

$$V_{OUTDiff} = \left(2 + 2 \cdot \frac{R2}{R1}\right) VOS1 \tag{13}$$

$$V_{OUTDiff} = 2 \cdot \frac{R2}{R1} VOS1 \tag{14}$$

Clearly, system 200 has superior performance over system 100.

[0018] Embodiments having different combinations of one or more of the features or steps described in the context of example embodiments having all or just some of such features or steps are intended to be covered hereby. Those skilled in the art will appreciate that many other embodiments and variations are also possible within the scope of the claimed invention.

CLAIMS

What is claimed is:

1. An apparatus comprising:

a first amplifier stage having an input terminal and an output terminal, wherein the first amplifier receives an input signal at its input terminal, and wherein the first amplifier stage includes a first offset voltage source that provide a first offset voltage to the first amplifier stage and that is coupled to a supply rail; and

a second amplifier stage having an input terminal and an output terminal, wherein the input terminal of the second amplifier stage is coupled to the output terminal of the first amplifier stage, and wherein the second amplifier offset includes a second offset voltage source that provides a second offset voltage to the second amplifier stage, and wherein the second offset voltage source is coupled to the first amplifier stage so as to substantially reduce noise contribution from the first offset voltage.

2. The apparatus of Claim 1, wherein the first and second amplifiers stages further comprise a first inverting amplifier and a second inverting amplifier, respectively.

3. The apparatus of Claim 2, wherein the first inverting amplifier further comprises:

an operational amplifier having a first input terminal, a second input terminal, and an output terminal, wherein the second offset voltage source is coupled to the first input terminal of the operational amplifier, and wherein the first voltage offset source is coupled to the second input terminal of the operational amplifier; and

a resistor network coupled to the input terminal of the first inverting amplifier, the first input terminal of the operational amplifier, and the output terminal of the operational amplifier.

4. The apparatus of Claim 3, wherein the resistor network further comprises a plurality of resistors coupled in series with one another.

5. The apparatus of Claim 4, wherein the first input terminal of the operational amplifier is a negative input terminal, and wherein the second input terminal of the operational amplifier is a positive input terminal.

6. The apparatus of Claim 2, wherein the second inverting amplifier further comprises:

an operational amplifier having a first input terminal, a second input terminal, and an output terminal, wherein the second voltage offset source is coupled to the second input terminal of the operational amplifier; and

a resistor network coupled to the output terminal of the first inverting amplifier, the first input terminal of the operational amplifier, and the output terminal of the operational amplifier.

7. The apparatus of Claim 6, wherein the resistor network further comprises a plurality of resistors coupled in series with one another.

8. The apparatus of Claim 7, wherein the first input terminal of the operational amplifier is a negative input terminal, and wherein the second input terminal of the operational amplifier is a positive input terminal.

9. An apparatus comprising:

a first inverting amplifier having:

a first resistor that receives an input signal;

a first operational amplifier having a positive input terminal, an negative input terminal, and an output terminal, wherein the negative input terminal is coupled to the first resistor;

a second resistor that is coupled between the output terminal of the first operational amplifier and the negative input terminal of the first operational amplifier; and

a first offset voltage source that is coupled between the positive input terminal of the first operational amplifier and ground; and

a second inverting amplifier having:

a third resistor that is coupled to the output terminal of the first operational amplifier;

a second operational amplifier having a negative input terminal, a positive input terminal, and an output terminal, wherein the negative input terminal of the second operational amplifier is coupled to the third resistor;

a fourth resistor that is coupled between the output terminal of the second operational amplifier and the negative input terminal of second operational amplifier; and

a second offset voltage source that is coupled between the positive input terminal of the second operational amplifier and the negative input terminal of the first operational amplifier.

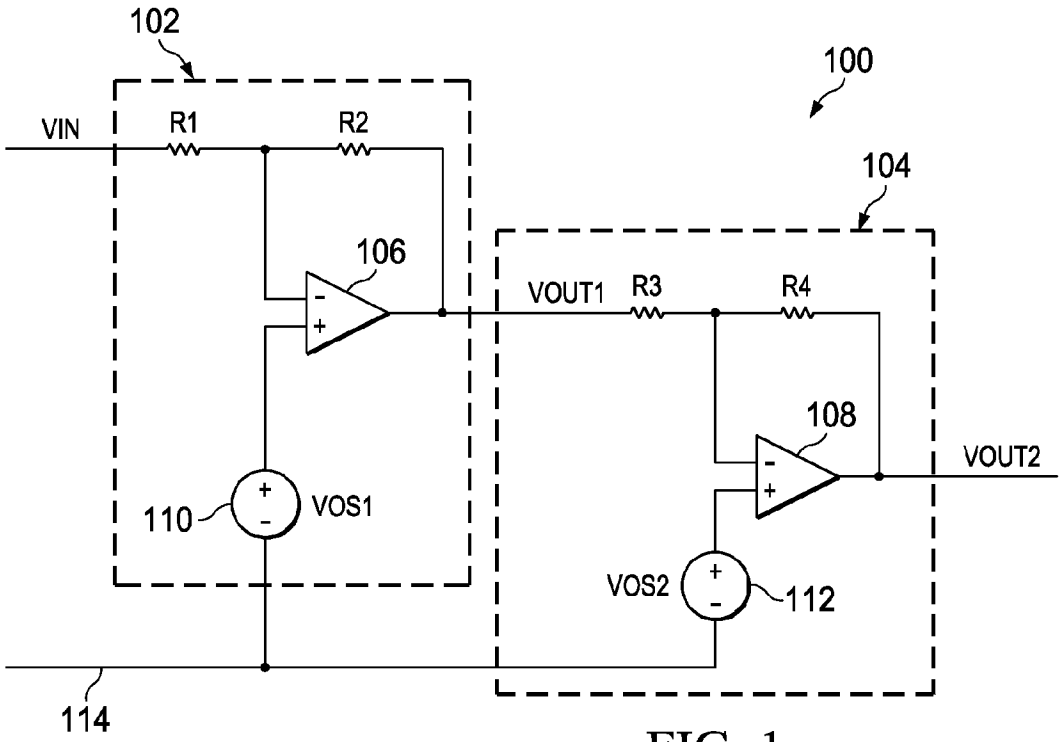

FIG. 1
(PRIOR ART)

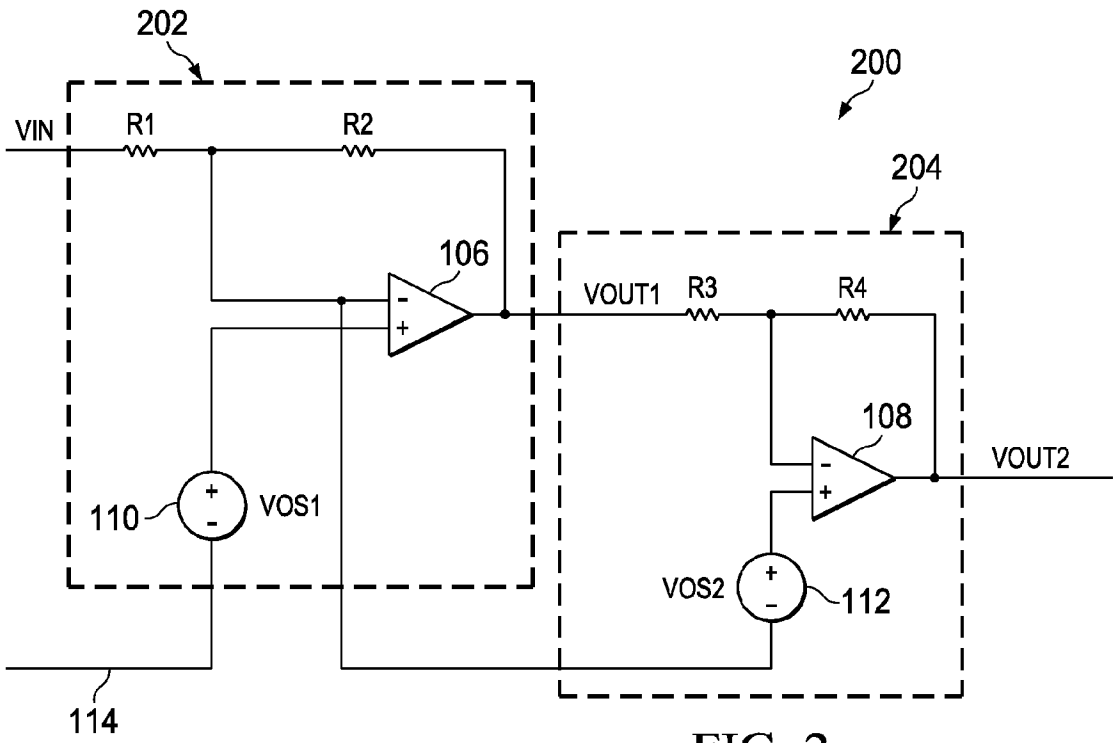

FIG. 2

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2010/061514

A. CLASSIFICATION OF SUBJECT MATTER

H03F 1/26(2006.01)i, H03F 1/22(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H03F 1/26; H03F 1/36; H03F 1/02; H03F 1/14

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords:offset voltage,reduce noise contribution,amplifier is coupled to a supply rail,resistor network,first and second offset voltage source,a second offset voltage source is coupled the positive and negative input terminal.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 6507241 B1 (RITTER; MARK B.) 14 January 2003 See Fig.1, claims 1-26	1-9
A	US 05663680A A (NORDENG; ARNOLD E.) 02 September 1997 See Fig.2, claims 1	1-9
A	US 2002-0140506 A1 (KEVIN WESLEY KOBAYASHI) 03 October 2002 See Fig.4-5, claims 1-20	1-9
A	Mohsen AYACHI et al. "a current mode CMOS IC for biological signals measurement in noisy environment", 2008. Dec. Microelectronics, ICM 2008, International Conference on. See Fig.4-11, abstracts	1-9
A	Lingchuan ZHOU et al. "a 100MHz current conveyor in 0.35㎛ CMOS technology", 2007 IEEE International Conference on signal processing and communications, 24-27, November 2007, Dubai, United Arab Emirates. See Fig.4-7, abstracts	1-9

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
18 AUGUST 2011 (18.08.2011)	**19 AUGUST 2011 (19.08.2011)**

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

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