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(54) **Title:** METHOD OF FABRICATING TRANSISTORS

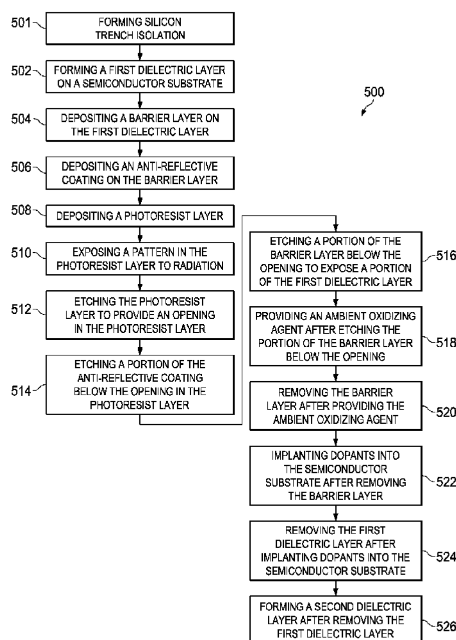

FIG. 5

(57) **Abstract:** A method (500) to fabricate a transistor includes: forming (502) a first dielectric layer on a semiconductor substrate; depositing (504) a barrier layer on the first dielectric layer; depositing (506) an anti -reflective coating on the barrier layer; depositing (508) and exposing (510) a pattern in a photoresist layer to radiation followed by etching (512) to provide an opening; etching (514) a portion of the anti -reflective coating below the opening; etching (516) a portion of the barrier layer below the opening to expose a portion of the first dielectric layer; providing (518) an ambient oxidizing agent to grow an oxide region followed by removing (520) the barrier layer; implanting dopants (522) into the semiconductor substrate after removing the barrier layer; removing (524) the first dielectric layer after implanting dopants into the semiconductor substrate; and forming (526) a second dielectric layer after removing the first dielectric layer, wherein the oxide region is grown to be thicker than the second dielectric layer.

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[Continued on next page]

TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:
— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*
— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

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METHOD OF FABRICATING TRANSISTORS

BACKGROUND

[0001] In many applications, transistors should have a relatively low specific resistance. For some field-effect-transistors, such as drain-extended metal-oxide-semiconductor (DEMOS) transistors, increasing the oxide thickness over part of the gate oxide may lower specific resistance.

SUMMARY

[0002] In at least one example, a method to fabricate a transistor comprises: forming a first dielectric layer on a semiconductor substrate; depositing a barrier layer on the first dielectric layer; depositing an anti-reflective coating on the barrier layer; depositing a photoresist layer; exposing a pattern in the photoresist layer to radiation; etching the photoresist layer according to the pattern to provide an opening in the photoresist layer; etching a portion of the anti-reflective coating below the opening in the photoresist layer; etching a portion of the barrier layer below the opening to expose a portion of the first dielectric layer; providing an ambient oxidizing agent after etching the portion of the barrier layer below the opening to grow an oxide region; removing the barrier layer after providing the ambient oxidizing agent; implanting dopants into the semiconductor substrate after removing the barrier layer; removing the first dielectric layer after implanting dopants into the semiconductor substrate; and forming a second dielectric layer after removing the first dielectric layer, wherein the oxide region is grown to be thicker than the second dielectric layer.

[0003] In at least one example, a method to fabricate a transistor comprises: forming a sacrificial oxide layer on a semiconductor substrate; depositing a silicon nitride layer on the sacrificial oxide layer; depositing an anti-reflective coating on the silicon nitride layer; depositing a photoresist layer; exposing a pattern in the photoresist layer to radiation; etching the photoresist layer according to the pattern to provide an opening in the photoresist layer; etching a portion of the anti-reflective coating below the opening; etching a portion of the silicon nitride layer below the opening to expose a portion of the sacrificial oxide layer; and growing an oxide region on the exposed portion of the sacrificial oxide layer; removing the silicon nitride layer after growing the oxide region; implanting dopants into the semiconductor substrate after removing the silicon

nitride layer; removing the sacrificial oxide layer after implanting dopants into the semiconductor substrate; and forming a gate oxide layer on the semiconductor substrate after removing the sacrificial oxide layer, wherein the oxide region is grown to thickness greater than a thickness of the gate oxide layer.

[0004] In at least one example, a method to fabricate a transistor comprises: forming a sacrificial oxide layer on a semiconductor substrate; depositing a silicon nitride layer on the sacrificial oxide layer; depositing a photoresist layer; exposing a pattern in the photoresist layer to radiation; etching the photoresist layer according to the pattern to provide an opening in the photoresist layer; etching a portion of the silicon nitride layer below the opening to expose a portion of the sacrificial oxide layer; growing an oxide region of at least 400 angstroms thick on the exposed portion of the sacrificial oxide layer; removing the silicon nitride layer after growing the oxide region; implanting dopants into the semiconductor substrate after removing the silicon nitride layer to form a drain region in the semiconductor substrate; removing the sacrificial oxide layer after implanting dopants into the semiconductor substrate; and forming a gate oxide layer on the semiconductor substrate after removing the sacrificial oxide layer, the gate oxide layer having a thickness less than 400 angstroms.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] FIG. 1 shows a transistor in various examples.

[0006] FIG. 2 shows a semiconductor substrate with several layers in various examples.

[0007] FIG. 3 shows a silicon substrate after etching in various examples.

[0008] FIG. 4 shows a silicon substrate with an oxide region in various examples.

[0009] FIG. 5 shows a process flow in various examples.

[0010] FIG. 6 shows two transistors in various examples.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0011] In the described embodiments, a method to fabricate transistors, such as a DEMOS transistor, includes growing a thick oxide below the transistor gate, where the process steps can be incorporated into a standard bipolar complementary-metal-oxide-semiconductor (BiCMOS) process flow.

[0012] FIG. 1 shows a cross-sectional view of an example transistor 100, not drawn to scale. In the example of FIG. 1, the example transistor 100 is a DEMOS transistor. A drain region 104 and a source region 106 are formed in a semiconductor substrate 102. In the example of FIG. 1, the

semiconductor substrate 102 is a silicon crystal, and the example transistor 100 is an n-type DEMOS transistor, where the drain region 104 and the source region 106 are each highly doped n-type regions. The source region 106 is formed within a lightly doped p-type well 108, and the drain region 104 is extended by way of the lightly doped n-type region 110.

[0013] A dielectric layer 112 is formed on the semiconductor substrate 102. The dielectric layer 112 is usually silicon dioxide, and the dielectric layer 112 is referred to as a gate oxide layer 112. A gate 114 is formed over the gate oxide layer 112. The gate 114 may comprise polysilicon. An oxide region 116 is grown on and into the semiconductor substrate 102. The oxide region 116 is adjacent to the drain region 104 and is below the gate 114, and the oxide region 116 is thicker than the dielectric layer 112. The oxide region 116 may comprise silicon dioxide. The presence of the oxide region 116 provides a lift-up to the gate 114. A highly doped p-type region 118 serves as a body contact for the example transistor 100.

[0014] When the example transistor 100 is ON, so that the channel below the gate 114 is in an inversion mode, a channel current of majority carriers (e.g., electrons for an n-type channel) flows from the source region 106 to the drain region 104. The presence of the oxide region 116 affects the path of the channel current. The relatively large depth of the oxide region 116 into the channel forces the majority carriers of the channel current to accelerate as they move underneath the oxide region 116 and toward the drain region 104. The acceleration of the majority carriers helps to reduce the specific resistance of the example transistor 100.

[0015] The oxide region 116 may be employed in other types of transistors, such as a double-diffusion metal-oxide-semiconductor (DMOS) transistor, as well as other types of lateral or vertical transistors. Although not shown in FIG. 1, other semiconductor devices may be formed in the semiconductor substrate 102 and coupled to the example transistor 100 to realize various circuits. In some embodiments in which other semiconductor devices are integrated with the example transistor 100, a silicon trench isolation (STI) region is formed around the example transistor 100 to provide electrical isolation from other semiconductor devices.

[0016] FIG. 2 shows a cross-sectional view (not drawn to scale) of the semiconductor substrate 102 and several layers formed during part of a process flow according to embodiments. A sacrificial dielectric layer 204 is formed over the semiconductor substrate 102. In silicon technology, the sacrificial dielectric layer 204 typically comprises silicon dioxide, and will be referred to as a sacrificial oxide layer 204. A barrier layer 206, typically silicon nitride, is

deposited on the sacrificial oxide layer 204. A bottom antireflective coating (BARC) 208 is deposited on the barrier layer 206, and a photoresist layer 210 is deposited on the BARC 208.

[0017] The photoresist layer 210 is exposed to radiation according to an illumination pattern defined by a mask (not shown). The pattern illuminated on the photoresist layer 210 defines an opening for growing the oxide region 116 of FIG. 1. In the example of FIG. 2, arrows, such as an arrow 212, pictorially represent the radiation. In some embodiments, the radiation may be in the deep ultraviolet (DUV) region, such as, for example, a wavelength of 248 nm, or a wavelength of 193 nm for an argon fluoride excimer laser source. As process technology nodes move to smaller sizes, embodiments may utilize other types of illumination sources and masks, such as extreme ultraviolet (EUC) lasers used with reflective masks (not shown).

[0018] FIG. 2 does not show all features formed within and on the semiconductor substrate 102. For example, buried layers and STI regions may be formed to electrically isolate various devices formed within and on the semiconductor substrate 102.

[0019] FIG. 3 shows a cross-sectional view (not drawn to scale) of the silicon substrate 102, with the layers of FIG. 2, after etching is performed to provide an opening 302, according to embodiments. The etching may include plasma reactive-ion etching (RIE). The plasma RIE may be performed in a gas mixture of oxygen (O_2), a carrier gas (e.g., argon), or fluorocarbons comprising carbon (C), Hydrogen (H), and Fluorine (F) having a stoichiometry CxHyFz with x = 1 or 2; y = 0, 1, 2, 3, or 4; and z = 1, 2, 3, or 4.

[0020] FIG. 4 shows a cross-sectional view (not drawn to scale) of the silicon substrate 102, with the layers of FIG. 3, where the oxide region 116 has been grown, according to embodiments. For some embodiments, the oxide region 116 may have a thickness of at least 400 angstroms, for example in the range of 400 angstroms to 4000 angstroms. The semiconductor substrate 102 is exposed to an ambient oxidizing agent to grow the oxide region 116. For some embodiments, the ambient oxidizing is performed in a thermal furnace oxidation process using oxygen and/or steam. For some embodiments, the semiconductor substrate 102 is exposed to oxygen and/or steam at a temperature above 900°C, for example in the range of 950°C to 1000°C.

[0021] The thickness of the barrier layer 206 affects formation of the “bird’s beak” (also sometimes referred to as a “birds beak”) shape of the oxide region 116 because of lateral oxidation under the barrier layer 206. The thickness of the barrier layer 206 may have a thickness from 300 angstroms to 1000 angstroms. In some embodiments, the barrier layer 206 may be about

950 angstroms thick.

[0022] After forming the oxide region 116, the various layers (excluding the oxide region 116) above the semiconductor substrate 102 illustrated in FIG. 4 are removed, followed by additional process steps to fabricate a transistor, such the example transistor 100 of FIG. 1. For example, dopants can be implanted to form the lightly doped n-type region 110, the drain region 104, and the source region 106. The sacrificial oxide layer 204 is removed before growing the gate oxide layer 112, and the gate 114 is formed over the gate oxide layer 112.

[0023] FIG. 5 shows an example process flow 500. The example process flow 500 includes, in step 501, formation of one or more STI regions; in step 502, forming a first dielectric layer (e.g., the sacrificial oxide layer 204) on a semiconductor substrate (e.g., the semiconductor substrate 102); in step 504, depositing a barrier layer 206 (e.g., a silicon nitride layer) on the first dielectric layer; in step 506, depositing an anti-reflective coating (e.g., the BARC 208) on the barrier layer; in step 508, depositing a photoresist layer (e.g., the photoresist layer 210); in step 510, exposing a pattern in the photoresist layer to radiation; in step 512, etching the photoresist layer according to the pattern to provide an opening in the photoresist layer; in step 514, etching a portion of the anti-reflective coating below the opening in the photoresist layer; in step 516, etching a portion of the barrier layer below the opening to expose a portion of the first dielectric layer; in step 518, providing an ambient oxidizing agent after etching the portion of the barrier layer below the opening; in step 520, removing the barrier layer after providing the ambient oxidizing agent; in step 522, implanting dopants into the semiconductor substrate after removing the barrier layer (e.g., to form the drain region 104 or the source region 106); in step 524, removing the first dielectric layer after implanting dopants into the semiconductor substrate; and in step 526, forming a second dielectric layer (e.g., the gate oxide layer 112) after removing the first dielectric layer.

[0024] The process steps in fabricating a transistor according to embodiments (e.g., the process flow 500) can be incorporated into a standard process flow, for example, a standard BiCMOS process, or a linear BiCMOS (LBC) process. Additional process steps may be performed before and after the process steps in an embodiment, such as the process steps described with respect to FIG. 5. For example, implanting dopants into the semiconductor substrate 102 to form buried regions may be performed before the process flow 500. As another example, an epitaxial layer may be grown on the semiconductor substrate 102 before the process flow 500.

[0025] Some or all of the steps illustrated in FIG. 5 may be repeated when fabricating multiple

devices on a wafer. For example, step 526 (and steps related to step 526) may be repeated to fabricate multiple transistors having different thicknesses for their respective gate oxide layers. As a specific example, the dielectric layer formed in an iteration of step 526 may have a thickness of about 40 angstroms, so that one or more transistors are fabricated having a gate oxide layer of about 40 angstroms. In another iteration of step 526, the dielectric layer may have a thickness of about 100 angstroms, so that one or more transistors are fabricated having a gate oxide layer of about 100 angstroms, suitable for a higher operating voltage.

[0026] FIG. 6 shows a cross-sectional view (not drawn to scale) of two example transistors. FIG. 6 shows a semiconductor substrate 602 in which the example transistor 100 is formed, but where the highly doped p-type region 118 (body contact) is not shown. Formed in the semiconductor substrate 602 is an example transistor 600 (with its body contact not shown). An STI region 601 isolates the example transistor 100 from the example transistor 600.

[0027] The example transistor 600 comprises a drain region 604 and a source region 606. In the example of FIG. 6, the example transistor 600 is an n-type DEMOS transistor, where the drain region 604 and the source region 606 are each highly doped n-type regions. The source region 606 is formed within a lightly doped p-type well 608, and the drain region 604 is extended by way of the lightly doped n-type region 610.

[0028] A gate oxide layer (a dielectric layer) 612 is formed on the semiconductor substrate 602. A gate 614 is formed over the gate oxide layer 612. An oxide region 616 is grown on and into the semiconductor substrate 602. The oxide region 616 is adjacent to the drain region 604 and is below the gate 614, and the oxide region 616 is thicker than the gate oxide layer 612. The gate oxide layer 612 is thicker than the gate oxide layer 112, so that the example transistor 600 can withstand a higher operating voltage than the example transistor 100.

[0029] Modifications are possible in the described embodiments, and other embodiments are possible, within the scope of the claims.

CLAIMS

What is claimed is:

1. A method to fabricate a transistor, the method comprising:

forming a first dielectric layer on a semiconductor substrate;

depositing a barrier layer on the first dielectric layer;

depositing an anti-reflective coating on the barrier layer;

depositing a photoresist layer;

exposing a pattern in the photoresist layer to radiation;

etching the photoresist layer according to the pattern to provide an opening in the photoresist layer;

etching a portion of the anti-reflective coating below the opening in the photoresist layer;

etching a portion of the barrier layer below the opening to expose a portion of the first dielectric layer;

providing an ambient oxidizing agent after etching the portion of the barrier layer below the opening to grow an oxide region;

removing the barrier layer after providing the ambient oxidizing agent;

implanting dopants into the semiconductor substrate after removing the barrier layer;

removing the first dielectric layer after implanting dopants into the semiconductor substrate; and

forming a second dielectric layer after removing the first dielectric layer, wherein the oxide region is grown to be thicker than the second dielectric layer.

2. The method of claim 1, further comprising:

forming a shallow trench isolation (STI) region; and

forming a third dielectric layer, wherein the third dielectric layer is thicker than the second dielectric layer.

3. The method of claim 1, further comprising:

depositing a second photoresist layer on the second dielectric layer;

exposing a second pattern in the second photoresist layer to radiation;

etching the second photoresist layer according to the second pattern to provide an opening in the second photoresist layer; and

depositing through the opening in the second photoresist layer a conductive material on the

second dielectric layer.

4. The method of claim 3, further comprising:

growing an epitaxial layer on the semiconductor substrate before forming the first dielectric layer on the semiconductor substrate.

5. The method of claim 4, further comprising:

implanting dopants into the semiconductor for form an n-type buried layer before growing the epitaxial layer.

6. The method of claim 5, wherein implanting dopants into the semiconductor forms a drain region in the semiconductor substrate.

7. The method of claim 1, wherein providing the ambient oxidizing agent comprises exposing the semiconductor substrate to the ambient oxidizing agent at a temperature above 900°C.

8. The method of claim 1, wherein the oxidizing agent comprises oxygen or steam.

9. The method of claim 1, wherein the first and second dielectric layers each comprise silicon dioxide.

10. The method of claim 1, wherein providing the ambient oxidizing agent comprises growing the oxide region into and on the semiconductor substrate to a thickness of at least 400 angstroms.

11. The method of claim 1, wherein the barrier layer has a thickness between 300 angstroms and 1000 angstroms.

12. The method of claim 1, wherein the barrier layer comprises silicon nitride.

13. The method of claim 1, wherein etching the portions of the anti-reflective coating and the barrier layer below the opening comprises plasma reactive-ion etching (RIE).

14. The method of claim 13, wherein the plasma RIE includes using a gas mixture of oxygen (O_2), a carrier gas, or fluorocarbons comprising carbon (C), Hydrogen (H), and Fluorine (F) having a stoichiometry CxHyFz with x = 1 or 2; y = 0, 1, 2, 3, or 4; and z = 1, 2, 3, or 4.

15. The method of claim 14, wherein the gas comprises argon and oxygen.

16. The method of claim 15, wherein the barrier layer comprises silicon nitride having a thickness between 300 angstroms and 1000 angstroms.

17. The method of claim 1, wherein providing the ambient oxidizing agent comprises growing the oxide region into and on the semiconductor substrate, the oxide region having a thickness of at least 400 angstroms.

18. A method to fabricate a transistor, the method comprising:

forming a sacrificial oxide layer on a semiconductor substrate;

depositing a silicon nitride layer on the sacrificial oxide layer;

depositing an anti-reflective coating on the silicon nitride layer;

depositing a photoresist layer;

exposing a pattern in the photoresist layer to radiation;

etching the photoresist layer according to the pattern to provide an opening in the photoresist layer;

etching a portion of the anti-reflective coating below the opening;

etching a portion of the silicon nitride layer below the opening to expose a portion of the sacrificial oxide layer; and

growing an oxide region on the exposed portion of the sacrificial oxide layer;

removing the silicon nitride layer after growing the oxide region;

implanting dopants into the semiconductor substrate after removing the silicon nitride layer;

removing the sacrificial oxide layer after implanting dopants into the semiconductor substrate; and

forming a gate oxide layer on the semiconductor substrate after removing the sacrificial oxide layer, wherein the oxide region is grown to thickness greater than a thickness of the gate oxide layer.

19. The method of claim 18, wherein growing the oxide region on the exposed portion of the sacrificial oxide layer comprises growing the oxide region to a thickness of at least 400 angstroms.

20. A method to fabricate a transistor, the method comprising:

forming a sacrificial oxide layer on a semiconductor substrate;

depositing a silicon nitride layer on the sacrificial oxide layer;

depositing a photoresist layer;

exposing a pattern in the photoresist layer to radiation;

etching the photoresist layer according to the pattern to provide an opening in the photoresist layer;

etching a portion of the silicon nitride layer below the opening to expose a portion of the sacrificial oxide layer;

growing an oxide region of at least 400 angstroms thick on the exposed portion of the sacrificial oxide layer;

removing the silicon nitride layer after growing the oxide region;

implanting dopants into the semiconductor substrate after removing the silicon nitride layer to form a drain region in the semiconductor substrate;

removing the sacrificial oxide layer after implanting dopants into the semiconductor substrate; and

forming a gate oxide layer on the semiconductor substrate after removing the sacrificial oxide layer, the gate oxide layer having a thickness less than 400 angstroms.

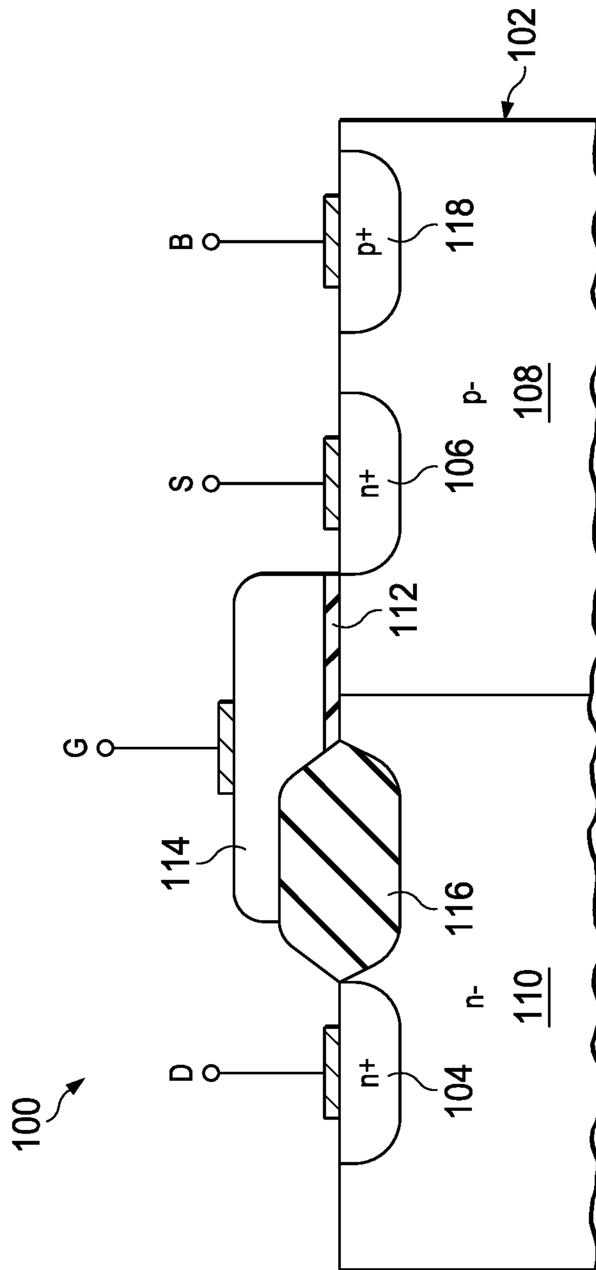

FIG. 1

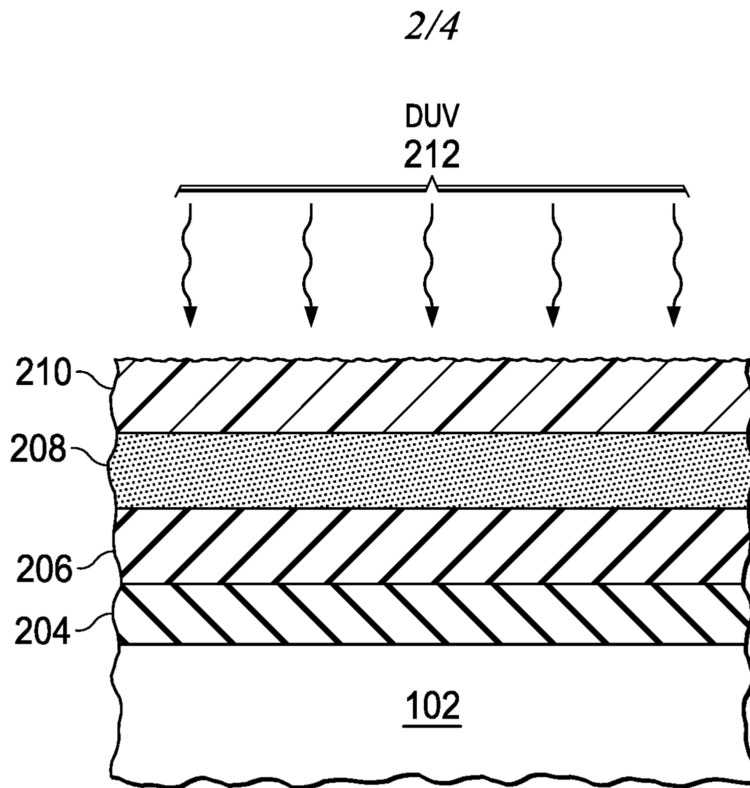

FIG. 2

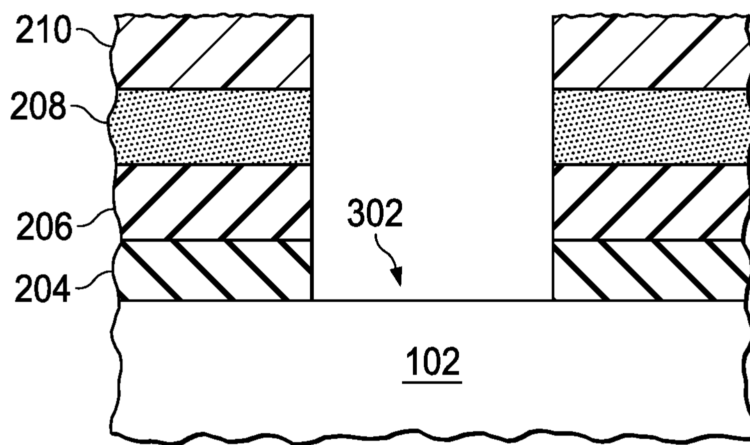

FIG. 3

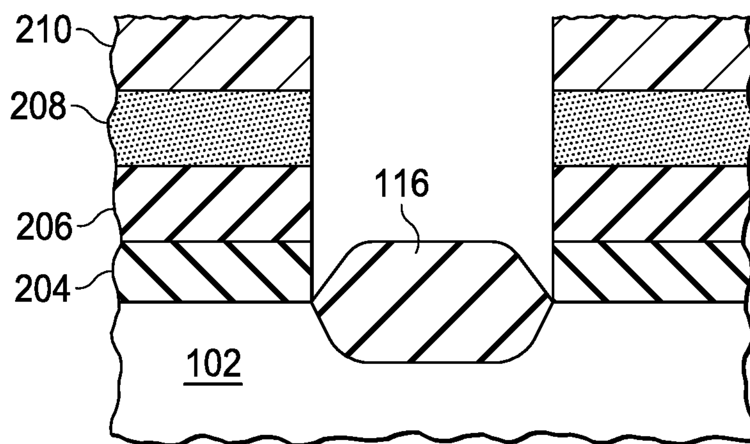

FIG. 4

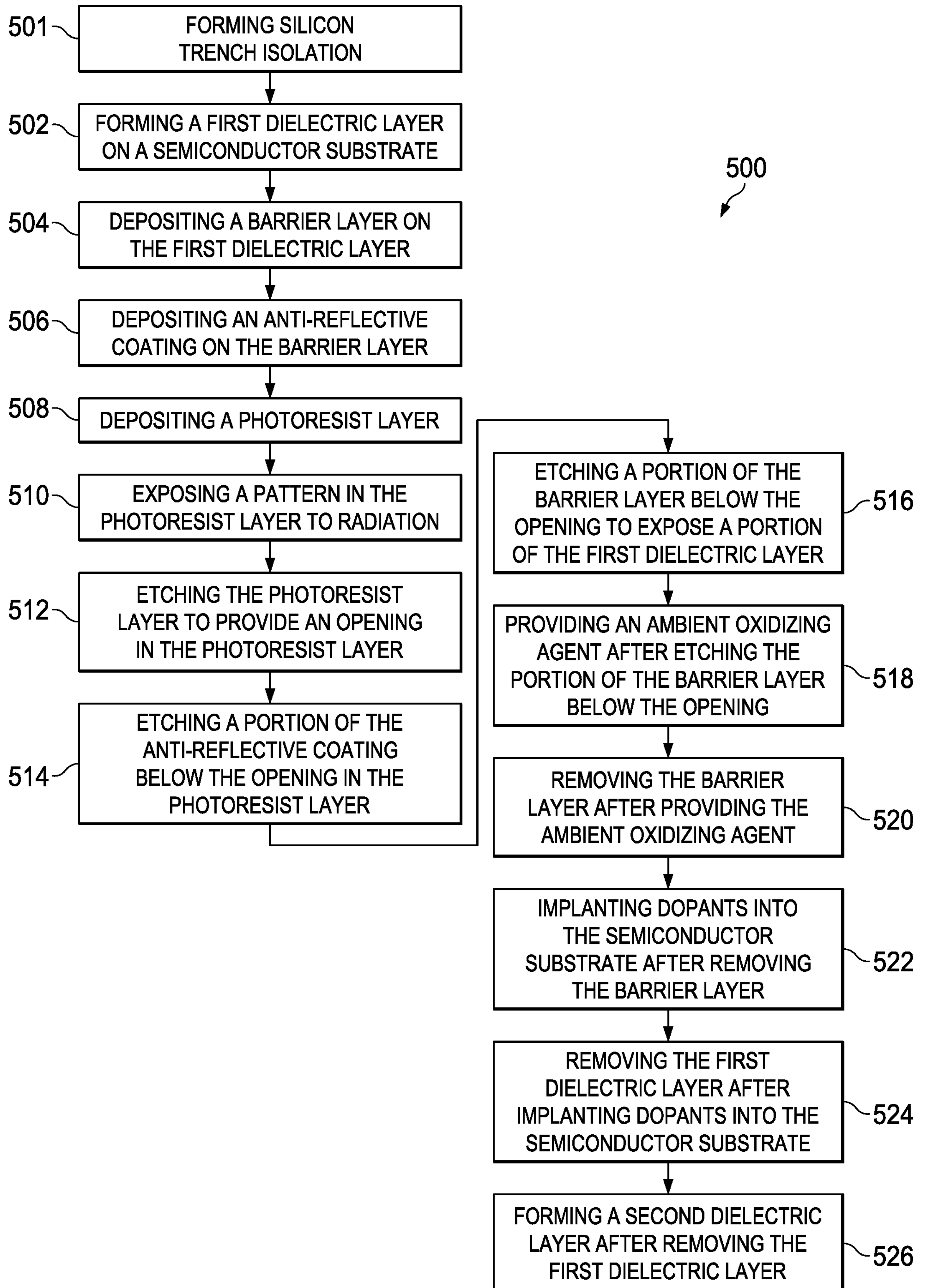

FIG. 5

FIG. 6

INTERNATIONAL SEARCH REPORT	International application No. PCT/US 2019/025599

A. CLASSIFICATION OF SUBJECT MATTER

H01L 21/331 *(2006.01)*
H01L 27/088 *(2006.01)*

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 21/00, 21/02, 21/302, 21/335, 21/336, 21/8238, 27/00, 27/02, 27/088, 29/66, 29/772

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

PatSearch (RUPTO internal), USPTO, PAJ, Esp@cenet, DWPI, EAPATIS, PATENTSCOPE, Information Retrieval System of FIPS

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2006/0003518 A1 (JOHANN HARTER et al.) 05.01.2006	1-20
A	EP 2479790 A2 (CREE, INC) 25.07.2012	1-20
A	US 4040168 A (RCA CORPORATION) 09.08.1977	1-20
A	KR 10-2006-0070334 A (SAMSUNG ELECTRONICS CO., LTD.) 23.06.2006	1-20

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
03 July 2019 (03.07.2019)	11 July 2019 (11.07.2019)

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