(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
4 December 2014 (04.12.2014)

WIPO | PCT

(10) International Publication Number
WO 2014/193109 A1

(51) International Patent Classification:
H01L 33/36 (2010.01) *H01L 33/20* (2010.01)

(21) International Application Number:
PCT/KR2014/004496

(22) International Filing Date:
20 May 2014 (20.05.2014)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
10-2013-0061220 29 May 2013 (29.05.2013) KR

(71) Applicant: **SEOUL VIOSYS CO., LTD.** [KR/KR]; 1B-36, 65-16, Sandan-ro 163beon-gil, Danwon-gu, Ansan-si, Gyeonggi-do 425-851 (KR).

(72) Inventors: **OH, Se Hee**; 1B-36, 65-16, Sandan-ro 163beon-gil, Danwon-gu, Ansan-si, Gyeonggi-do 425-851 (KR). **YOON, Yeo Jin**; 1B-36, 65-16, Sandan-ro 163beon-gil, Danwon-gu, Ansan-si, Gyeonggi-do 425-851 (KR). **KIM, Jong Kyu**; 1B-36, 65-16, Sandan-ro 163beon-gil, Danwon-gu, Ansan-si, Gyeonggi-do 425-851 (KR).

(74) Agent: **AIP PATENT & LAW FIRM**; 30-1, Teheran-ro 14-gil, Gangnam-gu, Seoul 135-935 (KR).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

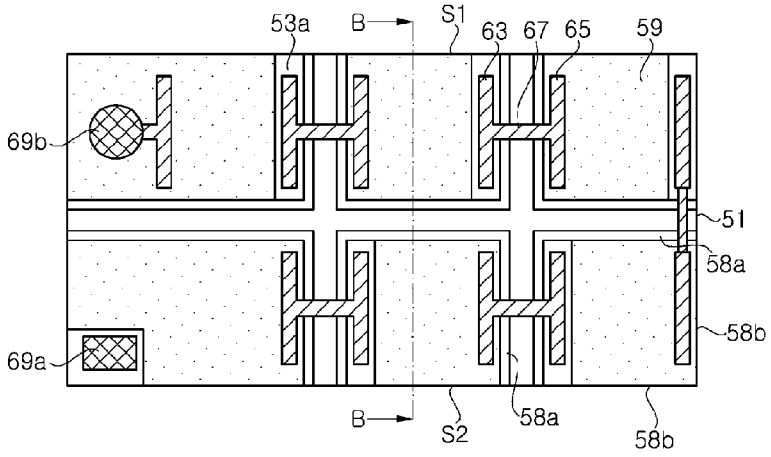
(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

(54) Title: LIGHT EMITTING DIODE HAVING PLURALITY OF LIGHT EMITTING ELEMENTS AND METHOD OF FABRICATING THE SAME

[Fig. 4]



(57) Abstract: Disclosed is a light emitting diode including a plurality of light emitting elements and a method of fabricating the same. The light emitting diode includes: a substrate; a plurality of light emitting elements disposed on the substrate; interconnection lines connecting the light emitting elements to each other, wherein the plurality of light emitting elements comprise outer light emitting elements aligned along an edge of the substrate, each of the outer light emitting elements comprises an inner face directed towards an adjacent light emitting element and an outer face disposed adjacent the edge of the substrate and directed towards an outside of the substrate, and the inner face of at least one of the outer light emitting elements comprises a more gently slanted side surface than the outer face thereof.

WO 2014/193109 A1

Description

Title of Invention: LIGHT EMITTING DIODE HAVING PLURALITY OF LIGHT EMITTING ELEMENTS AND METHOD OF FABRICATING THE SAME

Technical Field

[1] The present invention relates to a light emitting diode and a method of fabricating the same and, more particularly, to a light emitting diode including a plurality of light emitting elements and a method of fabricating the same.

Background Art

[2] Light emitting diodes are widely used for display devices and backlight units. In addition, with low power consumption and long lifespan as compared with existing incandescent lamps or fluorescent lamps, applications of the light emitting diodes have expanded to general lighting by replacing existing incandescent lamps, fluorescent lamps, and the like.

[3] Generally, light emitting diodes are operated at a predetermined forward voltage and thus cannot be operated at high voltage. To solve this problem, a light emitting diode capable of being operated at high voltage is developed by disposing a plurality of light emitting elements on a single substrate and connecting the light emitting elements to each other in series.

[4] Fig. 1 is a plan view of a typical light emitting diode including a plurality of light emitting elements and Fig. 2 is a cross-sectional view of the light emitting diode taken along line A-A of Fig. 1.

[5] Referring to Fig. 1 and Fig. 2, the light emitting diode includes a substrate 21, a plurality of light emitting elements including light emitting elements S1, S2, an insulation layer 31, an n-contact 33, a p-contact 35, interconnection lines 37, an n-pad 39a, and a p-pad 39b. In addition, each of the light emitting elements includes an n-type semiconductor layer 23, an active layer 25, and a p-type semiconductor layer 27.

[6] The plural light emitting elements are separated from each other and connected to each other in series between the n-pad 39a and the p-pad 39b by the interconnection lines 37. For example, each of the interconnection lines 37 connects the n-contact 33, which is electrically connected to the n-type semiconductor layer 23 of one light emitting element, to the p-contact 35, which is electrically connected to the p-type semiconductor layer 27 of another light emitting element. The n-contact 33 is connected to the n-type semiconductor layer 23a exposed by mesa-etching, and the p-contact 35 is electrically connected to the p-type semiconductor layer 27 through a transparent electrode 29.

[7] The insulation layer 31 is disposed under the interconnection lines 37 and prevents short circuit between the n-type semiconductor layer 23 and the p-type semiconductor layer 27 in a single light emitting element by the interconnection lines 37. In addition, the insulation layer 31 may cover side surfaces of the light emitting elements and the transparent electrode 29 to protect the same from moisture and the like.

[8] On the other hand, the n-contact 33, the p-contact 35 and the interconnection lines 37 are formed by depositing a conductive material by a deposition technique such as electron beam evaporation or sputtering, followed by patterning the conductive material. At this time, when the light emitting elements have perpendicular side surfaces, it is difficult to deposit the conductive material on the side surfaces of the light emitting elements, thereby causing easy disconnection of the interconnection lines 37 on the side surfaces of the light emitting elements.

[9] To prevent disconnection of the interconnection lines 37, as shown in Fig. 2, the side surfaces of all of the light emitting elements including the light emitting elements S1, S2 are slanted at an angle of less than 90 degrees relative to an upper surface of the substrate 21. Each of the light emitting elements S1, S2 has a slanted side surface 28a which faces an adjacent light emitting element, and a slanted side surface 28b which is adjacent an edge of the substrate 21.

[10] Fig. 3 is a schematic sectional view illustrating a dicing process using a laser to form a light emitting diode.

[11] Referring to Fig. 3, the light emitting elements are formed to have the slanted side surfaces 28a, 28b, and the transparent electrode 29, the insulation layer 31 and the interconnection lines 37 (see Fig. 1) are formed. Then, laser beams are radiated along a scribing line, followed by breaking the substrate 21, such that light emitting diodes are divided into individual chips. The scribing line is formed along an area between the slanted side surfaces 28b.

[12] As a result, the light emitting diode shown in Figs. 1 and 2 is completed, and includes the light emitting elements each having the slanted side surfaces 28a, 28b. Particularly, the side surfaces of the light emitting elements disposed adjacent the edge of the light emitting diode are constituted by the slanted side surfaces 28b.

[13] In the related art, disconnection of the interconnection lines 37 is prevented by forming the side surfaces of the light emitting elements to be slanted. However, when the side surfaces of the light emitting elements are slanted, light emitting areas of the light emitting elements, that is, the areas of the active layers 25 are decreased. A gentler slope of the slanted side surfaces 28a, 28b causes further reduction in light emitting area. Reduction in light emitting area of the light emitting elements results in deterioration in light output and increase in forward voltage Vf.

[14] The above information disclosed in this Background section is only for enhancement

of understanding of the background of the invention and, therefore, it may contain information that does not constitute prior art.

Disclosure of Invention

Technical Problem

[15] Exemplary embodiments of the present invention provide a light emitting diode including a plurality of light emitting elements and capable of increasing light emitting areas of the light emitting elements without disconnection of interconnection lines.

[16] Exemplary embodiments of the present invention provide a light emitting diode including a plurality of light emitting elements and capable of reducing forward voltage of the light emitting elements while enhancing light output.

[17] Additional features of the invention will be set forth in the description which follows, and in part will become apparent from the description, or may be learned from practice of the invention.

Solution to Problem

[18] Embodiments of the present invention disclose a light emitting diode including a plurality of light emitting elements disposed on a substrate. In addition, at least one of the light emitting elements includes a side surface slanted at an angle of less than 90° relative to the substrate and a side surface perpendicular to the substrate. With this structure, the light emitting diode provides increased light emitting areas to the light emitting element, thereby decreasing forward voltage of the light emitting elements while enhancing light output.

[19] The light emitting diode may include: a substrate; a plurality of light emitting elements disposed on the substrate; and interconnection lines connecting the light emitting elements to each other. In addition, the plurality of light emitting elements include outer light emitting elements aligned along an edge of the substrate, and each of the outer light emitting elements includes an inner face directed towards an adjacent light emitting element and an outer face disposed adjacent the edge of the substrate and directed towards an outside of the substrate. Further, the inner face of at least one of the outer light emitting elements may include a more gently slanted side surface than the outer face thereof.

[20] Each of the interconnection lines may connect adjacent light emitting elements to each other through the more gently slanted side surface than the outer face.

[21] In addition, the outer face of at least one of the outer light emitting elements may include a side surface substantially perpendicular to the substrate. Further, each of the outer faces of the outer light emitting elements may include a side surface perpendicular to the substrate. Furthermore, the perpendicular side surfaces may be flush with a side surface of the substrate.

[22] Each of the outer faces may be composed of a single plane, but is not limited thereto. Alternatively, each of the outer faces may include a stepped portion.

[23] In addition, each of the light emitting elements may include a first conductivity type semiconductor layer, an active layer, and a second conductivity type semiconductor layer. Here, the stepped portion may be formed on the first conductivity type semiconductor layer. Further, side surfaces of the active layer and the second conductivity type semiconductor layer may be covered with an insulation layer.

[24] Embodiments of the present invention provide a method of fabricating a light emitting diode including a plurality of light emitting elements, which includes: growing a semiconductor stack including a first conductivity type semiconductor layer, an active layer and a second conductivity type semiconductor layer on a substrate; patterning the semiconductor stack to form an isolation trench in a unit light emitting diode chip area; and dividing the semiconductor stack and the substrate using a laser. Here, the plurality of light emitting elements include outer light emitting elements aligned along an edge of the substrate, and each of the outer light emitting elements includes an inner face formed by the isolation trench and an outer face formed by dividing the semiconductor stack using the laser, in which the inner face includes a more gently slanted side surface than the outer face.

[25] During formation of the isolation trench, the inner face is formed to have a gentle slope and the outer face is formed by a laser beam, thereby increasing light emitting areas of the light emitting elements.

[26] The method may further include etching the second conductivity type semiconductor layer and the active layer to expose the first conductivity type semiconductor layer before or after forming the isolation trench.

[27] The method may further include forming interconnection lines, which connect adjacent first and second conductivity type semiconductor layers to each other across the isolation trench. With this structure, a relatively gently slanted inner face is provided to the interconnection lines, thereby preventing disconnection of the interconnection lines.

[28] The first conductivity type semiconductor layer may be exposed in a contact area for forming an ohmic contact. In addition, the first conductivity type semiconductor layer may also be exposed in a scribing line area.

[29] In addition, the method may further include forming an insulation layer covering the isolation trench and the scribing line area. The insulation layer exposes the contact area.

[30] It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

Advantageous Effects of Invention

[31] According to embodiments of the present invention, in a light emitting diode including a plurality of light emitting elements, inner and outer faces of the light emitting elements arranged along an edge of a substrate are formed to have different slopes, thereby increasing light emitting areas of the light emitting elements while preventing disconnection of interconnection lines. As a result, the light emitting diode can decrease forward voltage of the light emitting elements while enhancing light output.

Brief Description of Drawings

[32] Fig. 1 is a schematic plan view of a light emitting diode in the related art.

[33] Fig. 2 is a schematic cross-sectional view of the light emitting diode taken along line A-A of Fig. 1.

[34] Fig. 3 is a schematic sectional view illustrating a method of fabricating a light emitting diode in the related art.

[35] Fig. 4 is a schematic plan view of a light emitting diode according to an exemplary embodiment of the present invention.

[36] Fig. 5 is a schematic cross-sectional view of the light emitting diode taken along line B-B of Fig. 4.

[37] Fig. 6 is a schematic sectional view illustrating a method of fabricating a light emitting diode according to an exemplary embodiment of the present invention.

[38] Fig. 7 is a schematic plan view of a light emitting diode according to an exemplary embodiment of the present invention.

[39] Fig. 8 is a schematic cross-sectional view of the light emitting diode taken along line B-B of Fig. 7.

[40] Fig. 9 is a schematic sectional view illustrating a method of fabricating a light emitting diode according to an exemplary embodiment of the present invention.

Mode for the Invention

[41] The invention is described more fully hereinafter with reference to the accompanying drawings, in which exemplary embodiments of the invention are shown. This invention may, however, be embodied in many different forms and should not be construed as limited to the exemplary embodiments set forth herein. Rather, these exemplary embodiments are provided so that this disclosure is thorough, and will fully convey the scope of the invention to those skilled in the art.

[42] Further, it should be noted that the drawings are not to precise scale, and some of the dimensions, such as width, length, thickness, and the like, are exaggerated for clarity of description in the drawings. Like components are denoted by like reference numerals throughout the specification.

[43] Fig. 4 is a schematic plan view of a light emitting diode according to an exemplary embodiment of the present invention, and Fig. 5 is a schematic cross-sectional view of the light emitting diode taken along line B-B of Fig. 4.

[44] Referring to Fig. 4 and Fig. 5, the light emitting diode according to this embodiment includes a substrate 51, a plurality of light emitting elements (S1, S2, etc.), and inter-connection lines 67. Further, the light emitting diode may include a first contact 63, a second contact 65, first and second electrode pads 69a, 69b, a transparent electrode 59, and an insulation layer 61. Here, each of the light emitting elements may include a first conductivity type semiconductor layer 53, an active layer 55, and a second conductivity type semiconductor layer 57.

[45] The substrate 51 may be a sapphire (Al_2O_3) substrate, a silicon carbide (SiC) substrate, a gallium nitride (GaN) substrate, an indium gallium nitride (InGaN) substrate, an aluminum gallium nitride (AlGaN) substrate, an aluminum nitride (AlN) substrate, a gallium oxide (Ga_2O_3) substrate, or a silicon substrate, without being limited thereto. The substrate 51 may be an insulation substrate such as a sapphire substrate, or a conductivity type substrate which includes an insulation layer on an upper side thereof. Particularly, the substrate 51 is a patterned sapphire substrate.

[46] The substrate 51 has a generally quadrangular shape and may have a rectangular shape, as shown in the drawings, without being limited thereto. The substrate 51 has an upper surface, a lower surface, and side surfaces connecting the upper and lower surfaces to each other. The upper surface of the substrate 51 is surrounded by an edge thereof.

[47] The plurality of light emitting elements S1, S2, etc. are aligned on the upper surface of the substrate 51. As shown in Fig. 5, each of the light emitting elements is a semiconductor stack, which includes the first conductivity type semiconductor layer 53, the active layer 55 and the second conductivity type semiconductor layer 57.

[48] The active layer 55 may have a single quantum well structure or a multi-quantum well structure, and the materials and composition of the active layer are determined depending upon desired wavelengths of light emitted from the light emitting elements. For example, the active layer 55 may be formed of an AlInGaN-based compound semiconductor, for example, InGaN. On the other hand, the first and second conductivity type semiconductor layers 53, 57 are formed of a material having a greater band gap than the active layer 55, and formed of an AlInGaN-based compound semiconductor, for example, GaN.

[49] As shown, the second conductivity type semiconductor layer 57 is disposed on some regions of the first conductivity type semiconductor layer 53, and the active layer 55 is disposed between the first conductivity type semiconductor layer 53 and the second conductivity type semiconductor layer 57. A contact area 53a of the first conductivity

type semiconductor layer 53 is exposed. The first conductivity type semiconductor layer 53 and the second conductivity type semiconductor layer 57 may be an n-type semiconductor layer and a p-type semiconductor layer, respectively, or vice versa.

[50] As shown in Fig. 4, the light emitting elements include outer light emitting elements aligned along the edge of the substrate 51. Each of the outer light emitting elements includes an inner face 58a directed towards an adjacent light emitting element and an outer face 58b disposed adjacent the edge of the substrate 51 and directed towards an outside of the substrate 51. Although not shown in Fig. 4, the light emitting elements may include inner light emitting elements aligned on the substrate 51 and surrounded by the outer light emitting elements. The inner light emitting elements have side surfaces, which are constituted by the inner faces 58a directed towards adjacent light emitting elements, and do not have the outer face 58b.

[51] As shown in Fig. 5, the inner face 58a includes a more gently slanted side surface than the outer face 58b. The inner face 58a is gently slanted to prevent disconnection of the interconnection lines 67. The outer face 58b may include a side surface substantially perpendicular to the upper surface of the substrate 51. In addition, the outer face 58b may be flush with the side surface of the substrate 51 and may be formed together with the side surface of the substrate 51 by the same process.

[52] The transparent electrode 59 may be disposed on the second conductivity type semiconductor layer 57. The transparent electrode 59 may be formed of a transparent oxide, such as indium tin oxide (ITO), or a transparent metallic material, such as Ni/Au or the like.

[53] The first contact 63 may be disposed on the contact area 53a of the first conductivity type semiconductor layer 53 and the second contact 65 may be disposed on the second conductivity type semiconductor layer 57. The second contact 65 may be electrically connected to the second conductivity type semiconductor layer 57 through the transparent electrode 59.

[54] On the other hand, the first and second electrode pads 69a, 69b are disposed on the substrate 51. The first electrode pad 69a is electrically connected to the first conductivity type semiconductor layer 53 of one light emitting element, and the second electrode pad 69b is electrically connected to the second conductivity type semiconductor layer 57 of another light emitting element.

[55] As shown in Fig. 4, each of the first and second electrode pads 69a, 69b may be disposed on the light emitting elements, but is not limited thereto. Alternatively, the first and second electrode pads 69a, 69b may be separated from the light emitting elements. For example, the first and second electrode pads 69a, 69b may be formed on the substrate 51, on the first conductivity type semiconductor layer 53, on the second conductivity type semiconductor layer 57, or on the transparent electrode 59, while

being separated from the light emitting elements.

[56] The first and second electrode pads 69a, 69b receive power from an external power source and may be bonded to, for example, bonding wires. The light emitting diode is operated by power applied to the first and second electrode pads 69a, 69b.

[57] The interconnection lines 67 electrically connect adjacent light emitting elements to each other. The interconnection lines 67 may connect adjacent light emitting elements to each other in series. Specifically, the interconnection lines 67 connect the first contact 63 of one light emitting element to the second contact 65 of another light emitting element adjacent thereto. The interconnection lines 67 pass through the inner faces 58a of the light emitting elements. Particularly, the interconnection lines 67 pass through relatively gently slanted side surfaces, whereby disconnection of the interconnection lines can be prevented. The interconnection lines 67 may be formed of the same material as that of the first and second contacts 63, 65 by the same process.

[58] On the other hand, the insulation layer 61 is disposed between the interconnection lines 67 and the light emitting elements, and prevents short circuit between the second conductivity type semiconductor layer 57 and the first conductivity type semiconductor layer 53 in one light emitting element by the interconnection lines 67. Further, the insulation layer 61 may cover the inner faces 58a of the light emitting elements to protect the light emitting elements.

[59] In this embodiment, all of the inner faces 58a are illustrated as the relatively gently slanted side surfaces. In alternative embodiments, some inner faces passing through the interconnection lines 67 are gently slanted, and the other inner faces may be steeply slanted side surfaces like the outer faces 58b.

[60] According to this embodiment, the side surface of the light emitting element on which the interconnection lines 67 are formed, that is, the inner face 58a of the light emitting element, has a relatively gentle slope, and the outer face 58b thereof has a relatively steep slope. Accordingly, in this embodiment, the outer face 58b of the light emitting element may be disposed farther outside than the outer face 28b of the typical light emitting element, as shown in Fig. 5, thereby increasing a light emitting area of the light emitting element.

[61] Fig. 6 is a schematic sectional view illustrating a method of fabricating a light emitting diode according to an exemplary embodiment of the present invention.

[62] Referring to Fig. 6, a semiconductor stack, which includes a first conductivity type semiconductor layer 53, an active layer 55 and a second conductivity type semiconductor layer 57, is grown on a substrate 51. These semiconductor layers may be grown by various methods, such as metal organic chemical vapor deposition (MOCVD), molecular beam epitaxy (MBE), hydride vapor phase epitaxy (HVPE), and the like.

[63] Then, the semiconductor stack is subjected to patterning to form an isolation trench in a unit light emitting diode chip area. The isolation trench corresponds to a groove which divides the light emitting elements from each other in Figs. 4 and 5.

[64] Conventionally, the isolation trench is formed to divide not only individual light emitting elements in the unit light emitting diode chip area, but also the light emitting elements of adjacent light emitting diode chip areas. However, in this embodiment, the isolation trench is formed to divide the light emitting elements in the unit light emitting diode chip area from each other without dividing the light emitting elements of adjacent chip areas.

[65] Before or after dividing the semiconductor stack, etching, that is, mesa etching, is performed to partially expose the first conductivity type semiconductor layer 53. The first conductivity type semiconductor layer 53 of the contact area 53a is exposed by mesa etching.

[66] On the other hand, a transparent electrode 59 is formed on each of the light emitting elements. The transparent electrode 59 may be formed before or after formation of the isolation trench.

[67] Further, a first contact 63 and a second contact 65 are formed on each of the light emitting elements, and interconnection lines 67 may connect the first contact 63 of one light emitting element to the second contact 65 of another light emitting element adjacent thereto. The interconnection lines 67 are formed to pass through the isolation trench. Further, the interconnection lines 67 may be formed such that the first and second electrode pads 39a, 39b are electrically connected to the first and second conductivity type semiconductor layers 53, 57, respectively. The first contact 63, second contact 65, interconnection lines 67, first electrode pad 39a and second electrode pad 39b may be formed by the same process using photolithography and etching, or using a lift-off process.

[68] Before formation of the interconnection lines 67, an insulation layer 61 may be formed to isolate the interconnection lines 67 from the light emitting elements. The insulation layer 61 may be formed of, for example, SiO_2, without being limited thereto.

[69] Then, the semiconductor stack and the substrate are divided by a laser beam. The laser beam is radiated along a scribing line. Scribing may be performed using a laser, and then, the substrate may be divided into individual light emitting diode chips by breaking.

[70] Through division of the substrate using the laser, the substrate and light emitting elements between adjacent light emitting diode chip areas are divided. Thus, the outer light emitting elements are aligned along an edge of the substrate formed through division of the substrate, and the outer faces 58b of the outer light emitting elements are formed.

[71] The inner faces 58a formed by the isolation trench include more gently slanted side surfaces than the outer faces 58b formed by dividing the semiconductor stack using the laser. Accordingly, it is possible to prevent disconnection of the interconnection lines 67 passing through the isolation trench.

[72] On the other hand, the outer faces 58b are formed through division of the substrate using the laser instead of using the isolation trench, whereby the light emitting elements have increased light emitting areas.

[73] Fig. 7 is a schematic plan view of a light emitting diode according to an exemplary embodiment of the present invention and Fig. 8 is a schematic cross-sectional view of the light emitting diode taken along line B-B of Fig. 7.

[74] Referring to Fig. 7 and Fig. 8, the light emitting diode according to this embodiment is generally similar to the light emitting diode described with reference to Figs. 4 and 5 except that outer light emitting elements have stepped portions on outer faces thereof.

[75] Specifically, each of the outer light emitting elements includes not only a contact area 53a, but also a first conductivity type semiconductor layer area 53b exposed along an edge of a substrate 51. As a result, the outer light emitting elements have the stepped portion formed on the outer face 58b thereof. Each of the stepped portions is formed on the first conductivity type semiconductor layer 53 and side surfaces of the active layer 55 and the second conductivity type semiconductor layer 57 are disposed on an inner area of the substrate 51.

[76] On the other hand, as described with reference to Figs. 4 and 5, an insulation layer 61 isolates the interconnection lines 67 from the light emitting elements. The insulation layer 61 covers the exposed area 53b of the first conductivity semiconductor layer, and may cover side surfaces of an active layer 55 and a second conductivity type semiconductor layer 57.

[77] According to this embodiment, the insulation layer 61 may cover the sides surfaces of the active layer 55 and the second conductivity type semiconductor layer 57 to prevent the active layer 55 from being exposed outside, whereby the light emitting elements can be protected from moisture or the like, thereby improving reliability of the light emitting diode.

[78] Fig. 9 is a schematic sectional view illustrating a method of fabricating a light emitting diode according to an exemplary embodiment of the present invention.

[79] Referring to Fig. 9, the method according to this embodiment is generally similar to the method described with reference to Fig. 6 except that a first conductivity semiconductor layer area 53b is exposed along a scribing line before radiation of laser beams. The first conductivity semiconductor layer area 53b may be subjected to mesa etching to expose a contact area 53a.

[80] In this embodiment, an insulation layer 61 may be formed to cover the exposed area

53b of the first conductivity semiconductor layer while covering side surfaces of an active layer 55 and a second conductivity type semiconductor layer 57.

[81] According to this embodiment, as the first conductivity semiconductor layer area 53b is exposed along the scribing line by mesa etching, the insulation layer 61 may cover the side surfaces of the active layer 55 and the second conductivity type semiconductor layer 57.

[82] Although some embodiments have been described above, the present invention is not limited to these embodiments and features, and various modifications, changes, and alterations can be made without departing from the spirit and scope of the invention. Therefore, it should be understood that the embodiments are not to be construed as limiting the present invention, but are given to provide thorough understanding of the present invention to those skilled in the art. The scope of the present invention should be interpreted according to the following appended claims as covering all modifications or variations derived from the appended claims and equivalents thereof.

Claims

[Claim 1] A light emitting diode comprising:
a substrate;
a plurality of light emitting elements disposed on the substrate; and
interconnection lines connecting the light emitting elements to each other,
wherein the plurality of light emitting elements comprise outer light emitting elements aligned along an edge of the substrate,
each of the outer light emitting elements comprises an inner face directed towards an adjacent light emitting element and an outer face disposed adjacent the edge of the substrate and directed towards an outside of the substrate, and
the inner face of at least one of the outer light emitting elements comprises a more gently slanted side surface than the outer face thereof.

[Claim 2] The light emitting diode of claim 1, wherein each of the inter-connection lines connects adjacent light emitting elements to each other through the more gently slanted side surface than the outer face.

[Claim 3] The light emitting diode of claim 1, wherein the outer face of at least one of the outer light emitting elements comprises a side surface per-pendicular to the substrate.

[Claim 4] The light emitting diode of claim 1, wherein each of the outer faces of the outer light emitting elements comprises a side surface perpendicular to the substrate.

[Claim 5] The light emitting diode of claim 4, wherein the perpendicular side surfaces are flush with a side surface of the substrate.

[Claim 6] The light emitting diode of claim 4, wherein each of the outer faces has a stepped portion.

[Claim 7] The light emitting diode of claim 6, wherein each of the light emitting elements comprises a first conductivity type semiconductor layer, an active layer and a second conductivity type semiconductor layer,
the stepped portion being formed on the first conductivity type semi-conductor layer,
side surfaces of the active layer and the second conductivity type semi-conductor layer being covered with an insulation layer.

[Claim 8] A method of fabricating a light emitting diode including a plurality of light emitting elements, comprising:

growing a semiconductor stack on a substrate, the semiconductor stack comprising a first conductivity type semiconductor layer, an active layer, and a second conductivity type semiconductor layer;
patterning the semiconductor stack to form an isolation trench in a unit light emitting diode chip area; and
dividing the semiconductor stack and the substrate using a laser
wherein the plurality of light emitting elements comprise outer light emitting elements aligned along an edge of the substrate,
each of the outer light emitting elements comprises an inner face formed by the isolation trench and an outer face formed by dividing the semiconductor stack using the laser, and
the inner face comprises a more gently slanted side surface than the outer face.

[Claim 9] The method of claim 8, further comprising:
etching the second conductivity type semiconductor layer and the active layer to expose the first conductivity type semiconductor layer before or after forming the isolation trench.

[Claim 10] The method of claim 9, further comprising:
forming interconnection lines connecting adjacent first and second conductivity type semiconductor layers to each other across the isolation trench.

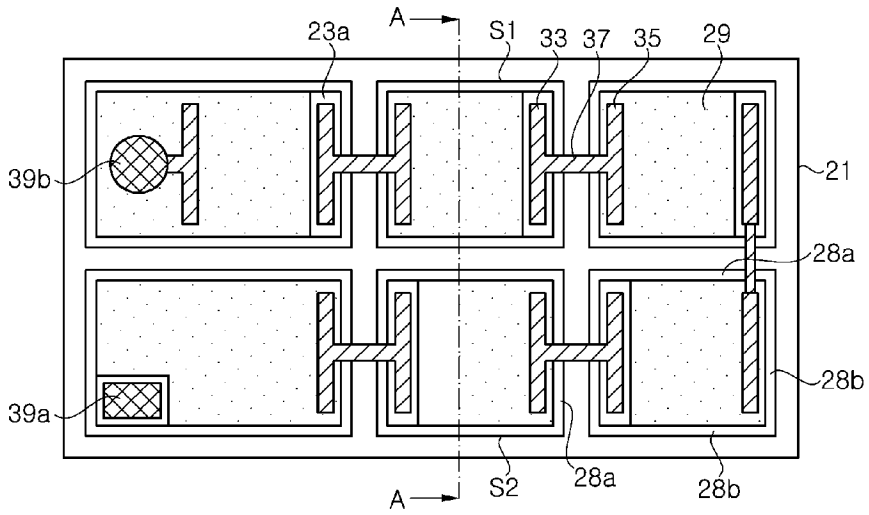
[Claim 11] The method of claim 10, wherein the first conductivity type semiconductor layer is exposed in a contact area for forming an ohmic contact and in a scribing line area.

[Claim 12] The method of claim 11, further comprising:
forming an insulation layer covering the isolation trench and the scribing line area, the insulation layer exposing the contact area.

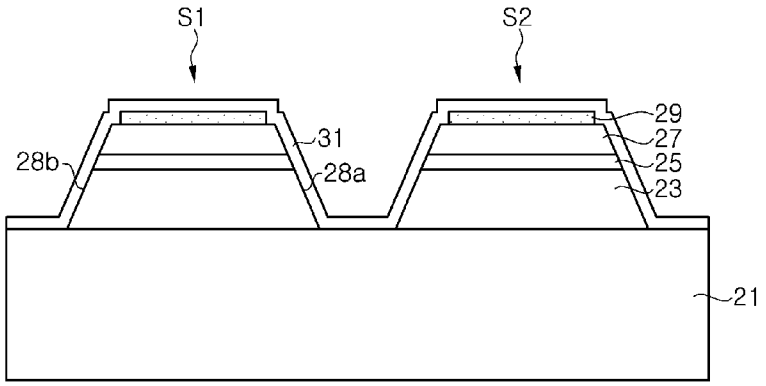
[Claim 13] A light emitting diode comprising:
a substrate; and
a plurality of light emitting elements disposed on the substrate,
at least one of the light emitting elements comprising a side surface slanted at an angle of less than 90° relative to an upper surface of the substrate and a side surface perpendicular to the upper surface of the substrate.

[Claim 14] The light emitting diode of claim 13, wherein the perpendicular side surface is flush with a side surface of the substrate.

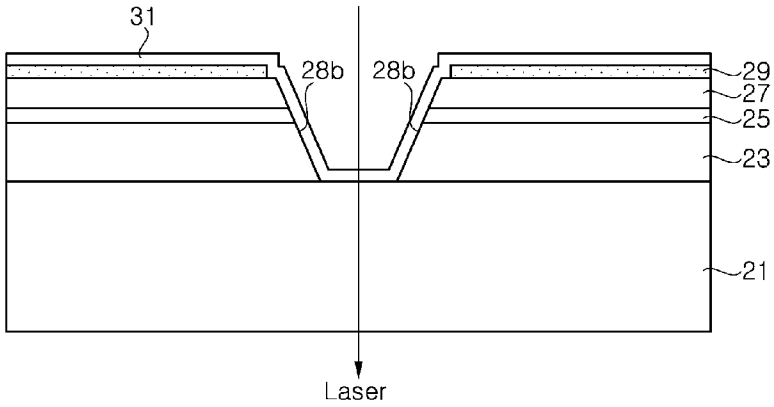
[Fig. 1]



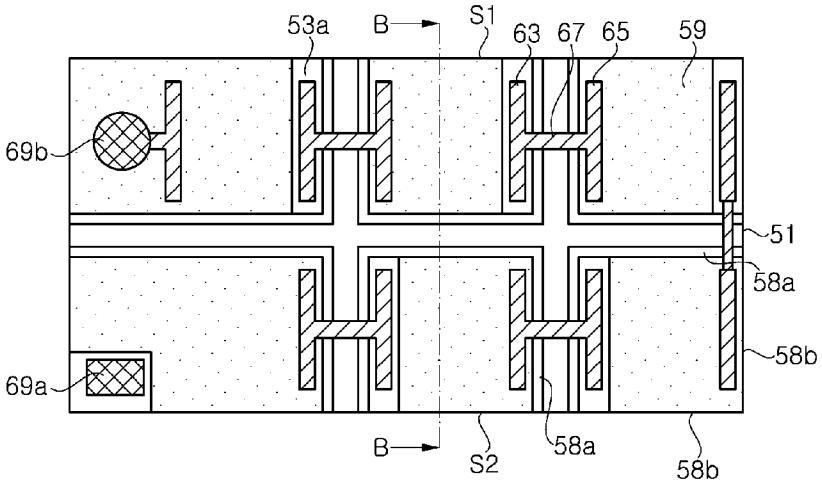
[Fig. 2]



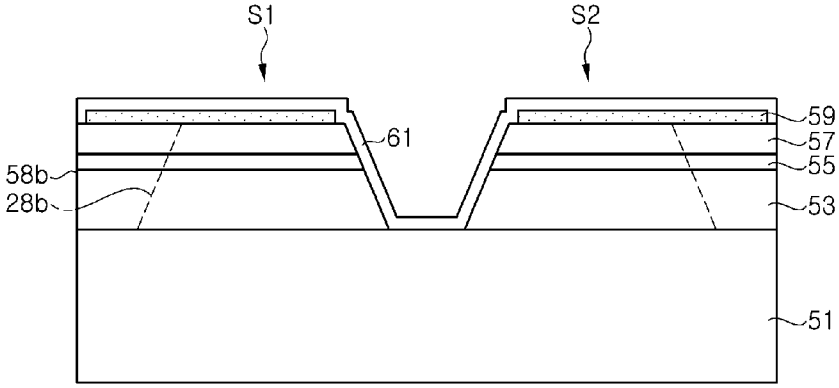
[Fig. 3]



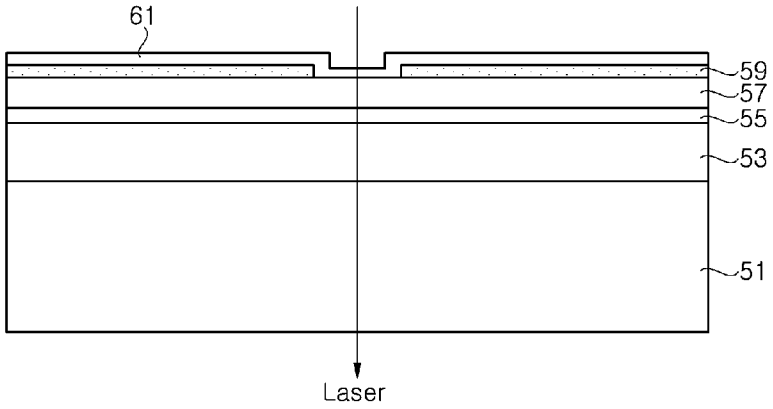
[Fig. 4]



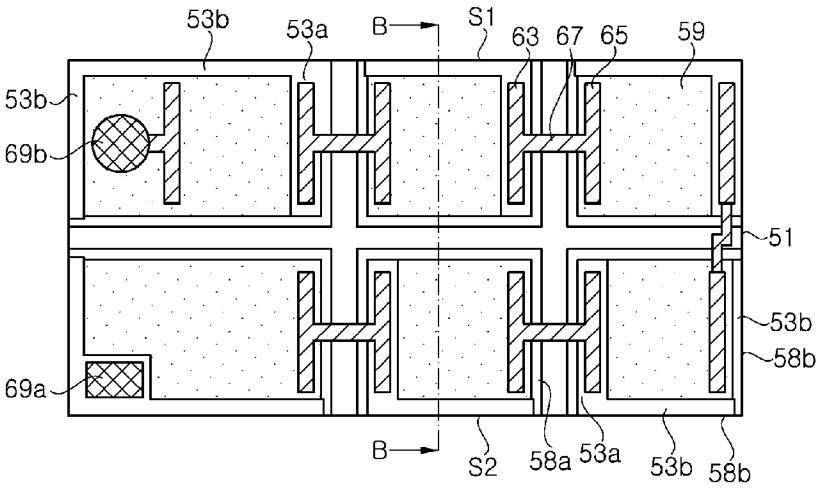
[Fig. 5]



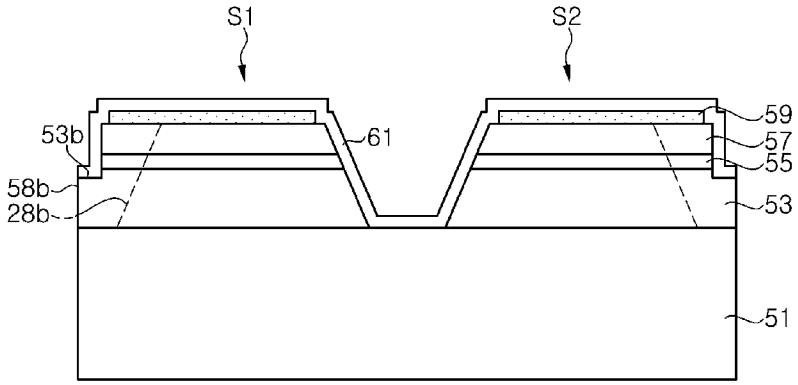
[Fig. 6]



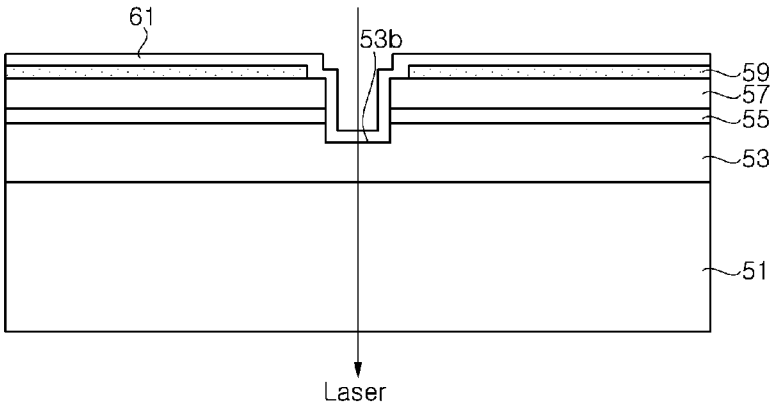
[Fig. 7]



[Fig. 8]



[Fig. 9]



INTERNATIONAL SEARCH REPORT

International application No.
PCT/KR2014/004496

A. CLASSIFICATION OF SUBJECT MATTER

H01L 33/36(2010.01)i, H01L 33/20(2010.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 33/36; H01S 5/323; H01L 33/20; H01L 33/10; H01L 33/02; H01L 33/00; H01S 5/18

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: LED, outer face, perpendicular, slanted side, light emitting area, flush

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	JP 2009-117662 A (SANYO ELECTRIC CO., LTD.) 28 May 2009 See abstract, paragraphs 21-40, claims 1-9 and figure 9.	13-14
Y		1-7
A		8-12
Y	KR 10-0663910 B1 (SEOUL OPTO DEVICE CO., LTD.) 02 January 2007 See abstract, paragraphs 47, 53 and figure 4d.	1-7
A		8-14
Y	KR 10-2012-0086878 A (LG INNOTEK CO., LTD.) 06 August 2012 See paragraphs 27, 33, claim 1 and figure 2.	6-7
A		1-5,8-14
A	US 2001-0000209 A1 (MICHAEL R. KRAMES et al.) 12 April 2001 See abstract, paragraphs 23-30, 41-42 and figures 2, 10-11.	1-14
A	JP 2759275 B2 (ANRITSU CORP. et al.) 28 May 1998 See pages 2-3, claim 1 and figures 1-2.	1-14

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
02 September 2014 (02.09.2014)	**02 September 2014 (02.09.2014)**

Name and mailing address of the ISA/KR
International Application Division
Korean Intellectual Property Office
189 Cheongsa-ro, Seo-gu, Daejeon Metropolitan City, 302-701,
Republic of Korea
Facsimile No. +82-42-472-7140

Authorized officer
PARK, Hye Lyun
Telephone No. +82-42-481-3463

Form PCT/ISA/210 (second sheet) (July 2009)

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/KR2014/004496

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
JP 2009-117662 A	28/05/2009	CN 101809833 A	18/08/2010
		CN 101809833 B	30/05/2012
		CN 101952982 A	19/01/2011
		CN 101952982 B	01/05/2013
		CN 102545055 A	04/07/2012
		CN 103199433 A	10/07/2013
		JP 2009-088103 A	23/04/2009
		JP 2009-152502 A	09/07/2009
		JP 2009-158896 A	16/07/2009
		JP 2009-170496 A	30/07/2009
		JP 2009-170609 A	30/07/2009
		JP 5078528 B2	21/11/2012
		JP 5172322 B2	27/03/2013
		JP 5232993 B2	10/07/2013
		JP 5245030 B2	24/07/2013
		JP 5245031 B2	24/07/2013
		JP 5250759 B2	31/07/2013
		US 2010-0246624 A1	30/09/2010
		US 2010-0265981 A1	21/10/2010
		US 8750343 B2	10/06/2014
		WO 2009-041462 A1	02/04/2009
		WO 2009-081762 A1	02/07/2009
KR 10-0663910 B1	02/01/2007	None	
KR 10-2012-0086878 A	06/08/2012	None	
US 2001-0000209 A1	12/04/2001	DE 19807758 A1	10/12/1998
		DE 19807758 B4	14/08/2008
		GB 2326023 A	09/12/1998
		GB 9811180 D0	22/07/1998
		JP 10-341035 A	22/12/1998
		JP 2006-135360 A	25/05/2006
		KR 10-0745229 B1	16/10/2007
		KR 10-0753710 B1	30/08/2007
		KR 10-2007-0042938 A	24/04/2007
		US 2001-0000410 A1	26/04/2001
		US 2002-0093023 A1	18/07/2002
		US 2004-0227148 A1	18/11/2004
		US 2006-0011935 A1	19/01/2006
		US 6229160 B1	08/05/2001
		US 6323063 B2	27/11/2001
		US 6570190 B2	27/05/2003
		US 6784463 B2	31/08/2004
		US 6946309 B2	20/09/2005
		US 7268371 B2	11/09/2007
JP 2759275 B2	28/05/1998	JP 02-218182 A	30/08/1990