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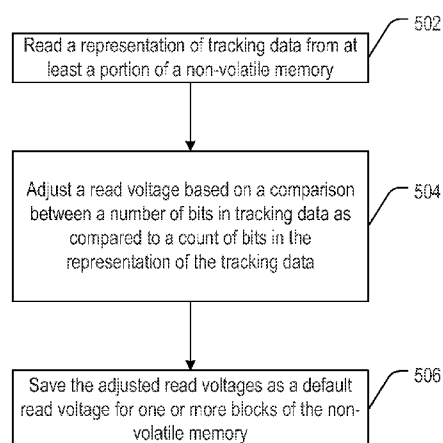


FIG. 5

(57) **Abstract:** A storage device includes a read voltage engine (114) which is located either in a controller (112) or in a memory (104). Due to various effects such as data retention, read disturb, and/or program disturb, threshold voltages of data storage elements may shift, producing errors when read using the original set of read voltages. The read voltage engine (114) adjusts a read voltage to be used by the controller (112) to read data from the non-volatile memory (104). During operation, when data is to be read from the memory (104), such as when a request is received from the host device (116), the controller (112) may be configured to read a representation (122) of the tracking data (109) from at least a portion of the memory (104), such as the first portion (108). Over time the stored tracking data (109) may be susceptible to errors, resulting in the representation (122) of the tracking data (109) that may include one or more errors. The controller (112) may further compare a count of bits in the representation (122) of the tracking data (109) corresponding to storage elements in one or more states read from the memory (104) to a corresponding count of bits in the tracking data (109) and the read voltage engine (114) may be configured to adjust a read voltage to be used by the controller (112) to read data from the memory (104) based on the comparison.

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SYSTEM AND METHOD TO UPDATE READ VOLTAGES IN A NON-VOLATILE MEMORY IN RESPONSE TO TRACKING DATA

CROSS-REFERENCE TO RELATED APPLICATIONS

The present application claims priority to U.S. Provisional Application No. 61/736,967,
5 filed December 13, 2012, and to U.S. Application No. 13/757,771, filed February 2,
2013. The contents of each of these applications are expressly incorporated herein by
reference in their entirety.

FIELD OF THE DISCLOSURE

The present disclosure is generally related to updating read voltages in a data storage
10 device.

BACKGROUND

Non-volatile data storage devices, such as universal serial bus (USB) flash memory
devices or removable storage cards, have allowed for increased portability of data and
software applications. Flash memory devices can enhance data storage density by
15 storing multiple bits in each flash memory cell. For example, Multi-Level Cell (MLC)
flash memory devices can provide increased storage density by storing 3 bits per cell, 4
bits per cell, or more.

Storing multiple bits of information in a single flash memory cell typically includes
mapping sequences of bits to states of the flash memory cell. For example, a first
20 sequence of bits “110” may correspond to a first state of a flash memory cell and a
second sequence of bits “010” may correspond to a second state of the flash memory
cell. After determining that a sequence of bits is to be stored into a particular flash
memory cell, the particular flash memory cell may be programmed to a state (e.g., by
setting a threshold voltage) that corresponds to the sequence of bits.

25 Once memory cells in a data storage device have been programmed, data may be read
from the memory cells by sensing the programmed state of each memory cell by
comparing the cell threshold voltage to one or more read voltages. However, the sensed

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programming states can sometimes vary from the written programmed states due to one or more factors, such as data retention and program disturb conditions.

SUMMARY

Accuracy of reading data stored in a data storage device may be improved by updating a
5 set of read voltages used to read the stored data in order to reduce a count of errors
associated with reading the stored data. Updating may be performed based on a
comparison of tracking data to a representation of the tracking data that is read from a
memory of the data storage device. For example, updating may be performed in
response to a comparison of a number of bits in the tracking data to a count of bits in a
10 representation of the tracking data read from the memory. The tracking data may
correspond to a portion of a tracking pattern that is stored in the memory and the
number of bits in the tracking data may indicate a first number of storage elements in
one or more states when the tracking pattern is stored to the memory. The count of bits
in the representation of the tracking data may indicate a second number of storage
15 elements in the one or more states when the representation of the tracking data is read
from the memory. One or more updated read voltages may be determined based on the
comparison.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of an illustrative embodiment of a system including a data
20 storage device configured to compare a representation of tracking data read from a
memory to tracking data;

FIG. 2 is a diagram illustrating an example of updating a read voltage that may be
performed by the data storage device 102 of FIG. 1;

FIG. 3 is a diagram illustrating generation and storage of tracking data that includes a
25 tracking pattern to be retrievable for determination of errors in the tracking data;

FIG. 4 is a flow diagram illustrating a particular embodiment of a method of comparing
a count of bits in a representation of tracking data read from a memory to a
corresponding count of bits in tracking data;

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FIG. 5 is a flow diagram illustrating another particular embodiment of a method of comparing a count bits in a representation of tracking data read from a memory to a corresponding count of bits in tracking data; and

FIG. 6 is a flow diagram illustrating a particular embodiment of a method of storing
5 tracking data with user data to be retrievable for updating of read voltages.

DETAILED DESCRIPTION

Referring to FIG. 1, a particular illustrative embodiment of a system 100 includes a data storage device 102 that is configured to update read voltages. The data storage device 102 includes a memory 104 coupled to a controller 112. The data storage device 102 is
10 configured to enable exchange of data between a host device 116 and the memory 104 of the data storage device 102.

The host device 116 may be configured to provide data to be stored at the memory 104 or to request data to be read from the memory 104. For example, the host device 116 may include a mobile telephone, a music or video player, a gaming console, an
15 electronic book reader, a personal digital assistant (PDA), a computer such as a laptop computer, a notebook computer, or a tablet, any other electronic device, or any combination thereof.

The data storage device 102 may be a memory card, such as a Secure Digital SD® card, a microSD® card, a miniSD.TM card (trademarks of SD-3C LLC, Wilmington,
20 Delaware), a MultiMediaCard.TM (MMC.TM) card (trademark of JEDEC Solid State Technology Association, Arlington, Virginia), or a CompactFlash® (CF) card (trademark of SanDisk Corporation, Milpitas, California). As another example, the data storage device 104 may be embedded memory in the host device 102, such as eMMC® (trademark of JEDEC Solid State Technology Association, Arlington, Virginia)
25 memory and eSD memory, as illustrative examples.

The memory 104 may be a non-volatile memory of a flash device, such as a NAND flash device, a NOR flash device, or any other type of flash device. The memory 104 may include a group of storage elements 106. For example, the group of storage elements 106 may include a word line, a page, or a block. The word line may include a

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first portion 108 configured to store tracking data 109 and a second portion 110 configured to store user data 111. The tracking data 109 may be retrievable for determination of errors in the tracking data 109. Each storage element in the group of storage elements 106 may be a memory cell of a multi-level cell (MLC) memory.

- 5 Each storage element may have an associated threshold voltage corresponding to a state of the storage element. Each state may correspond to a particular range of threshold voltage values, such as illustrated in FIG. 2. For example, a cell voltage distribution (CVD) for a multi-level-cell (MLC) memory may be approximated by a set of Gaussian functions. Each Gaussian function may represent a threshold voltage distribution of
10 cells programmed to a particular state.

The state of each storage element represents data stored at the storage element, such as according to a mapping of bits to states of the storage element. The data stored at the storage element may be read by comparing a threshold voltage of the storage element to one or more read voltages of a set of read voltages that are stored in the memory 104,
15 such as described with respect to FIG. 2. One or more read voltages of the set of read voltages may be used to sense one or more data bits stored in each of the storage elements of the group of storage elements 106.

The controller 112 may include a read voltage engine 114. Alternatively, the read voltage engine 114 may be within the memory 104. Due to various effects such as data
20 retention, read disturb, and/or program disturb, threshold voltages of the data storage elements may shift, producing errors when read using the original set of read voltages. The read voltage engine 114 may be configured to adjust a read voltage to be used by the controller 112 to read data from the non-volatile memory 104.

During operation, when data is to be read from the memory 104, such as when a request
25 is received from the host device 116, the controller 112 may be configured to read a representation 122 of the tracking data 109 from at least a portion of the memory 104, such as the first portion 108. For example, over time, the stored tracking data 109 may be susceptible to errors, resulting in the representation 122 of the tracking data 109 that may include one or more errors. Similarly, the controller 112 may be configured to read

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a representation 126 of the user data 111 from another portion of the memory 104, such as the second portion 110.

The controller 112 may further be configured to compare a count of bits in the representation 122 of the tracking data 109 corresponding to storage elements in one or
5 more states (such as an erase state, a state A, a state B, and a state C as illustrated in FIG. 2) read from the memory 104 to a corresponding count of bits in the tracking data 109. To illustrate, the tracking data 109 may correspond to a portion of a tracking pattern. For example, the tracking pattern may include a first sequence of bits that corresponds to a first state of a flash memory cell, a second sequence of bits that
10 correspond to a second state of the flash memory cell, etc. The tracking pattern may be interleaved across multiple logical pages when stored in the first portion 108, and the tracking data 109 may correspond to a single bit (e.g., a most significant bit) of each of the sequences of bits that is read by reading a single logical page of data from the group of storage elements 106.

15 The controller 112 may be configured to determine a number of bits in the tracking data 109 (e.g., a count of '1' bits in the tracking data 109) corresponding to a first number of storage elements in the first state when the tracking pattern is stored to the memory 104. The controller 112 may be configured to determine a count of bits in the representation 122 of the tracking data 109 read from the memory 104 (e.g., a count of '1' bits in the
20 representation 122) that corresponds to a second number of storage elements in the first state when the representation 122 of the tracking data 109 is read from the memory 104. The controller 112 may be configured to compare the number of bits in the tracking data 109 to the count of bits in the representation 122 of the tracking data, and the read voltage engine 114 may be configured to adjust a read voltage to be used by the
25 controller 112 to read data from the memory 104 based on the comparison.

For example, as described in further detail with respect to FIG. 2, when the tracking pattern corresponds to equal numbers of storage elements in each state but the representation 122 of the tracking data 109 indicates unequal numbers of storage elements in each state, the read voltage engine 114 may identify one or more states
30 having storage elements that have shifted from an originally programmed state to another state. To illustrate, storage elements that have shifted to another state may have

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threshold voltages that have been disturbed from a programmed value that is greater than a particular read voltage to a read value that is less than the particular read voltage. The read voltage engine 114 may adjust one or more read voltages to shift the boundaries between states to at least partially compensate for the shifted threshold

5 voltages. As a result, adjusted read voltages may enable the controller 112 to read the tracking data 109 from the group of storage elements 106 with fewer errors as compared to using unadjusted read voltages. For example, updated read voltages 124 may be sent by the controller 112 to the memory 104 and used by the memory 104 to perform a subsequent read of the group of storage elements 106 of the memory 104.

10 Because the first portion 108 and the second portion 110 are within the same group of storage elements 106, such as the same word line, processes that affect storage elements in the first portion 108, such as read disturb, program disturb, data retention, etc., are likely to have similar effects on storage elements in the second portion 110. By adjusting the read voltages to achieve a reduction in errors when the tracking data 109 is

15 read from the first portion 108, a similar reduction in errors may be achieved when the user data 111 is read from the second portion 110. As a result, the user data 111 may be read using the adjusted read voltages with greater accuracy and reduced errors based on comparing the representation 122 of the tracking data 109 read from the memory 104 to the originally programmed tracking data 109 without performing error correction coding

20 (ECC) on the representation 122 of the tracking data 109.

By adjusting read voltages based on comparing a count of bits in the representation 122 of the tracking data 109 read from the memory 104 to a number of bits in the tracking data 109, a reduction in errors may be achieved. As a result, a reliability of stored data may be improved due to fewer bit errors occurring during storage in the memory 104.

25 Improved reliability may enable operation using a less-powerful ECC engine, resulting in reduced power consumption, reduced device size, reduced manufacturing cost, or a combination thereof. Alternatively, or in addition, improved reliability may enable longer operational life of the memory 104. In addition, fewer errors may result in reduced ECC processing, enabling faster data retrieval and reduced latency detected by

30 the host device 116.

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FIG. 2 illustrates an example of updating a read voltage based on comparing a count of storage elements in one or more states in a representation of tracking data read from a memory to a count of storage elements in one or more corresponding states in tracking data, such as may be performed by the read voltage engine 114 of FIG. 1. For example, a first set of curves 210 represents cell voltage distributions (CVDs) of states of a multi-level-cell storage element (e.g., a 2-bit per cell storage element, a 3-bit per cell storage element, etc.), such as one or more storage elements of the group of storage elements 106 of FIG. 1, after threshold voltage shifting has occurred. A first curve 212 of the first set 210 represents a CVD of an erase state, a second curve 214 of the first set 210 represents a CVD of state A, a third curve 216 of the first set 210 represents a CVD of state B, and a fourth curve 218 of the first set 210 represents a CVD of state C. A first read voltage V_a 213, a second read voltage V_b 215, and a third read voltage V_c 217 are also illustrated.

The first curve 212 represents a CVD of an erase state including a portion that crosses over the first read voltage V_a 213. To illustrate, the first curve 212 has a portion that lies to the right of (i.e., having a greater voltage than) the read voltage V_a 213 and another portion that lies to the left of the read voltage V_a 213. Reading the storage elements with the read voltage V_a 213 causes the storage elements of the portion of the first curve 212 to the right of the read voltage V_a 213 to be misidentified as being in state A instead of in the erase state. Similarly, the second curve 214 has a portion that lies to the right of the read voltage V_b 215 and another portion that lies to the left of the read voltage V_b 215. Reading the storage elements with the read voltage V_a 213 causes the storage elements of the portion of the second curve 214 to the right of the read voltage V_b 215 to be misidentified as being in state B instead of in state A. Similarly, the third curve 216 has a portion that lies to the left of the read voltage V_b 215, a portion between the read voltage V_b 215 and the read voltage V_c 217, and a portion to the right of the read voltage V_c 217. Reading the storage elements with the read voltage V_c 217 causes the storage elements of the portion of the third curve 216 to the right of the read voltage V_c 217 to be misidentified as being in state C instead of in state B, and reading the storage elements with the read voltage V_b 215 causes the storage elements of the portion of the third curve 216 to the left of the read voltage V_b 215 to be misidentified as being in state A instead of in state B. Similarly, the fourth curve 218

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has a portion that lies to the left of the read voltage V_c 217. Reading the storage elements with the read voltage V_c 217 causes the storage elements of the portion of the fourth curve 218 to the left of the read voltage V_c 217 to be misidentified as being in state B instead of in state C.

5 A second set of curves 220 represents CVDs of the states of the multi-level-cell storage element after read voltage updating has occurred. A first curve 222 of the second set 220 represents a CVD of an erase state, a second curve 224 of the second set 220 represents a CVD of state A, a third curve 226 of the second set 220 represents a CVD of state B, and a fourth curve 228 of the second set 220 represents a CVD of state C. A
10 first adjusted read voltage V_a 223, a second adjusted read voltage V_b 225, and a third adjusted read voltage V_c 227 are also illustrated.

The tracking data 109 of FIG. 1 may be a portion of a tracking pattern with known locations in the memory 104 of FIG. 1. The tracking pattern includes a sequence of bits that correspond to one or more states of a flash memory cell. For example, in a 2-bit per
15 cell multi-level-cell memory, the sequence of bits may include a first sequence of bits that corresponds to a first state of a flash memory cell, a second sequence of bits that corresponds to a second state of the flash memory cell, a third sequence of bits that corresponds to a third state of the flash memory cell, and a fourth sequence of bits that corresponds to a fourth state of the flash memory cell. To illustrate, the first sequence
20 of bits may correspond to a logic level of "11" that corresponds to the erase state, the second sequence of bits may correspond to a logic level of "01" that corresponds to state A, the third sequence of bits may correspond to a logic level of "10" that corresponds to state B, and the fourth sequence of bits may correspond to a logic level of "00" that corresponds to state C. The tracking data 109 of FIG. 1 may also include a
25 known number of bits per pattern. For example, the tracking data 109 may include an equal number of each of the bit sequences (e.g., an equal number of each of the states) such as 64 bit sequences corresponding to an erase state, 64 bit sequences corresponding to state A, 64 bit sequences corresponding to state B, and 64 bit sequences corresponding to state C. Alternatively or in addition, the tracking data 109 may
30 include an unequal number of the bit sequences.

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As an illustrative example, a 2-bit per cell storage element with a tracking pattern corresponding to equal numbers of storage elements per state (e.g., an original bit sequence 230 corresponding to 64 storage elements per state) is shown in FIG. 2. Over time, the stored tracking data 109 may be susceptible to errors and the representation
5 122 of the tracking data 109 read from the memory 104 of FIG. 1 may indicate unequal numbers of storage elements in each state. For example, one or more states may have storage elements that have shifted from an originally programmed state to another state.

Because the tracking data 109 of FIG. 1 is in a known location in the memory 104 of FIG. 1 and corresponds to a known number of storage elements per state, the controller
10 112 of FIG. 1 may determine a number of storage elements in a particular state when the tracking data 109 is programmed to the memory 104. For example, an original read bit sequence 232 prior to voltage shifting may be determined as having 64 storage elements for the erase state, 64 storage elements for state A, 64 storage elements for state B, and 64 storage elements for state C. The controller 112 of FIG. 1 may further
15 determine a count of storage elements in a particular state in the representation 122 of the tracking data 109 of FIG. 1 and compare the number of storage elements in the particular state corresponding to the tracking data 109 to the count of storage elements in the particular state in the representation 122 of the tracking data 109.

For example, a bit sequence after voltage threshold shift 234 may be determined as
20 having 59 storage elements for the erase state, 69 storage elements for state A, 68 storage elements for state B, and 60 storage elements for state C. The controller 112 of FIG. 1 may compare the count of storage elements in the erase state in the tracking pattern (e.g., 64) to the count of storage elements in the erase state in the representation 122 of the tracking data 109 read from the memory 104 of FIG. 1 (e.g., 59), and based
25 on the comparison, the read voltage engine 114 of FIG. 1 may adjust a read voltage to be used by the controller 112 to read data from the memory 104. For example, the read voltage engine 114 may adjust one or more of the read voltages Va 213, Vb 215, and Vc 217 to shift the boundaries between states to at least partially compensate for the shifted threshold voltages, resulting in a partially corrected bit sequence 236 that more closely
30 matches the original bit sequence 232. As a result, the adjusted read voltages Va 223, Vb 225, and Vc 227 may enable the controller 112 of FIG. 1 to read the tracking data

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109 of FIG. 1 from the group of storage elements 106 of FIG. 1 with fewer errors as compared to using the unadjusted read voltages V_a 213, V_b 215, and V_c 217.

A reduction in errors may be achieved by adjusting read voltages based on comparing a count of storage elements in one or more states in the representation 122 of the tracking
5 data 109 read from the memory 104 to a count of storage elements in one or more corresponding states in the tracking data 109. As a result, a reliability of stored data may be improved due to fewer bit errors occurring during storage in the memory 104.

FIG. 3 illustrates a particular embodiment of generation and storage of tracking data to be retrievable from a memory, such as the memory 104 of FIG. 1, for determination of
10 errors in the tracking data. A memory cell array 300 includes a plurality of word lines 310 and a plurality of bit lines 330. A cross point between a particular word line and a particular bit line represents a memory cell, such as a representative memory cell 301. The representative memory cell 301 may be a NAND flash memory cell and may include a floating gate transistor 303.

15 A tracking data generator 302 may be configured to generate tracking data, such as the tracking data 109, to be stored in the memory cell array 300. The tracking data may include a portion of a tracking pattern such as the tracking pattern described with respect to FIG. 2. The tracking data generator 302 may include a linear feedback shift register (LFSR) 304 and a random access memory (RAM) 306. For example, the
20 tracking data generator 302 may load a bit sequence from the RAM 306 to initiate the LFSR 304 to generate a tracking pattern. Alternatively, or in addition, the tracking pattern may be stored in the RAM 306 in place of using the LFSR 304.

The tracking data generator 302 may receive a word line address 308 associated with a write request from a host device, such as the host device 116 of FIG. 1, and may be
25 configured to generate the tracking data 109 based on the word line address 308 and to store the tracking data 109 in a portion of a word line 312. The tracking data 109 may be stored in a first portion of the word line 312 in a group of memory cells at consecutive indices of the word line 312. Alternatively, or in addition, the tracking data 109 may be stored in multiple portions within the word line 312, such as in a first and
30 third portion of the word line 312 that may be separated by user data stored in a second

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- portion of the word line 312. The tracking data generator 302 may generate a tracking pattern that includes a repeating series of bit sequences “00”, “01”, “10”, and “11”. A starting sequence of the repeating series of sequences may be selected based on the word line address 308 so that neighboring adjacent cells in word lines store different bit sequences. In an implementation where user data is interleaved across multiple logical pages of the word line 312, the tracking data 109 may correspond to the tracking pattern. In an implementation where user data is not interleaved across multiple pages of the word line 312, the tracking data 109 may correspond to a single bit of each bit sequence of the tracking pattern.
- 10 An ECC engine 320 may be configured to receive user data, such as the user data 111, from a host device, such as the host device 116 of FIG. 1, and to generate a codeword 322 that includes the user data 111 and parity bits 324. The ECC engine 320 may be configured to store the codeword 322 in a second portion of the word line 312 such that the tracking data 109 in the first portion of the word line 312 is separated from the tracking data 109 in the third portion of the word line 312 by the user data 111 in the codeword 322. In a particular implementation, the tracking data 109 and the codeword 322 may be written to the word line 312 substantially concurrently. For example, the ECC engine 320 may include a Reed Solomon encoder, a Bose-Chaudhuri-Hocquenghem (BCH encoder), a low density parity check (LDPC) encoder, a turbo code encoder, an encoder configured to encode one or more other ECC encoding schemes, or any combination thereof. The ECC engine 320 may also include a decoder configured to decode data read from the memory cell array 300 to detect and correct, up to an error correction capability of a particular ECC scheme, bit errors that may be present in the user data 111.
- 25 During operation, the tracking data generator 302 may generate the tracking data 109 to be stored in a first portion of the word line 312 within the memory cell array 300 and the ECC engine 320 may generate the codeword 322 that includes the user data 111 and the parity bits 324 to be stored in a second portion of the word line 312. The tracking data 109 may be retrievable for determination of errors in the tracking data 109.
- 30 By storing the tracking data 109 with the user data 111 in the same word line of the memory cell array 300, processes that affect storage elements in the first portion of the

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word line 312, such as read disturb, program disturb, data retention, etc., are likely to have similar effects on storage elements in the second portion of the word line 312. By adjusting read voltages to achieve a reduction in errors in the tracking data 109 read from the first portion of the word line 312, a similar reduction in errors may be achieved in the user data 111 read from the second portion of the word line 312. As a result, the user data 111 (and the parity bits 324) may be read using the adjusted read voltages with greater accuracy and reduced errors.

Referring to FIG. 4, a flowchart of an illustrative embodiment of a method 400 of updating threshold voltages based on comparing a count of storage elements in one or more states in a representation of tracking data read from a memory to a count of storage elements in one or more corresponding states in tracking data is illustrated. The method 400 may be applied by the data storage device 102 of FIG. 1.

A host write command may be received, at 402. For example, the data storage device 102 of FIG. 1 may receive a write command from the host device 116 of FIG. 1 to provide data to be stored in the memory 104 of FIG. 1.

Tracking data may be written with user data to a known location in a memory, at 404. For example, the tracking data generator 302 of FIG. 3 may generate the tracking data 109 of FIG. 1 to be written to a first portion of the word line 312 of FIG. 3 within the memory cell array 300 of FIG. 3 and the ECC engine 320 of FIG. 3 may generate the codeword 322 of FIG. 3 that includes the user data 111 of FIG. 1 to be written to a second portion of the word line 312.

The integrity of the original user data may be verified, at 406. For example, the controller 112 of FIG. 1 may read the originally stored user data 111 of FIG. 1 from the memory 104 of FIG. 1 and may verify the integrity of the user data 111 via the ECC engine 320 of FIG. 3.

Over time, the stored tracking data 109 of FIG. 1 and the stored user data 111 of FIG. 1 may be susceptible to errors such as data retention, read disturb, and/or program disturb. As such, threshold voltages of data storage elements within the memory 104 of FIG. 1 may shift, producing errors when read using an original set of read voltages, as shown at 408.

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User data and tracking data may be read, at 410 (e.g., in response to a host request for the user data), and a determination may be made whether the user data is correctable via error correction coding, at 412. For example, the controller 112 of FIG. 1 may read the representation 126 of the user data 111 of FIG. 1 and the representation 122 of the tracking data 109 of FIG. 1 from the memory 104 of FIG. 1. The controller 112 of FIG. 1 may determine whether the representation 126 of the user data 111 of FIG. 1 is correctable via error correction coding (ECC) decoding. If the representation 126 of the user data 111 is correctable via ECC decoding, then corrected user data may be provided to the host, such as the host device 116 of FIG. 1, at 414.

10 If the representation 126 of the user data 111 is not correctable via ECC decoding, then a read operation may be performed on a lower page of the storage elements, at 416. A comparison of counts of bits in the lower page in a first set of states may be made to counts of bits in the lower page in a second set of states. For example, in a 2-bit per cell multi-level-cell memory, a first set of states may correspond to states that have a value of "1" in the lower page and a second set of states may correspond to states having a value of "0" in the lower page. A first count of bits with the value of "1" in the lower page may be compared to a second count of bits with the value of "0" in the lower page. To illustrate, the first set of states may correspond to the erase state (e.g., logic value "11") and the state A (e.g., logic value "01") of FIG. 2, and the second set of states may correspond to the state B (e.g., logic value "10") and the state C (e.g., logic value "00") of FIG. 2. The controller 112 of FIG. 1 may compare the first count of bits with the value of "1" in the erase state and in the state A to the second count of bits with the value of "0" in the state B and the state C, such as when the tracking data 109 corresponds to equal numbers of storage elements in each state. Alternatively, the controller 112 of FIG. 1 may compare the first count of bits with the value of "1" in the erase state and in the state A to a number of bits having a "1" value in the tracking data 109 (e.g., the bits of the tracking pattern of FIG. 3 stored in the lower page of the word line 312).

30 Voltage threshold shift(s) may be determined for the lower page, at 418. To illustrate, in an implementation where the tracking pattern corresponds to equal numbers of storage elements in each state, the read voltage V_b 215 of FIG. 2 may be shifted to

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substantially equalize the first count of bits with the value of “1” in the lower page with the second count of bits with the value of “0” in the lower page. For example, if the first count of bits in the lower page in the erase state and the state A equals the second count of bits in the lower page in the state B and the state C, then the read voltage Vb 215 is not shifted. If the first count of bits in the lower page in the erase state and the state A is less than the second count of bits in the lower page in the state B and the state C, then the read voltage Vb 215 is shifted to the right (e.g., increased). If the first count of bits in the lower page in the erase state and the state A is greater than the second count of bits in the lower page in the state B and the state C, then the read voltage Vb 215 is shifted to the left (e.g., decreased). The read voltage engine 114 of FIG. 1 may adjust one or more of the read voltages Va 213, Vb 215, or Vc 217 to be used by the controller 112 of FIG. 1 to read data from the memory 104 of FIG. 1.

A read operation may be performed on an upper page of the storage elements, at 420. A comparison of counts of bits in the upper page in a third set of states may be made to counts of bits in the upper page in a fourth set of states. For example, in the 2-bit per cell multi-level-cell memory, a third set of states may correspond to states that have a value of “1” in the upper page and a fourth set of states may correspond to states having a value of “0” in the upper page. A third count of bits with the value of “1” in the upper page may be compared to a fourth count of bits with a value of “0” in the upper page, and a fifth count of bits with the value of “0” in the upper page may be compared to a sixth count of bits with a value of “0” in the upper page. To illustrate, the third set of states may correspond to the erase state (e.g., logic value “11”) and the state B (e.g., logic value “10”) of FIG. 2, and the fourth set of states may correspond to the state A (e.g., logic value “01”) and the state C (e.g., logic value “00”) of FIG. 2. The third count of bits with the value of “1” in the upper page (corresponding to the erase state) may be compared to the fourth count of bits with the value of “0” in the upper page (corresponding to the state A). Similarly, the fifth count of bits with the value of “1” in the upper page (corresponding to the state B) may be compared to the sixth count of bits with the value of “0” in the upper page (corresponding to the state C).

Voltage threshold shift(s) may be determined for the upper page, at 422. For example, the read voltage Va 213 of FIG. 2 may be shifted to substantially equalize the third

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count of bits with the value of “1” in the upper page (corresponding to the erase state) with the fourth count of bits with the value of “0” in the upper page (corresponding to the state A). If the third count of bits in the upper page with a value of “1” in the erase state equals the fourth count of bits in the upper page with a value of “0” in the state A, then the read voltage Va 213 is not shifted. If the third count of bits in the upper page with a value of “1” in the erase state is less than the fourth count of bits in the upper page with a value of “0” in the state A, then the read voltage Va 213 is shifted to the right (e.g., increased). If the third count of bits in the upper page with a value of “1” in the erase state is greater than the fourth count of bits in the upper page with a value of “0” in the state A, then the read voltage Va 213 is shifted to the left (e.g., decreased).

Similarly, the read voltage Vc 217 of FIG. 2 may be shifted to substantially equalize the fifth count of bits with the value of “1” in the upper page (corresponding to the state B) with the sixth count of bits with the value of “0” in the upper page (corresponding to the state C). If the fifth count of bits in the upper page with a value of “1” in the state B equals the sixth count of bits in the upper page with a value of “0” in the state C, then the read voltage Vc 217 is not shifted. If the fifth of bits in the upper page with a value of “1” in the state B is less than the sixth count of bits in the upper page with a value of “0” in the state C, then the read voltage Vc 217 is shifted to the right (e.g., increased). If the fifth count of bits in the upper page with a value of “1” in the state B is greater than the sixth count of bits in the upper page with a value of “0” in the state C, then the read voltage Vc 217 is shifted to the left (e.g., decreased).

A subsequent read with updated read voltage(s) may be performed, at 424. For example, the updated read voltages 124 of FIG. 1 may be sent by the controller 112 of FIG. 1 to the memory 104 of FIG. 1 and used by the memory 104 of FIG. 1 to perform a subsequent read of the group of storage elements 106 of FIG. 1 of the memory 104 of FIG. 1.

Although the method 400 includes comparing counts of bits in data read from the memory, in other embodiments counts of bits in data read from the memory may be compared to corresponding numbers of bits of the tracking data. For example, in the example provided in FIG. 2 wherein 128 storage elements are in the erase state or state A, the tracking data for the lower page would be read as having 128 “1” bits and 128

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“0” bits if no storage elements have shifted states from originally programmed states. A count of “1” bits in the representation of the tracking data read from the lower page may be compared to the number 128 rather than compared to the count of “0” bits from the lower page tracking data. As another example, because 64 storage elements are in the erase state in the example of FIG. 2, a count of “1” bits corresponding to the upper
5 page of storage elements in the erase state may be compared to the number 64.

A reduction in errors may be achieved by adjusting read voltages based on comparing a count of storage elements in one or more states in the representation 122 of the tracking data 109 of FIG. 1 read from the memory 104 of FIG. 1 to a number of storage elements
10 corresponding to one or more corresponding states in the tracking data 109 of FIG. 1. As a result, a reliability of stored data may be improved due to fewer bit errors occurring during storage in the memory 104 of FIG. 1.

Referring to FIG. 5, a flowchart of an illustrative embodiment of a method 500 of updating read voltages based on comparing a count of bits in a representation of tracking data read from a memory to a number of bits in tracking data is illustrated. The
15 method 500 may be applied by the data storage device 102 of FIG. 1.

A representation of tracking data may be read from at least a portion of a non-volatile memory, at 502. For example, the representation 122 of the tracking data 109 of FIG. 1 may be read from the first portion 108 of FIG. 1 of the memory 104 of FIG. 1.

A read voltage may be adjusted based on a comparison between a number of bits in tracking data as compared to a count of bits in the representation of the tracking data, at 504. For example, the read voltage engine 114 of FIG. 1 may be configured to adjust a read voltage to be used by the controller 112 of FIG. 1 to read data from the memory 104 of FIG. 1 based on the comparison. To illustrate, the controller 112 of FIG. 1 may
20 compare the count of bits that correspond to storage elements in state A in the representation of the tracking data (e.g., 69 as illustrated in FIG. 2) to the count of bits that correspond to storage elements in state A in the originally stored tracking data (e.g., 64 as illustrated in FIG. 2). Based on the comparison, the read voltage engine 114 of FIG. 1 may identify that storage elements have shifted from another state (e.g., the erase
25 state and/or the state B) to the originally programmed state A. The read voltage engine
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114 of FIG. 1 may adjust one or more read voltages to shift the boundaries between states to compensate for the shifted threshold voltages.

The adjusted read voltage may be saved as a default read voltage for one or more blocks of the non-volatile memory, at 506. For example, the updated read voltage 124 of FIG. 1 may be sent by the controller 112 to the memory 104 and used by the memory 104 to perform a subsequent read of one or more blocks of the memory 104.

The method 500 therefore enables correction of read voltages to accommodate shifting threshold voltages to reduce errors without using error correction coding (ECC) decoding.

10 Referring to FIG. 6, a flowchart of an illustrative embodiment of a method 600 of storing tracking data with user data to be retrievable for updating of read voltages. The method 600 may be applied by the data storage device 102 of FIG. 1.

The method 600 may include storing, in a word line of a non-volatile memory, tracking data in a first portion of the word line with user data in a second portion of the word line, where the tracking data may include a tracking pattern to be retrievable for determination of errors in the tracking data. To illustrate, tracking data may be stored in a first portion of a word line of a non-volatile memory, where the tracking data may include a tracking pattern that is retrievable for determination of errors in the tracking data, at 602. For example, the tracking data generator 302 of FIG. 3 may generate the tracking data 109 of FIG. 1 to be written to a first portion of the word line 312 of FIG. 3 within the memory cell array 300 of FIG. 3.

User data may be stored in a second portion of the word line, at 604. For example, the ECC engine 320 of FIG. 3 may generate the codeword 322 of FIG. 3 that includes the user data 111 of FIG. 1 to be written to a second portion of the word line 312.

25 The tracking data is retrievable for determination of errors in the tracking data. To illustrate, when data is to be read from the memory 104 of FIG. 1, the controller 112 of FIG. 1 may read the representation 122 of the tracking data 109 from the first portion 108 of FIG. 1 and may compare a count of storage elements in one or more states in the representation 122 of the tracking data 109 read from the memory 104 of FIG. 1 to a

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count of storage elements in one or more corresponding states in the tracking data 109 of FIG. 1. The read voltage engine 114 of FIG. 1 may adjust a read voltage to be used by the controller 112 of FIG. 1 to read data from the memory 104 of FIG. 1 based on the comparison.

- 5 By adjusting read voltages based on comparing a count of storage elements in one or more states in the representation 122 of the tracking data 109 of FIG. 1 read from the memory 104 of FIG. 1 to a count of storage elements in one or more corresponding states in the tracking data 109 of FIG. 1, a reduction in errors may be achieved. As a result, a reliability of stored data may be improved due to fewer bit errors occurring
- 10 during storage in the memory 104 of FIG. 1.

Although various components depicted herein are illustrated as block components and described in general terms, such components may include one or more microprocessors, state machines, or other circuits configured to enable a data storage device, such as the data storage device 102 of FIG. 1, to perform the particular functions attributed to such

15 components. For example, the read voltage engine 114 of FIG. 1 may represent physical components, such as controllers, processors, state machines, logic circuits, or other structures to create an updated set of read voltages.

In a particular embodiment, the data storage device 102 may be a portable device configured to be selectively coupled to one or more external devices. For example, the

20 data storage device 102 may be a removable device such as a universal serial bus (USB) flash drive or a removable memory card. However, in other embodiments, the data storage device 102 may be attached or embedded within one or more host devices, such as within a housing of a portable communication device. For example, the data storage device 102 may be within a packaged apparatus, such as a wireless telephone, a

25 personal digital assistant (PDA), a gaming device or console, a portable navigation device, a computer, or other device that uses internal non-volatile memory. In a particular embodiment, the data storage device 104 includes a non-volatile memory, such as a Flash memory (e.g., NAND, NOR, Multi-Level Cell (MLC), Divided bit-line NOR (DINOR), AND, high capacitive coupling ratio (HiCR), asymmetrical contactless

30 transistor (ACT), or other Flash memories), an erasable programmable read-only memory (EPROM), an electrically-erasable programmable read-only memory

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(EEPROM), a read-only memory (ROM), a one-time programmable memory (OTP), or any other type of memory.

The illustrations of the embodiments described herein are intended to provide a general understanding of the various embodiments. Other embodiments may be utilized and
5 derived from the disclosure, such that structural and logical substitutions and changes may be made without departing from the scope of the disclosure. This disclosure is intended to cover any and all subsequent adaptations or variations of various embodiments.

The above-disclosed subject matter is to be considered illustrative, and not restrictive,
10 and the appended claims are intended to cover all such modifications, enhancements, and other embodiments, which fall within the scope of the present disclosure. Thus, to the maximum extent allowed by law, the scope of the present invention is to be determined by the broadest permissible interpretation of the following claims and their equivalents, and shall not be restricted or limited by the foregoing detailed description.

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WHAT IS CLAIMED IS:

1. A method comprising:
reading a representation of tracking data from at least a portion of a non-volatile
memory; and
5 adjusting a read voltage based on a comparison between a number of bits in the tracking
data to a count of bits in the representation of the tracking data.
2. The method of claim 1, wherein the number of bits in the tracking data corresponds
to a first number of storage elements in one or more states when the tracking data is
stored to a group of storage elements in the non-volatile memory, and wherein the count
10 of bits in the representation of the tracking data corresponds to a second count of
storage elements in the one or more states when the representation of the tracking data
is read from the group of storage elements.
3. The method of claim 1, wherein the tracking data is a portion of a tracking pattern
that is stored in the portion of the non-volatile memory.
- 15 4. The method of claim 3, wherein the tracking pattern is interleaved over multiple
logical pages in the non-volatile memory, and wherein the tracking data is the portion of
the tracking pattern at a single logical page of the multiple logical pages.
5. The method of claim 1, wherein the portion of the non-volatile memory comprises a
group of cells at consecutive indices of a wordline.
- 20 6. The method of claim 1, wherein the portion of the non-volatile memory comprises
multiple portions within a wordline and wherein the multiple portions are separated by
user data storage elements of the wordline.
7. The method of claim 1, wherein reading the representation of tracking data is
performed in response to a host read request.

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8. The method of claim 7, wherein data is read from the non-volatile memory in response to a host read request and wherein reading the representation of tracking data is performed in response to the read data being uncorrectable via error correction code (ECC) decoding.

5 9. The method of claim 1, further comprising saving the adjusted read voltage as a default read voltage for one or more blocks of the non-volatile memory.

10. The method of claim 1, wherein the read voltage is adjusted without error correction code (ECC) decoding of the representation of the tracking data.

11. A method comprising:

10 storing, in a wordline of a non-volatile memory, tracking data in a first portion of the wordline and storing user data in a second portion of the wordline, wherein the tracking data is retrievable for determination of errors in the tracking data.

12. The method of claim 11, further comprising retrieving the tracking data from the non-volatile memory.

15 13. The method of claim 11, wherein the tracking data is generated by a tracking data generator.

14. The method of claim 13, wherein the tracking data generator includes a linear feedback shift register.

20 15. The method of claim 11, wherein the portion of the non-volatile memory comprises a group of cells at consecutive indices of a wordline.

16. The method of claim 11, wherein the portion of the non-volatile memory comprises multiple portions within the wordline and wherein the multiple portions are separated by user data storage elements of the wordline.

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17. A data storage device comprising:
a non-volatile memory coupled to a controller; and
a read voltage correction engine configured to adjust a read voltage to be used by the
controller to read data from the non-volatile memory, wherein the read voltage is
5 adjusted based on a comparison between a count of storage elements in one or more
states in a representation of tracking data read from the non-volatile memory as
compared to a number of storage elements in the one or more corresponding states
according to a tracking pattern that includes the tracking data.
18. The data storage device of claim 17, wherein the read voltage correction engine is
10 in the controller.
19. The data storage device of claim 17, wherein the read voltage correction engine is
in the non-volatile memory.
20. The data storage device of claim 17, wherein the controller is configured to read the
representation of tracking data from a portion of the non-volatile memory, wherein the
15 portion of the non-volatile memory comprises a group of cells at consecutive indices of
a wordline.
21. The data storage device of claim 17, wherein the controller is configured to read the
representation of tracking data from a portion of the non-volatile memory, wherein the
portion of the non-volatile memory comprises multiple portions within a wordline, and
20 wherein the multiple portions are separated by user data storage elements of the
wordline.
22. The data storage device of claim 17, wherein the controller is configured to read the
data from the non-volatile memory in response to a host read request.

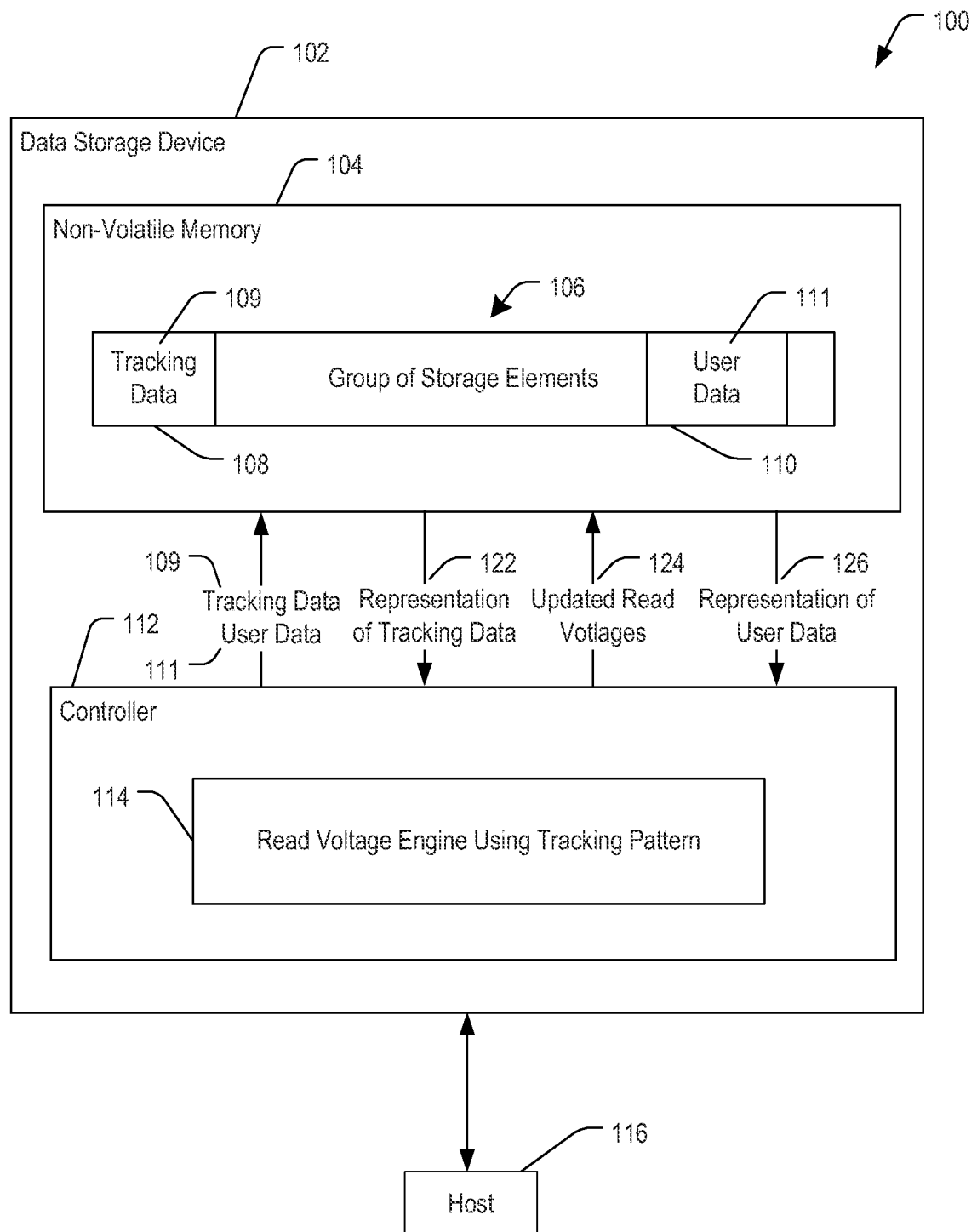
- 23 -

23. The data storage device of claim 22, wherein the controller is further configured to read the data from the non-volatile memory in response to determining that data read, in response to the host read request, is uncorrectable via error correction code (ECC) decoding.

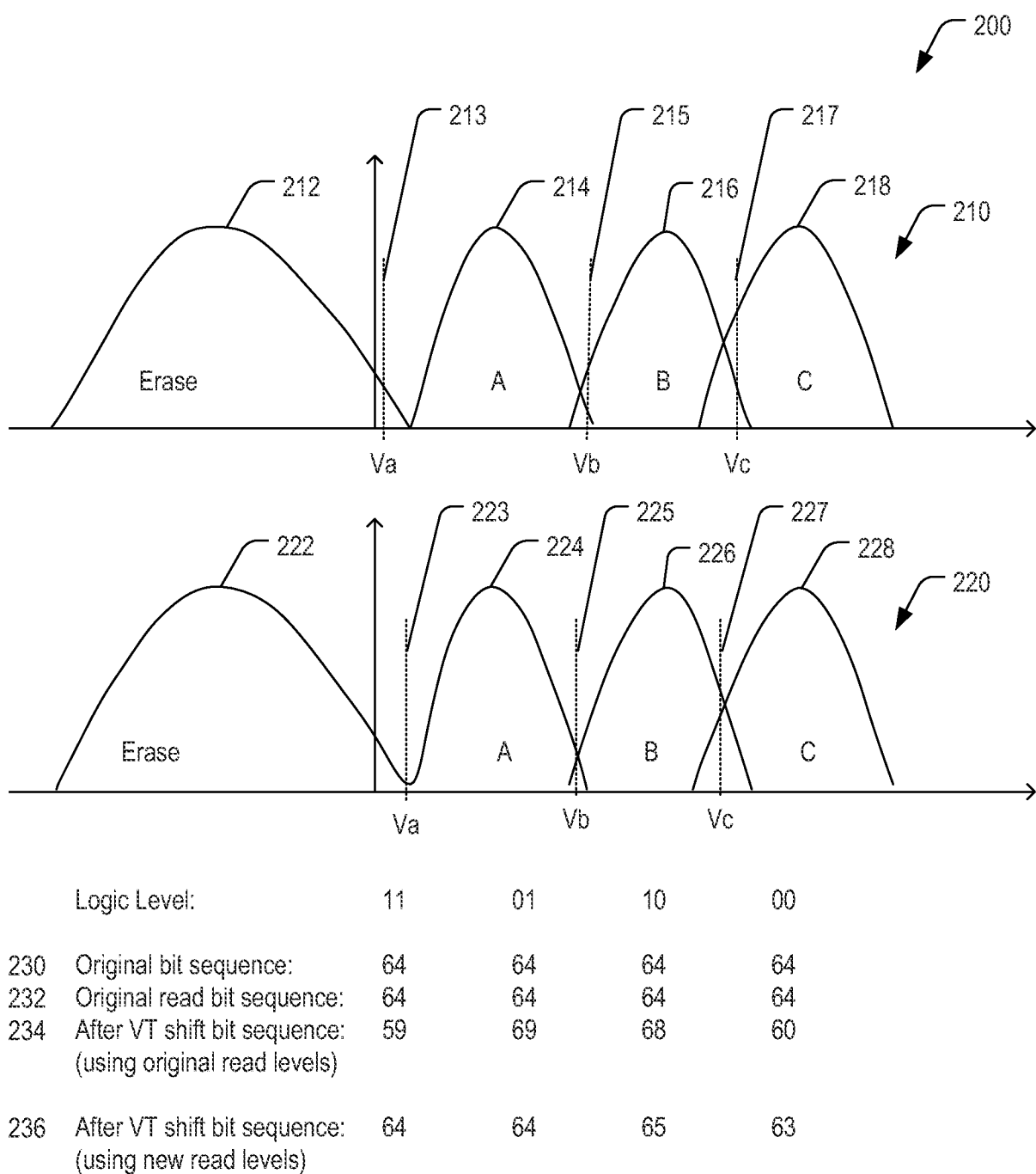
5 24. The data storage device of claim 17, wherein the controller is configured to save the adjusted read voltage as a default read voltage for one or more blocks of the non-volatile memory.

25. The data storage device of claim 17, wherein the read voltage correction engine is further configured to adjust the read voltage without error correction code (ECC)
10 decoding of the representation of the tracking data.

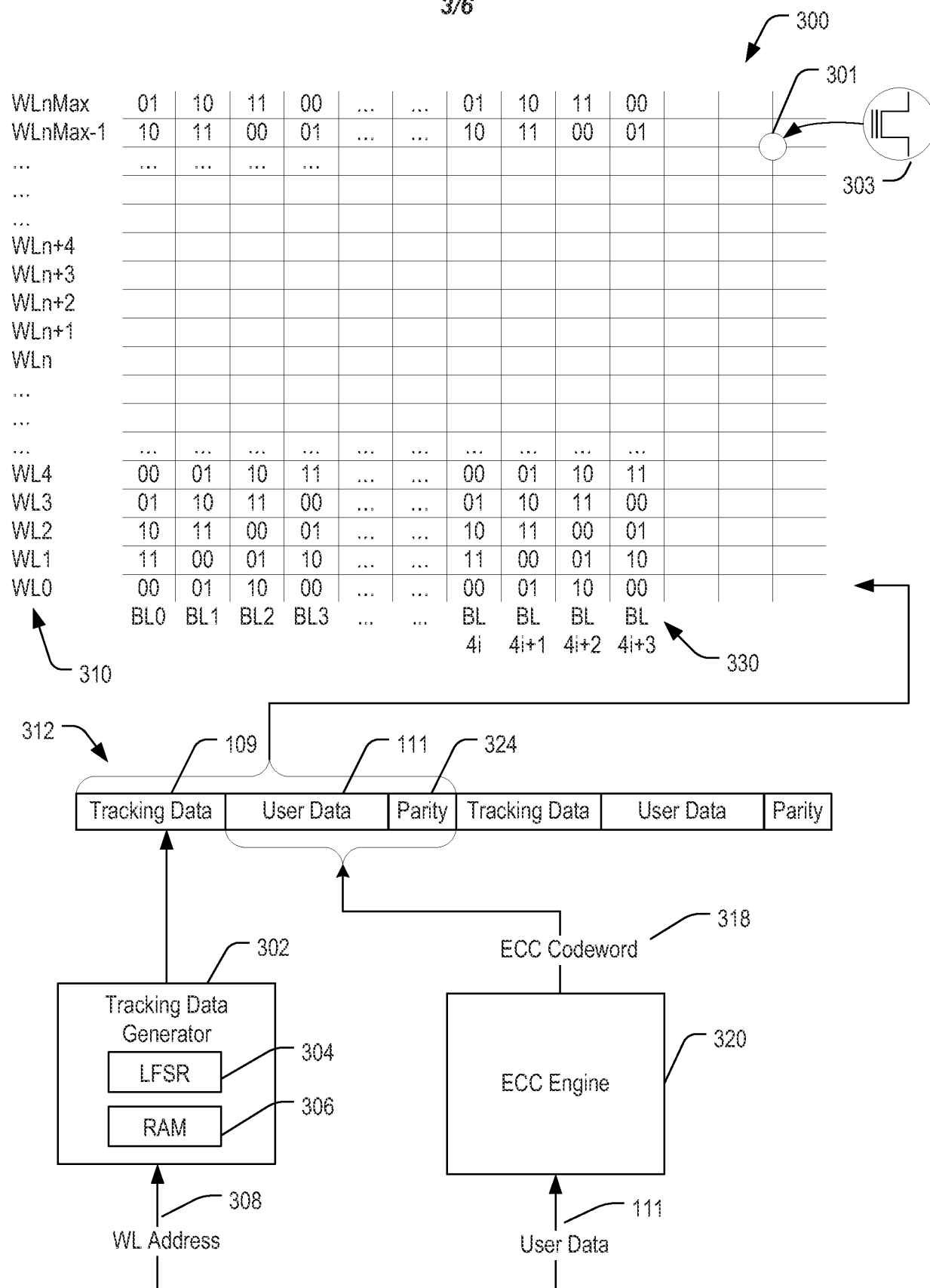
1/6

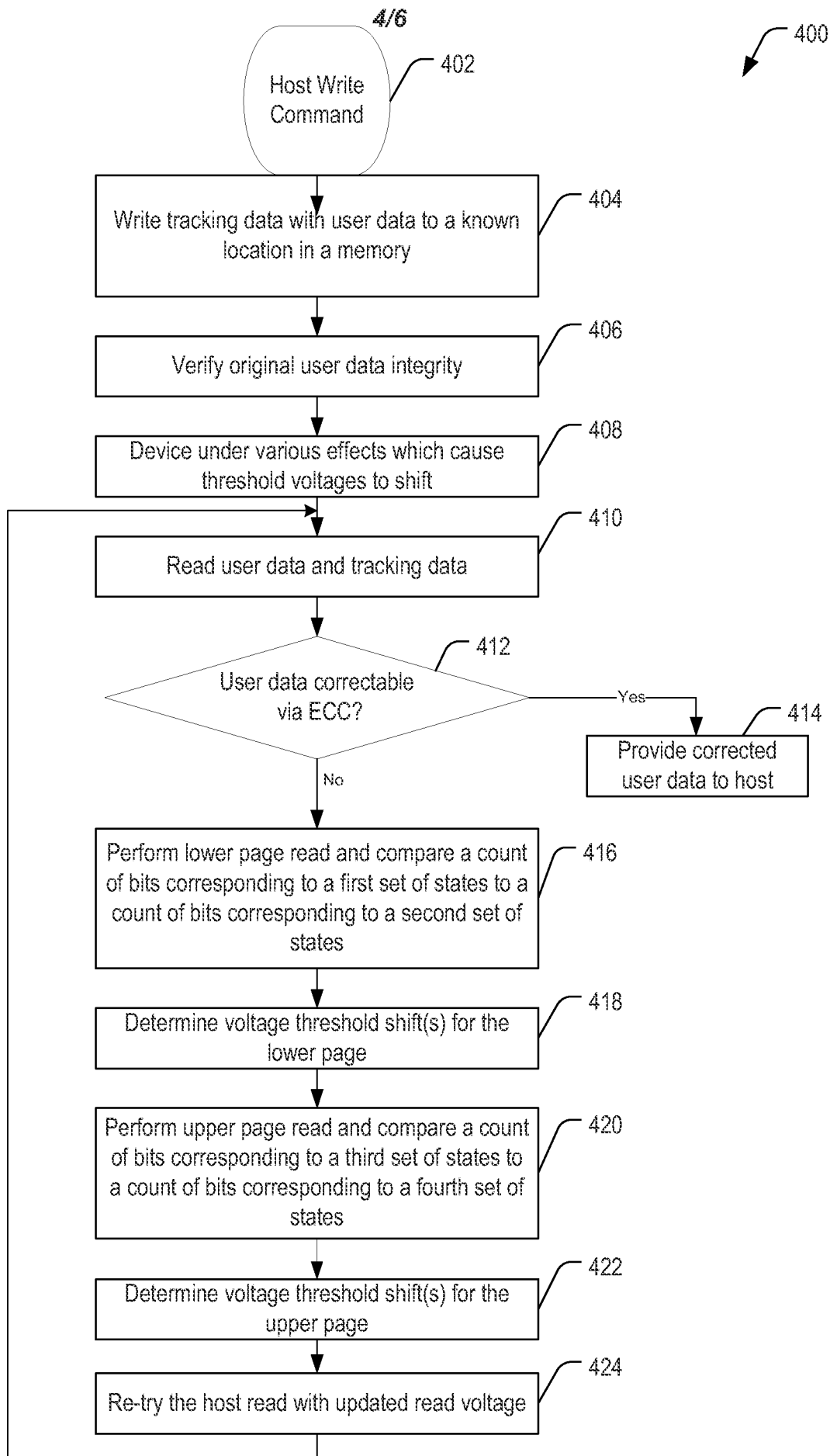
**FIG. 1**

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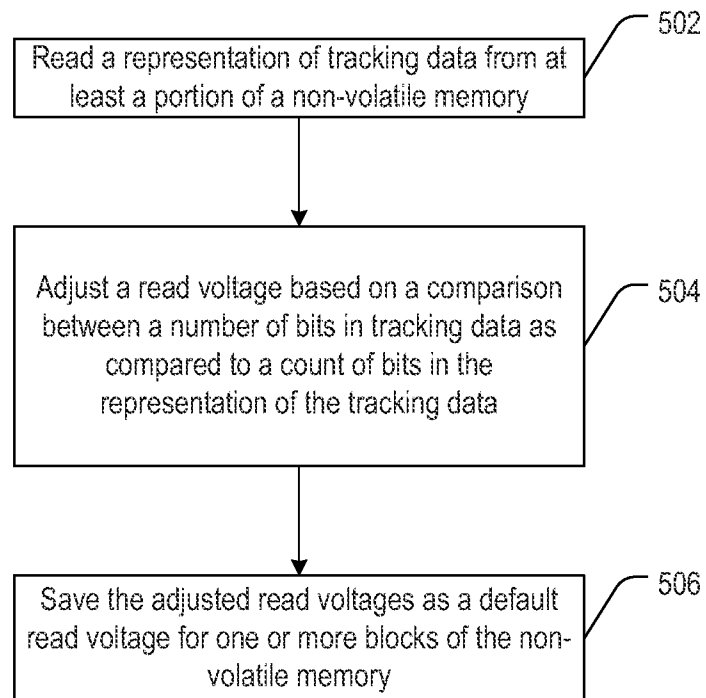
**FIG. 2**

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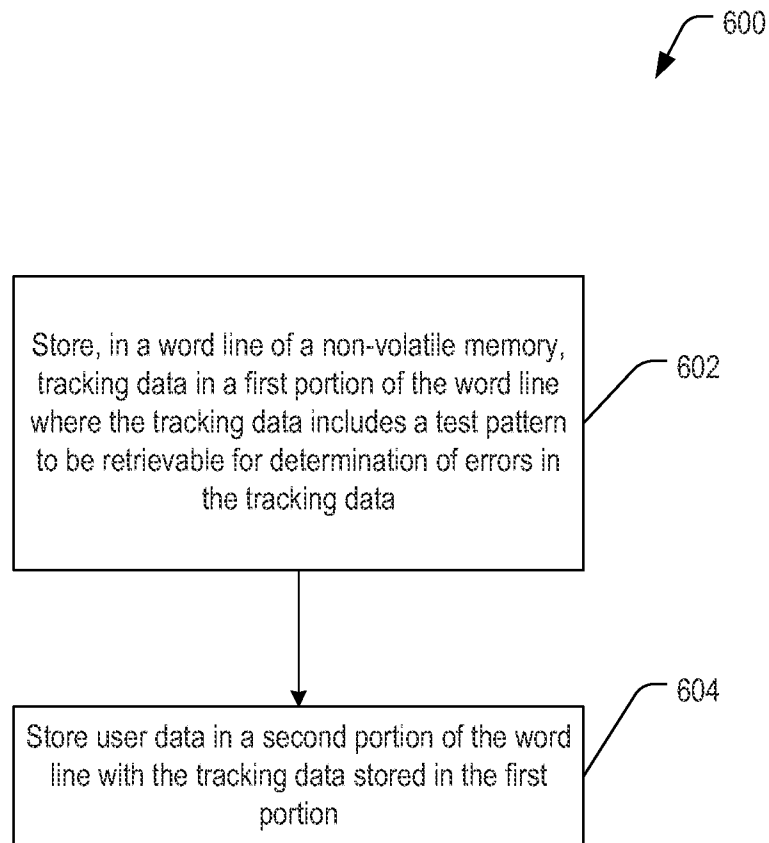
**FIG. 3**

**FIG. 4**

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**FIG. 5**

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**FIG. 6**

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2013/071272

A. CLASSIFICATION OF SUBJECT MATTER
INV. G11C29/02
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X A	US 2012/188820 A1 (NEUMEYER FREDERICK C [US] ET AL) 26 July 2012 (2012-07-26) paragraph [0005] paragraph [0024] - paragraph [0027]; figure 2a paragraph [0030] - paragraph [0042]; figures 3,4 -----	1-3, 17-19 4



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

10 March 2014

Date of mailing of the international search report

27/05/2014

Name and mailing address of the ISA/

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Authorized officer

Wolff, Norbert

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2013/071272

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:
2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:
3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:
4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

1-4, 17-19

Remark on Protest

- ☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
- ☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
- ☐ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1-4, 17-19

Configuration of a tracking pattern subject to data
comparison for adjustment of read reference voltages

2. claims: 5, 6, 11-16, 20, 21

Storage location of a tracking pattern subject to data
comparison for adjustment of read reference voltages

3. claims: 7-10, 22-25

When to perform a read voltage adjustment and different uses
of error correction code therefor

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/US2013/071272

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2012188820	A1	26-07-2012	NONE
