United States Patent [19]

Frankland et al.

[11] **3,829,834**

[45] **Aug. 13, 1974**

[54] **ELECTRICAL COMBINATION LOCK APPARATUS**

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[22] Filed: **Sept. 10, 1973**

[21] Appl. No.: **395,973**

[52] **U.S. Cl.** ..... **340/149 R,** 340/164 R

[51] **Int. Cl.** **H04q 9/00**

[58] **Field of Search** .... 340/149 R, 149 A, 147 MD, 340/164 R

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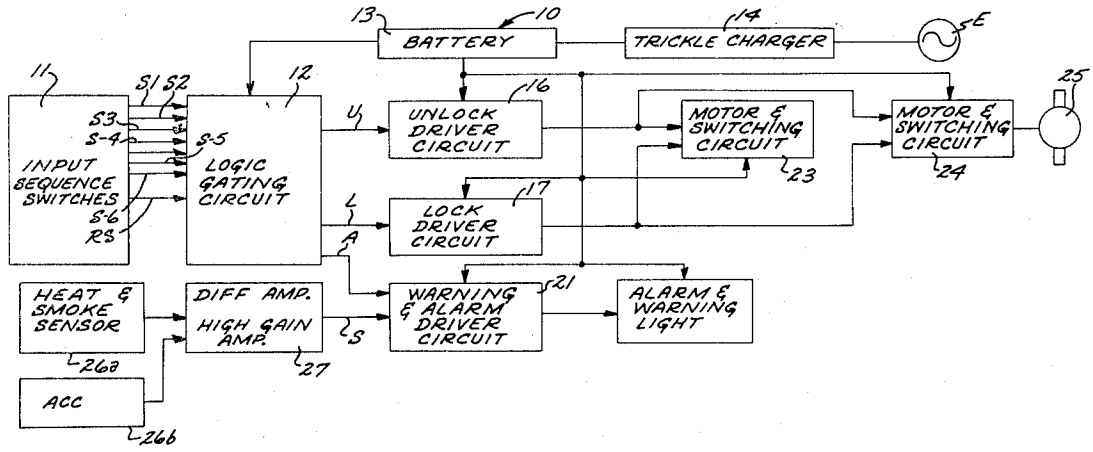
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[57] **ABSTRACT**

An electrical combination lock including a plurality of switches, connected in parallel to ground across a capacitor, for respectively producing when depressed a ground signal to corresponding first terminals of NAND gate latches. The NAND gate latches are connected in cascade to a reset signal switch at the second input terminals thereof whereby each NAND gate is switched to one state upon the depression of the reset switch and then to the other state upon depression of the corresponding combination switches. The same cascade connection of the latches will latch the latches in their switched states if the switch depression sequence follows the connection sequence and any other switch sequence will only register a change in state of one of the latch outputs concurrent with the depression of the switch while the second output will remain in its original state. Thus any switching sequence can be obtained, which, if followed, will latch all of the latches in the second state. This change in state of all of the latches is collected at a combination NAND gate, which, when receiving all signals of a particular state, activates a lock drive motor in a direction determined by the position thereof, either to open or close a lock. All other permutations of latch state, except one, are collected at other NAND gates to activate an alarm. The remaining permutation is reserved to reset the lock if a wrong sequence is depressed by error. The respective switches are connected to ground across an R-C circuit such that the depression thereof must occur within a predetermined interval. Also the power for the circuits is supplied by a battery continuously charged by a battery charger such that the combination lock is independent of an external power supply.

10 Claims, 5 Drawing Figures



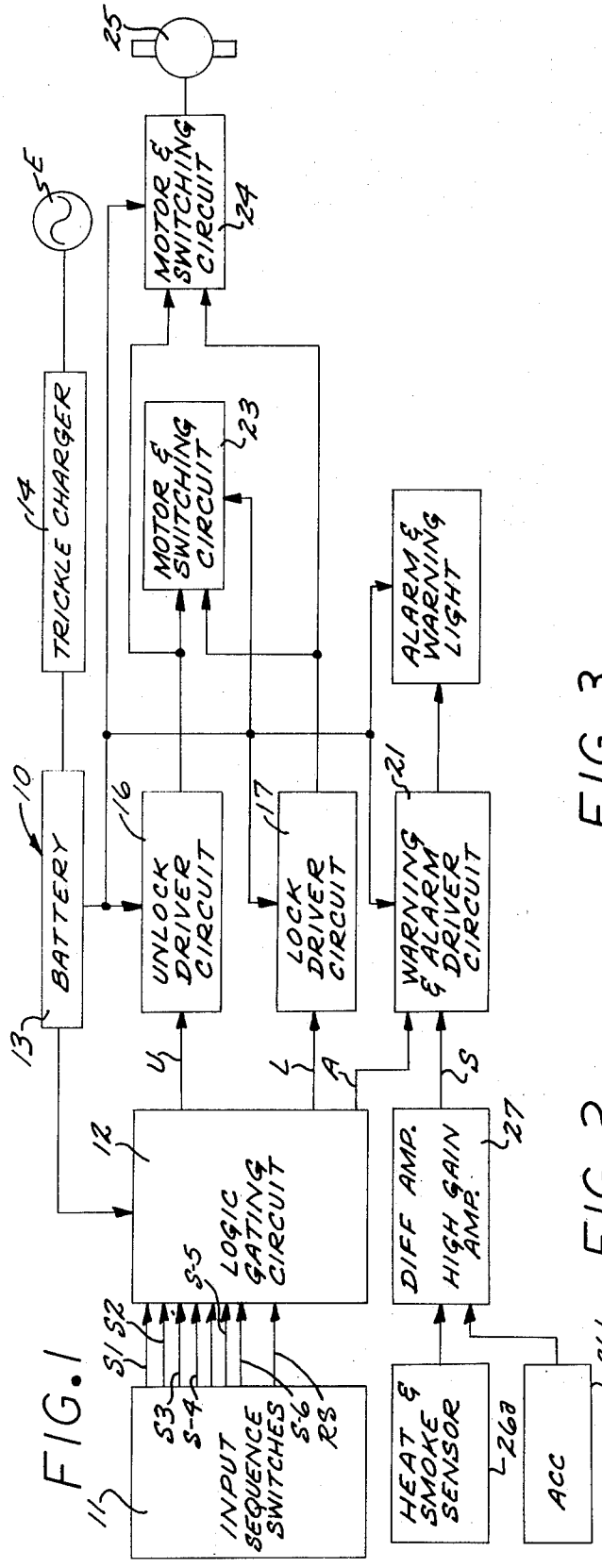


FIG. 1

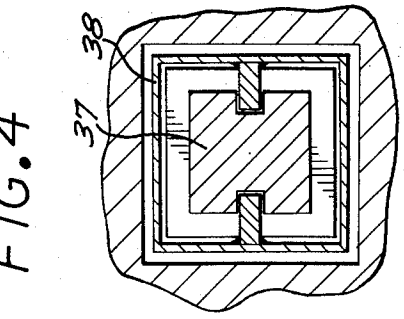


FIG. 4

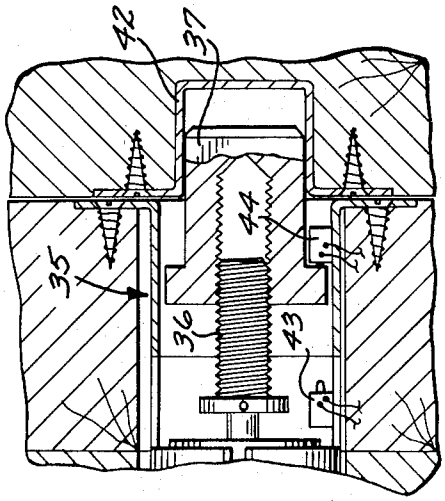


FIG. 3

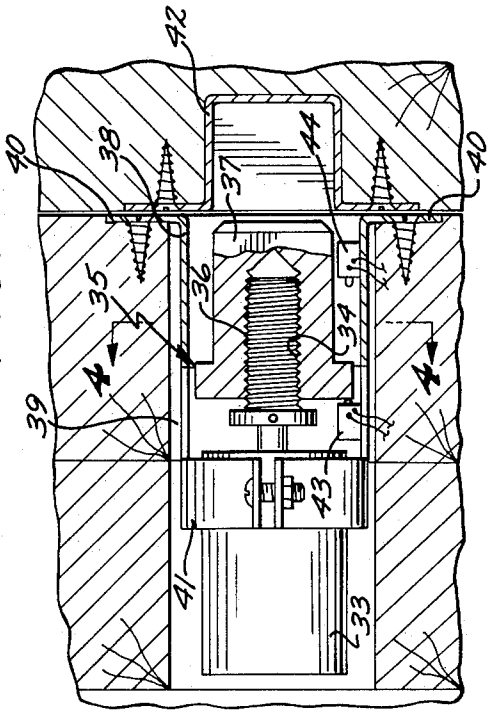


FIG. 2

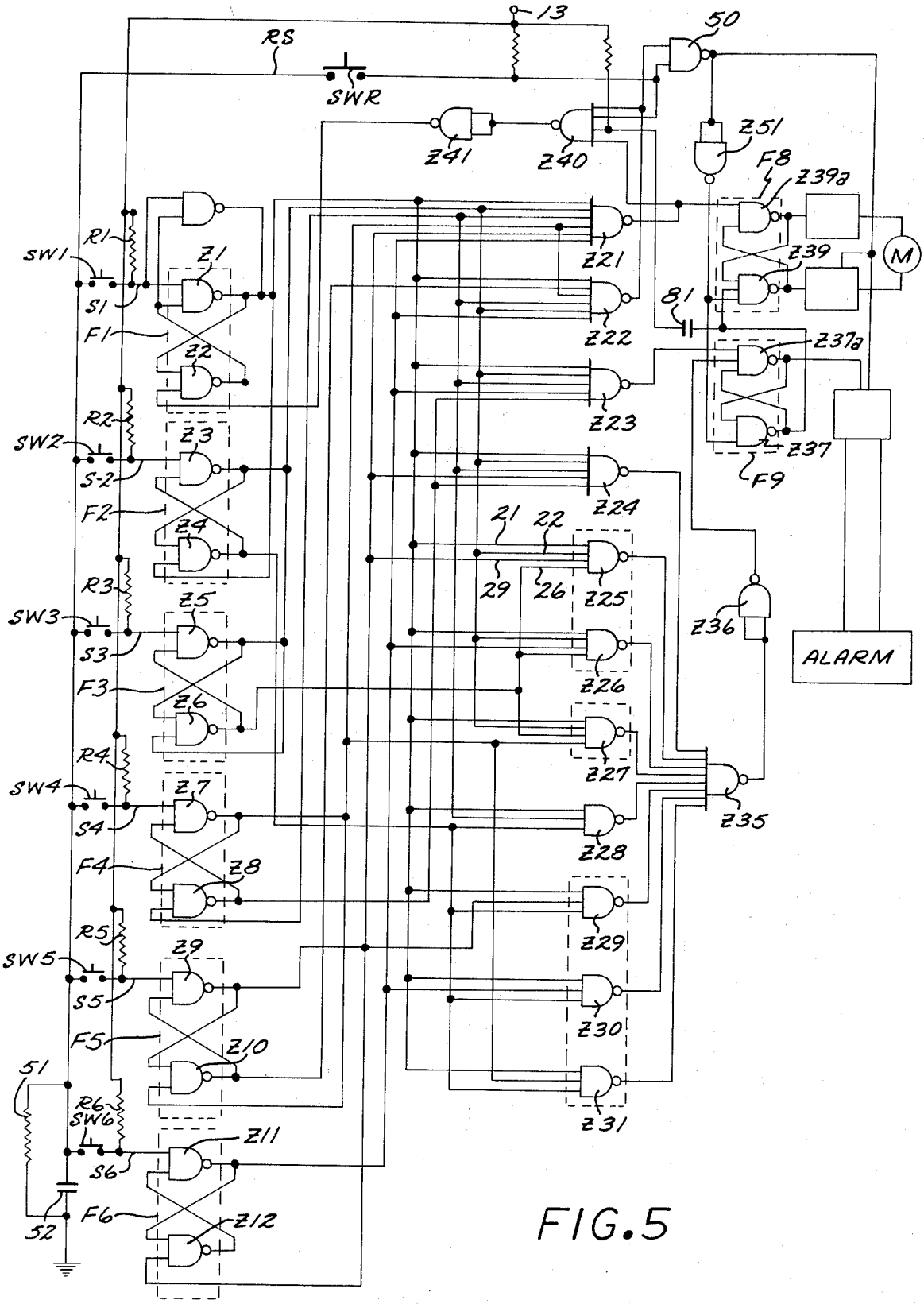

13
50
RS
SWR
Z41
Z40
Z51
F8
Z39a
Z39
M
R1
SW1
S1
Z1
F1
Z2
Z21
Z22
81
Z37a
R2
SW2
S2
Z3
F2
Z4
Z23
Z24
Z37
F9
21
22
29
26
Z25
R3
SW3
S3
Z5
F3
Z6
Z26
Z36
ALARM
R4
SW4
S4
Z7
F4
Z8
Z27
Z28
Z35
R5
SW5
S5
Z9
F5
Z10
Z29
Z30
51
R6
SW6
S6
Z11
52
F6
Z12
Z31

FIG. 5

ELECTRICAL COMBINATION LOCK APPARATUS

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to electrical locking apparatus, and more particularly, to electrical locks rendered operative by a predetermined, logical combination of switching signals.

2. Description of the Prior Art

Electrical locks, and particularly electronic combination locks, have acquired extensive use in commercial applications, such as securing access to banks or various other commercial buildings, as well as for securing access to residential buildings and the like. Such combination locks characteristically have a finite number of switching combinations and therefore can be tampered with, where, on a simple trial and error basis, a proper switching sequence can be learned. Furthermore, such combination locks are also typically tied to an outside power source and in the event of power source interruption or failure the doorway including such locks is either rendered open, or totally closed. The heretofore proposed combination locks of this type operate by responding to a predetermined sequence of switching signals, being typically nonresponsive to all other permutations thereof. Thus the prior art locks of this type did not provide an indication which would respond to the permutations in the switching sequence to activate an alarm. Furthermore due to the lack of an independent power supply such prior art locks could be easily circumvented by an interruption of power, thereby increasing the chances of unauthorized entry. As a means to overcome this latter inadequacy it has been heretofore practiced to directly connect an alarm system responsive to a power loss to the lock, such that even accidental power losses would trigger an alarm.

SUMMARY OF THE INVENTION

Accordingly, it is the general purpose and object of the present invention to provide an electrical combination lock activated to open upon receiving a predetermined sequence of switching signals and which is also responsive to any other sequence for triggering an alarm. Another object of the invention is to provide in such electrical combination lock a power storage device which can render the lock operative independently of any outside power supply. Yet another object of the invention is to provide force or impact responsive elements in the combination lock which would also trigger the alarm upon sensing any forcible entry therethrough. Further objects of the invention are to provide time increments in which the switching sequence has to be accomplished such that only personnel familiar with the sequence and generally facile with the operation thereof can gain access.

Briefly, these other objects are accomplished within the present invention by providing a storage battery connected to a battery charger, where the battery provides the power for a plurality of push-to-make switches connected in parallel to ground on one side, each switch being respectively connected on the other side to a first tier of complementary NAND gate pairs, each pair being connected to form a bistable switch conditoned to switch over from one stable state to the other by the preceding bistable NAND gate pair and by

the corresponding switch. Specifically the respective NAND gate pairs are connected in a manner similar to a bistable latch where the respective outputs of the individual NAND gates of each pair are connected to the inputs of the other complementary NAND gates. In each such complementary pair of NAND gates the other input signal to one of the gates is connected to the corresponding switch while the second NAND gate receives at the other input either a reset signal or the output signal of the preceding NAND gate pair. The output signals of the bistable NAND gate pairs are collected at a plurality of second tier NAND gates, where selected ones thereof are either rendered operative by the combination of the bistable NAND gate pair output signals or alternatively selected other NAND gates of the second tier are rendered operative by any permutation of the NAND gate pair signals. The output of the combination NAND gates is then operatively connected to a motor which operates a lock driver for either opening or closing the lock, while the collected output of the permutation NAND gates is operatively connected to an alarm system for activating an alarm. Also included in the NAND gate logic is a reset switch, which at any time in the sequence of switch depression can reset all of the NAND gates to their original state in order to initiate a new switching sequence. A further input to the alarm system is a force or accelerometer sensing device and a heat sensitive device, both being logically switched to be operative only when the lock is in a closed position, for activating the alarm system upon sensing any attempts of forcible entry.

DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of an electrical combination lock constructed according to the present invention;

FIG. 2 is a partial cross sectional view of a lock drive mechanism constructed according to the present invention;

FIG. 3 is a sectional view of the lock drive mechanism of FIG. 2 extended in its normally locked position;

FIG. 4 is a front sectional view of a locking bolt according to the present invention; and

FIG. 5 is a circuit schematic embodying the logical switching arrangement of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

As shown in FIG. 1 an electrical combination lock, generally designated **10**, comprises a plurality of push-to-make switches SW1–SW6 arranged in a switch box **11**, illustrated as a plurality of six switching outputs S1–S6 connected to a logic gating circuit **12**. Also included in switch box **11** is a reset switch SWR producing a reset signal RS_1 to circuit **12**. Connected to the switch box **11** is the output of the battery **13** which also provides power to the gating circuit **12**. Battery **13** is maintained charged by a conventional trickle charger **14** powered from a power source E, such as a conventional home power outlet. Accordingly, any abnormal interruptions in the power outlet E only interrupt the charging outputs from the charger **14** and the switching circuit **11** and logic gating circuit **12** are still operable. The logic gating circuit **12**, according to means further described hereinbelow, provides an unlock signal U to an unlock driver circuit **16**, a lock signal L to a lock

driver circuit 17 and an alarm signal A to a warning and alarm driver circuit 21.

Driver circuits 16 and 17 and the warning and alarm driver circuit 21 are further connected to receive the output of battery 13 such output supplying the power thereto according to an arrangement further described hereinbelow. The respective drivers 16 and 17 also provide outputs across corresponding switching circuits 23 and 24 to drive motor 25. Connected in parallel with switch box 11 and circuit 12 is a heat and smoke sensor 26*a* and a conventional accelerometer 26*b* (in combination with various pressure sensors, temperature sensors, and/or any or all of the above). The output signals of these sensors are collected to be amplified by an amplifier 27 to provide a second input S to the warning and alarm driver circuit 21. The warning and alarm driver circuit 21 generates an output signal to enable an alarm and warning light 22 which is also powered by battery 13.

As shown in FIGS. 2 and 3, a lock assembly 35 includes a motor 33 having a threaded output shaft 36 threadably engaging a threaded bore 34 formed in a door bolt 37. The bolt 37 is square in cross section to be freely received in a square in cross section carriage 38 which is further received in a horizontal cavity 39 formed in the free edge of the door. The carriage 38 is formed at the free edge of the door with outwardly turned flanges 40 for attachment to the door, and at its opposite end includes a clamping ring 41 for mounting the motor 33 therefrom. Thus the rotation of the motor will either project or retract the bolt 37 along threaded shaft 36, the direction being determined by a pair of limit switches 43 and 44 mounted in the carriage to be depressed by the bolt at the opposite extremes of its travel. A bolt receiver 42 is mounted in a cavity formed in a doorjamb in alignment with the bolt 37 to receive such bolt and lock the door to such doorjamb. In the alternative the lock assembly 35 may be received in the doorjamb while the bolt receiver 42 is mounted in the opposing edge of the door.

As shown in FIG. 5 switch box 11 includes a plurality of normally open push button switches SW1–SW6 all connected in parallel to ground at one of the terminals thereof across a parallel RC circuit comprising a resistor 51 connected across a capacitor 52.

The other terminals of switches SW1–SW6 each connect to one end of corresponding dropping resistors R1–R6 and the other ends of the resistors R1–R6 are connected in common to battery 13. Thus each switch SW1–SW6 generates a corresponding output signal S1–S6, the voltage thereof being determined by the position of the switch. The respective signals S1–S6 are connected in parallel to the gating circuit 12 and terminate within circuit 12 at corresponding bistable latch or switch circuits F1–F6.

Since the respective switch circuits F1–F6 are substantially identical in structure and in function, the subsequent description of the circuits is made with reference to circuits F1 and F2 only. The bistable switch circuit F1 comprises a pair of NAND gates Z1 and Z2 each receiving two inputs and generating one output according to the conventional Boolean equivalent of a logical AND x NOT. Thus NAND gate Z1, and all other NAND gates referred to hereinbelow, will operate according to the following truth algorithm:

Input		Output
1 = 0, 1, 0 2 = 0, 0, 1	=	1

and

Input		Output
1 = 1 2 = 1	=	0

where the respective logical 0 and 1 correspond to either an absence or presence of a voltage above a predetermined level at that terminal. Accordingly, a minimum of two inputs is necessary to any one of the NAND gates in order that the NAND gate function according to the logical function. Specifically, in the circuit F1, the upper NAND gate Z1 receives at one input thereof the switching signal S1 which is either a logical 0 or 1 according to the state of the switch SW1. The second input to the NAND gate Z1 is the output of NAND gate Z2. Thus the output state of gate Z1 is dependent on the state of switch SW1 and gate Z2.

In a similar manner NAND gate Z2 is connected to receive the output of gate Z1, the gate pair forming a conventional tail-to-mouth configuration to a toggle circuit or a latch. In this configuration the circuit F1 is indeterminate and will form one stable state if the input to gate Z2 (or the output of gate Z1) is a 0. Accordingly a second input to gate Z2 is provided in order to resolve this indeterminancy. This signal is provided by a reset circuit RS. Thus circuit F1 takes the form of a latch having a pair of output signals in inverse relationship with a pair of input signals and will switch over between output states upon a complementary reversal of input signals. The successive switch circuits F2–F6 are preset in a similar manner by connecting in cascade the output of the odd numbered gate of the preceding switch circuit to the input of the even numbered gate in the next switch circuit. Accordingly a single depression of a reset switch SWR in the reset circuit RS, producing a 0 to gate Z2, will reset all of the first tier switching circuits.

In a similar fashion circuit F2 receives at the upper NAND gate Z3 the signal S2 from the switch SW2 while receiving at the lower NAND gate Z4 the output of gate Z1 from circuit F1. Thus the switching of circuit F1 produces a 1 input to gate Z4 enabling it to switch over to a 0 at the output thereof when switch SW3 is depressed and thus latch in this state when switch SW3 is opened.

The remaining latch circuits F3–F6 are connected in a similar fashion receiving at the respective odd numbered gates Z5–Z11 corresponding switching signals S3–S6 and being connected at the even numbered gates Z6–Z12 to the preceding switch circuit. Thus the respective switch circuits F1–F6 each will produce two outputs, one output per NAND gate, where the state of the latch circuit is determined by the upper or odd numbered NAND gate and the sequence is determined by the even numbered gate within each switch circuit.

The selected outputs of circuits F1–F6 are collected at a second tier of NAND gates where a NAND gate Z21 receives the outputs of gates Z1, Z3, Z5, Z7, Z9 and Z11 and a NAND gate Z22 receives the output of

gates Z1, Z3, Z5, Z7, Z10 and Z11. Gate Z21 will continue to produce a 1 until all of the switches SW1–SW6 are depressed at which time it will switch over to produce a 0. The output of gate Z21 is connected both to the input of gate Z40 in reset circuit RS and to the input of a gate Z39(a) in a motor actuating bistable circuit F8. Gate Z39(a) is connected in complement with a gate Z39. Gate Z40 further receives the output signal from gate Z22 which, as previously stated, combines to form a 0 if the last switch depression made occurs at switch SW5. In a similar manner a NAND gate Z23 collects the outputs of gates Z1, Z3, Z5, Z11 and Z8, producing a 1 at the output when gate Z8 is at 0. Also included in the second tier of gates is a NAND gate Z24 which collects the outputs of gates Z1, Z8, Z9, Z5 and Z3 and NAND gates Z25 and Z27 each collecting in parallel the outputs of gates Z6, Z1, Z3 and respectively the outputs of gates Z9, Z11 and Z7. Additional gates Z28–Z31 each collect in parallel the outputs from gates Z1 and Z4 while respectively collecting singly outputs from gates Z5, Z9, Z11 and Z7. Gates Z23–Z31 are all collected at gate Z37(a), gates Z24–Z31 being first combined in a NAND gate Z35 and inverted through gate Z36 to reduce the number of input leads thereto. Thus gate Z37(a) will produce a 1 if any of the gates Z23–Z31 produce a 0. Since gates Z23–Z31 respectively receive at least one of the even numbered gates Z4, Z6, Z8 and Z10 in various combinations with the odd numbered gates Z1, Z3, Z5, Z7, Z9, and Z11 all permutations of switching sequence are covered. In this context it is necessary to note that following reset the output pairs of circuits F1–F6 are complementary accordingly the connection of the even numbered gates to gates Z23–Z31 must always include at least one 0 rendering the output of gate Z37(a) a 1. Gate Z37(a) and gate Z37 are connected in complement in an alarm circuit F9, where the input to gate Z37 further includes the inverted output of a reset NAND gate Z50. Gate Z50, inverted through gate Z51, combines the reset signal RS from switch SWR and the output of gate Z22 where gate Z22 changes to a 1 state upon completion of a switching sequence.

The operation of the present invention will now be set forth with particular reference to FIGS. 1 and 5. For purposes of illustration an abbreviated switching sequence will be referred to, initiated by the depressing of the reset switch SWR followed by switches SW1 and SW2. Switch SWR, through the NAND gate Z40, is converted to a logical 1 which is then inverted to a 0 through the NAND gate Z41. The NAND gate Z41 is receiving the output of gate Z40 at both terminals thereof, being thus connected to function as an inverter. Accordingly since a 0 input at any input terminal of gate Z40 will produce a 1 output to gate Z41, the corresponding state of the output signal from gate Z41 is a 0. Thus at least one input to gate Z2 is a 0 and the output thereof is accordingly a logical 1. Gate Z1, prior to the depression of switch SW1, is therefore receiving two 1 inputs satisfying the above algorithm to produce a 0 output. Upon depression of switch SW1 the output of gate Z1 changes state to produce a 1 which is also connected to the input of NAND gate z21. Since the gate Z1 output state depends on the output state of gate Z2, and conversely, the gate pair is initially indeterminant. This indeterminancy is resolved by providing a 0 to gate Z2 by depressing the reset switch SWR. The gate pair is thus set to produce a 0 from gate Z1 and a 1 from gate Z2. In a similar fashion the 0 output of gate Z1 resolves the indeterminancy in circuit F2 comprising gates Z3 and Z4. Accordingly the depression of switch SW1 provides a 1 on the output of gate Z1 and on the connected input of gate Z4. Gate Z4 is therefore ready to change state in response to the depression of switch SW2 which produces a 1 output from gate Z3. Upon depression of switch SW2 at least one of the inputs to gate Z3 is a 0 and the output thereof changes to a 1 state. Thus both inputs to gate Z4 are 1 resulting in a 0 output which insures at least one 0 input to gate Z3 and the complementary gate pair switches over to the other stable state. In a similar fashion the successive complementary NAND gate pairs are each conditioned to change state in an order according to the respective connections thereof. Although shown in this embodiment as a predetermined switching sequence of single switch depressions the number of switching combinations can be increased by interposing a counter of any length on the output of any one or more of the circuits F1–F6, connected in a similar manner, to produce any desired combination of repetitive switch depressions.

Thus as switch SW1 is depressed, the state of gate Z1 changes to a 1 and gate Z21 receives at least one 1 input. Gate Z21 is connected to receive all of the first gate outputs of the respective switching gate pairs and will produce a 0 when switch SW2 is depressed if limited to the state of gates Z1 and Z3. The output of gate Z21 is connected both to the input of gate Z40 and to the input of gate Z39(a) which forms the upper complementary NAND gate of a NAND gate pair connected to activate across the limit switches 43 and 44 the motor 33. Simultaneously gate Z28 is connected to receive the outputs of gates Z1 and Z4 where the output of gate Z4 will be a 1 following the depression of switches SW1 and SW2. Gate Z28 will therefore produce a 0 output until correct switching is completed at which time a 1 will be produced at the output thereof. Similarly gates Z29, Z30 and Z31 act in parallel with gate Z28 if limited to the inputs corresponding to the switches SW1 and SW2. As embodied in FIG. 5, gates Z28, Z29, Z30 and Z31 further each receive the corresponding outputs of gates Z5, Z9, Z11 and Z7. Thus as all of switches corresponding to these gates are depressed gates Z28–Z31 all switch over to produce a 1. In a similar fashion, gates Z25–Z27 are commonly responsive to the outputs of gates Z1, Z2 and Z6 being further individually responsive to corresponding gates Z9, Z11 and Z7. Thus gates Z28–Z31 effectively check the outputs of gates Z5, Z9, Z11 and Z7 following the switch over of gate Z1 while gates Z25–Z27 check the switch condition of gates Z9, Z11 and Z7 following the switching sequence of switches SW1 and SW2. Gates Z22–Z24 provide the switching sequence checks such that all possible permutations will produce at least one 1 condition at the output thereof. Gates Z24–Z31 are collected at the input of NAND gate Z35 which is inverted through NAND gate Z36 to register a 0 for any permutation sequence. The output of gates Z36 and Z23 are both received at the input of gate Z37(a) which is the upper gate of a complementary gate pair. The output of gate Z37(a) is directly connected to alarm driver circuit Z. The lower NAND gate Z37 of the complementary pair is connected to receive both the output reset signal and the output of Z37(a) to operate in a manner similar to gate Z2 for providing a bistable gate circuit conditioned to switch over to an

alarm condition by gate Z51. Accordingly, once conditioned or reset by gate Z51 any zero input to gate Z37(a) will generate a 1 at the output thereof enabling an alarm.

Some of the many advantages of the present invention can be listed as follows:

1. It cannot be tampered with without setting off an alarm;
2. It cannot be picked (mechanically or electronically);
3. The combination can be changed as often as desired;
4. It has a warning time prior to energizing an alarm for purpose of resetting circuit before alarm goes off;
5. It is adaptable to any type of enclosure such as a building, an auto, a truck, etc., that requires a secure locking system;
6. It is compatable with any sensing device;
7. The bolt cannot be forced open;
8. It requires very little power;
9. The use of the motor eliminates solenoids which cause magnetic disturbance and consume large amounts of power;
10. Keys are no longer required; and
11. The external connector used for a failure mode cannot by-pass the combination.

It is understood that many modifications may be made to the subject invention, in addition to those described above, which fall within the true scope and spirit of the subject invention. Therefore, the scope of the subject invention is intended to be limited only by the recitation of the foregoing claims.

I claim:

1. An electrical combination lock comprising, in combination:

lock means adapted to be mounted in a doorway for effecting locking and unlocking thereof upon receiving a first electrical signal;

switching means disposed for sequential manual actuation for producing a plurality of consecutively actuated parallel switching signals according to the manual actuation thereof;

first electronic latch means connected to receive said switching signals for latching to a first state to produce a predetermined combination of maintained output signals at corresponding one output terminals thereof upon receiving a predetermined sequence of said switching signals and for producing temporary signals concurrent with the manual actuation of said switching means at corresponding other output terminals thereof upon receiving corresponding other sequences of said switching signals;

combination means connected to receive corresponding one output terminals of said first latching means for producing said first electrical signal upon receiving said maintained output signals thereon;

permutation means connected to receive corresponding one and other output terminals of said first latching means output signals for producing a reset signal upon receiving a one selected combination of said temporary signals and selected ones of said maintained signals and for producing a first alarm indicative signal upon receiving any other combination of said temporary and maintained signals;

reset means connected to receive said reset signal for producing a reset output signal latching said latch means to a second state;

second latch means connected to receive said first alarm indicative signal and said reset signal for latching to an alarm state upon the first receipt of said first alarm indicative signal and for unlatching from said alarm state upon receiving said reset signal; and

alarm generating means connected to said second latch means for generating an alarm operating signal upon the latching of said second latch means in said alarm state.

2. An electrical combination lock according to claim **1**, further comprising:

a reset switch connected in parallel with said reset means for alternatively producing said reset signal upon the manual actuation thereof.

3. An electrical combination lock according to claim **2**, wherein:

said first latch means including first latching circuits each comprising paired first NAND gates connected to receive at one input thereof the output of the other corresponding first NAND gate of each pair and connected to receive at the other inputs of the one first NAND gate thereof respective ones of said switching signals, being connected at the other inputs of the other first NAND gates to selected other output terminals of said first latching circuits, the respective connections between said latching circuits corresponding to said predetermined sequence of said switching signals.

4. An electrical combination lock according to claim **3**, wherein:

said combination means including a second NAND gate disposed to receive the output signal of the one first NAND gates of said first NAND gate pairs for producing a change in the output signal thereof when all said one NAND gate output signals are at one selected state.

5. An electrical combination lock according to claim **4**, wherein:

said permutations means including a plurality of third NAND gates selectively connected to receive predetermined combinations of said one and other first NAND gate output signals.

6. An electrical combination lock according to claim **5**, wherein:

said second latch means including fourth latching circuits each comprising paired fourth NAND gates connected to receive at one input thereof the output of the other corresponding fourth NAND gate of each pair and connected to receive at the other inputs of the one fourth NAND gate thereof selected ones of said third NAND gates output signals.

7. An electrical combination lock according to claim **1** wherein:

said lock means including an electrical motor rendered operative upon receipt of said first electrical signal, a bolt disposed laterally in said doorway and connected to be actuated in response to said motor, and limit switches disposed in said doorway and aligned to be selectively switched when said bolt is at the extremes of the travel thereof produc-

ing signals for controlling the rotation of the motor in a direction opposite to the position of said bolt.

8. An electrical combination lock according to claim **1**, further comprising:

environment-responsive means disposed in said doorway for producing a second alarm indicative signal to said alarm means upon sensing change in the environment.

9. An electrical combination lock according to claim **1**, further including:

timing means connected to said switching means for rendering said switching means operative within a predetermined interval of time.

10. An electrical combination lock according to claim **1**, further including:

a storage battery connected to supply electrical power to said lock means, first electronic latch means, combination means, permutation means, second latch means and said alarm generating means; and

charging means adapted to receive an electrical signal for providing electrical power to said storage battery.

* * * * *