Oct. 27, 1959 T. M. STRONG 2,910,597

SWITCHING APPARATUS

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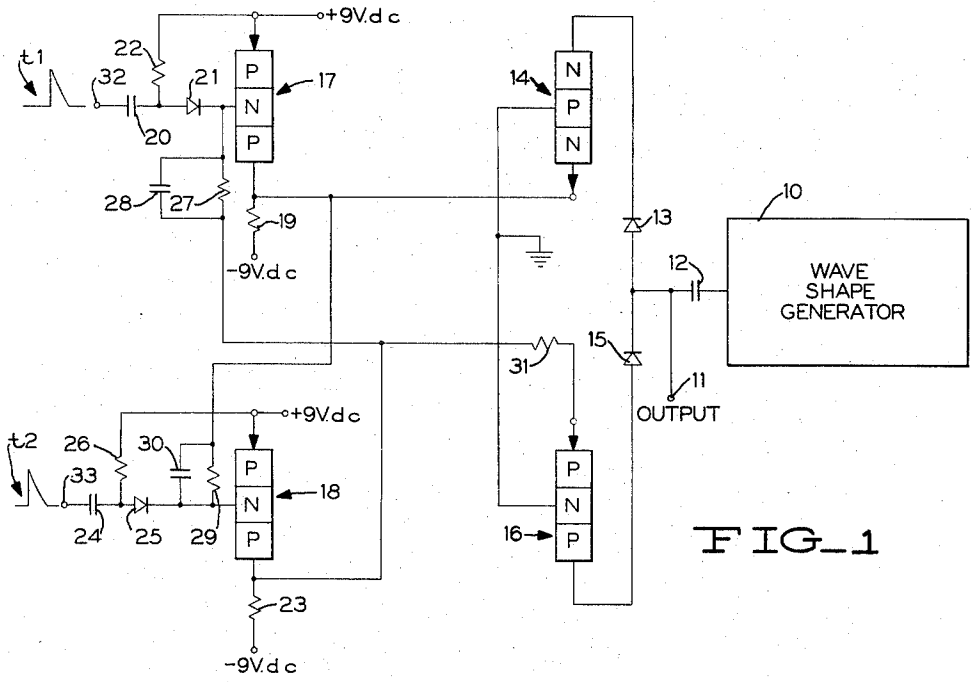


FIG_1

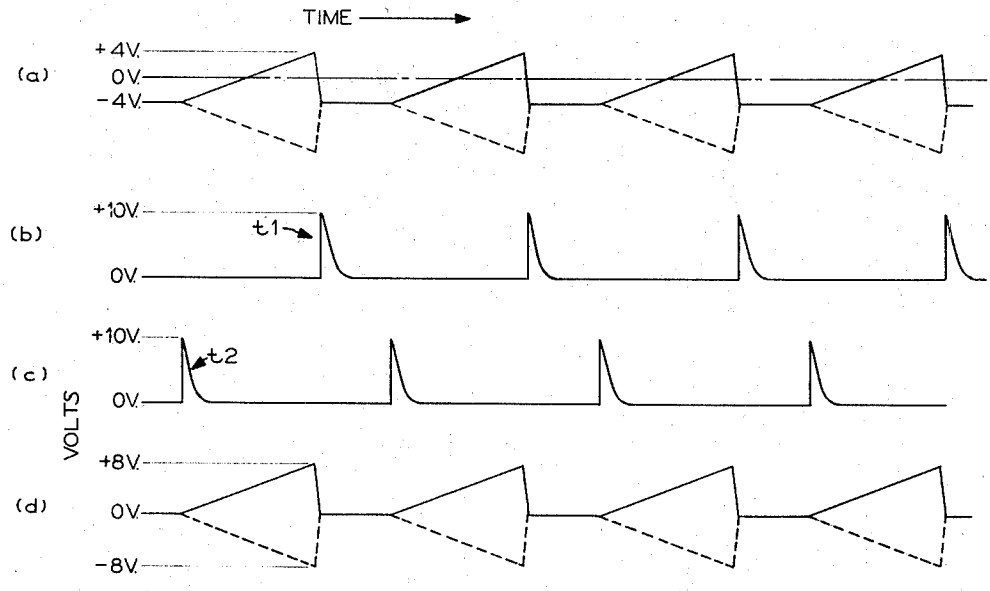


FIG_2

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SWITCHING APPARATUS

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4 Claims. (Cl. 307—88.5)

The present invention relates to signal translating apparatus, and particularly to an arrangement for controllably providing a bipolar clamping action to a signal line.

An object of this invention is to provide a new and improved signal translating apparatus.

Another object of the invention is to furnish a new and improved arrangement for selectively clamping a signal line to a fixed voltage.

Still another object of the present invention is to provide a circuit arrangement which affords a bipolar clamping action to a signal line.

A further object of the invention is to provide a new and improved switching arrangement which utilizes the unique properties of transistors for controlling a signal line.

Other objects of the invention will be pointed out in the following description and claims and illustrated in the accompanying drawings, which disclose, by way of examples, the principle of the invention and the best mode, which has been contemplated, of applying that principle.

In the drawings:

Fig. 1 is a schematic diagram of the present invention; and

Fig. 2 shows sample waveforms which may be produced at various points in the circuit shown in Fig. 1.

Briefly, the present invention utilizes a first diode having its plate connected to a signal line and a second diode having its cathode connected to said signal line. The cathode of the first diode is connected to a fixed voltage by means of a switch in the form of an NPN junction type transistor which is connected in the grounded base configuration. The plate of the second diode is connected to a fixed voltage by means of a switch in the form of a PNP junction type transistor which is connected in the grounded base configuration. A signal line is connected by means of a capacitor to waveshape generating apparatus. Clamping action is afforded by determining the conducting period of the NPN and PNP transistors. That is, when the two transistors are in conduction, they offer a low impedance path to the signal line through their respective diodes, thus placing the signal line at said fixed voltage. When they are not in conduction, they offer a high impedance path to the signal line, thus allowing the signal line to follow the output of the waveshape generator. By supplying input signals of opposite polarity to the two transistors, it is possible to have both diodes conduct. When the signals to the transistors are reversed in polarity, both devices are cut off and present an effective open circuit to the diodes connected to the signal line.

Referring now to Fig. 1 of the drawings, there is illustrated in block form a waveshape generator **10**. As shown at (*a*) in Fig. 2, the output from the waveshape generator may be in the form of a sawtooth voltage. This sawtooth voltage may be positive going, as shown in solid lines, or negative going, as shown in dotted lines. Insofar as the present invention is concerned, either positive or

negative sawtooth voltages may be used. It will be appreciated that the use of a sawtooth voltage is by way of illustration only. Waveshape generators for producing other types of waveforms may be utilized in the present invention.

The output voltage from the waveshape generator **10** is coupled to an output terminal **11** by way of a capacitor **12**. The voltage appearing at the output terminal is shown at (*d*) at Fig. 2. It will be seen that the voltage at the output terminal is clamped to ground, this clamping action being afforded by the circuitry now to be described. Terminal **11** is connected to the plate of a diode **13** whose cathode is connected to the collector electrode of an NPN junction type transistor which is provided with reference numeral **14**. In the drawings, the convention used to designate the collector electrode of a transistor is that it is always at the top of an NPN transistor and at the bottom of a PNP transistor. The base electrode of the transistor is always connected to the center block thereof and the emitter electrode is connected to one end of the transistor and is illustrated as an arrow. In the NPN transistor, the emitter electrode is always at the bottom of the block with the arrow pointing away from the block, and in a PNP transistor, the emitter electrode is at the top of the block with the arrow pointing toward the block.

Output terminal **11** is also connected to the cathode of a diode **15** whose plate is connected to the collector of a PNP junction type transistor provided with the reference numeral **16**. It will be seen that the base of each of the transistors **14** and **16** is connected to a fixed reference voltage which, in the present instance, is ground voltage. The emitter electrode of each of these transistors is controlled from a trigger circuit which will now be described.

The trigger shown in Fig. 1 which is intended to be illustrative only, comprises two PNP junction type transistors which are labeled with reference numerals **17** and **18**. Transistor **17** has its emitter electrode connected to a positive source of D.C. voltage and its collector connected by way of a resistor **19** to a negative source of D.C. voltage. The input signal applied to terminal **32** is connected to the base electrode of transistor **17** by way of capacitor **20** and diode **21**, there being a resistor **22** connecting a point intermediate the capacitor and diode with the afore-mentioned positive source of D.C. voltage. Transistor **18** has its emitter electrode connected to a positive source of D.C. voltage and its collector electrode connected through a resistor **23** to a negative source of D.C. voltage. The input pulse applied to terminal **33** is connected to the base electrode of transistor **18** by way of a capacitor **24** and a diode **25**. Intermediate the capacitor **24** and diode **25** there is provided a connection therefrom through a resistor **26** to the last-mentioned positive source of D.C. voltage. It will also be seen that the two transistors are cross-coupled in a rather conventional manner in that the collector electrode of transistor **18** is connected by way of a resistor **27**, having a capacitor **28** in parallel therewith, to the base electrode of transistor **17**. On the other hand, the collector electrode of transistor **17** is connected by way of a resistor **29**, having a capacitor **30** in parallel therewith, to the base of transistor **18**.

The operation of the trigger is such that one of the transistors will be normally conducting and the other normally cut off. For descriptive purposes, let it be assumed that when transistor **17** is in conduction, the trigger is considered to be in its Off condition, and when the transistor **18** is in conduction, the trigger is considered to be On. Starting with the trigger in the Off condition, transistor **17** will be in conduction and the voltage at the collector thereof will approach the emitter voltage. The voltage at the collector is applied through resistor **29** and capacitor **30** to the base of transistor **18**

and is sufficiently positive to keep transistor **18** in its cut off condition. On the other hand, the collector of transistor **18** will approach the negative D.C. voltage to which it is connected and aid in keeping transistor **17** in conduction by way of resistor **27** and capacitor **28**.

When it is desired to turn the trigger On, an input pulse *t1*, as shown at (*b*) in Fig. 2, is applied to terminal **32**. This pulse drives the base of transistor **17** further positive and cuts the transistor off. As this action occurs, the collector of transistor **17** drops toward the negative D.C. voltage and supplies a negative going voltage to the base of transistor **18**, thereby placing the transistor in conduction. As transistor **18** goes into conduction, a positive going voltage is supplied from the collector thereof to the base of transistor **17** to keep the last-mentioned transistor off.

To turn the trigger Off, an input pulse *t2*, as shown at (*c*) in Fig. 2, is applied to terminal **33**. This pulse drives the base of transistor **18** further positive and cuts the transistor off. As this action occurs, the collector of transistor **18** drops toward a negative D.C. voltage and supplies a negative going voltage to the base of transistor **17**, thereby placing the transistor in conduction. As transistor **17** goes into conduction, a positive going voltage is supplied from the collector thereof to the base of transistor **18** to keep the last-mentioned transistor off.

It will be appreciated that the output voltages from the collectors of transistors **17** and **18** are substantially square wave in nature and 180° out of phase. That is, as the output voltage from the collector of transistor **17** is going positive, the output voltage from the collector of transistor **18** will be going negative, and when the output voltage from the collector of transistor **17** is going negative, the output voltage from the collector of transistor **18** will be going positive. These alternate conditions occur as the transistor is switched On, Off, On, etc.

With the above-described trigger Off, the arrangement is such that the output voltage from the collector of transistor **17** will be relatively positive while the output voltage from the collector of transistor **18** will be relatively negative. Since the emitter of the NPN transistor, illustrated by reference numeral **14**, is connected to the collector of transistor **17**, transistor **14** will be kept off as long as the collector of transistor **17** is relatively positive. It will be appreciated that this is due to the fact that with the emitter of transistor **14** more positive than the base the transistor is reverse biased. Similarly, when the collector of transistor **18** is relatively negative, the emitter of PNP transistor **16**, which is connected to the collector of transistor **18** by way of resistor **31**, will also be relatively negative. Thus, the transistor **16** will be reverse biased since the base therefore is at ground. When it is desired to clamp the voltage at output terminal **11** to ground, the trigger is turned On by an input pulse *t1* and the output from the collectors of transistors **17** and **18** are respectively used to place transistors **14** and **16** in conduction. The arrangement is such that should terminal **11** attempt to go positive, there will be substantially a short circuit path through diode **13** and the collector and base of transistor **14** to ground. On the other hand, should terminal **11** try to go negative, current will be allowed to flow from ground through the base and collector of transistor **16** and through diode **15** to terminal **11**. When it is desired to unclamp the voltage at terminal **11**, the trigger is turned Off by the input pulse *t2* and the voltages at the collectors of transistors **17** and **18** are reversed. Under these circumstances, transistors **14** and **16** become reverse biased and provide a high impedance to flow of current through both of the diodes **13** and **15** from terminal **11**. Under these circumstances, terminal **11** will tend to follow the output from the waveshape generator **10**.

It will be noted that the diodes **13** and **14** prevent the collectors of transistors **14** and **16** from becoming improperly biased when the trigger is Off. For example, if the output of the waveshape generator causes point **11** to go positive the NPN transistor **14** will have a positive voltage applied to its collector and will be correctly biased to present a high impedance to current flow. However, this same positive voltage at point **11** causes the collector of the PNP transistor **16** to be biased so that it has a low impedance in spite of the fact that its emitter is reverse biased. The diode **15** is reverse biased, however, preventing a low impedance path from point **11** to ground through transistor **16**.

If the voltage at point **11** is negative during the time that the trigger is Off, diode **13** prevents the formation of a low impedance path to ground through transistor **14**.

It will be appreciated from the above-detailed description that the present invention is suitable for clamping waveforms, which are either positive going or negative going, to ground or some other suitable reference voltage. The means for performing the clamp switching operation is relatively simple and capable of operation from any device suitable for supplying the proper control voltages. Obviously, it would be possible to supply separate control voltages to the emitters of transistors **14** and **16** for turning them on or off simultaneously.

While there have been shown and described and pointed out the fundamental novel features of the invention as applied to a preferred embodiment, it will be understood that various omissions and substitutions and changes in the form and details of the device illustrated and in its operation may be made by those skilled in the art, without departing from the spirit of the invention. It is the intention, therefore, to be limited only as indicated by the scope of the following claims.

What is claimed is:

1. Apparatus for periodically clamping a signal line to a reference voltage, a first circuit including a unidirectional conducting means and a switching means coupling said signal line and said reference voltage, a second circuit including a unidirectional conducting means and a switching means coupling said signal line and said reference voltage, control means connected to each of said switching means for periodically and simultaneously causing each switching means to offer a low impedance to current flow therethrough, the unidirectional conducting means in said first circuit being oriented to offer a low impedance to current flow therethrough when said signal line is more positive than said reference voltage and the unidirectional conducting means in said second circuit being oriented to offer a low impedance to current flow therethrough when said signal line is more negative than said reference voltage, the switching means in said first circuit including an NPN transistor and the switching means in said second circuit including a PNP transistor.

2. Apparatus for periodically clamping a signal line to a reference voltage comprising first and second transistors of opposite conductivity type, each of said transistors having emitter, base and collector electrodes, unidirectional conducting means connecting the collector electrode of each of said transistors to said signal line, means connecting the base electrode of each transistor to a fixed voltage, and means for applying input signals to the emitter electrodes of each of the transistors, said input signals causing predetermined periods of simultaneous conduction of said transistors to thereby offer a low impedance to current flow therethrough, the unidirectional conducting means associated with said first transistor being oriented opposite to the unidirectional conducting means associated with said second transistor.

3. Apparatus for periodically clamping a signal line to a reference voltage, an NPN transistor and a PNP transistor, each of said transistors having an emitter, a base and a collector electrode, the base electrode of each transistor being connected to a fixed voltage, means for applying input signals to the emitter electrode of each

of said transistors, said input signals at one time biasing each transistor for conduction and at another time biasing each transistor for non-conduction, and unidirectional conducting means connecting the collector electrode of each transistor to said signal line, one of said unidirectional conducting means being oriented to offer a low impedance during periods of transistor conduction when said signal line is more positive than said fixed voltage and the other unidirectional conducting means being oriented to offer a low impedance during periods of transistor conduction when said signal line is more negative than said fixed voltage.

4. Apparatus for periodically clamping a signal line to a reference voltage, which signal line is coupled by an impedance element to a waveshape generator, said apparatus having a first circuit comprising an NPN transistor and a unidirectional conducting device and a second circuit comprising a PNP transistor and a unidirectional conducting device, each of said transistors having at least emitter, base and collector electrodes, means connecting the base electrodes of each transistor to a fixed voltage, the collector electrode of each transistor being connected to the unidirectional conducting device in circuit therewith, and means for periodically applying an input signal to the emitter electrode of each of said transistors to cause them to go into conduction and thereby offer a low impedance path for current flow between the collector and base electrodes of each transistor, the unidirectional conducting device in said first circuit being oriented to offer a low impedance to current flow when said signal line is more positive than said fixed voltage, and the unidirectional conducting device in said second circuit being oriented to offer a low impedance to current flow when said signal line is more negative than said fixed voltage.

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