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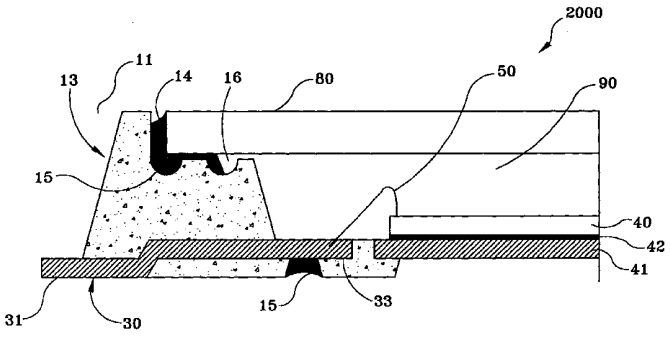
(54) Title: LEADLESS SEMICONDUCTOR PRODUCT PACKAGING APPARATUS HAVING A WINDOW LID AND METHOD FOR PACKAGING



(57) Abstract: A natural-resource-conservative, environmentlaly-friendly, cost-effective, leadless semiconductor packaging apparatus, having superior mechanical and electrical properties, and having an optional windowed housing which uniquely seals and provides a mechanism for viewing the internally packaged integrated semiconductor circuits (chips/die). A uniquely stamped and/or bent lead-frame is packaged by a polymeric material during a unique compression-modling process using a mold, specially contoured to avoid the common "over-packaging" problem in related art techniques. The specially contoured mold facilitates delineation of the internal portions from the external portions of the lead-frame, as the external portions are the effective solderable areas that contact pads on a printed circuit board, thereby avoiding a laborious environmentally-unfriendly masking step and de-flashing step, streamlining the device packaging process. The compression-mold effectively provides a compressive sealing orifice from which the effective solderable areas of the lead-frame may extend and be exposed and, thus, avoid being coated with the polymer which is uniquely contained by the mold for packaging the internal portions of the lead-frame. The lead-frame is uniquely stamped and/or bent, conforming it to electro-mechanical requirements of a particular semiconductor product. By uniquely stamping and/or bending, the related art "half-etching" of the lead for conforming it to electro-mechanical requirements of the packaged semiconductor product is no longer required. Environmental enhancement is achieved by conserving natural resources and by eliminating hazardous material by-products otherwise liberated in related art packaging techniques.

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LEADLESS SEMICONDUCTOR PRODUCT PACKAGING APPARATUS HAVING A WINDOW LID AND METHOD FOR PACKAGING

RELATED APPLICATION

This application is related to co-pending U.S. Provisional Patent Application, Ser. No. 60/193,319, filed March 30, 2000 and U.S. Non-Provisional Patent Application, Ser. No. 09/668,423, filed September 22, 2000, both entitled "LEADLESS SEMICONDUCTOR PRODUCT PACKAGING APPARATUS HAVING GLASS WINDOW LID AND METHOD FOR PACKAGING," by the same Applicants.

TECHNICAL FIELD

The present invention relates to semiconductor product packaging and methods of fabrication for producing a packaged semiconductor product. More particularly, the present invention relates to leadless semiconductor product packaging and methods of fabrication for producing leadless packaged semiconductor product. Even more particularly, the present invention relates to leadless semiconductor product packaging and methods of fabrication for mass-producing packaged semiconductor product without employing time-consuming, environmentally-unfriendly related art lead-frame etching and de-flashing techniques.

BACKGROUND ART

In response to manufacturing cost concerns relating to populating printed circuit boards with electronic product having the requisite functional circuits, the semiconductor product packaging industry has developed a leadless circuit component product (also known as a surface mountable electronic product), hereinafter referred to as a "leadless product." The leadless product, as the name implies, is a packaged electronic product that does not require the use of physical leads for being inserted into mating holes provided on a planar board as a mechanical mounting means nor as an electrical connection with other electronic components forming the circuit on such a planar board. In general, the leadless product facilitates manufacturing of a printed circuit card, thereby eliminating the inserting of component leads into the board holes and the soldering of these leads to the board's solder pads. The leadless technology has been well accepted as an option for packaging electronic components since early 1980. By example, a current related art industrial product includes "QFN" (Quad Flat No Lead, registered as JEDEC STD MO 197, 198, 208, 209, and 220). Of course, the electronic component function may still be available in a lead-type packaging structure.

In the related leadless semiconductor product packaging art, "half-etching" techniques are used for forming the lead-frame, generating considerable hazardous material (e.g., acid waste, metals waste, and possibly organic solvent waste); and an adhesive tape is used to temporarily mask effective solderable areas of the lead-frame (also known as the "outer I/O") from the packaging material to be applied during the molding process in order to preserve such effective solderable areas of the lead-frame in an un-insulated state, generating undue tape and possibly organic solvent waste. In another related semiconductor product packaging art technique, the lead-frame is completely packaged by a molding process; and the effective solderable areas of the lead-frame must be subsequently "de-flashed" in a process wherein such portions are blasted with a highly pressurized aqueous slurry of particulates (i.e., wet-blasting) to remove the "over-packaging," thereby generating considerable hazardous material in the form of polymeric waste slurry. Therefore, a need exists for providing a natural resource-conservative and environmentally-friendly method and apparatus for packaging a leadless semiconductor product.

DISCLOSURE OF INVENTION

The present invention, a leadless semiconductor packaging apparatus, provides a cost-effective product, having superior mechanical, electrical, and thermal properties, and having an optional window lid feature (i.e., a sight lid) which not only uniquely seals, but also provides a mechanism for viewing the internally packaged integrated semiconductor circuits (chips/die). Cost reduction is achieved by (a) optionally using polymeric materials, such as epoxies, rather than conventional related art ceramic materials for packaging devices, and (b) simplifying the packaging process, thereby improving productivity.

The present invention employs a unique "stamped" and/or "bent" standard solder-plated or pre-plated lead-frame which is packaged by a polymeric material during a molding process, in contrast to the related art "half-etched" lead-frame. The process of the present invention involves providing a unique compression-type mold, specially contoured to avoid "over-packaging," of the effective solderable areas of the lead-frame which is a common problem in the related art techniques. Applicants' invention results in streamlining the device fabrication and packaging process. The specially contoured compression-mold facilitates delineation of the internal portions from the external portions of the lead-frame, where the external portions have the effective solderable areas that contact pads on a printed circuit board. The mold effectively provides a

"compressive sealing orifice" from which the effective solderable areas of the lead-frame may extend and be exposed and, thus, avoid being coated with the polymer which is contained by the mold for packaging the internal portions of the lead-frame, thereby avoiding a laborious masking step and a tedious de-flashing step.

The present invention applies the unique technique of "stamping" and/or "bending" of the lead-frame, thereby conforming it to electro-mechanical requirements of a particular semiconductor product. By stamping and/or bending the lead-frame material into the desired configuration, the present invention does not require old art "half-etching" of the lead for conforming it to electro-mechanical requirements of the packaged semiconductor product. By example, the related art process "half-etches" the lead-frame (e.g., 10 mils of raw conducting material are etched to about 5 mils, thereby generating a large volume of acid and conducting material hazardous waste) in order to create the requisite shape. Thus, thinner lead-frame material, such as that in a range of 6 mils or less, may be used with the present invention. The present invention offers several more distinctive advantages: (a) customer-specifiable package size, (b) applicable existing surface mount technology (SMT) processes, (c) overall improved performance at a lower cost, (d) complete absence of hazardous material by-products in full-scale production (environmentally-friendly, i.e., no acid waste, no metals waste, no liberation of volatile organic compounds, and no solid polymeric slurry waste), and (e) thinner lead-frame material (natural-resource-conservative).

BRIEF DESCRIPTION OF DRAWINGS

For a better understanding of the present invention, reference is made to the below-referenced accompanying drawings.

Figure 1.1 is a cross-sectional view of a near chip-size basic leadless semiconductor packaging apparatus having packaging mold-lines shown with respect to a leadless semiconductor device configuration having a die located in the "up" position with a wire bonded to a stamped lead frame and another wire bonded to a die attach pad, in accordance with the present invention.

Figure 1.2 is a cross-sectional view of a near chip-size leadless semiconductor packaging apparatus having packaging mold-lines shown with respect to a leadless semiconductor device configuration having a stamped lead-frame and a die with a wire therebetween bonded in the "down" position, in accordance with the present invention.

Figure 1.3 is a cross-sectional view of a near chip-size thermal leadless semiconductor

packaging apparatus having packaging mold-lines shown with respect to a leadless semiconductor device configuration having a stamped lead-frame and a die with a wire therebetween bonded in the "up" position and with the die sharing a common die attach pad, in accordance with the present invention.

Figure 1.3a is a cross-sectional view of a near chip-size thermal leadless semiconductor packaging apparatus having packaging mold-lines shown with respect to a leadless semiconductor device configuration having a stamped lead-frame and a die with a wire therebetween bonded in the "up" position and with a lower surface of the die attach pad being unmolded (i.e., exposed), in accordance with the present invention.

Figure 1.4 is a cross-sectional view of a near chip-size leadless semiconductor packaging apparatus having packaging mold-lines shown with respect to a leadless semiconductor device configuration having a stamped lead-frame and a center pad located beneath the stamped lead-frame with a wire bonded therebetween in the "up" position, in accordance with the present invention.

Figure 1.4a is a cross-sectional view of a near chip-size leadless semiconductor packaging apparatus having packaging mold-lines shown with respect to a leadless semiconductor device configuration having a stamped lead-frame and a center pad located beneath the stamped lead-frame with a wire bonded therebetween in the "up" position and a lower surface of the center pad being unmolded, in accordance with the present invention.

Figure 1.4b is a cross-sectional view of a near chip-size leadless semiconductor packaging apparatus having packaging mold-lines shown with respect to a leadless semiconductor device configuration having a stamped lead-frame and a flip chip located beneath the stamped lead-frame with at least one conducting particle contacting and being disposed between the lead-frame and the flip chip, in accordance with the present invention.

Figure 1.4c is a cross-sectional view of a chip-size leadless semiconductor packaging apparatus having packaging mold-lines shown with respect to a leadless semiconductor device configuration having a stamped lead-frame and a flip chip located above the stamped lead-frame with at least one conducting particle contacting and being disposed between the lead-frame and the flip chip, in accordance with the present invention.

Figure 1.5 is a cross-sectional view of a chip-size leadless semiconductor packaging apparatus having packaging mold-lines shown with respect to a leadless semiconductor device configuration having a die located on a lead-frame and a wire bonded therebetween in the "up"

position, in accordance with the present invention.

Figure 1.6 is a cross-sectional view of a chip-size leadless semiconductor packaging apparatus having packaging mold-lines shown with respect to a leadless semiconductor device configuration having a die located on at least one lead-frame and a wire bonded therebetween in the "up" position, in accordance with the present invention.

Figure 1.7 is a cross-sectional view of a chip-size leadless semiconductor packaging apparatus having packaging mold-lines shown with respect to a leadless semiconductor device configuration having an exposed die laterally located with regard to the lead-frame and a wire bonded therebetween in the "up" position, in accordance with the present invention.

Figure 1.8 is a cross-sectional view of a leadless semiconductor packaging apparatus having packaging mold-lines shown with respect to at least one leadless semiconductor device, as would occur during a manufacturing process, in accordance with the present invention.

Figure 2.0 is a cross-sectional view of a windowed leadless semiconductor packaging apparatus with a leadless semiconductor device configuration having a stamped lead frame, a die, and a bonded wire being packaged by a sight lid sealed against a cured polymeric material having a flush mold-line located at the interior portion of the stamped lead frame, in accordance with the present invention.

Figure 3.0 is a perspective view of a windowed leadless semiconductor packaging apparatus having a stamped lead-frame having a plurality of leads sharing a common die by bonding a wire therebetween as viewed through a sight lid, in accordance with the present invention.

Figure 4.0 is a flow-chart of a fabrication method for packaging a leadless semiconductor packaging apparatus, in accordance with the present invention.

Figure 5.0 is a flow-chart of a fabrication method for packaging a windowed leadless semiconductor packaging apparatus, in accordance with the present invention.

Reference numbers refer to the same or equivalent parts of the present invention throughout the several figures of the drawings.

MODE FOR CARRYING OUT THE INVENTION

Figure 1.1 illustrates, in cross-section, a first embodiment, a "near chip-size" leadless semiconductor packaging apparatus 1000 (i.e., where the packaging and external lead portions extend minimally beyond the plan-form area of a given chip) having packaging mold-lines 10 and

a unique "stamped" and "bent" lead-frame 30 formed by "stamping" and "bending" a conductive material such as copper, with an effective solderable length 60 and effecting a bend 34, the unique stamped and bent lead-frame 30 being uniquely compressively retained by a mold 11 (not shown), in accordance with the present invention. Other leadless semiconductor device components therein shown are a die 40, a die attach pad 41 which may be formed of a pad metal, and a bonded wire 50 formed from a conductive material such as gold. The mold 11 (not shown) uniquely effectively retains, by compression (e.g., using a hot-press), a polymeric material 12, such as a polymeric molding compound, for surrounding only the interior portion of the stamped and bent lead-frame 30, thereby uniquely preserving a clean solderable area on the stamped and bent lead-frame 30, and thereby avoiding the environmentally-unfriendly related art need for de-flashing of excess packaging material. A method for trimming the stamped and bent lead-frame 30 may include sawing or punch-cutting in the direction indicated by arrow 70.

Figure 1.2 is a cross-sectional view of a second embodiment, a near chip-size leadless semiconductor packaging apparatus 1000, having packaging mold-lines 10, a unique stamped and bent lead-frame 30 formed by stamping and bending a conductive material such as copper, effecting a bend 34, and a die 40 with a wire 50, formed from a conductive material such as gold, therebetween bonded in the "down" position, in accordance with the present invention. These components are uniquely compression-molded in the manner discussed with respect to Figure 1.1.

Figure 1.3 is a cross-sectional view of a third embodiment, a near chip-size thermal leadless semiconductor packaging apparatus 1000 having packaging mold-lines 10, a unique stamped and bent lead-frame 30 formed by stamping and bending a conductive material such as copper, effecting a bend 34, and a die 40 with a wire 50 formed from a conductive material such as gold, therebetween bonded in the "up" position and with the stamped and bent lead-frame 30 and the die 40 sharing a common die attach pad 41 being unmolded (i.e., exposed), in accordance with the present invention. These components are uniquely compression-molded in the manner discussed with respect to Figure 1.1.

Figure 1.3a is a cross-sectional view of a fourth embodiment, a near chip-size thermal leadless semiconductor packaging apparatus 1000 having packaging mold-lines 10, a unique stamped and bent lead-frame 30 formed stamping and bending a conductive material such as copper, effecting a bend 34, and a die 40 with a wire 50 formed from a conductive material such as gold, therebetween bonded in the "up" position and with a lower surface of the die attach pad 41 being unmolded (i.e., exposed), in accordance with the present invention. These components

are uniquely compression-molded in the manner discussed with respect to Figure 1.1.

Figure 1.4 is a cross-sectional view of a fifth embodiment, a near chip-size leadless semiconductor packaging apparatus 1000 having packaging mold-lines 10, a unique stamped and bent lead-frame 30 formed by stamping and bending a conductive material such as copper, effecting a bend 34, and a center pad 40a located beneath the stamped and bent lead-frame 30 with a wire 50 formed from a conductive material such as gold, bonded therebetween in the "up" position, in accordance with the present invention. These components are uniquely compression-molded in the manner discussed with respect to Figure 1.1.

Figure 1.4a is a cross-sectional view of a sixth embodiment, a near chip-size leadless semiconductor packaging apparatus 1000 having packaging mold-lines 10, a stamped and bent lead-frame 30 formed by stamping and bending a conductive material such as copper, effecting a bend 34, and a center pad 40a located beneath the stamped and bent lead-frame 30 with a wire 50 formed from a conductive material such as gold, bonded therebetween in the "up" position and a lower surface of the center pad 40a being unmolded (i.e., exposed), in accordance with the present invention. These components are uniquely compression-molded in the manner discussed with respect to Figure 1.1.

Figure 1.4b is a cross-sectional view of a seventh embodiment, a near chip-size leadless semiconductor packaging apparatus 1000 having packaging mold-lines, a unique stamped and bent lead-frame 30 formed by stamping and bending a conductive material such as copper, effecting a bend 34, and a flip chip 40b located beneath the stamped and bent lead-frame 30 with at least one conducting particle 51 contacting and being disposed between the stamped and bent lead-frame 30 and the flip chip 40b, in accordance with the present invention. These components are uniquely compression-molded in the manner discussed with respect to Figure 1.1.

Figure 1.4c is a cross-sectional view of an eighth embodiment, a "chip-size" leadless semiconductor packaging apparatus 1000 having packaging mold-lines 10, a unique stamped lead-frame 30 formed by stamping a conductive material such as copper, and a flip chip 40b located above the stamped lead-frame 30 with at least one conducting particle 51 contacting and being disposed between the stamped lead-frame 30 and the flip chip 40b, in accordance with the present invention. These components are uniquely compression-molded in the manner discussed with respect to Figure 1.1.

Figure 1.5 is a cross-sectional view of a ninth embodiment, a chip-size leadless semiconductor packaging apparatus 1000 (i.e., where the packaging and external lead portions

extend *very* minimally beyond the plan-form area of a given chip, where the plan-form package area is less than or equal to 1.2 times the die plan-form area) having packaging mold-lines 10, a die 40 located on a unique stamped lead-frame 30 formed by stamping a conductive material such as copper, and a wire 50 formed from a conductive material such as gold, bonded therebetween in the "up" position, in accordance with the present invention. These components are uniquely compression-molded in the manner discussed with respect to Figure 1.1.

Figure 1.6 is a cross-sectional view of a tenth embodiment, a chip-size leadless semiconductor packaging apparatus 1000 having packaging mold-lines 10, a die 40 located on at least one unique stamped lead-frame 30 formed by stamping a conductive material such as copper, and a wire 50 formed from a conductive material such as gold, bonded therebetween in the "up" position, in accordance with the present invention. These components are uniquely compression-molded in the manner discussed with respect to Figure 1.1.

Figure 1.7 is a cross-sectional view of an eleventh embodiment, a leadless semiconductor packaging apparatus 1000 having packaging mold-lines, an exposed die 40 laterally located with regard to the unique stamped lead-frame 30 formed by stamping a conductive material such as copper, and a wire 50 formed from a conductive material such as gold, bonded therebetween in the "up" position, in accordance with the present invention. These components are uniquely compression-molded in the manner discussed with respect to Figure 1.1.

Figure 1.8 illustrates, in cross-section, a near chip-size leadless semiconductor packaging apparatus 1000, consistent with the third embodiment, having packaging mold-lines 10, at least one unique stamped and bent lead-frame 30 which may be formed by stamping and bending a conductive material such as copper, effecting a bend 34, with an effective solder able length 60, being retained by a mold 11 (not shown) as would occur during a manufacturing process, in accordance with the present invention. Other leadless semiconductor device components therein shown are at least one die 40, at least one die attach pad 41 which may be formed of a pad metal, and at least one bonded wire 50 formed from a conductive material such as gold. In packaging a plurality of leadless semiconductor devices, a method for separating the mass-produced packaged devices in an assembly line fashion may include sawing or punch-cutting in the direction indicated by arrow 70. The mold 11 (not shown) uniquely and effectively retains, via compressive forces, at least one polymeric material 12 for surrounding only the interior portion of the at least one unique stamped and bent lead-frame 30 (i.e., without leakage to an exterior portion the at least one stamped lead-frame), thereby preserving clean solder able areas on an external portion of the at

least one unique stamped and bent lead-frame 30, and thereby avoiding the related art need for de-flashing of excess packaging material.

Figure 2.0 illustrates, in cross-section, another embodiment of the present invention, a windowed leadless semiconductor packaging apparatus 2000 having a leadless semiconductor device comprising a unique stamped and bent lead-frame 30 formed by stamping and bending a conductive material such as copper, effecting a bend 34, a die 40 adhered to a die attach pad 41 by a non-electrically conductive adhesive material 42, and a wire 50 formed from a material such as gold, being packaged by a sight lid 80, formed from a visually transparent material such as a glass or a high temperature polymer, uniquely sealed against a cured polymeric material body 13 by a sealant material 14 such as a UV-curable epoxy resin, in accordance with the present invention. Sealant material 14 is compressed by the sight lid 80 into an outboard channel 15 of a unique dual channel sealant seat such that a portion of the sealant material 14 flows into an inboard channel 16 for providing a uniquely larger sealing surface area and better sealing against contaminant entry. The present invention, however, is not limited to the use of dual channels, but may utilize at least one channel as required by the given semiconductor circuit to be packaged. The cured polymeric material body 13 has an overlapping tapered mold line located at both the exterior portion 31 and the interior portion 32 of the stamped lead-frame 30 and a flush mold line located between the die attach pad 41 and the interior portion 33 of stamped lead-frame 30. A reinforced fill material 15 is cured unto a lower surface of the interior portion 33 of the stamped lead-frame 30, such interior portion 33 formerly being uniquely compressively retained by the mold 11 (not shown).

Figure 3.0 illustrates, in perspective view, a windowed leadless semiconductor packaging apparatus 2000 having a stamped and/or bent lead-frame 30 formed by stamping and/or bending a conductive material such as copper, such unique stamping effecting removal of lead-frame material as indicated by void 35, sharing a common die 40 by bonding a wire 50 therebetween as viewed through the sight lid 80 sealed against a unique sealant seat 15, 16 having at least one channel formed in the cured polymeric body 13, the polymeric body 13 being formed by the foregoing unique compression-molding technique, in accordance with the present invention.

Figure 4.0 flow-charts the general fabrication method M-1 for packaging at least one leadless semiconductor packaging apparatus 1000, in accordance with the present invention. Method M-1 comprises the steps of: (a) providing at least one stamped lead-frame having at least one lead, by sawing or punch-cutting a lead-frame material as indicated by process block 100, (b)

attaching a die to the at least one lead-frame by applying a non-electrically conductive adhesive material (die attach) as indicated by process block 200, (c) curing the non-electrically conductive adhesive material as indicated by process block 300, (d) bonding a wire from the die to each of the at least one lead as indicated by process block 400, (e) molding the semiconductor device components in another polymeric material, such as a polymeric molding compound, by a technique such as hot compression-molding using a hot-press having an upper platen and a lower platen, effecting a unique sealing orifice from which the external lead portion extends via a compressive force and a nominally localized deformation, thereby forming the at least one leadless semiconductor packaging apparatus 1000, as indicated by process block 500, (f) marking, by lasing, the at least one formed leadless semiconductor packaging apparatus 1000 as indicated by process block 600, (g) singulating, the at least one laser-marked leadless semiconductor packaging apparatus 1000, as indicated by process block 700, (h) packing the at least one singulated leadless semiconductor packaging apparatus 1000 as indicated by process block 800, and (i) shipping the at least one packed leadless semiconductor packaging apparatus 1000 as indicated by process block 900.

Figure 5.0 flow-charts the general fabrication method M-2 for packaging at least one windowed leadless semiconductor packaging apparatus 2000, in accordance with the present invention. Method M-2 comprises the steps of: (a) providing at least one stamped lead-frame having at least one lead, by pre-plating a lead-frame material as indicated by process block 102, (b) molding the at least one stamped pre-plated lead-frame in a polymeric material, such as a polymeric molding compound, by a technique such as hot compression-molding using a hot-press having an upper platen and a lower platen, effecting a unique sealing orifice from which the external lead portion extends via a compressive force and a nominally localized deformation, as indicated by process block 103, (c) sawing or punch-cutting the lead-frame material as indicated by process block 101, (d) attaching a die to the at least one lead-frame (die attach) as indicated by process block 202, (e) curing the non-electrically conductive adhesive material as indicated by process block 303, (f) bonding a wire from the die to the at least one lead as indicated by process block 404, (g) installing a window onto the molded lead-frame by applying a sealant such as a UV-curable epoxy as indicated by process block 505, thereby forming the at least one leadless semiconductor packaging apparatus 2000, (h) marking, by laser techniques, the at least one formed windowed leadless semiconductor packaging apparatus 2000 as indicated by process block 606, (i) singulating the at least one laser-marked windowed leadless semiconductor packaging apparatus

2000, as indicated by process block 707, (j) packing the at least one singulated windowed leadless semiconductor packaging apparatus 2000 as indicated by process block 808, and (k) shipping the at least one packed windowed leadless semiconductor packaging apparatus 2000 as indicated by process block 909.

Information as herein shown and described in detail is fully capable of attaining the above-described object of the invention, the presently preferred embodiment of the invention, and is, thus, representative of the subject matter which is broadly contemplated by the present invention. The scope of the present invention fully encompasses other embodiments which may become obvious to those skilled in the art, and is to be limited, accordingly, by nothing other than the appended claims, wherein reference to an element in the singular is not intended to mean "one and only one" unless explicitly so stated, but rather "one or more." All structural and functional equivalents to the elements of the above-described preferred embodiment and additional embodiments that are known to those of ordinary skill in the art are hereby expressly incorporated by reference and are intended to be encompassed by the present claims. Moreover, no requirement exists for a device or method to address each and every problem sought to be resolved by the present invention, for such to be encompassed by the present claims. Furthermore, no element, component, or method step in the present disclosure is intended to be dedicated to the public regardless of whether the element, component, or method step is explicitly recited in the claims. However, it should be readily apparent to those of ordinary skill in the art that various changes and modifications in form, semiconductor material, and fabrication material detail may be made without departing from the spirit and scope of the inventions as set forth in the appended claims. No claim herein is to be construed under the provisions of 35 U.S.C. 112, sixth paragraph, unless the element is expressly recited using the phrase "means for."

CLAIMS

What is claimed:

1. A leadless semiconductor product packaging apparatus for packaging a semiconductor circuit, comprising:

a. a lead-frame,

said lead-frame having an internal lead portion and an external lead portion,

said lead-frame being in electrical contact with said semiconductor circuit, and

said lead-frame being formed by stamping a lead frame material; and

b. a housing member,

said housing member comprising a housing material, and

said housing material encapsulating said lead-frame such that said external lead portions are exposed to provide solderable regions.

2. The leadless semiconductor product packaging apparatus, as recited in claim 1, wherein said semiconductor circuit comprises:

a. at least one die attach pad,

wherein said semiconductor circuit is mounted on said die attach pad; and

b. at least one wire,

wherein said at least one wire is wire-bonded to effect an electrical connection between said circuit and said internal lead portion,

wherein said at least one wire is formed from an electrically conducting material selected from a group of electrically conducting materials consisting essentially of copper, aluminum, and gold,

wherein said housing material is further compression-molded around said die attach pad, said at least one wire, and said internal lead portion,

wherein said housing material is not compression-molded around said lead external portion, and

wherein said stamped lead-frame is mechanically bent into a desired configuration for facilitating fit of said leadless semiconductor product packaging apparatus to a size in a range of chip-size to near chip-size.

3. The leadless semiconductor product packaging apparatus, as recited in claim 2, wherein said lead frame material has a thickness in a range of 6 mils or less.

4. The leadless semiconductor product packaging apparatus, as recited in claim 1, wherein said lead frame material has a thickness in a range of 6 mils or less.

5. The leadless semiconductor product packaging apparatus, as recited in claim 4, wherein said leadless semiconductor product comprises:

a. at least one die attach pad,

wherein said semiconductor circuit is mounted on said die attach pad; and

b. at least one wire,

wherein said at least one wire is wire-bonded to effect an electrical connection between said circuit and said internal lead portion,

wherein said at least one wire is formed from an electrically conducting material selected from a group of electrically conducting materials consisting essentially of copper, aluminum, and gold,

wherein said housing material is further compression-molded around said die attach pad, said at least one wire, and said internal lead portion,

wherein said housing material is not compression-molded around said lead external portion, and

wherein said stamped lead-frame is mechanically bent into a desired configuration for facilitating fit of said leadless semiconductor product packaging apparatus to a size in a range of chip-size to near chip-size.

6. The leadless semiconductor product packaging apparatus, as recited in claim 1, further comprising:

a. a window lid member,

wherein said window lid member forms a portion of said housing member, and

wherein said window lid member is formed from a visually transparent material selected from a group of visually transparent materials consisting essentially of a polymer and a glass;

b. a sealant material;

c. a sealant seat,

said sealant seat comprising at least one channel disposed on an upper surface of said housing member for providing a larger sealing surface area, and

said sealant material being disposed between said housing member and said window lid member within said at least one channel for preventing contaminant entry.

7. The leadless semiconductor product packaging apparatus, as recited in claim 2, wherein a die is attachable, by a non-electrically conductive polymer, to each said internal portion of said lead-frame.

8. The leadless semiconductor product packaging apparatus, as recited in claim 5, wherein a die is attachable, by a non-electrically conductive polymer, to each said internal portion of said lead-frame.

9. The leadless semiconductor product packaging apparatus, as recited in claim 1,
wherein said housing material comprises a polymeric molding compound,
wherein said housing member comprises said housing material being compression-molded,
whereby said external lead portion is exposed,
thereby preserving a solderable area on said external lead portion, and
thereby avoiding de-flashing of said external lead portion.

10. The leadless semiconductor product packaging apparatus, as recited in claim 1,
wherein said lead-frame is formed from at least one electrically conducting material selected from a group of electrically conducting materials consisting essentially of copper, aluminum, and gold,
wherein said housing material comprises at least one material selected from a group of housing materials consisting essentially of a polymer and a ceramic, and
wherein said polymer is selected from a group of polymers consisting essentially of an epoxy, a polyimide, and a bismaleimide.

11. A method for fabricating a leadless semiconductor product packaging apparatus for packaging a semiconductor circuit, comprising the steps of:

a. providing a lead-frame,

said lead-frame having an internal lead portion and an external lead portion,

said lead-frame being in electrical contact with said semiconductor circuit, and

said lead-frame being formed by stamping a lead-frame material; and

b. providing a housing member,

said housing member comprising a housing material, and

said housing material encapsulating said lead-frame such that said external lead portions are exposed to provide solderable regions, and

thereby forming said leadless semiconductor product packaging apparatus.

12. The method for fabricating a leadless semiconductor product packaging apparatus, as recited in claim 11, wherein said leadless semiconductor circuit comprises:

a. at least one die attach pad,

wherein said semiconductor circuit is mounted on said die attach pad; and

b. at least one wire,

wherein said at least one wire is wire-bonded to effect an electrical connection between said circuit and said internal lead portion,

wherein said at least one wire is formed from an electrically conducting material selected from a group of electrically conducting materials consisting essentially of copper, aluminum, and gold,

wherein said housing material is further compression-molded around said die attach pad, said at least one wire, and said internal lead portion,

wherein said housing material is not compression-molded around said lead external portion, and

wherein said lead-frame is mechanically bent into a desired configuration for facilitating fit of said leadless semiconductor product packaging apparatus to a size in a range of chip-size to near chip-size, and

thereby forming said leadless semiconductor product packaging apparatus.

13. The method for fabricating a leadless semiconductor product packaging apparatus, as

recited in claim 12, wherein said lead frame material has a thickness in a range of 6 mils or less.

14. The method for fabricating a leadless semiconductor product packaging apparatus, as recited in claim 11, wherein said lead frame material has a thickness in a range of 6 mils or less.

15. The method for fabricating a leadless semiconductor product packaging apparatus, as recited in claim 14, wherein said leadless semiconductor product comprises:

a. at least one die attach pad,

wherein said at least one semiconductor circuit is mounted on said die attach pad; and

b. at least one wire,

wherein said at least one wire is wire-bonded to effect an electrical connection between said circuit and said internal lead portion,

wherein said at least one wire is formed from an electrically conducting material selected from a group of electrically conducting materials consisting essentially of copper, aluminum, and gold,

wherein said housing material is further compression-molded around said die attach pad, said at least one wire, and said internal lead portion,

wherein said housing material is not compression-molded around said lead external portion, and

wherein said lead-frame is mechanically bent into a desired configuration for facilitating fit of said leadless semiconductor product packaging apparatus to a size in a range of chip-size to near chip-size, and

thereby forming said leadless semiconductor product packaging apparatus.

16. The method for fabricating a leadless semiconductor product packaging apparatus, as recited in claim 14, further comprising the steps of:

a. providing a window lid member,

wherein said window lid member forms a portion of said housing member, and

wherein said window lid member is formed from a visually transparent material

selected from a group of visually transparent materials consisting essentially of a polymer and a glass;

b. providing a sealant material;

c. providing a sealant seat,

said sealant seat comprising at least one channel disposed on an upper surface of said housing member for providing a larger sealing surface area, and

said sealant material being disposed between said housing member and said window lid member within said at least one channel for preventing contaminant entry, and

thereby forming said leadless semiconductor product packaging apparatus.

17. The method for fabricating a leadless semiconductor product packaging apparatus, as recited in claim 12, wherein a die is attachable, by a non-electrically conductive polymer, to each said internal portion of said lead-frame.

18. The method for fabricating a leadless semiconductor product packaging apparatus, as recited in claim 15, wherein a die is attachable, by a non-electrically conductive polymer, to each said internal portion of said lead-frame.

19. The method for fabricating a leadless semiconductor product packaging apparatus, as recited in claim 11,

wherein said housing material comprises a polymeric molding compound,

wherein said housing member comprises said housing material being compression-molded,

whereby said external lead portion is exposed,

thereby preserving a solderable area on said external lead portion, and

thereby avoiding de-flashing of said external lead portion.

20. The method for fabricating a leadless semiconductor product packaging apparatus, as recited in claim 11,

wherein said lead-frame is formed from an electrically conducting material,

said electrically conducting material comprising copper,

wherein said housing material comprises at least one material selected from a group of housing materials consisting essentially of a polymer and a ceramic, and

wherein said polymer is selected from a group of polymers consisting essentially of an epoxy, a polyimide, and a bismaleimide.

21. A method for fabricating at least one leadless semiconductor product packaging apparatus for packaging at least one semiconductor circuit, comprising the steps of:

a. stamping a lead-frame material for providing at least one stamped lead-frame, said lead-frame material having a thickness in a range of less than 6 mils, said at least one stamped lead-frame having an internal lead portion and an external lead portion;

b. applying a non-electrically conductive adhesive material to an interface between a die and said internal lead portion for attaching said die to said internal lead portion for each of said at least one lead frame;

c. curing said non-electrically conductive adhesive material for each of said at least one stamped lead-frame;

d. providing a wire for each of said at least one stamped lead-frame,
said wire having a first end and a second end,
wherein said first wire end is bonded to said die, and
wherein said second wire end is bonded to said lead internal portion;

e. molding a housing material around said lead internal portion in a mold using a hot-press to form a housing member for each of said at least one stamped lead-frame,
said mold having an upper portion and a lower portion,
said hot-press having an upper platen and a lower platen being parallel to one another,
said upper mold portion being inwardly disposed on said upper platen,
said lower mold portion being inwardly disposed on said lower platen,
said lead internal portion being attached to said die,
said upper hot-press platen and said lower hot-press platen being translated together in a direction normal to said platens respectively compressing said upper mold portion against said lower mold portion,
whereby a compressive force is exerted by said mold portions on said external lead

portion to create a nominally localized deformation on said external lead portion,

whereby a leak-proof seal, between said internal lead portion and said external lead portion, is effected via said compressive force and said nominally localized deformation, and

whereby said housing material is cured within said mold,

thereby forming said housing member, and

thereby forming said at least one leadless semiconductor product packaging apparatus,

f. marking, by lasing, said external lead portion of each of said at least one formed leadless semiconductor product packaging apparatus;

g. singulating said external lead portion of each of said at least one formed leadless semiconductor product packaging apparatus from one another;

h. packing said singulated said at least one leadless semiconductor product packaging apparatus; and

i. shipping said packed leadless semiconductor product packaging apparatus.

22. The method for fabricating at least one leadless semiconductor product packaging apparatus for packaging at least one semiconductor circuit, as recited in claim 21, wherein said lead-frame is mechanically bent into a desired configuration for facilitating fit of said leadless semiconductor product packaging apparatus to a size in a range of chip-size to near chip-size.

23. A method for fabricating at least one windowed leadless semiconductor product packaging apparatus for packaging at least one semiconductor circuit, comprising the steps of:

a. stamping a lead-frame material for providing at least one stamped lead-frame, said lead-frame material having a thickness in a range of less than 6 mils, said at least one stamped lead-frame having an internal lead portion and an external lead portion;

b. pre-plating said at least one stamped lead-frame;

c. molding a housing material around said lead internal portion in a mold using a hot-press to form a housing member for each of said at least one stamped lead-frame,

said mold having an upper portion and a lower portion,

said upper mold portion having a mold-line for accommodating a sight lid,

said hot-press having an upper platen and a lower platen being parallel to one another,

said upper mold portion being inwardly disposed on said upper platen,

said lower mold portion being inwardly disposed on said lower platen,

said lead internal portion being attached to said die,

said upper hot-press platen and said lower hot-press platen being translated together in a direction normal to said platens respectively compressing said upper mold portion against said lower mold portion,

whereby a compressive force is exerted by said mold portions on said external lead portion to create a nominally localized deformation on said external lead portion,

whereby a leak-proof seal, between said internal lead portion and said external lead portion, is effected via said compressive force and said nominally localized deformation, and

whereby said housing material is cured within said mold,

thereby forming said housing member, and

thereby forming said at least one leadless semiconductor product packaging apparatus,

d. applying a non-electrically conductive adhesive material to an interface between a die and said internal lead portion for attaching said die to said internal lead portion for each of said at least one lead frame;

e. curing the non-electrically conductive adhesive material for each of said at least one lead frame;

f. providing a wire for each of said at least one lead frame,

said wire having a first end and a second end,

wherein said first wire end is bonded to said die, and

wherein said second wire end is bonded to said lead internal portion;

g. installing a window lid member onto said housing member by curing a sealant material into a sealant seat having at least one channel,

said sealant being interracially disposed between said window and said molded

lead-frame,

said sealant being compressed by said sight lid, a portion of said sealant material being thereby pressed into said at least one channel,

whereby seal is effected, and

thereby forming said at least one windowed leadless semiconductor product packaging apparatus having said window lid member;

h. marking, by lasing, said external lead portion of said at least one windowed formed leadless semiconductor product packaging apparatus;

i. singulating said external lead portion of said at least one windowed formed leadless semiconductor product packaging apparatus from one another;

j. packing said singulated at least one windowed leadless semiconductor product packaging apparatus; and

k. shipping said packed at least one windowed leadless semiconductor product packaging apparatus.

24. The method for fabricating at least one windowed leadless semiconductor product packaging apparatus for packaging at least one semiconductor circuit, as recited in claim 22, wherein said lead-frame is mechanically bent into a desired configuration for facilitating fit of said leadless semiconductor product packaging apparatus to a size in a range of chip-size to near chip-size.

Figure 1.1

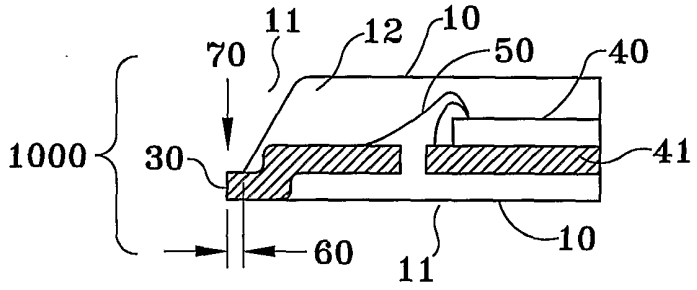


Figure 1.2

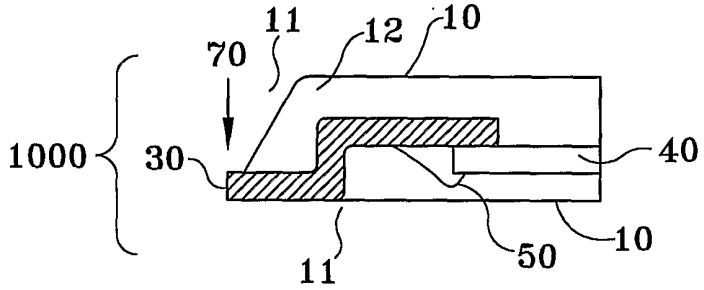


Figure 1.3

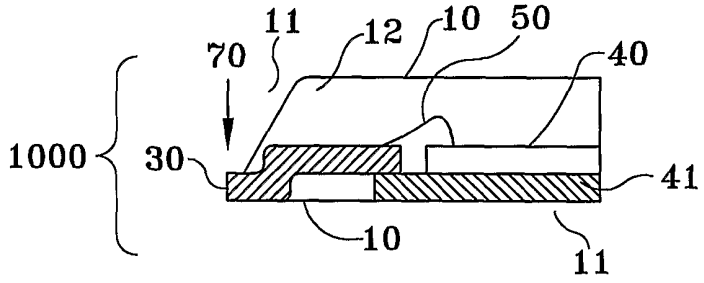


Figure 1.3a

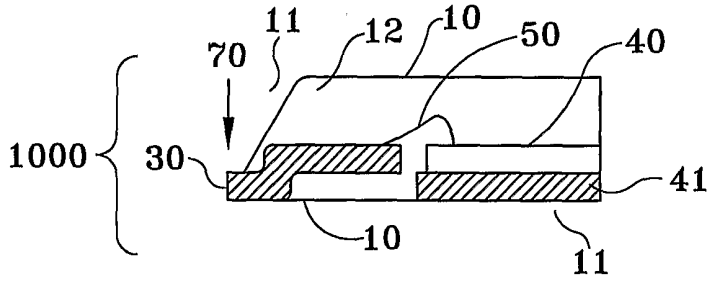
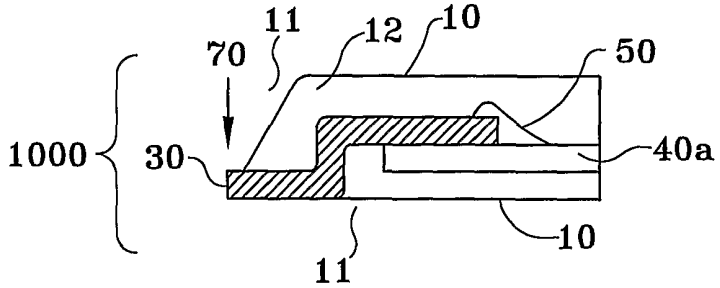


Figure 1.4



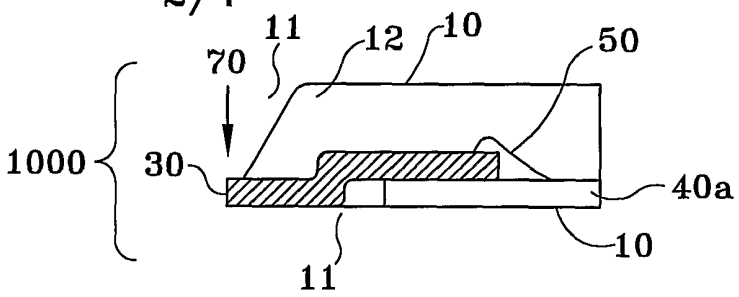


Figure 1.4a

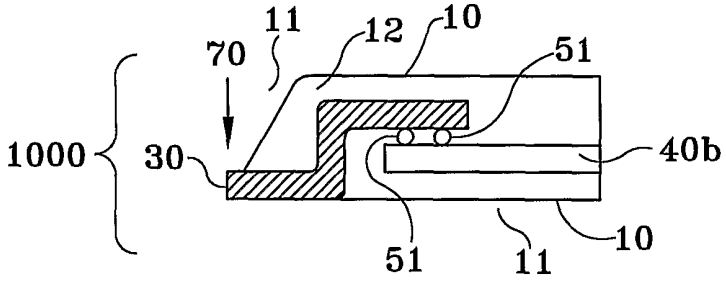


Figure 1.4b

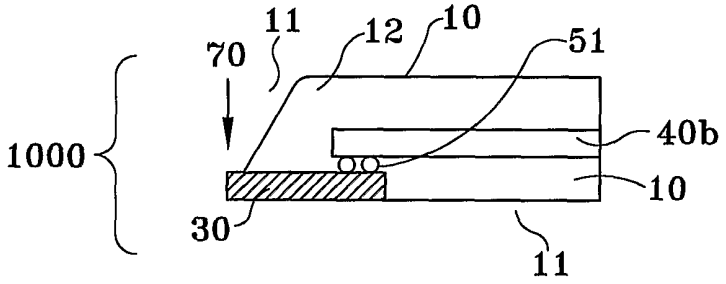


Figure 1.4c

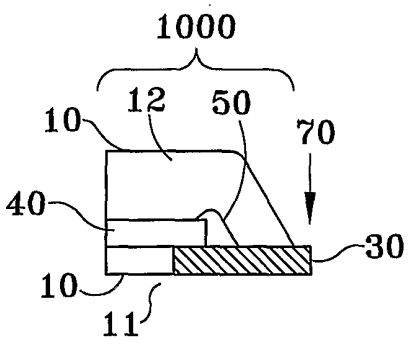


Figure 1.5

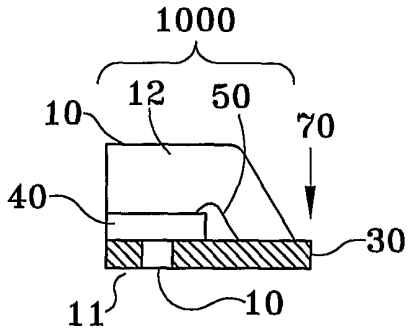


Figure 1.6

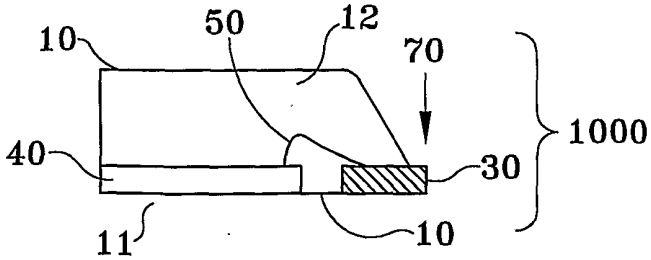


Figure 1.7

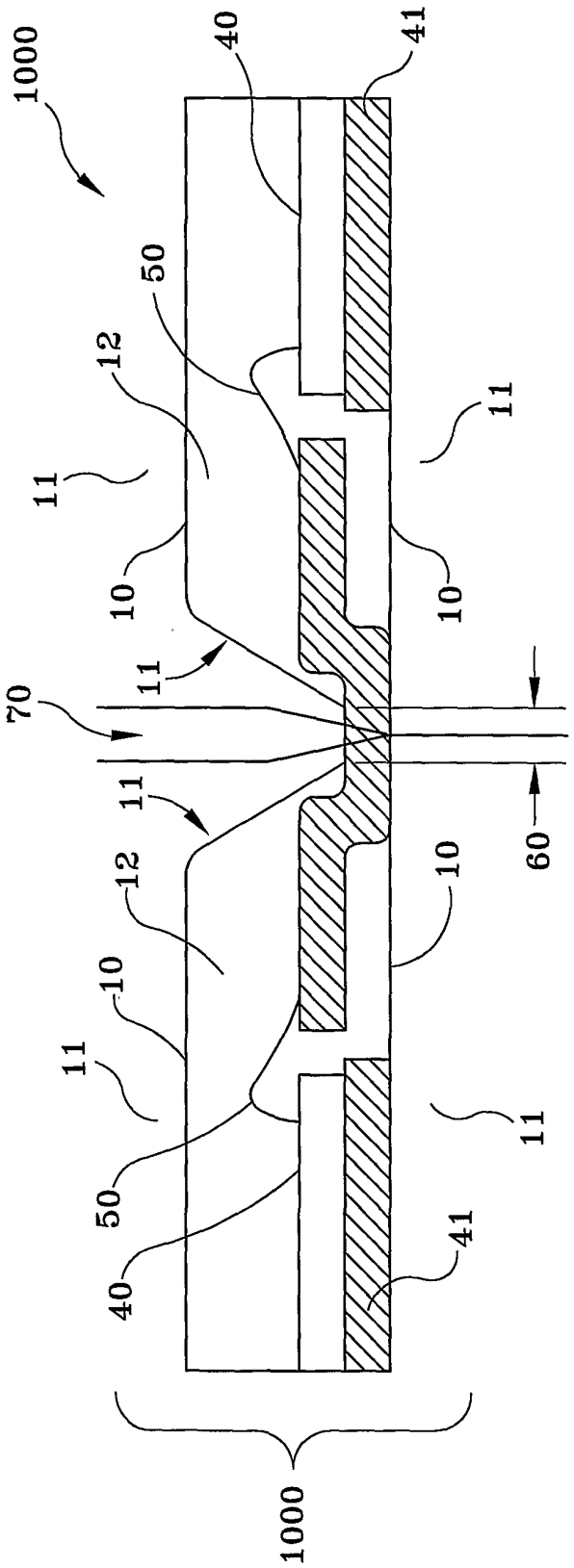


Figure 1.8

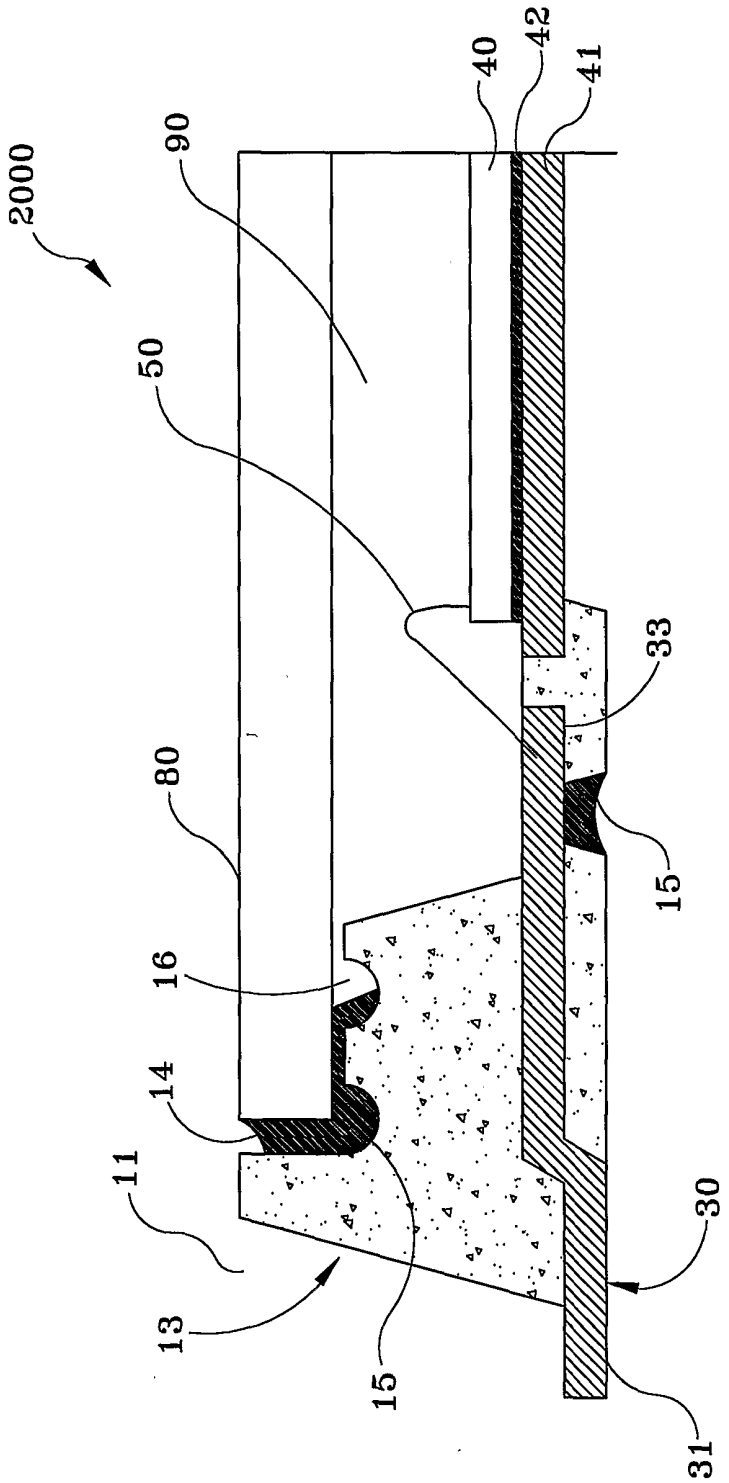


Figure 2.0

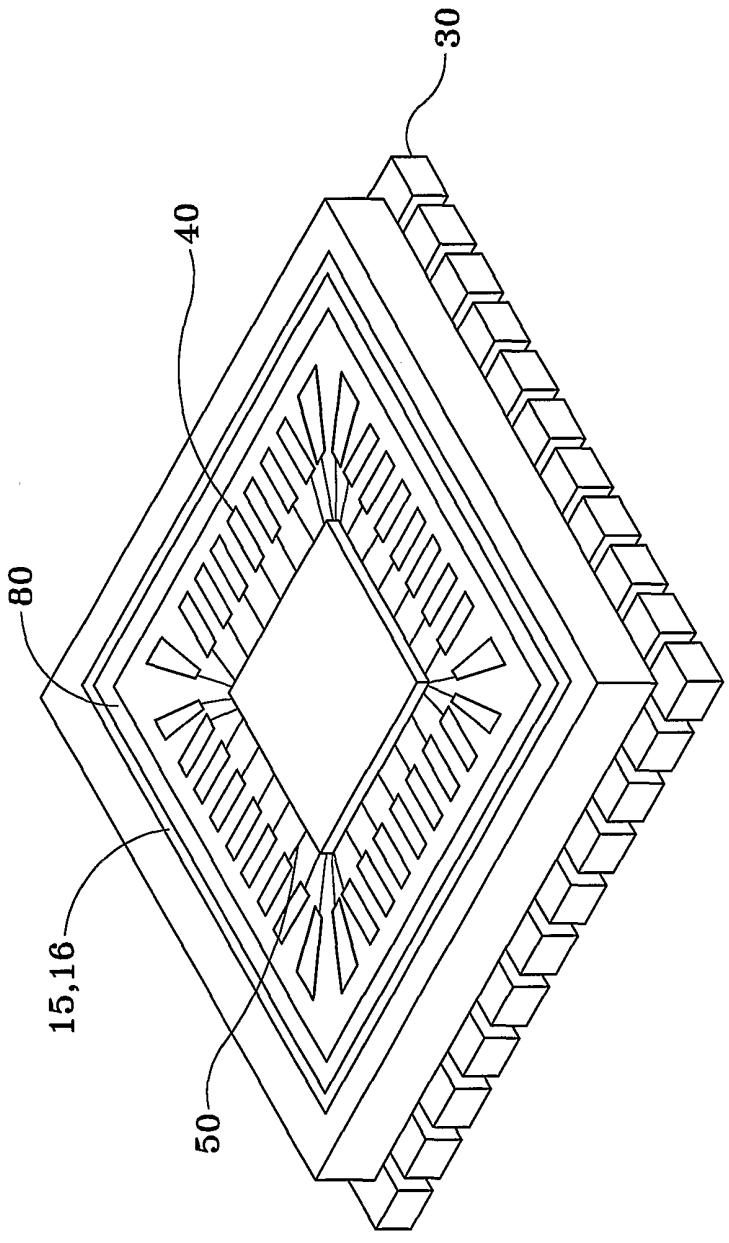


Figure 3.0

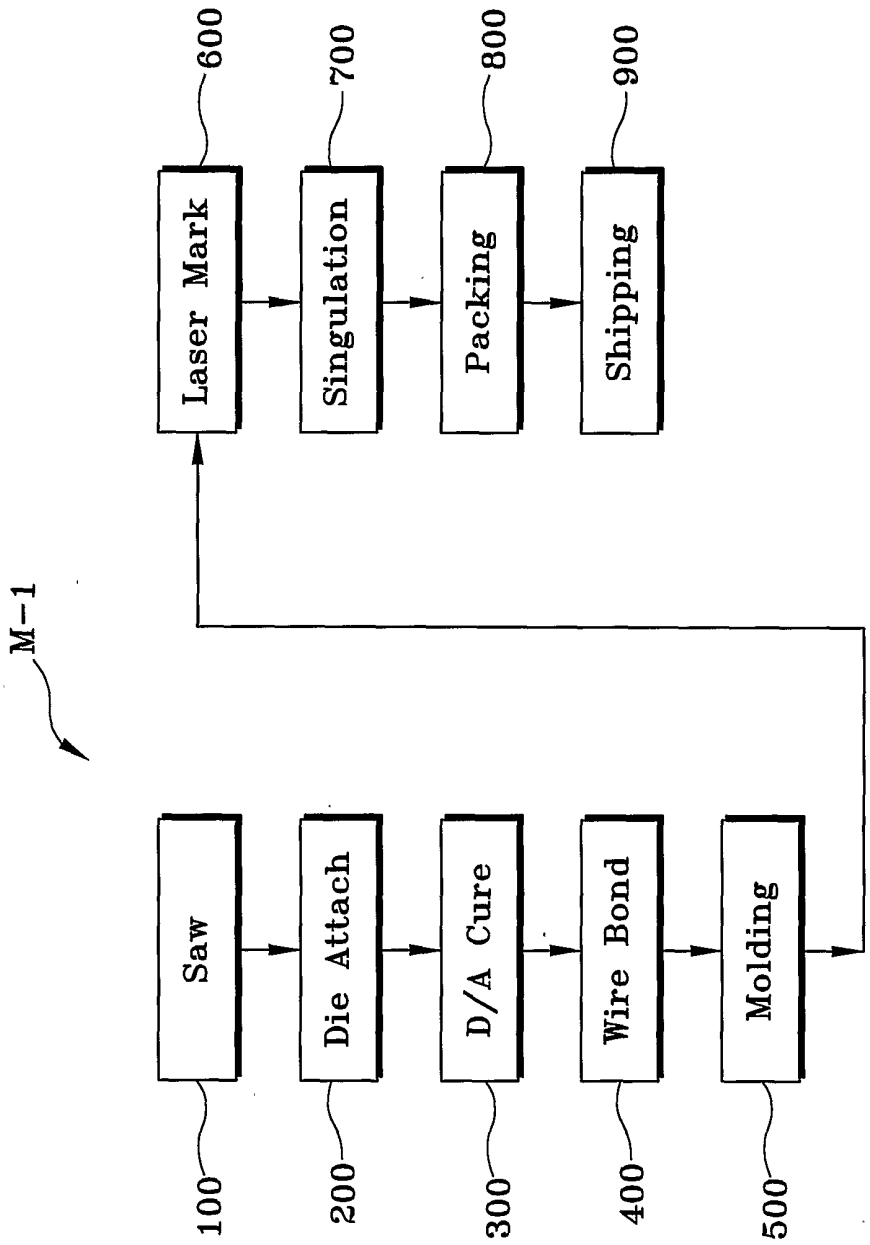

M-1
Saw
Die Attach
D/A Cure
Wire Bond
Molding
Laser Mark
Singulation
Packing
Shipping
100
200
300
400
500
600
700
800
900

Figure 4

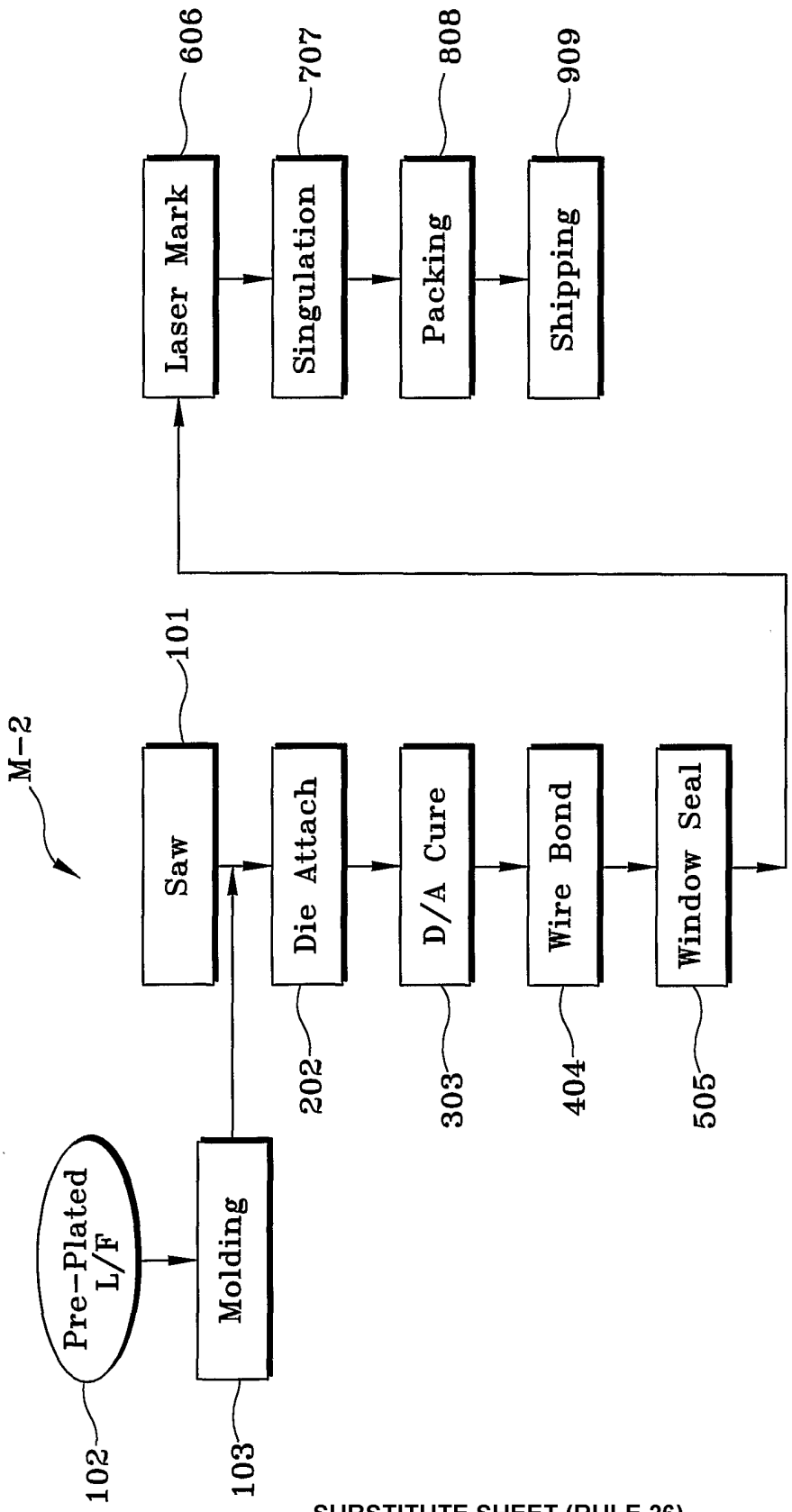

M-2
Pre-Plated L/F
Molding
Saw
Die Attach
D/A Cure
Wire Bond
Window Seal
Laser Mark
Singulation
Packing
Shipping
101
102
103
202
303
404
505
606
707
808
909

Figure 5