METHODS, SYSTEMS AND STRUCTURES FOR FORMING SEMICONDUCTOR STRUCTURES INCORPORATING HIGH-TEMPERATURE PROCESSING STEPS

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METHODS, SYSTEMS AND STRUCTURES FOR FORMING SEMICONDUCTOR STRUCTURES INCORPORATING HIGH-TEMPERATURE PROCESSING STEPS

A method (100) of forming semiconductor structures (202) including high-temperature processing steps (step 118), incorporates the use of a high-temperature nitride-oxide mask (220) over protected regions (214) of the device (202). The invention has application in many different embodiments, including but not limited to, the formation of recess, strained device regions (224).

6 Claims, 3 Drawing Sheets

NMOS REGION

PMOS REGION
100

104 WELL FORMATION, ISOLATION PROCESSING

106 FORM GATE OXIDE LAYER

108 FORM GATE ELECTRODE

110 FORM CAP OXIDE AND OFFSET SPACER

112 FORM NITRIDE-OXIDE MASK

114 REMOVE NITRIDE-OXIDE MASK FROM SELECTED REGIONS

116 REMOVE CONVENTIONAL PHOTORESIST

118 PERFORM HIGH-TEMPERATURE PROCESSING STEPS

FIG. 1
METHODS, SYSTEMS AND STRUCTURES
FOR FORMING SEMICONDUCTOR
STRUCTURES INCORPORATING
HIGH-TEMPERATURE PROCESSING STEPS

This is a divisional application of Ser. No. 11/046,141 filed

FIELD OF INVENTION

The present invention relates generally to semiconductor
devices and more particularly to methods, structures and sys-
tems for performing high temperature processing in the for-
mation of semiconductor devices where there are processing
differences between the n and p versions of the device.

BACKGROUND OF THE INVENTION

A conventional field effect transistor (FET), also known as
a metal oxide semiconductor (MOS) transistor, generally
includes a semiconductor substrate, such as silicon, having a
source, a drain, and a channel positioned between the source
and drain. A gate stack composed of a conductive material (a
gate conductor), an oxide layer (a gate oxide), and sidewall
spacers, is typically located above the channel. The gate oxide
is typically located directly above the channel, while the gate
conductor, generally comprised of polycrystalline silicon
(poly-silicon) material, is located above the gate oxide. The
sidewall spacers protect the sidewalls of the gate conductor.

The formation of semiconductor devices, including field
effect transistors, often requires high temperature processing
steps. For example, for a given electric field across the chan-
nel of a MOS transistor, the amount of current that flows
through the channel is directly proportional to a mobility of
carriers in the channel. Thus the higher the mobility of the
carriers in the channel, the more current can flow and the
faster a circuit can perform. One way to increase the mobility
of the carriers in the channel of an MOS transistor is to pro-
cede a mechanical stress in the channel. However, the for-
mation of a strained channel typically requires a high
temperature processing step sufficient to destroy a con-
tventional photoresist mask.

Another example of a high temperature processing step is
the formation of a layer that is deposited on top of the poly
silicon, known as a poly cap, in the formation of semicon-
ductor devices. While desirable from a standpoint of device per-
formance, the temperatures needed to form a poly cap are
sufficient to destroy conventional photoresist masks.

It would be advantageous to provide methods and systems
facilitating the performance of high-temperature processing
steps in the manufacture of semiconductor devices.

SUMMARY OF THE INVENTION

New and improved methods and systems are provided for
using nitride and nitride-oxide layers to facilitate the perfor-
mance of high-temperature processing steps in the manufac-
ure of semiconductor devices.

When differential processing is required for the N and P
types of a CMOS device, photoresists have traditionally been
used to mask the regions which need to be kept from the pro-
cessing step. This works well for low temperature pro-
cesses such as the implants, etches and cleans. However, as
noted above, high temperature processing can destroy photo-
resist masks. The present inventors have thus recognized a
need for a film that can protect unprocessed areas of the
semiconductor device during high-temperature steps. The
invention uses an oxide or a nitride or a combination thereof
to accomplish this task. Conventional photoresist is used to
remove the film from the regions where the processing can
take place while, in accordance with the present invention, the
other regions of the high-temperature masking layer remains
to protect the underlying silicon layer from being processed.

In accordance with one aspect of the present invention
there is provided a process of forming a semiconductor struc-
ture, comprising: providing a semiconductor substrate; form-
ing a masking layer of a high-temperature masking material
conformally over the semiconductor substrate; patterning,
using a photoresist mask, portions of the masking layer to
selectively leave portions of the masking layer over portions
of the semiconductor substrate; and performing a high-tem-
perature processing step using the remaining portions of the
masking layer to protect underlying regions of the semi-
conductor substrate.

In accordance with another aspect of the present invention
there is provided a process of, forming a field effect transistor
device, comprising: providing a semiconductor substrate
having at least one NMOS and at least one PMOS device
region; forming a masking layer of a high-temperature
masking material conformally over the semiconductor sub-
strate; patterning, using a photoresist mask, portions of the
masking layer to selectively removing the portions of the
masking layer over at least one of the NMOS and PMOS device
regions; removing the photoresist mask; and performing at
least one high-temperature processing step over the exposed
device region using the remaining portion of the masking
layer to protect the unexposed device region.

In accordance with yet another aspect of the present inven-
tion, there is provided a semiconductor device structure
developed in the formation of a field effect transistor device,
comprising: a semiconductor substrate having at least one
NMOS and at least one PMOS device region; a masking layer
or of a high-temperature masking material conformally over
the semiconductor substrate; a photoresist mask positioned to
selectively removing portions of the masking layer over at least
one of the NMOS and PMOS device regions; and means for
performing at least one high-temperature processing step
over the exposed device region using the remaining portion of
the masking layer to protect the unexposed device region.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other objects, features and advantages of the
invention will be apparent from a consideration of the follow-
ing detailed description of the invention when read in con-
junction with the drawing Figures, in which:

FIG. 1 is a flow chart illustrating a method of performing a
high temperature processing step in the fabrication of a semi-
conductor device in accordance with one aspect of the present
invention; and

FIGS. 2A-F are fragmentary cross-sectional diagrams illus-
trating various steps of forming semiconductor device
structures in accordance with the process of FIG. 1.

DETAILED DESCRIPTION OF THE INVENTION

One or more implementations of the present invention will
now be described with reference to the attached drawings,
wherein like reference numerals are used to refer to like
elements throughout, and wherein the illustrated structures
are not necessarily drawn to scale. The invention facilitates
the manufacture of transistor structures requiring high-temp
erature processing steps.
Referring now to FIGS. 1 and 2A-2F, further aspects of the invention relate to methods of fabricating integrated circuits, wherein FIG. 1 illustrates an exemplary method 100 in accordance with the invention, and FIGS. 2A-2F illustrate an exemplary transistor device at various stages of fabrication in accordance with the invention. While the exemplary method 100 is illustrated and described below as a series of acts or events, it will be appreciated that the present invention is not limited by the illustrated ordering of such acts or events. For example, some acts may occur in different orders and/or concurrently with other acts or events apart from those illustrated and/or described herein, in accordance with the invention. In addition, not all illustrated steps may be required to implement a methodology in accordance with the present invention. Furthermore, the methods according to the present invention may be implemented in association with the fabrication of ICs and composite transistors illustrated and described herein, as well as in association with other transistors and structures not illustrated.

The method 100 begins at step 104 with transistor well formation and isolation processing performed in preparation for the manufacture of a CMOS integrated circuit. Act 104 thus defines NMOS and PMOS regions, wherein NMOS regions comprise a P-well in which n-type source/drain regions will later be formed, and PMOS regions comprise an N-well in which p-type source/drain regions will later be formed, respectively. In addition, isolation regions may comprise shallow trench isolation (STI) or field oxide regions (LOCOS) and/or other isolation structures that serve to define various active areas and electrically isolate various active areas from one another. The corresponding structure is shown in FIG. 2A, wherein a transistor device 202 is provided, including a semiconductor body 204, such as a substrate, having a number of wells formed therein, such as a P-well 206 to define an NMOS transistor device region and an N-well 208 to define a PMOS transistor device region, respectively. Further, isolation regions 210 such as STI regions are formed in the semiconductor body to define active area regions 211.

The method 100 continues at 106, wherein a gate oxide layer is formed in active areas defined by the various formed isolation regions. In one example, the gate oxide comprises a thin, thermally grown silicon dioxide layer, however, other types of gate dielectrics (such as high-k dielectrics) may be formed and are contemplated by the present invention. A conductive gate layer is then deposited over the gate oxide at 108 and patterned to form a conductive gate electrode. For example, a polysilicon layer may be deposited via chemical vapor deposition (CVD) and patterned via etching to form gate electrodes in both NMOS and PMOS regions, respectively.

In FIG. 2B, the transistor device 202 is illustrated, wherein a gate oxide 212 has been formed, for example, thermally grown SiO₂, over the active areas 211. A patterned polysilicon gate 214 is shown positioned centrally over each of the PMOS and CMOS regions, overlying the upper surface of oxide layer 212.

A cap layer is formed conformally over the device, and an offset spacer is then formed on the lateral edges of the conductive gate electrodes at step 110 of FIG. 1. For example, a thin offset layer (e.g., an oxide or nitride layer) is formed generally conformally over the patterned gate and then etched using a generally anisotropic dry etch to remove offset layer material on top of the gate and in the source/drain regions, leaving a thin offset spacer material on lateral edges of the gate.
While the invention has been illustrated and described with respect to one or more embodiments, numerous alterations and/or modifications may be made to the illustrated examples without departing from the spirit and scope of the appended claims.

What is claimed is:

1. A semiconductor device structure developed in the formation of a field effect transistor device, comprising:
   a semiconductor substrate having at least one NMOS and at least one PMOS device region;
   a masking layer or of a high-temperature masking material conformally over the semiconductor substrate;
   a photoresist mask positioned to selectively removing portions of the masking layer over least one of the NMOS and PMOS device regions; and
   means for performing at least one high-temperature processing step over the exposed device region using the remaining portion of the masking layer to protect the unexposed device region.

2. The device of claim 1 wherein the masking layer is selected from the group comprising oxide, nitride and a combination of oxide and nitride.

3. The device of claim 1 wherein the high-temperature masking material is positioned to enable the formation of a film selected from the group including SiGe and SiC.

4. The device of claim 1 wherein the high-temperature masking material is positioned to enable a metal gate formation.

5. The device of claim 1 wherein the photoresist mask is further positioned to perform a doping implantation in at least one region of the field effect transistor.

6. The device of claim 1 wherein the photoresist mask the photoresist mask is further positioned to enable the formation of dual thickness gate oxides.

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