



- (51) **International Patent Classification:**
H01L 21/768 (2006.01) *H01L 21/31* (2006.01)
H01L 21/205 (2006.01)
- (21) **International Application Number:**
PCT/US2015/000428
- (22) **International Filing Date:**
24 December 2015 (24.12.2015)
- (25) **Filing Language:** English
- (26) **Publication Language:** English
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- (81) **Designated States** (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.
- (84) **Designated States** (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).
- Published:**
— with international search report (Art. 21(3))

(54) **Title:** METHODS OF FORMING LOW CAPACITANCE INTERCONNECT STRUCTURES UTILIZING LOW DIELECTRIC MATERIALS

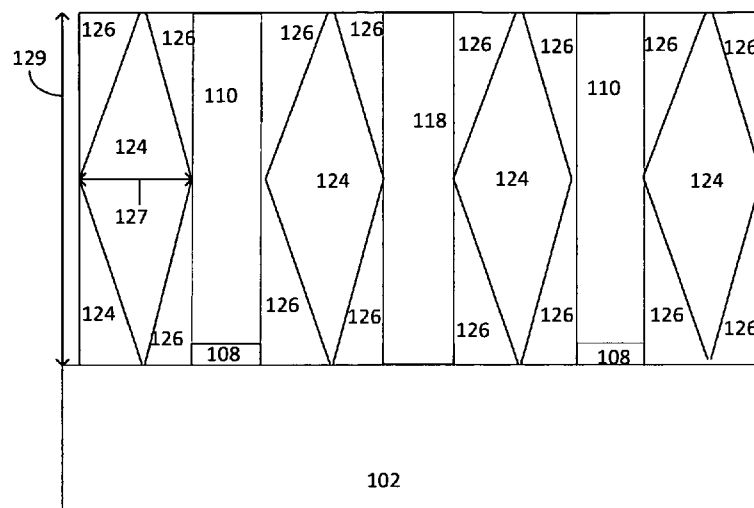


FIG. 1

(57) **Abstract:** Methods of lowering the capacitance of interconnect patterns comprising adjacent metal lines with differing metal compositions, are described. Those methods/structures may include providing a substrate comprising a first conductive interconnect structure comprising a first material, and a second interconnect structure comprising a second material, wherein the first and second conductive interconnect structures are disposed adjacent to one another on the substrate, forming an air gap disposed between the first and second conductive interconnect structures by utilizing a vapor phase etch process, and encapsulating the air gap with a low k dielectric material.



METHODS OF FORMING LOW CAPACITANCE INTERCONNECT STRUCTURES UTILIZING LOW DIELECTRIC MATERIALS

BACKGROUND OF THE INVENTION

Higher performance, lower cost, increased miniaturization of integrated circuit components are ongoing goals of the microelectronic industry for the fabrication of microelectronic devices. To achieve these goals, transistors within the microelectronic devices must scale down, i.e. become smaller. Along with the reduction in the size of transistors, there has also been a drive to improve their efficiency with improvement in their designs, materials used, and/or in their fabrication processes.

Interconnect structures may be incorporated into device/transistor structures, wherein the device may include one or more levels of metal lines that may be utilized as conductive interconnect structures within the device. An interlayer dielectric (ILD) may be placed between the metal lines, for example.

BRIEF DESCRIPTION OF THE DRAWINGS

While the specification concludes with claims particularly pointing out and distinctly claiming certain embodiments, the advantages of these embodiments can be more readily ascertained from the following description of the invention when read in conjunction with the accompanying drawings in which:

- FIGS. 1a-1m represent cross-sectional views of a structures according to embodiments.
- FIG. 2 represents a flow chart of a method according to embodiments.
- FIG.3 represents an interposer implementing one or more embodiments.
- FIG. 4 represents a schematic of a system according to embodiments.

DETAILED DESCRIPTION OF THE PRESENT INVENTION

In the following detailed description, reference is made to the accompanying drawings that show, by way of illustration, specific embodiments in which the methods and structures may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the embodiments. It is to be understood that the various embodiments, although different, are not necessarily mutually exclusive. For example, a particular feature, structure, or characteristic described herein, in connection with one embodiment, may be implemented within other embodiments without departing from the spirit and scope of the embodiments. In addition, it is to be understood that the location or arrangement of individual elements within each

disclosed embodiment may be modified without departing from the spirit and scope of the embodiments.

The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the embodiments is defined only by the appended claims, appropriately interpreted, along with the full range of equivalents to which the claims are entitled. In the drawings, like numerals may refer to the same or similar functionality throughout the several views. The terms “over”, “to”, “between” and “on” as used herein may refer to a relative position of one layer with respect to other layers. One layer “over” or “on” another layer or bonded “to” another layer may be directly in contact with the other layer or may have one or more intervening layers. One layer “between” layers may be directly in contact with the layers or may have one or more intervening layers. Layers and/or structures “adjacent” to one another may or may not have intervening structures/layers between them.

Implementations of the embodiments herein may be formed or carried out on a substrate, such as a semiconductor substrate. In one implementation, the semiconductor substrate may be a crystalline substrate formed using a bulk silicon or a silicon-on-insulator substructure. In other implementations, the semiconductor substrate may be formed using alternate materials, which may or may not be combined with silicon, that include but are not limited to germanium, indium antimonide, lead telluride, indium arsenide, indium phosphide, gallium arsenide, indium gallium arsenide, gallium antimonide, or other combinations of group III-V or group IV materials. Although a few examples of materials from which the substrate may be formed are described here, any material that may serve as a foundation upon which a semiconductor device may be built falls within the spirit and scope.

A plurality of transistors, such as metal-oxide-semiconductor field-effect transistors (MOSFET or simply MOS transistors), may be fabricated on the substrate. In various implementations, the MOS transistors may be planar transistors, nonplanar transistors, or a combination of both. Nonplanar transistors include FinFET transistors such as double-gate transistors and tri-gate transistors, TFET and wrap-around or all-around gate transistors such as nanoribbon and nanowire transistors.

Each transistor may include a gate stack formed of at least two layers, for example, a gate dielectric layer and a gate electrode layer. The gate dielectric layer may include one layer or a stack of layers. The one or more layers may include silicon oxide, silicon dioxide (SiO₂) and/or a high-k dielectric material. The high-k dielectric material may include elements such as hafnium, silicon, oxygen, titanium, tantalum, lanthanum, aluminum, zirconium, barium, strontium, yttrium, lead, scandium, niobium, and zinc.

The gate electrode layer may be formed on the gate dielectric layer and may consist of at least one P-type workfunction metal or N-type workfunction metal, depending on whether the transistor is to be a PMOS or an NMOS transistor. In some implementations, the gate electrode layer may consist of a stack of two or more metal layers, where one or more metal layers are
5 workfunction metal layers and at least one metal layer is a fill metal layer.

Source and drain regions may be formed within the substrate adjacent to the gate stack of each MOS transistor. The source and drain regions are generally formed using either an implantation/diffusion process or an etching/deposition process. In the former process, dopants such as boron, aluminum, antimony, phosphorous, or arsenic may be ion-implanted into the
10 substrate to form the source and drain regions. An annealing process that activates the dopants and causes them to diffuse further into the substrate typically follows the ion implantation process. Source/drain may comprise a source or a drain structure/region, depending upon the particular implementation within the device, in an embodiment.

One or more interlayer dielectrics (ILD) are deposited over/within the MOS transistor
15 structures. The ILD layers may be formed using dielectric materials known for their applicability in integrated circuit structures, such as low-k dielectric materials. Examples of dielectric materials that may be used include, but are not limited to, silicon dioxide (SiO₂), carbon doped oxide (CDO), silicon nitride, organic polymers such as perfluorocyclobutane or polytetrafluoroethylene, fluorosilicate glass (FSG), and organosilicates such as silsesquioxane,
20 siloxane, or organosilicate glass. The ILD layers may include pores or air gaps to further reduce their dielectric constant.

Conductive Interconnect structures, such as metal lines that may interconnect components within transistor structures, for example, may be disposed within and/or on the ILD, in some embodiments. For example, lower level (i.e. metal levels/layers that are closest to a
25 device region, such as gate, source/drain regions) metal/conductive interconnect structures, may comprise metal structures adjacent one another that comprise different metal compositions. For example, source/drain contact metals structures may comprise a different metal composition than gate contact metal compositions. These adjacent metal structures may comprise dielectric material, such as high k ILD materials, between them. The high k dielectric materials may
30 contribute to higher capacitance coupling between the adjacent conductive interconnect structures.

Embodiments of methods of forming microelectronic device structures, such as methods of lowering the capacitance of interconnect patterns comprising adjacent metal lines with differing metal compositions, are described. Those methods/structures may include providing a substrate comprising a first conductive interconnect structure comprising a first material, and a

second interconnect structure comprising a second material, wherein the first and second conductive interconnect structures are disposed adjacent to one another on the substrate, forming an air gap disposed between the first and second conductive interconnect structures by utilizing a vapor phase etch process, and encapsulating the air gap with a low k dielectric material. The embodiments herein significantly reduce capacitance of metal lines in multi-level metallization devices, in embodiments.

FIGS. 1a-1m illustrate side cross-sectional views of embodiments of fabricating low capacitance interconnect structures in microelectronic devices. In FIG. 1a, a portion of device 100, such as a non-planar transistor device 100, may comprise a substrate 102, such as a silicon substrate or a silicon on insulator substrate 102, for example. In an embodiment, the substrate
5 may comprise a portion of a transistor device, such as gate and source/drain regions (not shown). A sacrificial structure 104 may be formed/disposed on the substrate 102. The sacrificial structure 104 may comprise polysilicon, in an embodiment. An etch stop/hard mask material 106, such as a dielectric, such as silicon nitride, may be disposed on a top surface of the sacrificial structure 104. In an embodiment, a distance (pitch) between adjacent sacrificial structures 104 is
10 less than about 80 nm. In one embodiment, the pitch is from about 10 nanometers (nm) to about 80 nm.

A spacer material 108 may be formed on the sacrificial structure 104 (FIG. 1b). The spacer material 106 may comprise a dielectric material, such as an oxide material, a carbide, a nitride, for example, and may line the surfaces of the sacrificial structure 104. In an embodiment,
15 the spacer material may comprise a high k dielectric material, and may comprise a thickness below about 10 nm, for example. Openings 105 may be adjacent the sacrificial structures 104. In an embodiment, a first conductive material 110, which may comprise a portion of a first conductive interconnect structure 110, such as metal interconnect lines/structures in a microelectronic device, may be formed in the openings 105 (FIG. 1c). In an embodiment, the
20 first conductive material 110 may comprise such materials as copper, ruthenium, nickel, cobalt, chromium, iron, manganese, titanium, aluminum, hafnium, tantalum, tungsten, Vanadium, Molybdenum, palladium, gold, silver, platinum, tin, lead, metal alloys, metal carbides, e.g., hafnium carbide, zirconium carbide, titanium carbide, tantalum carbide, aluminum carbide, other conductive materials, or any combination thereof.

25 In alternative embodiments, examples of the first conductive material 110 may comprise, but is not limited to, metals, e.g., copper, tantalum, tungsten, ruthenium, titanium, hafnium, zirconium, aluminum, silver, tin, lead, metal alloys, metal carbides, e.g., hafnium carbide, zirconium carbide, titanium carbide, tantalum carbide, aluminum carbide, other

conductive materials, or any combination thereof. In one embodiment, a width of the first conductive material/interconnect structure is less than about 40 nm. In one embodiment, a width of the first conductive material/interconnect structure 110 may comprise an approximate range of about 5 nm to about 40 nm. In one embodiment, a height of the first conductive structure may
5 comprise less than about 65 nm. In one embodiment, a height of the first conductive material/structure may comprise about 8 nm to about 65 nm.

In an embodiment, a seed layer (not shown) may be formed in the opening 105 prior to the formation of the first conductive structure 110. In an embodiment, the seed layer may comprise copper, titanium nitride, ruthenium, nickel, cobalt, tungsten, or any combination
10 thereof. In an embodiment, the first conductive structure 110 may further comprise a conductive barrier layer, such as aluminum, titanium, titanium nitride, tantalum, tantalum nitride, tungsten, cobalt, ruthenium, the like metals, or any combination thereof. In an embodiment, any of the conductive, seed layers and/or barrier layers may be formed utilizing such formation processes as chemical vapor deposition ("CVD"), plasma enhanced chemical vapor deposition
15 ("PECVD"), physical vapor deposition ("PVD"), molecular beam epitaxy ("MBE"), metalorganic chemical vapor deposition ("MOCVD"), atomic layer deposition ("ALD"), or any other suitable deposition techniques.

In an embodiment, a polishing process, such as chemical mechanical processing (CMP) 112 may be performed, wherein a portion of a top surface of the first conductive interconnect
20 structure 110 may be removed, and a portion of a top surface of the etch stop material 106 may be removed (FIG. 1d). In an embodiment, a top surface of the first conductive structure 110 and a top surface of the etch stop material 106 may be co-planar with each other. In an embodiment, the sacrificial material 104 and the etch stop material 106 may be removed from the substrate 102 by utilizing any suitable etch process 114, such as a dry and/or a wet etch process, to form
25 an opening 109 (FIG. 1e). A second conductive interconnect structure 118 may be formed utilizing any suitable formation process 116. The second conductive interconnect structure may be formed with any of the previously listed materials as described for the first conductive structure 110 material composition, but the first conductive structure 110 may comprise different material/s than the second conductive material/s 118 (FIG. 1f).

30 In an embodiment, the first conductive material 110 may comprise a first material, and the second conductive structure may comprise a second material 118. In an embodiment, the first and second conductive structures 110, 118 may comprise an aspect ratio (height: width) of greater than 3:1. A vapor phase chemical etch process 120 may be performed (FIG. 1g), wherein

the spacer material 108 is removed from between the first and second conductive interconnect structures 110, 118, and wherein air gaps 124 may be formed between the first and second conductive interconnect structures 110, 118. In an embodiment, etch rates of the conductive structures 110, 118 may be substantially zero, and an etch rate of the spacer 108 material may be high compared to the conductive materials 110, 118. In an embodiment, the etch selectivity between two materials may be defined as the ratio between their etching rates at similar etching conditions. In one embodiment, the ratio between the etching rate of the conductive structures 110, 118 to the etching rate of the spacer material 108 may comprise at least 8:1. The vapor phase chemical etch 120 composition/parameters may comprise NF₃, HF, F₂, H₂O or mixtures thereof, at varying temperatures, flows, and pressures. In an embodiment, the vapor phase chemical etch may comprise a vapor based isotropic etch that is selective to multiple metals in a particular conductive interconnect film stack, such as a seed layer, barrier layer, that may be associated with the conductive interconnect structures 110, 118. In some embodiment, a wet etch, which may comprise a HF wet etch for example, in an embodiment, may be performed, either instead of the vapor phase chemical etch, or in combination with the vapor phase chemical etch.

The vapor phase chemical etch process 120 may comprise a controlled etch, wherein the vapor phase chemical etch comprises little to no over-etch, in comparison with wet or dry etches, which typically comprise a greater level of over-etch.

The air gaps 124 may be disposed between the first and second conductive interconnect structures 110, 118. In an embodiment, the air gaps 124 may be sealed/encapsulated with a non-conformal film 126, by utilizing an encapsulating process 122, such as a PECVD process, however other suitable types of processes may be employed, according to the particular application, in an embodiment (FIG. 1h). In an embodiment, the non-conformal film 126 may comprise a dielectric film, such as a low k dielectric film. In an embodiment, the non-conformal film 126 may surround the air gap 124. In an embodiment, the non-conformal film 126 may comprise a PECVD ILD deposition, wherein the non-conformal film may trap the air-gap (which may comprise various shapes) during the deposition, since the aspect ratio of the conductive interconnect structures 110, 118 are greater than 3:1 (height:width).

In FIG. 1i, the first and second conductive interconnect structures 110, 118 may comprise etch stop/hard masks 123, 125 on their respective top surfaces, and a high k material 121, such as a high k ILD material, may be disposed between the conductive interconnect structures 110, 118. The etch stops 123, 125 may comprise different materials from each other, and may comprise a height of between about 5 to about 20 nm, in various embodiments. The first

and second conductive structures 110, 118 may comprise different compositions from each other as well. In an embodiment, the etch stop materials 123, 125 may include silicon nitride, silicon carbide, an oxide layer, e.g., a silicon oxide layer, a carbon doped oxide layer, e.g., a carbon doped silicon oxide layer, a silicon oxy carbide (SiOC) layer, a fluorine-doped silicon oxide, a metal oxide, e.g., a titanium oxide, an aluminum oxide, a hafnium oxide, or any other metal oxide; a hydrogensilsequioxane (HSQ), a fluorinated amorphous carbon, a methylsequioxane (MSQ), a nitride layer, e.g., a silicon nitride, a titanium nitride, a silicon oxide nitride, silicon carbide, or other etch stop layer. In another embodiment, the etch stop materials may include metallic nanoparticles, such as hafnium, zirconium, other metallic nanoparticle, or a combination thereof) and/or metal oxides, e.g., hafnium oxide, zirconium oxide, other metal oxide, or any combination thereof.

In an embodiment, the first conductive structure 110 may comprise a portion of a source/drain contact structure, and may comprise a source/drain contact 132 material that may be in direct, or in other embodiments, not directly, in contact with a source/drain region 134 of the substrate 102. The second conductive structure 118 may comprise a portion of a gate contact structure, and may be adjacent a gate region 135 of the substrate 102. In an embodiment, the gate structure may comprise gate spacers adjacent the gate structure, wherein the gate spacer material may comprise a different composition, than the encapsulating material subsequently formed. In an embodiment, a pitch may comprise less than about 80 nm between the first and second interconnect structures 110, 118. A vapor phase chemical etch process 120 may be performed, wherein the etch stops 123, 125 may be removed, and the high k material 121 may be removed from between the conductive interconnect structures 110, 118. Air gaps 124 may be formed between the conductive interconnect structures 110, 118 (FIG. 1j).

In an embodiment, the etch rates of the conductive structures 110, 118 may be substantially zero, and the etch rate of the high k material 121 may be high compared to the conductive materials of the conductive structures 110, 118. In some embodiments, the etch rate of the high k material 121 may be greater than 8 times the etch rate of the conductive structures 110, 118. In another embodiment, the etch stops may be polished by a polishing process, such as by a chemical mechanical processing process (CMP), prior to performing the vapor phase chemical etch process 120, in order to reduce etch times. In an embodiment, the air gaps 124 may be sealed by an encapsulating material 126 during an encapsulating process 122 (FIG. 1k). In an embodiment, the encapsulating material 126 may be similar to the encapsulating material 126 of (FIG. 1h).

In FIG. 11, the air gaps have a keyhole structure, wherein a width 127 of the air gap may vary along a height 129 of the air gap 124, and wherein the encapsulating material 126 may surround at least a portion of the air gap 124. In another embodiment, the encapsulating material may completely seal the air gap, and may comprise an hermetic seal. In an embodiment, the air gap may comprise a void, where there is no solid material, and may comprise air, and other gases. In FIG. 1m, a process 140 may be employed wherein the air gaps 124, such as the air gaps 124 in FIG. 1j, for example, may be filled by a low k dielectric 142. In an embodiment, the low k dielectric 142 may be formed by a spin on glass process 140, and may be disposed between the conductive interconnect structures 110, 118.

The embodiments herein enable improved device performance by providing structures that serve to reduce capacitance coupling between adjacent metal lines, and thus improve speed and lower power consumption of the device. The embodiments herein may be applied to device structures with greater than two conductive interconnect structures adjacently disposed on a substrate. For example, any number of metal lines comprising different compositions may be disposed adjacently on a substrate, and may be separated by high k dielectric material, for example. The embodiments herein enable selective etching by a vapor phase chemical process, wherein the high k material may be removed between the conductive metal lines, and a low k material may be formed in between the lines, with or without an encapsulated air-gap, in embodiments.

FIG. 2 depicts a method according to embodiments herein. At step 202, a substrate may be provided comprising a first conductive interconnect structure comprising a first material, and a second interconnect structure comprising a second material, wherein the first and second conductive interconnect structures are disposed adjacent to one another on the substrate. At step 204, an air gap may be formed disposed between the first and second conductive interconnect structures by utilizing a vapor phase etch process. At step 206, the air gap may be encapsulated with a low k dielectric material.

The structures of the embodiments herein may be coupled with any suitable type of structures capable of providing electrical communications between a microelectronic device, such as a die, disposed in package structures, and a next-level component to which the package structures may be coupled (e.g., a circuit board).

The device structures, and the components thereof, of the embodiments herein may comprise circuitry elements such as logic circuitry for use in a processor die, for example. Metallization layers and insulating material may be included in the structures herein, as well as

conductive contacts/bumps that may couple metal layers/interconnects to external devices/layers. The structures/devices described in the various figures herein may comprise portions of a silicon logic die or a memory die, for example, or any type of suitable microelectronic device/die. In some embodiments the devices may further comprise a plurality of dies, which may be stacked
 5 upon one another, depending upon the particular embodiment. In an embodiment, the die(s) may be partially or fully embedded in a package structure.

The various embodiments of the device structures included herein may be used for system on a chip (SOC) products, and may find application in such devices as smart phones, notebooks, tablets, wearable devices and other electronic mobile devices. In various
 10 implementations, the package structures may be included in a laptop, a netbook, a notebook, an ultrabook, a smartphone, a tablet, a personal digital assistant (PDA), an ultra-mobile PC, a mobile phone, a desktop computer, a server, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a digital camera, a portable music player, or a digital video recorder, and wearable devices. In further implementations, the package devices herein may be included in
 15 any other electronic devices that process data.

FIG. 3 illustrates a device 300 that includes one or more embodiments included herein. The device 300 may include interposer 301, which may comprise an intervening substrate used to bridge a first substrate 302 to a second substrate 304. The first substrate 302 may be, for instance, any type of integrated circuit die, and may include embodiments of the nanowire spacer
 20 structures described herein, and may comprise a memory device, in an embodiment. The second substrate 304 may be, for instance, a memory module, a computer motherboard, a processor device, or any other integrated circuit die, and may include embodiments of the low capacitance interconnect structures described herein. Generally, the purpose of an interposer 301 is to spread a connection to a wider pitch or to reroute a connection to a different connection.

For example, an interposer 301 may couple an integrated circuit die to a ball grid array (BGA) 306 that can subsequently be coupled to the second substrate 304. In some embodiments, the first and second substrates 302/304 are attached to opposing sides of the interposer 301. In other embodiments, the first and second substrates 302/304 are attached to the same side of the interposer 301. And in further embodiments, three or more substrates are interconnected by way
 25 of the interposer 301.
 30

The interposer 301 may be formed of an epoxy resin, a fiberglass-reinforced epoxy resin, a ceramic material, or a polymer material such as polyimide. In further implementations, the interposer may be formed of alternate rigid or flexible materials that may include the same materials described above for use in a semiconductor substrate, such as silicon, germanium, and

other group III-V and group IV materials. The interposer may include metal interconnects 308 and vias 310, and may also include through-silicon vias (TSVs) 312. The interposer 301 may further include embedded devices 314, including both passive and active devices. Such devices include, but are not limited to, capacitors, decoupling capacitors, resistors, inductors, fuses, diodes, transformers, sensors, and electrostatic discharge (ESD) devices. More complex devices such as radio-frequency (RF) devices, power amplifiers, power management devices, antennas, arrays, sensors, and MEMS devices may also be formed on the interposer 301. In accordance with embodiments, apparatuses or processes disclosed herein may be used in the fabrication of interposer 301.

FIG. 4 is a schematic of a computing device 400 that may be implemented incorporating embodiments of the device structures described herein. In an embodiment, the computing device 400 houses a board 402, such as a motherboard 402 for example. The board 402 may include a number of components, including but not limited to a processor 404, and an on-die memory 406, that may be communicatively coupled with an integrated circuit die 403, and at least one communication chip 408. The processor 404 may be physically and electrically coupled to the board 402. In some implementations the at least one communication chip 408 may be physically and electrically coupled to the board 402. In further implementations, the communication chip 406 is part of the processor 404.

Depending on its applications, computing device 400 may include other components that may or may not be physically and electrically coupled to the board 402, and may or may not be communicatively coupled to each other. These other components include, but are not limited to, volatile memory (e.g., DRAM) 410, non-volatile memory (e.g., ROM) 412, flash memory (not shown), a graphics processor unit (GPU) 414, a digital signal processor (DSP) 416, a crypto processor 442, a chipset 420, an antenna 422, a display 424 such as a touchscreen display, a touchscreen controller 426, a battery 428, an audio codec (not shown), a video codec (not shown), a global positioning system (GPS) device 429, a compass 430, accelerometer, a gyroscope and other inertial sensors 432, a speaker 434, a camera 436, various input devices 438 and a mass storage device (such as hard disk drive, or solid state drive) 440, compact disk (CD) (not shown), digital versatile disk (DVD) (not shown), and so forth). These components may be connected to the system board 402, mounted to the system board, or combined with any of the other components.

The communication chip 408 enables wireless and/or wired communications for the transfer of data to and from the computing device 400. The term “wireless” and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic

radiation through a non-solid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not. The communication chip 408 may implement any of a number of wireless or wired standards or protocols, including but not limited to Wi-Fi (IEEE 802.11 family), WiMAX (IEEE 802.16 family), IEEE 802.20, long term evolution (LTE), Ev-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Bluetooth, Ethernet derivatives thereof, as well as any other wireless and wired protocols that are designated as 3G, 4G, 5G, and beyond. The computing device 400 may include a plurality of communication chips 408. For instance, a first communication chip may be dedicated to shorter range wireless communications such as Wi-Fi and Bluetooth and a second communication chip may be dedicated to longer range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, Ev-DO, and others. The term "processor" may refer to any device or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory.

In various implementations, the computing device 400 may be a laptop, a netbook, a notebook, an ultrabook, a smartphone, a tablet, a personal digital assistant (PDA), an ultra mobile PC, a wearable device, a mobile phone, a desktop computer, a server, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a digital camera, a portable music player, or a digital video recorder. In further implementations, the computing device 400 may be any other electronic device that processes data.

Embodiments of the transistor/interconnect structures described herein may be implemented as a part of one or more memory chips, controllers, CPUs (Central Processing Unit), microchips or integrated circuits interconnected using a motherboard, an application specific integrated circuit (ASIC), and/or a field programmable gate array (FPGA).

25

EXAMPLES

Example 1 is a microelectronic structure comprising a substrate comprising silicon, a first conductive interconnect structure, comprising a first material on the substrate, a second interconnect structure comprising a second material on the substrate, wherein the first and second conductive interconnect structures are adjacent each other on the substrate, an air gap disposed between the first and second conductive interconnect structures, and an encapsulating material disposed on and around the air gap, wherein the encapsulating material comprises a non-conformal material.

Example 2 includes the structure of example 1 wherein the non-conformal material comprises a low k dielectric material.

Example 3 includes the structure of example 1 wherein the non-conformal material comprises a dielectric layer, wherein the dielectric layer comprises a PECVD dielectric layer.

Example 4 includes the structure of example 1 wherein the non-conformal material comprises PECVD silicon dioxide.

5 Example 5 includes the structure of example 1 wherein the first conductive interconnect structure comprises a portion of a source/drain contact metal structure, and the second conductive interconnect structure comprises a portion of a gate contact metal structure.

Example 6 includes the structure of example 1 wherein the non-conformal dielectric surrounds at least a portion of the air gap.

10 Example 7 includes the structure of example 1 wherein the first conductive interconnect structure and the second conductive interconnect structure have a low etch rate in a vapor etchant comprising an etchant selected from the group consisting of NF₃, HF, F₂ and H₂O.

Example 8 includes the structure of example 1 wherein the air gap comprises a keyhole structure.

15 Example 9 is a device structure comprising, a substrate, a first conductive interconnect structure, comprising a first material, and a second conductive interconnect structure comprising a second material, wherein the first and second conductive interconnect structures are disposed adjacently on the substrate, and wherein a pitch between the first and second interconnect structures comprises less than about 80nm, and a low k material disposed between the first and
20 second interconnect structures.

Example 10 is the device structure of example 9 wherein the low k material comprises a spin on glass material.

Example 11 is the device structure of example 9 wherein the first conductive interconnect structure comprises a source/drain contact structure and the second conductive interconnect
25 structure comprises a gate contact structure.

Example 12 is the device structure of example 9 wherein the device comprises a portion of one of a NMOS or a PMOS transistor structure.

Example 13 is the device structure of example 9 wherein the device comprises a portion of one of a non-planar device, a gate all around device, or a nanowire device.

30 Example 14 is the device structure of example 9 wherein one of the first conductive interconnect structure comprises a gate contact structure, and wherein a gate structure adjacent the gate contact structure comprises a gate spacer.

Example 15 is the device structure of example 14 wherein the gate spacer is adjacent a portion of the low k material, and wherein the gate spacer comprises a different material than the
35 low k material.

Example 16 is the device structure of example 9, wherein the first conductive interconnect structure and the second conductive interconnect structure have a low etch rate in a vapor phase etchant comprising an etchant selected from the group consisting of NF₃, HF, F₂ and H₂O.

5 Example 17 is a method of forming a microelectronic structure, comprising:
providing a first conductive interconnect structure adjacent a second conductive interconnect structure on a substrate, wherein the first conductive interconnect structure comprises a first material and the second conductive interconnect structure comprises a second material, wherein the first and second materials are different from each other, and wherein a high
10 k material is disposed between the first and second conductive interconnect structures, a first etch stop on the first conductive structure, and a second etch stop on the second conductive structure, wherein the first and second etch stops comprise different materials from each other, etching the high k material between the first and second conductive structures with a vapor phase chemical etch process, wherein at least a portion of the first and second conductive materials
15 remain, and forming a low k material between the first and second conductive materials.

Example 18 includes the method of example 17 and further comprising wherein the etching is performed with a vapor phase etchant process, wherein the vapor phase etchant is selected from the group consisting of NF₃, HF, F₂ and H₂O.

20 Example 19 includes the method of example claim 18 and further comprising wherein the low k material is formed with a non-conformal PECVD process.

Example 20 includes the method of example 17 and further comprising forming the low k material with a non-conformal low k material process, wherein an air gap region between the first and second conductive interconnect structures is sealed.

25 Example 21 includes the method of example 20 and further comprises wherein the air gap comprises a keyhole structure.

Example 22 includes the method of example 17 and further comprising wherein the low k material is formed by using a spin on glass process.

30 Example 23 includes the method of example 22 further comprising wherein the first and second etch stop structures are substantially removed during the vapor phase chemical etch process.

Example 24 includes the method of example 17 further comprising wherein the structure comprises a portion of one of a FINFET, a tri-gate, a nanowire, or a nanoribbon transistor structure.

35 Example 25 includes the method of example 17 further comprising wherein the first and second etch stop structures comprise nanoparticles. Example 1 is a nanowire channel structure

comprising a first nanowire and a second nanowire; a source/drain structure adjacent the nanowire channel structure, wherein the source/drain structure comprises a liner adjacent a sidewall region of the source/drain structure, and wherein the liner is also adjacent at least one of the first and second nanowires, a nanowire spacer structure in between the first nanowire and the
5 second nanowire, wherein the nanowire spacer structure comprises a chemically converted portion of the liner material.

Although the foregoing description has specified certain steps and materials that may be used in the methods of the embodiments, those skilled in the art will appreciate that many modifications and substitutions may be made. Accordingly, it is intended that all such
10 modifications, alterations, substitutions and additions be considered to fall within the spirit and scope of the embodiments as defined by the appended claims. In addition, the Figures provided herein illustrate only portions of exemplary microelectronic devices and associated package structures that pertain to the practice of the embodiments. Thus the embodiments are not limited
15 to the structures described herein.

IN THE CLAIMS

What is claimed is:

1. A microelectronic structure comprising:
 - a substrate comprising silicon;
 - a first conductive interconnect structure, comprising a first material on the
5 substrate;
 - a second interconnect structure comprising a second material on the
substrate, wherein the first and second conductive interconnect structures are
adjacent each other on the substrate;
 - 10 an air gap disposed between the first and second conductive interconnect
structures; and
 - an encapsulating material disposed on and around the air gap, wherein the
encapsulating material comprises a non-conformal material.
2. The structure of claim 1 wherein the non-conformal material comprises a low k
dielectric material.
- 15 3. The structure of claim 1 wherein the non-conformal material comprises a
dielectric layer, wherein the dielectric layer comprises a PECVD dielectric layer.
4. The structure of claim 1 wherein the non-conformal material comprises PECVD
silicon dioxide.
- 20 5. The structure of claim 1 wherein the first conductive interconnect structure
comprises a portion of a source/drain contact metal structure, and the second conductive
interconnect structure comprises a portion of a gate contact metal structure.
6. The structure of claim 1 wherein the non-conformal dielectric surrounds at least a
portion of the air gap.
- 25 7. The structure of claim 1 wherein the first conductive interconnect structure and
the second conductive interconnect structure have a low etch rate in a vapor phase

etchant comprising an etchant selected from the group consisting of NF₃, HF, F₂ and H₂O.

8. The structure of claim 1 wherein the air gap comprises a keyhole structure.

9. A device structure comprising:

- 5 a substrate;
- a first conductive interconnect structure, comprising a first material, and a second conductive interconnect structure comprising a second material, wherein the first and second conductive interconnect structures are disposed adjacently on the substrate, and wherein a pitch between the first and second interconnect
- 10 structures comprises less than about 80nm; and
- a low k material disposed between the first and second interconnect structures.

10. The device structure of claim 9 wherein the low k material comprises a spin on glass material.

15 11. The device structure of claim 9 wherein the first conductive interconnect structure comprises a source/drain contact structure and the second conductive interconnect structure comprises a gate contact structure.

12. The device structure of claim 9 wherein the device comprises a portion of one of a NMOS or a PMOS transistor structure.

20 13. The device structure of claim 9 wherein the device comprises a portion of one of a non-planar device, a gate all around device, or a nanowire device.

14. The device structure of claim 9 wherein one of the first conductive interconnect structure comprises a gate contact structure, and wherein a gate structure adjacent the

25 gate contact structure comprises a gate spacer.

15. The device structure of claim 14 wherein the gate spacer is adjacent a portion of the low k material, and wherein the gate spacer comprises a different material than the low k material.

16. The device structure of claim 9, wherein the first conductive interconnect structure and the second conductive interconnect structure have a low etch rate in a vapor phase etchant comprising an etchant selected from the group consisting of NF₃, HF, F₂ and H₂O.

17. A method of forming a microelectronic structure, comprising:

providing a first conductive interconnect structure adjacent a second conductive interconnect structure on a substrate, wherein the first conductive interconnect structure comprises a first material and the second conductive interconnect structure comprises a second material, wherein the first and second materials are different from each other, and wherein a high k material is disposed between the first and second conductive interconnect structures;

a first etch stop on the first conductive structure, and a second etch stop on the second conductive structure, wherein the first and second etch stops comprise different materials from each other;

etching the high k material between the first and second conductive structures with a vapor phase chemical etch process, wherein at least a portion of the first and second conductive materials remain; and

forming a low k material between the first and second conductive materials.

18. The method of claim 17 further comprising wherein the etching is performed with a vapor phase etchant comprising an etchant selected from the group consisting of NF₃, HF, F₂ and H₂O.

19. The method of claim 18 further comprising wherein the low k material is formed with a non-conformal PECVD process.

20. The method of claim 17 further comprising forming the low k material with a non-conformal low k material process, wherein an air gap region between the first and second conductive interconnect structures is sealed.

5 21. The method of claim 20 further comprising wherein the air gap comprises a keyhole structure.

22. The method of claim 17 further comprising wherein the low k material is formed by using a spin on glass process.

10

23. The method of claim 22 further comprising wherein the first and second etch stop structures are substantially removed during the vapor phase chemical etch process.

15 24. The method of claim 17 further comprising wherein the structure comprises a portion of one of a FINFET, a tri-gate, a nanowire, or a nanoribbon transistor structure.

25. The method of claim 17 further comprising wherein the first and second etch stop structures comprise nanoparticles.

20

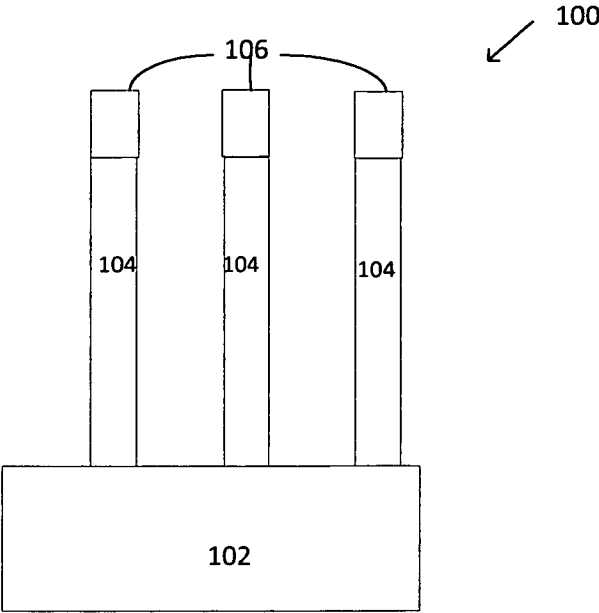


FIG. 1a

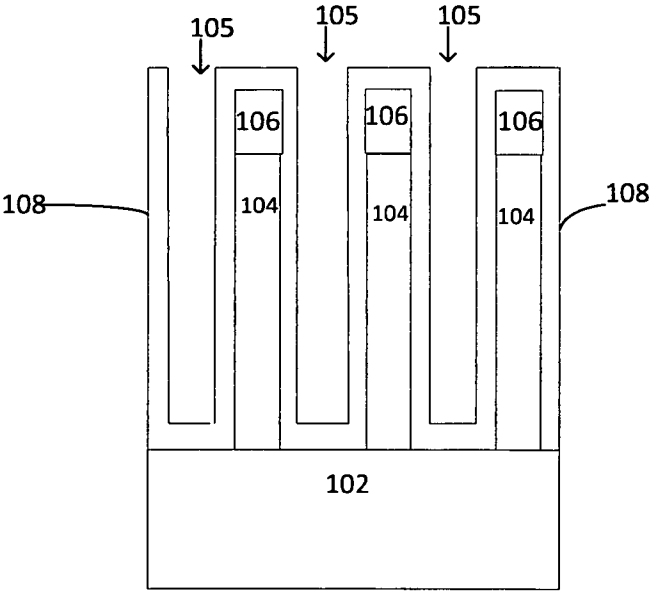


FIG. 1b

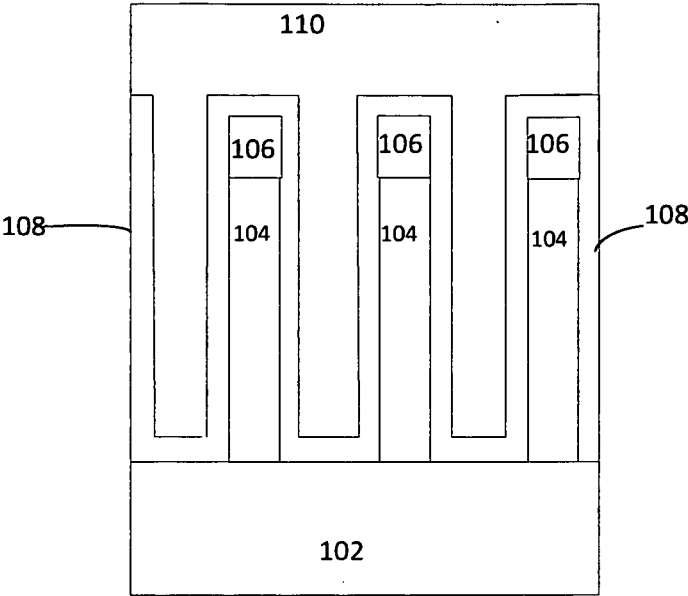


FIG. 1c

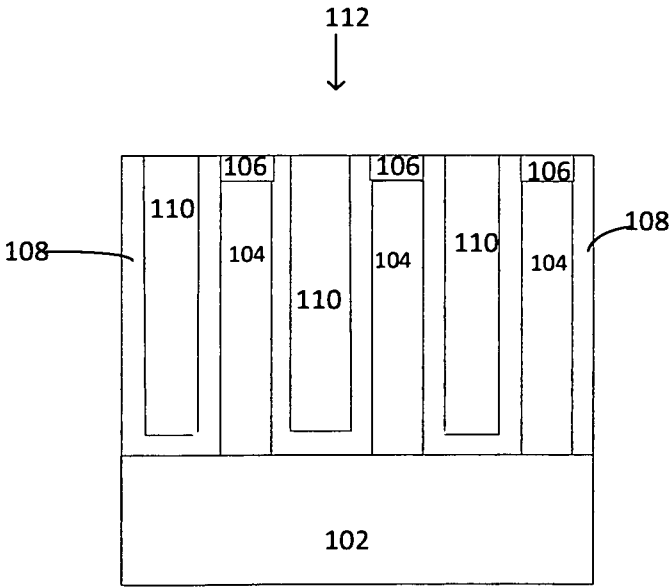


FIG. 1d

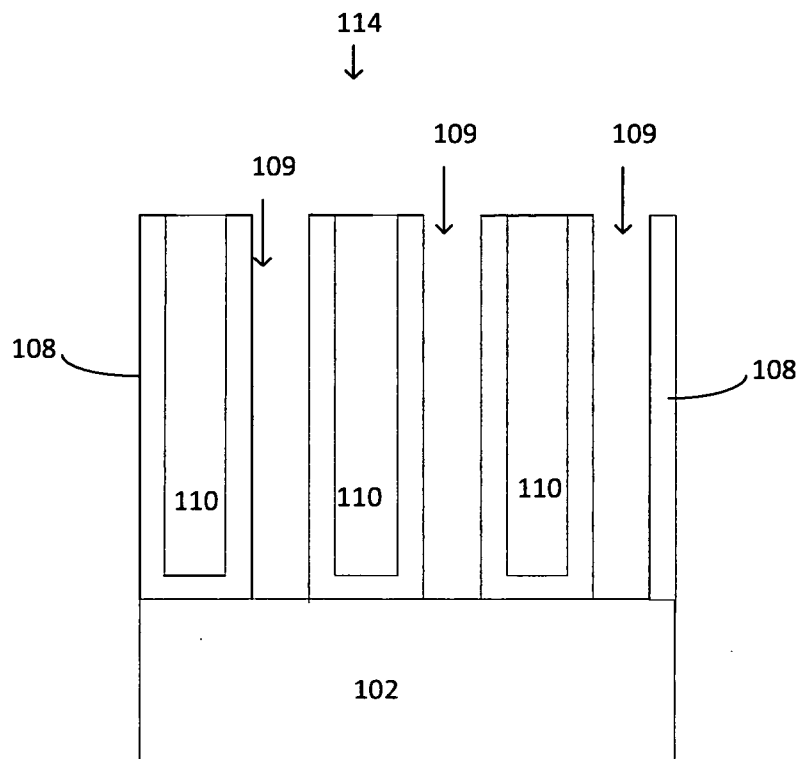


FIG. 1e

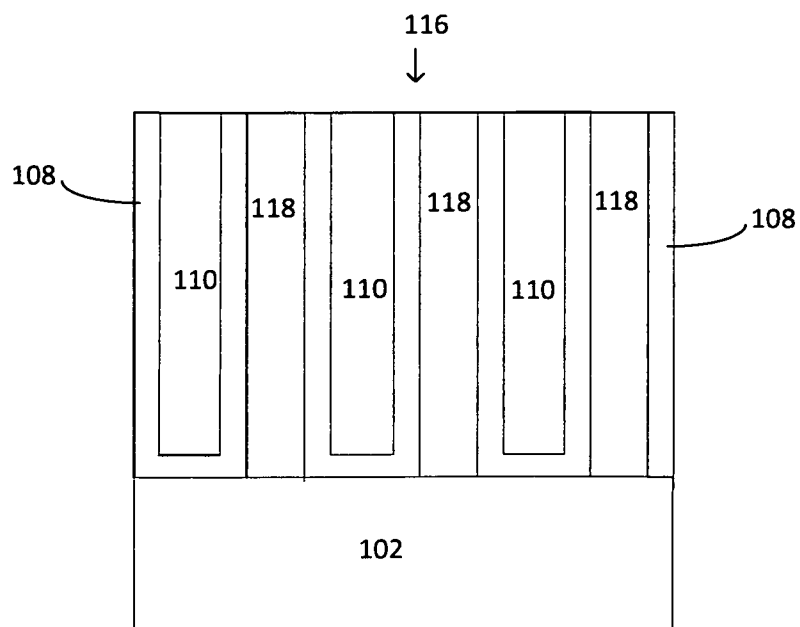


FIG. 1f

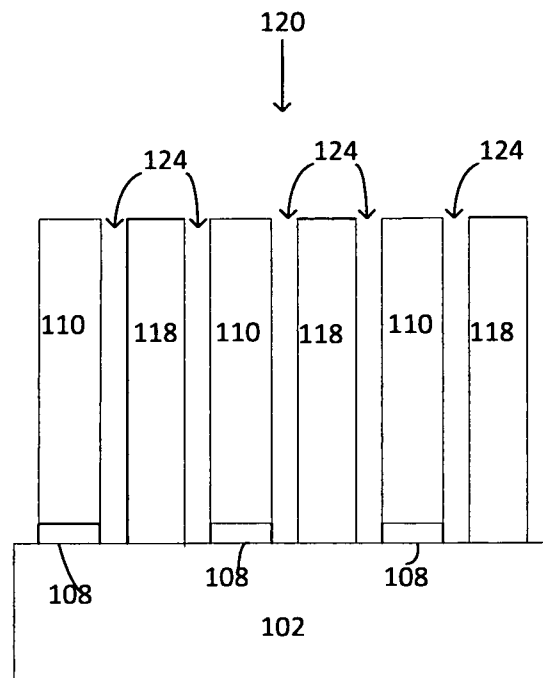


FIG. 1g

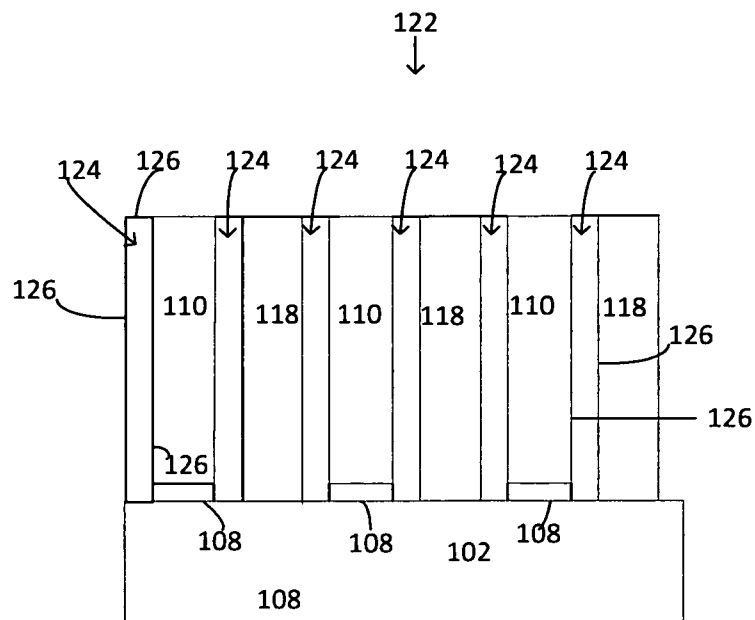
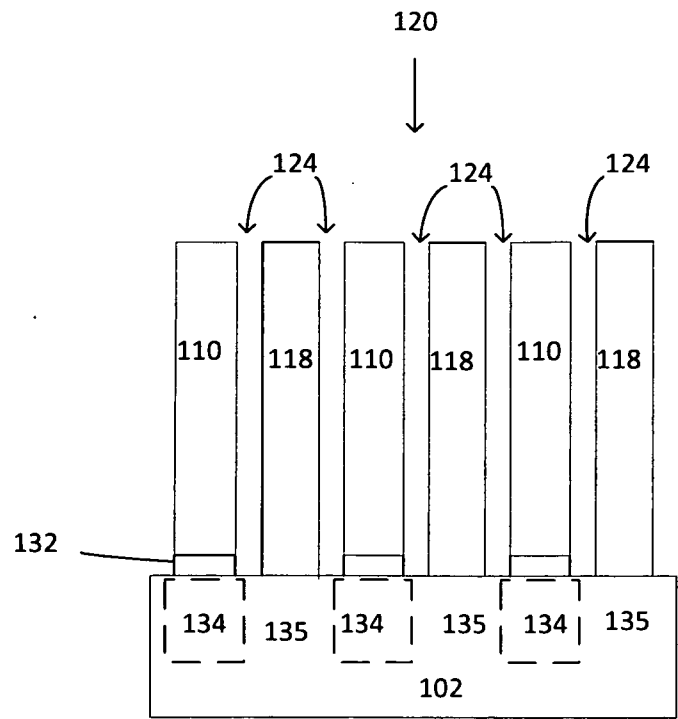
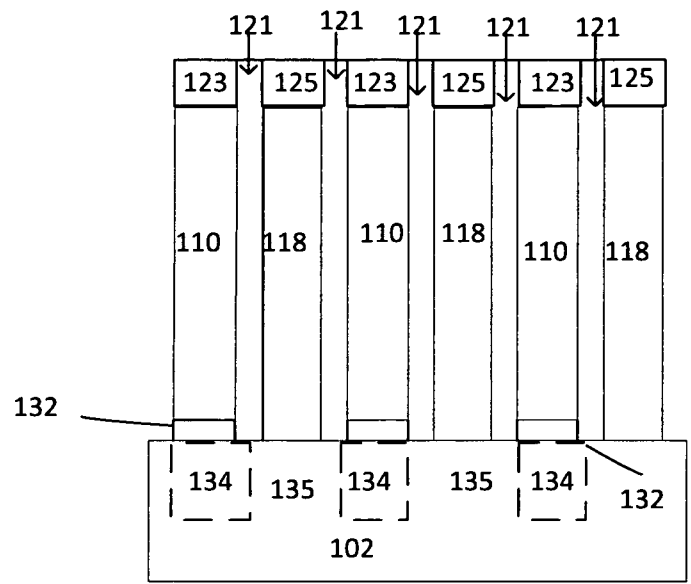


FIG. 1h



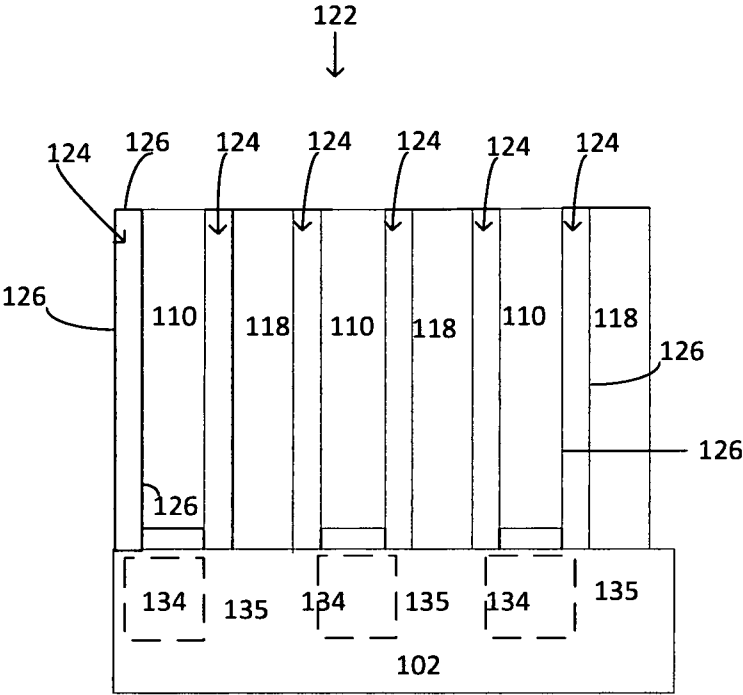


FIG. 1k

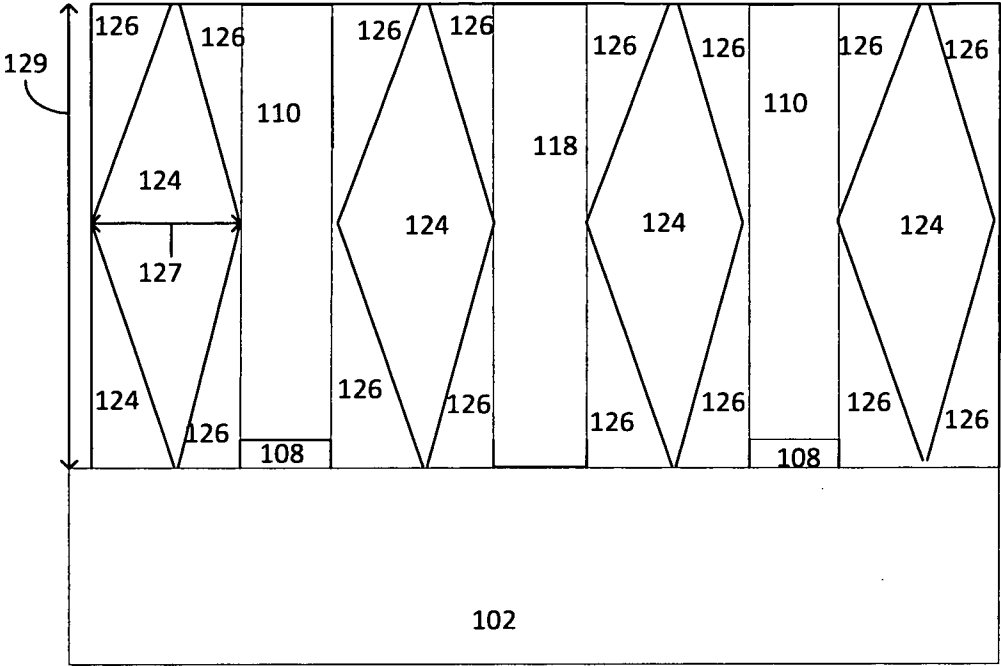


FIG. 1I

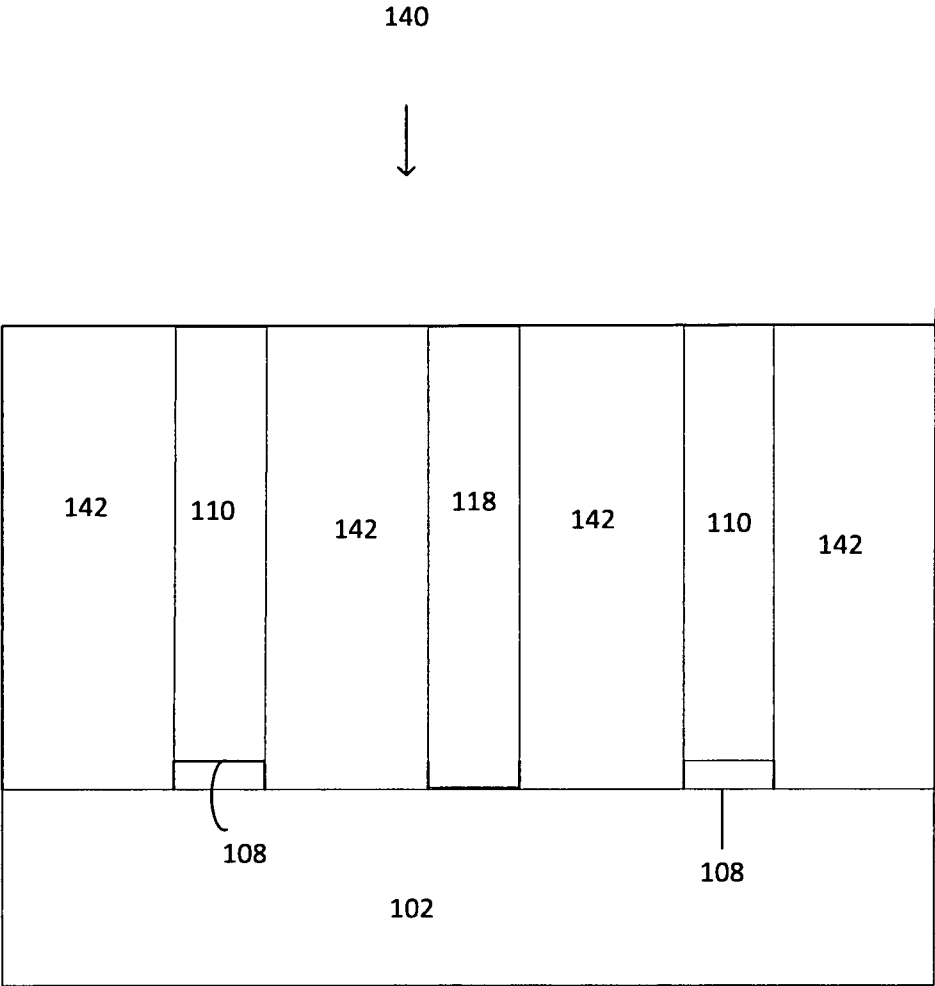


FIG. 1m

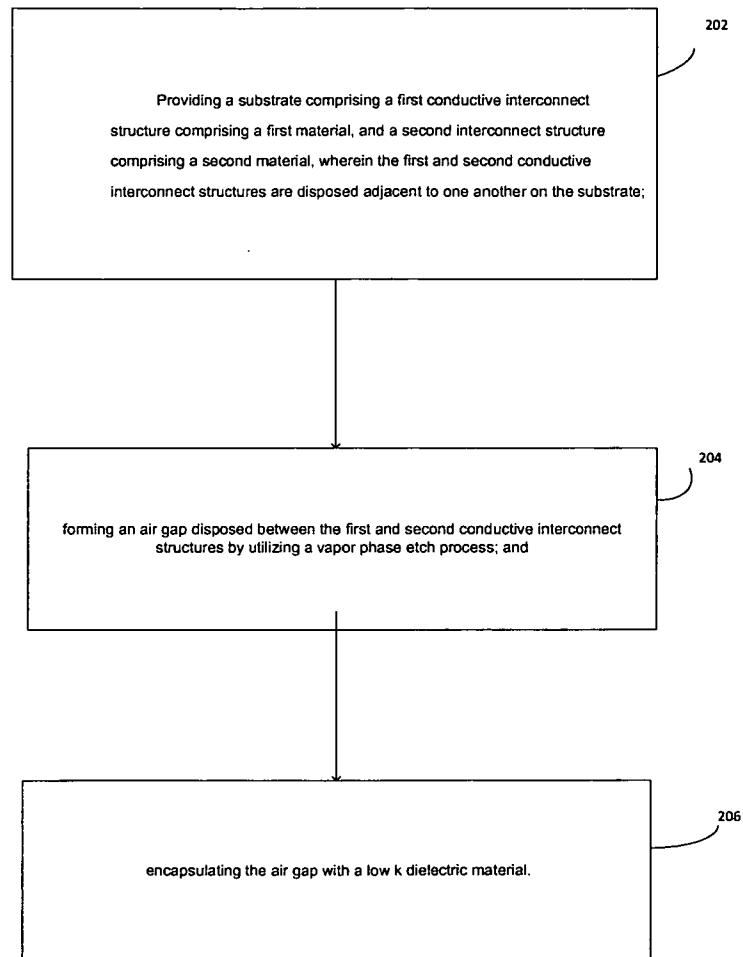


FIG. 2

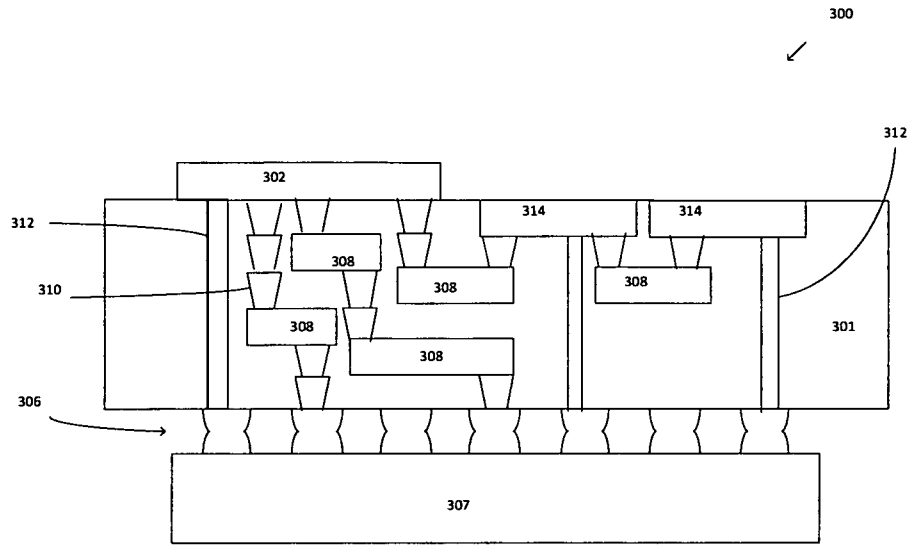


FIG. 3

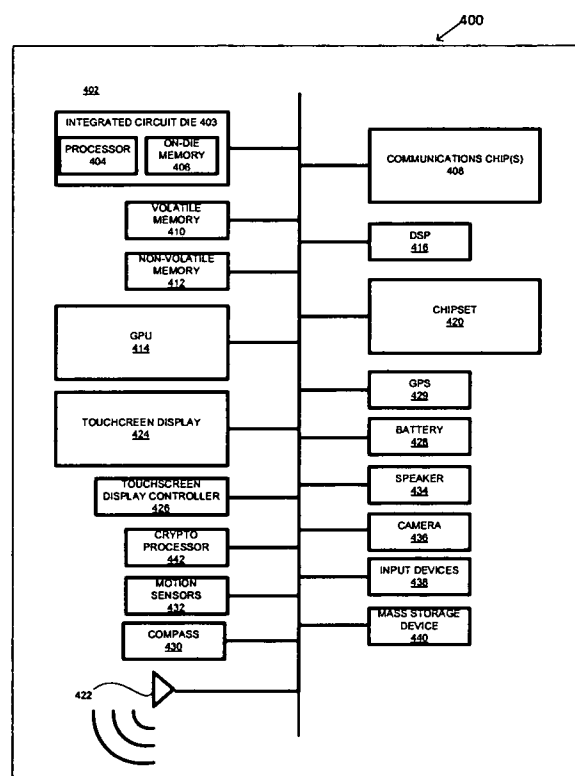


FIG. 4

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2015/000428**A. CLASSIFICATION OF SUBJECT MATTER****H01L 21/768(2006.01)i, H01L 21/205(2006.01)i, H01L 21/31(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 21/768; H01L 23/52; H01L 29/00; H01L 21/764; H01L 21/4763; H01L 23/48; H01L 29/06; H01L 29/40; H01L 21/205; H01L 21/31

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & keywords: dielectric, air gap, conductive structure, interconnect

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2010-0133648 A1 (ROBERT SEIDEL et al.) 03 June 2010 See abstract, paragraphs [0030]-[0043] and figures 1a-1i.	1-16
A		17-25
A	US 2008-0174017 A1 (CHIH-CHAO YANG et al.) 24 July 2008 See abstract, paragraphs [0033]-[0063] and figures 3A-3F.	1-25
A	US 2007-0246831 A1 (ZVONIMIR GABRIC et al.) 25 October 2007 See abstract, paragraphs [0081]-[0090] and figures 1-7.	1-25
A	US 2007-0096319 A1 (LOUIS LU-CHEN HSU et al.) 03 May 2007 See abstract, paragraphs [0022]-[0034] and figures 1-5.	1-25
A	US 2004-0094821 A1 (WATER LUR et al.) 20 May 2004 See abstract, paragraphs [0050]-[0074] and figures 10-13.	1-25



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

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"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

23 September 2016 (23.09.2016)

Date of mailing of the international search report

23 September 2016 (23.09.2016)

Name and mailing address of the ISA/KR

International Application Division

Korean Intellectual Property Office

189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea



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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2015/000428

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