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[54] CALLIGRAPHIC SYMBOL GENERATOR USING DIGITAL CIRCUITRY
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## [57]

ABSTRACT
A symbol generator includes digital circuitry for providing signals which are applied to X and Y deflection and Z axis bright up circuits of a cathode ray tube (CRT) for presenting calligraphically written symbology on the face of the CRT in response to signals from an external source. The symbology is repeated at a predetermined refresh rate to give the illusion of a continuous presentation.

9 Claims, 7 Drawing Figures


## SHEET 10 O 7






## SHEET 5 OF 7




SHEET 7 OF 7


## CALLIGRAPHIC SYMBOL GENERATOR USING DIGITAL CIRCUITRY

## BACKGROUND OF THE INVENTION

## 1. Field of the Invention

This invention relates generally to symbol generators and, more particularly, to digital symbol generators for calligraphically writing symbols on the face of a CRT in response to signals from an external source, and which symbols may be used for flight control purposes.

## 2. Description of the Prior Art

Heretofore apparatus for generating symbols for CRT displays has been relatively inaccurate and highly unstable. Moreover, prior art devices have not optimized symbol flexibility for making a wide range of options available to the display system designer. Additionally, in the present invention, all of the symbology is provided using stroke or calligraphic techniques to provide a clear, crisp, display. All symbols are written at a constant rate significantly lower than would be the case if raster scan apparatus were used, and thus maximum CRT brightness is assured.

## SUMMARY OF THE INVENTION

This invention contemplates a calligraphic symbol generator wherein symbology is generated by symbol makers including a line maker, a vector generator, an alphanumeric character generator, a circle maker and a moving tape, and only one of which symbol makers is active at a given instant. The symbol makers provide outputs which are applied to $x, y$ and $z$ axis circuits of a CRT. The $x$ and $y$ outputs are connected to adder-limiter-latch circuits, which combine position information with symbol description information developed by the symbol makers. The combined output is applied to a digital to analog converter for conversion to the necessary analog voltages for affecting the CRT. The $z$ axis outputs are applied to display bright-up circuitry. The symbol makers are controlled by instructions stored in a 512 word X 20 bit read only memory instruction (ROM) device. Associated with the instruction device is a 512 word X 20 bit read only position memory (ROM) device. The instruction device establishes the type of symbol to be made while the position device determines the location of the symbol on the CRT screen area.

One object of this invention is to provide a calligraphic symbol generator for providing outputs which are applied to $x$ and $y$ axis deflection circuits and the $z$ bright-up circuit of a CRT to produce symbology on the face of the CRT in response to signals from an external source, and which symbology may be used for flight control purposes.

Another object of this invention is to repeat the symbology at a predetermined refresh rate to give the illusion of a continuous presentation.

Another object of this invention is to provide a device of the type described using digital circuitry to eliminate senstivity to power supply variations as well as circuit drift, and to provide a device which will be relatively accurate and highly stable.

Another object of this invention is to provide a symbol generator of the type described including a plurality of symbol makers arranged to provide nearly an infinite
variety of symbology for maximum display system design flexibility.

The foregoing and other objects and advantages of the invention will appear more fully hereinafter from a consideration of the detailed description which follows, taken together with the accompanying drawings wherein one embodiment of the invention is illustrated by way of example. It is to be expressly understood, however, that the drawings are for illustration purposes only and are not to be construed as defining the limits of the invention.

## DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of the overall system of the invention.

FIGS. 2-6 are block diagrams of a line maker, vector generator, alphanumeric character generator, circle maker and moving tape, respectively, included in the device of the invention.

## DESCRIPTION OF THE INVENTION

With reference to FIG. 1, the symbol generator of the invention includes symbol makers $2,4,6,8$ and 10. Symbol maker 2 is a line maker, symbol maker 4 is a vector generator, symbol maker 6 is an alphanumeric character generator, symbol maker $\mathbf{8}$ is a circle maker and symbol maker $\mathbf{1 0}$ is a moving tape. The symbol makers provide $x, y$ and $z$ outputs.
The $x$ and $y$ outputs of symbol makers $2,4,6,8$ and 10 are combined in OR configuration and connected to $x$ and $y$ adderlimiter-latch circuits 12 and 14 respectively. Circuits 12 and 14 combine position information from a position memory device 28 , which is a 512 word X 20 bit read only memory (ROM), with symbolic information developed by the symbol makers. ROM device 28 is controlled by a control computer address complex $2^{0}-2^{8}$. The outputs from circuits 12 and 14 are applied to digital to analog converters 16 and 18 and therefrom to a resolver $\mathbf{2 0}$ for conversion to analog voltages required for controlling $x$ and $y$ deflection amplifiers of a cathode ray tube (CRT) not shown in the Figure. The $z$ outputs of symbol makers 2, 4, 6,8 and 10 are combined in OR configuration and connected through a gate $\mathbf{2 2}$ to CRT bright-up circuitry, also not shown in the Figure.
Symbol makers 2, 4, 6, 8 and 10 are controlled by instructions stored in an instruction memory device 24. Instruction memory device 24 is a 512 word X 20 bit read only memory (ROM) and is controlled by control computer address complex $2^{0}-2^{8}$. The symbol generator address provided by ROM 24 consists of a 5 bit address code, said bits designated in the Figure as B1-B5. This code is used to identify which particular type of symbol is desired. Each of the symbol makers 2, 4, 6, 8 and 10 is assigned a unique code or address corresponding to the particular symbols it is capable of making. For purposes of illustration, if the address code B1-B5 is 00000 , then vector generator symbol maker 4 will make a vector at an angle of $10^{\circ}$ from a reference. If $\mathrm{B} 1-\mathrm{B5}$ is 00001 , then line maker symbol generator 2 makes a horizontal line from right to left.
Symbol parameter data is given by a 10 bit word, siad bits designated in the Figure as B6-B15. This word has a different meaning for each of the symbol makers 2 , 4, 6, 8 and 10. For purposes of illustration, B6-B15 describe the line length when line maker 2 is active and
describe the circle diameter when circle maker $\mathbf{8}$ is active.
The 5 bit address code including the bits designated in the Figure as B16-B20 is used for controlling routines within control and timing logic circuitry $\mathbf{2 6}$, and is not connected to the symbol makers. B16, for example, is used to denote the first instruction associated with a particular symbol. For purposes of illustration, it may require 6 instructions to make an aircraft display. The first instruction will contain a 1 at the B16 position since it is the first instruction. The next 5 instructions will contain $\mathrm{B} 16=0$. Since the next instruction, in sequence, will contain B16 $=1$ (because it denotes the start of the next symbol), a means for grouping instructions on a display basis has been accomplished.

B17 is used to determine if the instruction executed should also be resolved. In the sense used, the term resolved means that an Euler coordinate transformation is to be performed. This capability is required since, for an aircraft control display, some symbols must be roll and pitch stabilized. B18 allows a choice between a short ( $\mathrm{B} 18=0$ ) or a long ( $\mathrm{B} 18=1$ ) slew delay. A slew delay is necessary since the deflection system requires a finite time to move the CRT spot from one location to another and, thus, it is not possible to begin symbol writing after finishing the preceding symbol until the spot can move over to the initial position of the next symbol. The choice of short or long slew delay is dependent on the distance between the last symbol location and the initial position of the next symbol.
Bits B19 and B20 are used to signify that in addition to a static position in the X and Y axis for the symbol written, there will be a dynamic position which must be combined with the static position. For example, if B19 $=1$, then the X static position must be combined with a dynamic position. The particular dynamic position will be available at a symbol variable memory device 27 and will be updated by an external source (not shown).

Associated with each 20 bit instruction word is a 20 bit position word stored in ROM device 28. X axis static position is given, for example, by bits B1 - B10 and Y axis static position is given by bits B11-B20. The instruction word establishes what type of a symbol will be made while the position word determines the location of the symbol on the useful CRT screen area.
With reference now to the specific components of the device, line maker $\mathbf{2}$ is a digital circuit which imparts to the symbol generator of the invention the capability of writing a line of any length up to 1,023 bits either horizontally (left to right, or right to left) or vertically (top to bottom or bottom to top). The instructions for the type of line are decoded from the 5 bit address B1-B5 from ROM device 24 (FIG. 1) while the length of the line is specified by the 10 bit address B6 - B15 from device 24.
A horizontal line is written by changing the X position of the CRT beam incrementally while holding the Y position constant, and a vertical line is written by changing the Y position of the beam incrementally while holding the X position constant. If a line is to be written in the positive sense (that is, from left to right or bottom to top), the changing parameter is increased and, conversely, if the line is to be written in the negative sense the changing parameter is decreased.

The output of line maker 2 is in the form of 10 bit binary words for the X and Y positions. These binary words are converted to analog voltages by converters 16 and 18 in cooperation with resolver 20 (FIG. 1) for providing CRT beam deflection voltages.

A block diagram illustrating the arrangement of the components of line maker 2 is illustrated in FIG. 2. Address bits B1-B5 are received by a register $\mathbf{3 0}$ and serially stored thereby and address bits B6-B10 and B11 - B15 are received by registers $\mathbf{3 2}$ and $\mathbf{3 4}$ respectively, and serially stored thereby. A decoding logic device 36 provides information to a 10 bit counter 38 and a true/complement element 40 is driven by the counter for controlling an output logic device $\mathbf{4 2}$ which provides $x$ and $y$ outputs for drawing the lines in the positive or negative sense and horizontal or vertical, as the case may be.
A comparator 44 driven by counter 38 produces signals at the completion of the line, i.e., when the symbol parameter output $\mathbf{B 6}-\mathrm{B} 10, \mathrm{~B} 11-\mathrm{B5}$ equals the state of the counter. This action inhibits a master counter clock 39 shown in FlG. 1, and at this time a signal is given by the clock to affect control and timing logic circuitry 26 indicating that the line maker is writing its final bit of the symbol. A ready/busy signal provided by device $\mathbf{3 6}$ indicates to control and timing logic circuitry 26 the actual time that the signal is being written. Output logic device 42 provides separate 10 bit, X and Y outputs and decoding device 36 provides a 1 bit, $Z$ output. Decoding logic device 36 is controlled by validity and initiate signals from control and timing circuitry 26.

Vector generator 4 provides the symbol maker of the invention with the capability of writing a vector of a length up to 1,023 bits, and at any one of 14 discrete angles with the vertical, which for purposes of illustration may be nominally $\pm 10^{\circ}, 20^{\circ}, 30^{\circ}, 45^{\circ}, 60^{\circ}, 70^{\circ}$ and $80^{\circ}$. The instruction for the angle and slope of the vector is decoded by the 5 bit address B1 - B5 while the length is specified by the 10 bit address B6-B10 and B11-B15.

It is to be noted that a line at any angle may be written by changing the X and Y position of the CRT beam incrementally but at different rates. Depending upon the angle, the $X$ position of the beam may be incremented faster than the $Y$ position or vice versa. For angles with a negative slope, one parameter is increased while the other is decreased, but still at different rates. The output of vector generator 4 is in the form of 10 bit, binary X and Y words. These binary words are converted to analog voltages by converters 16 and 18 (FIG. 1) for providing CRT beam deflection voltages.

A block diagram of vector generator 4 is shown in FIG. 3. Thus, the address B1-B5 is received serially and stored by a register 44 and the addresses B6-B10 and B11-B15 are received serially and stored by registers 46 and 48, respectively. Address decoding logic means $\mathbf{5 0}$ is controlled by validity and initiate signals from timing circuit 26 (FIG. 1). Logic means 50 provides information to $X$ and $Y$ counters 52 and 54 which drive true-complement elements $\mathbf{5 6}$ and $\mathbf{5 8}$, respectively, indicating whether the line is of positive or negative slope, and to count enable selectors 60 and 62 indicating the angle to be written. A comparator 64 signals the final value of the line which occurs when the state of a magnitude counter 65 equals the symbol parame-
ter address B6-B10, B11-B15, indicating that the symbol maker is writing its final bit of the symbol. A ready/busy signal indicates to control and timing logic circuitry 26 (FIG. 1) the actual time that the symbol is being written or in other words indicates that the system is "ready" to write another symbol, but is "busy" writing a previous one. The circuit provides separate 10 bit, X and Y outputs and a 1 bit, bright-Up output Z .

Alphanumeric Character Generator 6 provides the symbol maker of the invention with the capability of making all alphanumerics A through Z and 0 through 9 , and also a plus or minus sign.
With reference to the block diagram of FIG. 4, an input register 66 receives 15 bits of information, 5 bits being symbol select bits B1-B5 and 10 bits being symbol parameter bits B6 to B15. The symbol parameter address contains character size commands.
When the symbol address is proper, and validity and initiate signals are provided by timing device 26 (FIG. 1), clock signals from a clock circuit 68 are applied through the character generator. The signals are applied to a waveform maker 70 which then provides a required character format in terms of $x$ and $y$ outputs. The outputs from waveform maker 70 are digital representations of $x$ and $y$ CRT deflection signals.
The signals from clock circuit 68 are also applied to bright-up and complete circuit 72 which selects the proper signals and stores them in read only memories (not shown). The outputs of circuit 72 are the brightup or $z$ axis signal and the final value and ready/busy signals for the symbol maker. The final value signal indicates when the final bit of a character has been reached and the ready/busy signal designates the state of the character generator, that is, whether it is writing a character, or if it is available to write a character.

Circle maker 8 provides the device of the invention with the capability of displaying a circle of variable radius ( 4 bits to 512 bits). The circle display instruction is contained in the 5 bit address B1-B5 while the radius is contained in the 10 bit address B6-B15.
A circle is written on a CRT face by varying the $x$ position of the CRT beam sinosuidally while simultaneously varying the Y beam position cosinosuidally. In a digitally derived system, this amounts to drawing connected line segments at many angles. The radius of the circle is varied by modifying the number of angles sampled (a small radius requires fewer angles) and the length of the line segments at each angle.
With reference to FIG. 5, the address B1 - B5 is applied to a register 81 and addresses B1-B10 and B11 - B15 are applied to registers 87 and 91 , respectively. The sine and cosine values are obtained from read only memories (ROM) 80 and 82 , respectively, which are driven by an up-down binary counter 84 receiving radius logic from a control logic device 87 . Devices 82 and $\mathbf{8 0}$ are identical, but are addressed by an up-count for sine and a downcount for cosine values. The outputs of the counter are shifted in the direction of more significance to accommodate circles requiring fewer angles per quadrant.
The read only memory outputs are used as gating signals to binary rate multipliers (BRM) 86 and 88 which are incremented at 10 times the writing clock rate. Multipliers 86 and 88 , therefore, provide pulse trains at frequency ratios corresponding to the values of sine and cosine. The pulse trains are then divided by 10 by
dividers 89 and 93 and summed by binary counters 90 and 92 for providing $X$ and $Y$ outputs respectively. The factor of 10 is used for smoothing the uneven spacing of the pulses.

In the connection it is noted that a binary rate multiplier such as the multipliers 86 and 88 is a circuit which generates a pulse train having, on the average, a specified fraction of the number of input pulses. The circuit includes a binary counter whose outputs are gated with a binary input word. This binary word specifies the fractional output frequency by allowing the pulse train to advance a counter, such as the counters 90 and 92 , a binary word, which increments at a rate specified by the input word. By controlling the up-down counting modes of counters 90 and 92 , according to the circle quadrant being written, a circular beam path is provided. A counter directional command is provided by a decoding logic device 87.

The initial X output value is obtained by clearing X output counter 90 to all " 0 's". The initial value of Y is obtained by presetting the value of the radius R into Y output counter 92. Both counters count up in the first quadrant, with the X counter starting from zero and the Y counter starting from the value of the radius. The X counter counts up at a rate proportional to the sine (if zero degrees is the count-up starting point) toward the radius value. The Y counter also counts up from the radius value to a value twice the radius at a rate proportional to the cosine.
Moving tape symbol maker 10 provides the device of the invention with the capability of making three types of scales namely, a unipolar scale, a bipolar scale and a continuous scale. In addition, these scales may be either positive or negative. A positive scale is one in which the numbers are of greater magnitude or more positive at the top, in the case of a vertical instrument scale, or to the right, in the case of a horizontal scale.

Scale generator $\mathbf{1 0}$ is designed to be flexible in that selection of a different scale does not require a change in hardware. A simple change in the instructions to the symbol maker permits variations to be made in type of scale, digits per scale number, difference between numbers, scale factor and maximum value of a continuous scale.
It is to be noted that moving tape symbol maker 10 does not actually produce any symbol wave forms, but rather provides control signals for other circuitry in the symbol generator. Specifically, it accepts input signals and generates dynamic position, character selection signals, and a bright-up signal. The scale and its associated numerics are generated by the line maker 2 and character generator 6 respectively.

With reference now to FIG. 6, it will be seen that moving tape symbol maker 10 receives three sets of instructions. Instruction (1) selects the type of scale the number of digits each number should contain and the scale factor for the dynamic position signal. It also selects the upper and lower scale limits signal which determines the width of a bright-up window. Instruction (2) determines a value (G), which is the quantity between major graduations on the scale and value (M), the maximum signal. Instruction (3) determines the operation of the symbol makers. All instructions are provided in response to bits B1-B15.

A binary counter $\mathbf{1 0 0}$ is preset to some value which is dependent upon scale select address B11-B13 ap-
plied to the counter through preset circuit 102. The output of counter 100 is the address for a command (ROM) device 104. Device 104 instructs an arithmetic unit 106 to perform the necessary functions to make the scale.
The output of arithmetic unit 106 is converted from binary to binary coded decimal (BCD) by a converter 108. The proper decode command is selected by a decode select device 110 in response to bits $\mathrm{B6}$ - B7, and applied to the appropriate character generator to make the desired number. Another output of arthmetic unit 106 is a dynamic position signal which, after being properly scaled by a scale factor device 112 , is combined with the static position signals of the scale and its numerics causing them to move.
Bit B14 of the first instruction determines whether a vertical or horizontal scale is to be made. If for example a vertical scale is selected, the Y output of the character generator is compared with upper and lower limit signals by a window comparator 114 . When the Y output becomes greater in magnitude that the lower limit, but less than the upper limit, a bright-up window is enabled. When the $Y$ output exceeds the upper limit, the bright-up window is disabled.
BCD converter 108 drives a decoder 109 which provides final value and ready/busy signals to timing circuit 26 (FIG. 1) and decoder 109 is controlled by a timing circuit 111 in response to the output of a register 113.

The funtion of adder-limiter-latch circuits 12 and 14 shown generally in FIG. 1, is to algebraically add the 10 bit binary word for symbol data with the 11 bit binary (sign-magnitude) word for symbol initial position. The circuit also limits the output to 0 (if the algebraic sum is less than 0 ) and to 1023 (if the sum is greater than 1023). A further function of the circuit is to hold this sum if it is the final beam position of a symbol until the "validity" signal for a new symbol instruction is generated. This procedure is the same for both X and Y components of the symbol. The $Z$ (bright-up) component is provided when the beam position is not being limited or stored.
Symbol makers 2, 4, 6, 8 and 10 find their own starting positions for the symbols (typically ( $\mathrm{X}=0, \mathrm{Y}=0$ ), and the initial position (the sum of static and dynamic positions) is algebraically added to the symbol data in order that the symbol may be positioned anywhere on the screen.
The latch portion of circuits 12 and 14 is provided to store the final position ( X and Y ) of a symbol. Without this storage capability, after each symbol is written, the beam would return to its quiesant point at, for example, the bottom left of the CRT screen. Thus, a long slew delay would be required before each symbol is written. In addition, the latches are also used to store the beam position during writing time while simultaneously computing the next beam position, if propogation delay due to the adder-subtract circuitry becomes excessive.
Control and logic circuitry 26, shown generally in FIG. 1, provides the basic timing and control functions for the entire symbol generator. The writing clock (CW), twice the writing clock (2CW), (5CW) and shift pulses are all generated by this circuitry. All clock signals are symmetrical and slaved to a master clock oscillator. In addition control signals such as the aforenoted validity and initiate signals and frame sync signals are provided by timing and control logic circuitry 26 . The
addresses for ROM device $\mathbf{2 4}$ and for ROM device $\mathbf{2 8}$ are generated and controlled by this circuitry.

## OPERATION OF THE INVENTION

From the aforegoing description of the invention with reference to the accompanying drawings, it will be seen that the symbol generator of the invention provides signals for CRT X and $Y$ deflection amplifiers and $Z$ axis bright-up circuits so as to provide symbols and characters on the screen of the CRT. The symbology is generated and positioned in response to signals from an external source, and is repeated at a refresh rate to give the illusion of continuous presentation
The manner in which the symbol generator is organized rather than the specific structural details of the components therein represents the novel feature of the invention, it now being understood that the components of the invention include digital and logic equipment of a type well known in the art.

Nearly any display which consists of a line, a vector. an alphanumeric, a circle or a moving tape individually or in combination can be made using the symbol generator. The ROM devices, which store instructions and positioning information, are the only components specifically designed for a given display. All other components are designed for general application and are not dedicated to a specific symbology requirement.
The symbology is generated by symbol makers including line maker 2 , vector generator 4 , alphannumeric character generator 6 , circule maker 8 , and moving tape 10. Only one of these symbol makers is active at any given instant and provides $X, Y$ and $Z$ outputs for CRT control. The $X$ and $Y$ outputs are connected to adder-limiter-latch circuits 12,14 and the outputs of these circuits are applied to digital to analog converters 16 and 18 for conversion to analog voltages required for the CRT control circuits. The Z axis output is connected to final bright-up circuitry.
The symbol, makers are controlled by instructions stored in ROM device 24. The symbol address consists of bits B1-B5. This 5 bit address code is used to identify which particular type of symbol is desired. Each symbol maker is assigned a unique code or address corresponding to the particular symbols it is capable of making. Symbol parameter data is given by the 10 bit word B6-B15. This word has different meaing to different symbol makers. Bits B16 through B20 are used for control purposes and are not connected to the symbol makers. These bits operate through control and timing logic circuitry 26. Associated with each instruction word is a 20 bit position word stored in ROM device 28 . The $Z$ static position is given by bits B1-B10 and the Y static position is given by bits $\mathrm{B} 11-\mathrm{B} 20$. The instruction address establishes what type of symbol will be made while the position address determines the location on the useful CRT screen area where the symbol will start
Although but a single embodiment of the invention has been illustrated and described in detail, it is to be expressly understood that the invention is not limited thereto. Various changes may also be made in the design and arrangement of the parts without departing from the spirit and scope of the invention as the same will now be understood by those skilled in the art.
What is claimed is:
I. A symbol generator comprising:
a first memory device for storing symbol description instructions and for providing first digital signals identifying a partcular type of symbol and second signals indicative of symbol parameter data;
a second memory device for storing symbol position instructions and for providing first digital signals which define the position of the symbol relative to one axis and second digital signals which define the position of the symbol relative to another axis normal to the one axis;
a plurality of symbol makers connected to the first instruction memory device and controlled by the first and second digital signals therefrom for providing digital symbol description signals;
means for combining the first and second digital signals from the second memory device and the digital description signals; and
means connected to the combining means for converting the combined digital signals to analog signals.
2. A symbol generator as described by claim 1, wherein:
the plurality of symbol makers are controlled by the digital signals from the first instruction memory device so that only one of said symbol makers is active at a given instant.
3. A symbol generator as described by claim 1, including:
circuitry connected to selected symbol makers of the plurality of symbol makers and affected thereby for providing symbol maker control and timing logic;
said circuitry including means for providing a signal at the completion of a symbol, clock means inhibited by said signal and thereupon providing a control signal, and means responsive to the control signal for controlling the symbol makers.
4. A symbol generator as described by claim 1 wherein the plurality of symbol makers include:
a line maker connected to the first memory device and controlled by the first digital signals for providing digital signals corresponding to the sense of a line, and controlled by the second digital signals for providing digital signals corresponding to the length of the line.
5. A symbol generator as described by claim 1, wherein the plurality of symbol makers includes:
a vector generator connected to the first memory device and controlled by the first digital signals for
providing digital signals corresponding to the slope of a vector relative to a reference, and controlled by the second digital signals for providing digital signals corresponding to the length of the vector.
6. A symbol generator as described by claim 1, wherein the plurality of symbol makers includes:
an alphanumeric character generator connected to the first memory device and controlled by the first digital signals for providing digital signals corresponding to a selected character, and controlled by the second digital signals for providing digital signals corresponding to character size.
7. A symbol generator as described by claim 1, wherein the plurality of symbol makers includes:
a circle maker connected to the first memory device and controlled by the first digital signals for providing digital signals corresponding to a selected circle and controlled by the second digital signals for providing digital signals corresponding to the radius of the selected circle.
8. A symbol maker as described by claim 1, wherein the plurality of symbol makers includes:
a moving tape symbol maker connected to the first memory device and controlled by the first and second digital signals for providing digital dynamic position and character selection signals.
9. A symbol maker as described by claim 1, wherein the plurality of symbol makers includes:
a line maker connected to the first memory device and controlled by the first digital signals for providing digital signals corresponding to the sense of a line, and controlled by the second digital signals for providing digital signals corresponding to the length of the line;
an alphanumeric character generator controlled by the first digital signals for providing digital signals corresponding to a selected character, and controlled by the second digital signals for providing digital signals corresponding to the character size;
a moving tape symbol maker controlled by the first and the second digital signals for providing digital dynamic scale position and character select signals; and
the line maker and character generator connected to the moving tape symbol maker for generating the scale in response to the signals therefrom.

