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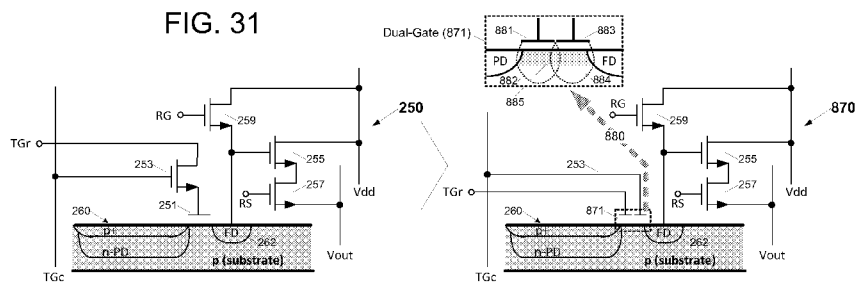
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(54) Title: SPLIT-GATE CONDITIONAL- RESET IMAGE SENSOR



(57) Abstract: In a pixel array within an integrated-circuit image sensor, a pixel (870) includes a photodetector (260) and floating diffusion (262) formed within a substrate. First (881) and second (883) gate elements are disposed adjacent one another over a region (885) of the substrate between the photodetector and the floating diffusion and coupled respectively to a row line (TGr) that extends in a row direction within the pixel array and a column line (TGc) that extends in a column direction within the pixel array.

SPLIT-GATE CONDITIONAL-RESET IMAGE SENSOR

TECHNICAL FIELD

[0001] The present disclosure relates to the field of electronic image sensors, and more specifically to a sampling architecture for use in such image sensors.

BACKGROUND

[0002] Digital image sensors, such as CMOS or CCD sensors, include a plurality of photosensitive elements (“photosensors”) each configured to convert photons incident upon the photosensors (“captured light”) into electric charge. The electric charge can then be converted into image data representing the light captured by each photosensor. The image data includes a digital representation of the captured light, and may be manipulated or processed to produce a digital image capable of display on a viewing device. Image sensors are implemented in integrated circuits (“ICs”) with a physical surface that may be divided into a plurality of pixel regions (for instance, one or more photosensors and attendant control circuitry) configured to convert light into an electrical signal (charge, voltage, current, etc.). For convenience, pixel regions within an image sensor may also be referred to as image pixels (“IPs”) and the aggregate of the pixel regions or image pixels will be referred to as the image sensor region. An image sensor IC typically will also include areas outside of the image sensor region, for example certain types of control, sampling, or interface circuitry. Most CMOS image sensors contain A/D (analog-to-digital) circuitry to convert pixel electrical signals into digital image data. The A/D circuitry can be one or more ADCs (analog-to-digital converters) located within or at the periphery of the image sensor region.

BRIEF DESCRIPTION OF THE DRAWINGS

[0003] The various embodiments disclosed herein are illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings and in which like reference numerals refer to similar elements and in which:

[0004] Figure 1 illustrates a cross-section of a portion of an image sensor, according to one embodiment;

[0005] Figure 2 illustrates partial array circuitry of an analog pixel image sensor with multiple pixel signal thresholds, according to one embodiment useful, e.g., in the layout of Figure 1;

- [0006] Figure 3 illustrates an example image sensor read circuit configured to convert a pixel signal into a multi-bit digital conversion, according to one embodiment useful, e.g., with the embodiments of Figures 1 and 2;
- [0007] Figure 4 illustrates an example circuit block diagram embodiment of an image sensor system with a multi-bit architecture, according to one embodiment using, e.g., the cross-section of Figure 1 and the circuitry of Figures 2 and 3;
- [0008] Figure 5 illustrates another example circuit block diagram of an image sensor system architecture with read circuit arrays located peripherally to an IP array, according to one embodiment using, e.g., the cross-section of Figure 1 and the circuitry of Figures 2 and 3;
- [0009] Figure 6a illustrates a top view of a pixel array IC in an example two-layer image sensor system architecture alternative to Figures 4 and 5, according to one embodiment using, e.g., the array circuitry of Figure 2;
- [0010] Figure 6b illustrates a top view of a preprocessor IC in an example two-layer image sensor system architecture alternative to Figures 4 and 5, according to one embodiment using, e.g., the read circuitry of Figure 3;
- [0011] Figure 6c illustrates a partial cross section of the pixel array IC of Figure 6a and the preprocessor IC of Figure 6b in an example two-layer image sensor system architecture, according to one embodiment;
- [0012] Figure 7 illustrates the operation of an image sensor read circuit, such as the read circuit of Figure 3, according to one embodiment;
- [0013] Figure 8 illustrates data flow in an image capture system, according to one embodiment useful with the systems described herein;
- [0014] Figure 9 illustrates various temporal sampling policies for use by an image sensor read circuit, such as the read circuit of Figure 3, according to one embodiment;
- [0015] Figure 10 illustrates an embodiment of a modified 4-transistor pixel in which a non-destructive over-threshold detection operation is executed to enable conditional-reset operation in conjunction with correlated double sampling;
- [0016] Figure 11 is a timing diagram illustrating an exemplary pixel cycle within the progressive read-out pixel of Figure 10;
- [0017] Figures 12 and 13 illustrate exemplary electrostatic potential diagrams for the photodiode, transfer gate and floating diffusion of Figure 10 below their corresponding schematic cross-section diagrams;
- [0018] Figure 14 illustrates an embodiment of an image sensor 300 having a progressive-readout pixel array;

[0019] Figures 15A-15C illustrate alternative column read-out circuit embodiments that may be employed in connection with the progressive read-out pixels described in reference to Figures 10-14;

[0020] Figure 16 illustrates a quad-pixel, shared floating diffusion image sensor architecture in which the row and column transfer-gate control lines disclosed in the embodiments of Figures 10-14 may be applied in a manner that enables multiple decimation modes without requiring additional array-traversing control lines;

[0021] Figure 17 illustrates an exemplary physical layout of the quad-pixel architecture shown in Figure 16;

[0022] Figures 18A and 18B illustrate color filter array (CFA) patterns that may be employed with respect to the quad-pixel architecture of Figures 16 and 17;

[0023] Figures 19 and 20 present timing diagrams illustrating exemplary phases of full-resolution (non-binning) and binned-mode pixel read-out operations, respectively, within an image sensor containing the 2x2 quad-pixel arrangement shown in Figure 16;

[0024] Figure 21 illustrates an alternative binning strategy that may be executed with respect a collection of 4x1 quad-pixel blocks in conjunction with a color filter array;

[0025] Figure 22 illustrates a column-interconnect architecture that may be applied to enable voltage-binning of analog signals read-out from selected columns of 4x1 quad-pixel blocks;

[0026] Figure 23 illustrates an exemplary timing diagram of binned-mode read-out operations within the 4x1 quad-pixel architecture of Figures 21 and 22;

[0027] Figure 24 illustrates a more detailed embodiment of an image sensor having an array of 4x1 quad pixel blocks operable in the decimation (binning) mode described in reference to Figures 21-23;

[0028] Figures 25A-25C illustrate an embodiment of a selectable-gain (or multi-gain) read-out circuit that may be used to effect a high-gain partial read-out and near-unity gain full read-out within a pixel column;

[0029] Figure 26 presents an exemplary timing diagram illustrating the alternating application of common-source and source-follower gain configurations during hard-reset, integration, partial read-out and (conditional) full read-out operations within the multi-gain architecture of Figure 25A;

[0030] Figure 27 illustrates an alternative embodiment of a selectable-gain (or multi-gain) read-out circuit that may be used to effect a high-gain partial read-out and near-unity gain full read-out within a pixel column;

- [0031] Figure 28 illustrates an embodiment of an image sensor having a pixel array disposed between upper and lower read-out circuits;
- [0032] Figure 29 illustrates an embodiment of an imaging system having a conditional-reset image sensor together with an image processor, memory and display;
- [0033] Figure 30 illustrates an exemplary sequence of operations that may be executed within the imaging system of Figure 29 in connection with an image processing operation;
- [0034] Figure 31 contrasts embodiments of the conditional-reset pixel of Figure 10 and a “split-gate” pixel;
- [0035] Figure 32 is a timing diagram illustrating an exemplary pixel cycle (reset/charge integration/read-out) within the split-gate pixel of Figure 31;
- [0036] Figure 33 illustrates exemplary low-light and high-light operation of the split-gate pixel of Figure 31, showing electrostatic potential diagrams in each case beneath schematic cross-section diagrams of the photodetector, dual-control transfer gate and floating diffusion;
- [0037] Figure 34 illustrates an alternative overthreshold detection operation within the split-gate pixel of Figure 31;
- [0038] Figure 35 illustrates an exemplary implementation of the dual-control gate shown in Figure 31;
- [0039] Figure 36 illustrates an alternative manner of implementing the dual-control gate structure of Figure 31;
- [0040] Figure 37 illustrates a quad-pixel, shared floating diffusion image sensor architecture in which pairs of row and column transfer-gate control lines are coupled to a dual-gate structure within each of four split-gate pixels;
- [0041] Figures 38 and 39 illustrate exemplary physical layouts of the quad-pixel of Figure 37, showing the four photodiodes disposed about and switchably coupled to a centralized floating diffusion via respective dual-control gate structures;
- [0042] Figures 40 and 41 illustrate a split-gate pixel architecture and corresponding timing diagram according to an alternative embodiment that lacks a dedicated row transfer-gate (TGr) line;
- [0043] Figure 42A illustrates an alternative dual-control gate arrangement in which the gate elements of a dual-control gate are formed by respective p-doped and n-doped regions of a diode;
- [0044] Figure 42B illustrates another alternative dual-control gate arrangement in which the gate elements of a dual-control gate are formed by respective p-doped regions of back-to-back diodes having a shared n-doped region; and

[0045] Figure 43 illustrates a 4x1 block of split-pixels (a quad, split-pixel block) that may be operated in binned or independent-pixel modes as described above, for example, in reference to Figure 21.

DETAILED DESCRIPTION

[0046] In some image sensors, electrical information representing a photon response and resulting from light incident upon a pixel region (referred to herein as a “pixel signal”) is converted to a digital image data value by read circuitry. The read circuitry can reside within the image sensor, or can be located external to the image sensor. In some approaches, a read circuit can be located within the image sensor for use by one or more pixel regions adjacent or near the read circuit. For read circuits located external to the image sensor, the pixel signals of one or more pixel regions associated with the read circuits can be transferred from the pixel regions to the read circuits.

[0047] Each read circuit samples a pixel region, receives a pixel signal from the sampled pixel region, and converts the pixel signal to a multi-bit digital value representative of the pixel signal. In the event that a pixel signal or a digital value representative of the pixel signal exceeds a sampling threshold, the pixel signal stored at the pixel region associated with the pixel signal is reset (for instance, by resetting a photosensitive element associated with the pixel region). If the pixel signal or the digital value do not exceed the sampling threshold, the pixel signal stored at the pixel region is not reset. The sampling of a pixel region and the resetting of a pixel signal at the pixel region only when the pixel signal exceeds a sampling threshold is referred to herein as “non-destructive sampling with conditional reset.”

Image Sensor Overview

[0048] Figure 1 illustrates a partial cross-section of an image sensor 25 useful in an embodiment. In image sensor 25, light passing through a microlens array 10 and a color filter array 12 (useful for color imaging) is incident upon a silicon section 20 of the image sensor. The use of microlenses (or other concentrating optics) and color filters is optional and is shown here for illustrative purposes only. Silicon 20 contains photodiodes (not shown) to collect charge generated by photons absorbed by the silicon, and access transistors (also not shown) to operate the photodiodes. Pixel array IC wiring 14 provides connections used to route signals and supply voltages within the array. As shown, image sensor 25 is a BackSide Illuminated (BSI) sensor because light enters the silicon from the side of the integrated circuit opposite the wiring layers and primary active circuit formation. Optionally, pixel array IC wiring 14 can be arranged

between the color filter array 12 and silicon 20 (with primary active circuit formation within the “top” of the silicon as oriented in Figure 1) for FrontSide Illumination (FSI).

[0049] The image sensor 25 includes a plurality of IPs (“image pixels”), IP1-IP3 shown, upon which light collected by the lenses of the microlens array 10 is respectively incident. Each IP includes one or more photodiodes embedded within the silicon 20. At least some photons entering silicon 20 are converted to electron-hole pairs in the silicon and the resulting electrons (or holes in alternate embodiments) are collected by the IPs. The description herein will refer to this process as the capture and conversion of light by the IPs into image data for the purposes of simplicity. Each IP of the image sensor represents a portion of the surface area of the image sensor, and the IPs of the image sensor may be organized into various arrays of columns and rows. In a CMOS or CCD image pixel technology, each IP (for instance, each photosensor) converts light incident upon the IP into a charge and includes readout circuitry configured to convert the charge into a voltage or current. In one embodiment, the light captured by each IP of the image sensor represents one pixel of image data for an associated digital image, though in other embodiments image data from multiple IPs is combined to represent a fewer number (one or more) of pixels (downscaling).

[0050] The image sensor 25 may include components outside the IP array. Similarly, portions of the IP array may include components that do not convert light into charge. The region defined by the IPs in the aggregate will be referred to as the image sensor region. As described herein, the image sensor may include amplifiers, analog-to-digital converters (“ADCs”), comparators, controllers, counters, accumulators, registers, transistors, photodiodes, and the like. In different architectures, some of these components may be located within the image sensor region or external to the image sensor region, and some components may be located on a companion integrated circuit. In these embodiments, a lens (such as those of the microlens array 10) may be configured to direct light toward the actual light-sensing elements within the IP rather than, for example, on the amplifiers, comparators, controllers, and other components.

[0051] As noted above, an image sensor may include an array of multiple IPs. Each IP, in response to light (for instance, one or more photons), captures and stores a corresponding charge. In one embodiment, upon sampling an IP, if a pixel signal representative of the charge stored at the IP exceeds a sampling threshold, the pixel signal is converted to a digital value representing the pixel signal and the charge stored by the IP is reset. Alternatively, upon sampling an IP, a pixel signal representative of the charge stored at the IP is converted to a digital value representative of the pixel signal, and if the digital value exceeds a sampling

threshold, the charge stored by the IP is reset. In other embodiments, an analog-to-digital conversion is begun, and when enough of the conversion has been completed to determine whether the threshold is exceeded, a determination is made as to whether to continue the conversion. For instance, in a successive approximation register (“SAR”) ADC, if the threshold is equal to a most-significant-bit(s) pattern, as soon as the pattern is resolved a determination can be made as to whether to continue the conversion and perform a reset of the pixel, or stop the conversion. A determination of whether a pixel signal or a digital value representative of a pixel signal exceeds a sampling threshold can be made through the use of a comparator configured to compare the pixel signal or the digital value to a sampling threshold.

[0052] Figure 2 illustrates an analog pixel image sensor with multiple pixel signal thresholds, according to one embodiment. The image sensor of Figure 2 is a CMOS sensor, and includes an IP array 40. The IP array can include any number of columns and rows, with any number of IPs per column and per row. IP column 50, a column representative of full or partial IP columns in the IP array, is highlighted in Figure 2. The IP column 50 includes a plurality of IPs communicatively coupled via the column line 55. IP 60, an IP representative of IPs in the IP array, is highlighted in Figure 2.

[0053] The IP 60 includes a photo diode 65 together with control elements that enable the photo diode to be precharged in preparation for exposure and then sampled after exposure. In operation, a transistor 70 is switched on to couple the cathode of the photo diode to a voltage source and thus “precharge” the cathode of the photo diode to a precharge voltage. The transistor 70 is switched off at or before the start of an exposure interval. With the transistor 70 off, the cathode voltage incrementally discharges in response to photon strikes, lowering the photo diode potential, V_{DET} , in proportion to the amount of light detected. At the conclusion of the exposure interval, an access transistor 72 is switched on to enable a signal representative of the photo diode potential to be amplified/driven onto the column line 55 via follower-transistor 74 as pixel signal 80.

[0054] An ADC 85 is communicatively coupled to the IP column 50 via the column line 55. In the embodiment of Figure 2, the ADC is located at the edge of the pixel array 40, and may be located within or external to the image sensor on which the IP array is located. The ADC receives the pixel signal 80 (the representation of the analog photo diode potential) from the IP 60. The ADC digitizes the pixel signal to generate a 3-bit digital value (“Pix[2:0]”) representative of the pixel signal. The ADC includes 7 pixel thresholds, Threshold 1 to Threshold 7 (referred to herein as “ V_{T1} to V_{T7} ”). If the magnitude of the pixel signal is less than V_{pre} but greater than V_{T1} , the ADC converts the pixel signal to the digital value “000”. Pixel

signals less than V_{T1} but greater than V_{T2} are converted to the digital value “001”, pixel signals between V_{T2} and V_{T3} are converted to “010”, and so forth, up to pixel signals less than V_{T7} , which are converted to “111”.

[0055] In the embodiment of Figure 2, the potential difference between successive pixel thresholds is approximately the same (e.g., $V_{T3} - V_{T4} \approx V_{T5} - V_{T6}$). In other words, the pixel thresholds are linearly distributed between V_{T1} and V_{T7} . In addition, in the embodiment of Figure 2, the potential difference between V_{pre} and V_{T1} is greater than the potential difference between successive pixel thresholds (e.g., $V_{pre} - V_{T1} > V_{T3} - V_{T4}$), although in other embodiments all steps are equal. The selection of V_{T1} such that $V_{pre} - V_{T1} > V_{T3} - V_{T4}$ reduces the effect of, e.g., dark noise when sampling an IP. The potential difference between V_{T7} and V_{floor} in the embodiment of Figure 2 also can be greater than the potential difference between successive pixel thresholds (e.g., $V_{T7} - V_{floor} > V_{T3} - V_{T4}$). Finally, instead of linear threshold spacing, a given embodiment can space the thresholds exponentially, e.g., with each threshold spacing doubling from the one below. For systems that accumulate multiple ADC samples to form an image, exponential spacing is converted to a linear value prior to accumulation.

[0056] V_{floor} represents the pixel saturation threshold at which the cathode voltage of the photo diode 65 no longer linearly discharges in response to photon strikes. For pixel signals within the linear sensitivity region 90, the conversion of pixel signals to digital values is shown in graph 95. It should be noted that the maximum number of detectable photon strikes (i.e., the pixel saturation point) is proportional to the capacitance of the photo diode and thus its physical size. Consequently, in a traditional sensor design the photo diode footprint is dictated by the dynamic range required in a given application and does not scale appreciably with shrinking process geometries.

[0057] During the capture of an image, in one embodiment the IPs of a given row or rows in the IP column 50 and each other column in the IP array 40 are successively sampled and the pixel signals associated with each are converted into digital values using the ADC or ADCs associated with each column. The digital values output by the ADCs are accumulated (conditionally in some embodiments, as explained below) and stored during the image capture period. Other types and configurations of IPs than that illustrated in Figure 2 can be used in the image sensor system. For instance, a different arrangement of transistors can be used than the transistors 70, 72, and 74. In addition, although one ADC 85 is shown in Figure 2 in conjunction with the IP column 50, in other embodiments, more than one ADC can be used per IP column, with different ADC groups serving different sections of the array rows of the ADC column. Additional combinations of ADCs (in the form of read circuits) and IPs are described below in

greater detail. Finally, the output of the ADC (e.g. Pix[2:0] in the embodiment of Figure 2) can be any multi-bit length, and can be associated with any number of thresholds distributed in any manner between V_{pre} and V_{floor} .

Image Sensor System with Multi-bit Sampling and Conditional Reset

[0058] Figure 3 illustrates an example image sensor read circuit configured to convert a pixel signal into a multi-bit digital conversion, according to one embodiment. The embodiment of Figure 3 illustrates an IP 100, an IP memory 116, and a read circuit 110, the read circuit including an ADC/comparator circuit 112 (hereinafter “ADC/comparator”) and an adder 114. It should be noted that in other embodiments, the modules of Figure 3 can include additional, fewer, and/or different components. For example, the ADC/comparator can be implemented as separate components, and the adder can be located external to the read circuit.

[0059] The IP 100 represents an IP in an image sensor, and can be, for instance, the IP 60 of Figure 2. The IP 100 receives one or more control signals, for instance from external control logic. A control signal can enable the IP to begin an image capture, for instance by resetting the IP to V_{pre} and enabling the exposure of the IP’s photosensitive element to light to result in the storing of charge relative to V_{pre} . Similarly, a control signal can enable the IP to end an image capture, for instance by disabling the exposure of the IP’s photosensitive element to light after the passing of an image capture period. A control signal can also enable the outputting of a pixel signal by an IP and the subsequent conversion of the pixel signal to a digital value representative of the pixel signal by a read circuit (referred to herein as “sampling the IP” or “sampling the pixel signals”). As described above, a pixel signal can be a representation of the integrated charge (e.g., a source follower voltage, an amplified voltage, or a current having a component proportional to the integrated charge).

[0060] The IP 100 receives a reset signal, for instance from external control logic. The reset signal resets the charge stored by the IP to V_{pre} , for instance at the beginning of an image capture period. The IP also receives a conditional reset signal from the ADC/comparator 112 (in some circuits, the conditional reset and initial reset are supplied using common circuitry). The conditional reset signal resets the charge stored by the IP, for instance during an image capture period in response to a pixel signal exceeding a sampling threshold when the IP is sampled. It should be noted that in other embodiments, the conditional reset signal is received from a different entity. In one implementation, the ADC/comparator may determine that the pixel signal exceeds a sampling threshold, and may enable external control logic to output a conditional reset signal to the IP; in such an embodiment, the reset signal (a row-wise signal) and the conditional reset signal (a column-wise signal) may be ANDed by the IP to initiate all resets. For simplicity,

the remainder of the description will be limited to embodiments in which the ADC/comparator provides conditional reset signals to the IP.

[0061] The read circuit 110 receives a threshold signal, a sample signal (or “sample enable signal”), a compare signal (or “compare enable signal”), a residue signal (or “residue enable signal”), and a reset signal, for instance from external control logic, and receives pixel signals from the IP 100. The IP memory element 116 corresponding to IP 100 receives a readout signal that selects it for readout/write by adder 114 and for external readout. The ADC/comparator 112 samples the IP 100 in response to receiving one or more sample signals. During an image capture, the ADC/comparator receives a sample signal at various sampling intervals, for instance periodically or according to a pre-defined sampling interval pattern (referred to herein as a “sampling policy”). Alternatively, the sample signal received by the ADC/comparator can include a sampling policy, and the ADC/comparator can be configured to sample the IP based on the sampling policy. In other embodiments, the IP receives one or more sample signals and outputs pixel signals based on the received sample signals. In yet other embodiments, the IP outputs pixel signals periodically or according to a sampling policy, or the ADC/comparator samples pixel signals periodically or according to a sampling policy, independent of received sample signals. The ADC/comparator can request a pixel signal from the IP prior to sampling the pixel signal from the IP.

[0062] During a sampling of the IP, the ADC/comparator 112 receives a pixel signal from the IP and converts (optionally in some embodiments based on the pixel signal exceeding the sampling threshold) the pixel signal to a multiple-bit digital value representative of the pixel signal. If the pixel signal exceeds a sampling threshold, the ADC/comparator outputs a conditional reset signal to reset the charge stored at the IP. If the pixel signal does not exceed a sampling threshold, the ADC/comparator does not output a conditional reset signal to reset the charge stored at the IP. The sampling threshold can be varied during the image capture and received via the threshold signal, or can be pre-determined or preset for a given image capture. One sampling threshold can be used during multiple image captures, different sampling thresholds can be used for different image captures, and multiple sampling thresholds can be used during a single image capture. In one embodiment, the sampling threshold varies in response to detected changing light conditions (for instance, the sampling threshold can decrease in response to low light conditions, and can increase in response to high light conditions).

[0063] In one embodiment, the sampling threshold is an analog signal threshold. In this embodiment, the ADC/comparator 112 includes an analog comparator and compares the pixel signal to the sampling threshold to determine if the pixel signal exceeds the sampling threshold.

If the pixel signal includes a voltage representative of the charge stored by the IP 100, the sampling threshold is exceeded if the pixel signal is lower than the sampling threshold. Using the embodiment of Figure 2 as an example, if the sampling threshold of the ADC/comparator is Threshold 4, then the pixel signal will exceed the sampling threshold only if the pixel signal includes a voltage lower than the voltage associated with Threshold 4.

[0064] In one embodiment, the sampling threshold is a digital signal threshold. In this embodiment, the ADC/comparator 112 includes a digital comparator, and first converts the pixel signal to a digital value representative of the pixel signal. The ADC/comparator then compares the digital value to the sampling threshold to determine if the pixel signal exceeds the sampling threshold. Using the embodiment of Figure 2 as an example, for a sampling threshold of “101”, if the ADC/comparator converts a pixel signal to a digital value of “001” (indicating that the pixel signal is between Threshold 1 and Threshold 2), then the pixel signal does not exceed the sampling threshold and a conditional reset signal is not outputted. However, if the ADC/comparator converts a pixel signal to a digital value of “110” (indicating that the pixel signal is between Threshold 6 and Threshold 7), then the pixel signal does exceed the sampling threshold and a conditional reset signal is outputted.

[0065] In another embodiment, the sampling threshold is a digital signal threshold that can be evaluated prior to the complete digital conversion of the pixel signal. This can be advantageous in some embodiments or use cases to allow faster conditional reset of a pixel, and/or power savings by avoiding unneeded ADC operations. For instance, with a successive approximation register ADC, multiple clock cycles are used to resolve the digital representation of the pixel signal. The first clock cycle resolves the most significant bit, the second clock cycle the next most significant bit, etc., until all bit positions have been resolved. Using the embodiment of Figure 2 as an example, for a sampling threshold of “100,” a determination of whether the threshold is met or not can be resolved after the first SAR ADC clock cycle. For a sampling threshold of “110,” a determination of whether the threshold is met or not can be resolved after the second SAR ADC clock cycle. For embodiments with a bit depth of, e.g., 6 or 8 bits, making a reset determination after one or two conversion cycles can result in significant time/power savings, which can be realized by selecting a sampling threshold with one or more LSBs that are 0.

[0066] In one embodiment, a row-wise compare signal is supplied to each ADC/comparator “compare” signal input, and signals the ADC/comparator as to the appropriate clock cycle to perform the comparison. When the compare signal is asserted, the comparison is performed based on the current state of the analog-to-digital conversion. If the threshold is met by the

compare for ADC/comparator 112, the conditional reset signal is asserted to IP 100 and to adder 114, and the SAR ADC continues converting the pixel signal. If the threshold is not met, the conditional reset signal is not asserted, and can be used in conjunction with the compare signal to gate the clock signal of SAR ADC to terminate the conversion.

[0067] The ADC/comparator 112 outputs a digital value representative of a pixel signal received by the ADC/comparator (referred to herein as a “digital conversion”) to the adder 114. The ADC/comparator 112 can output a digital conversion in response to the pixel signal associated with the digital conversion exceeding a sampling threshold. The conditional reset signal can be used as an enable to signal to the adder 114 to load the digital conversion and add it to the IP memory 116 location corresponding to IP 100 (which in this embodiment is selected from a plurality of such locations by address selection of the readout line). In other embodiments, the ADC/comparator outputs a digital conversion during each sampling of the IP 100, regardless of whether the pixel signal associated with the digital conversion exceeds a sampling threshold. In these embodiments, the adder can be configured to accumulate digital conversions associated with pixel signals that exceed a sampling threshold and to disregard digital conversions associated with pixel signals that do not exceed a sampling threshold. Alternately, if the threshold is set to “001” in Figure 2, for example, the adder can unconditionally add the digital conversion to IP memory 116 each time IP 100 is read, while still producing correct results.

[0068] In one embodiment, the ADC/comparator 112 also outputs a digital conversion in response to receiving a residue signal assertion (without the compare signal being asserted). The residue signal assertion is associated with the end of an image capture, and enables the ADC/comparator to output a full digital conversion to the adder 114 regardless of whether the pixel signal associated with the digital conversion exceeds a sampling threshold, and asserts the conditional reset. The residue signal can prevent the loss of image information associated with light received by the IP 100 but not surpassing the threshold at the end of a capture period. If the pixel signal representative of such received light does not exceed the sampling threshold, the ADC/comparator otherwise may not output the digital conversion associated with the pixel signal, and the charge stored by the IP would not be reset by the conditional reset signal (which is also triggered by assertion of the residue signal). In embodiments where the ADC/comparator outputs digital conversions to the adder regardless of whether the pixel signals associated with the digital conversions exceed a sampling threshold, the adder can receive the residue signal, and can be configured to accumulate a digital conversion associated with a pixel signal received at the end of a capture period in response to receiving the signal.

[0069] The adder 114 is configured to accumulate digital conversions received during a capture period. As discussed above, in embodiments in which the ADC/comparator 112 outputs digital conversions only if the pixel signals associated with the digital conversions exceed a sampling threshold, the adder accumulates all received digital conversions (including the additional digital conversion output by the ADC/comparator in response to receiving a residue signal) into IP memory 116. In embodiments in which the ADC/comparator outputs digital conversions associated with each received pixel signal, the adder accumulates only the digital conversions associated with pixel signals that exceed the sampling threshold, plus the digital conversion output by the ADC/comparator in response to receive a residue signal, into IP memory 116; such embodiments require the adder to be aware of when pixel signals exceed a sampling threshold and when a residue signal is received, and are not discussed further herein for the purpose of simplicity.

[0070] The adder 114 receives reset/add control signaling, for instance from external control logic. In response to receiving a reset signal (for instance at the beginning of an image capture period), the accumulator stores all zeros to the selected IP memory location 116 the accumulation of received digital conversions as image data. The adder also receives a reset signal and resets the accumulation of received digital conversions.

[0071] In alternative embodiments, the adder is located external to the read circuit 110. For instance, the ADC/comparator can output a stream of conversions to a digital channel (e.g., multiplexed with other conversions from other ADCs) to a separate circuit that supplies the accumulation function. In such a case, the ADC/comparator must also output a symbol for “no conversion,” which can be 0. One possibility is for a circuit in the digital channel interface (e.g., PHY 134 in Figure 4) to code digital conversions to reduce bandwidth. A “no conversion” in one embodiment is output as a “00,” a upper threshold exceeded ADC conversion is output as a “01,” and all other ADC conversions are output as “1xxxxxx,” where an x represents one of the resolved bits of the ADC conversion and the number of x positions is equal to the bit depth of the ADC.

[0072] In one embodiment, the IP is configured to output a pixel signal and receive a conditional reset on the same line. In this embodiment, the IP and the ADC/comparator 112 alternately drive the pixel signal and the conditional reset on the shared line. For example, the IP can output a pixel signal on the shared line during a first portion of a sample period, and can receive conditional resets on the shared line during a second portion of a sample period. Finally, the ADC/comparator can receive a threshold signal, a sample signal, and a residue signal on a shared line. For example, the ADC/comparator can receive a threshold signal at the beginning of

an image capture, can receive sample signals throughout the image capture period, and can receive a residue signal at the end of the image capture period. It should also be noted that the reset signal received by the IP can be the same reset signal received by the accumulator 114, and can be received on a shared line.

[0073] Figure 4 illustrates an example embodiment of an image sensor system with a multi-bit architecture, according to one embodiment. The image sensor system 120 of Figure 4 includes an image sensor region 125, a read circuit array 130, control logic 132, and a physical signaling interface 134. In other embodiments, the image sensor system may include fewer, additional, or different components than illustrated in the embodiment of Figure 4 (for instance, the circuit may have memory 116 integrated therewith). The image sensor system shown in Figure 4 can be implemented as a single IC, or can be implemented as multiple ICs (for instance, the image sensor region and the read circuit array can be located on separate ICs). Further, various components (such as the read circuit array, the control logic, and the physical signaling interface) can be integrated within the image sensor region 125.

[0074] For purposes of example, the image sensor system 120 and a host IC (not shown in Figure 4) communicatively coupled to the image sensor system are assumed to form the primary image acquisition components within a camera (e.g., a still-image or video camera within a mobile device, compact camera, digital SLR camera, stand-alone or platform-integrated webcam, high-definition video camera, security camera, automotive camera, etc.). The image sensor IC and host IC can be more generally deployed alone or together with like or different imaging components within virtually any imaging system or device including without limitation metrology instruments, medical instruments, gaming systems or other consumer electronics devices, military and industrial imaging systems, transportation-related systems, space-based imaging systems and so forth. Operation of the image sensor system generally involves the capture of an image or frame through the exposure of IPs to light, the conversion of stored charge as a result of the exposure into image data, and the outputting of the image data to a storage medium.

[0075] The image sensor region 125 includes an IP array 127 including N-rows (indexed from 0 to N-1) and M-columns (indexed from 0 to M-1). The physical signaling interface 134 is configured to receive commands and configuration information from a host IC (e.g., a general-purpose or special-purpose processor, application-specific integrated circuit (ASIC) or any other control component configured to control the image sensor IC), and is configured to provide the received commands and configuration information to the control logic 132. The physical

signaling interface is also configured to receive image data from the read circuit array 130 and to output received image data to the host IC.

[0076] The control logic 132 is configured to receive commands and configuration information from the physical signaling interface 134, and is configured to transmit signals configured to manipulate the operations and functionality of the image sensor system 120. For example, in response to receiving a command to capture an image or frame, the control logic may output a series of exposure signals (configured to cause IPs to reset) and sample signals (configured to cause the read circuits in the read circuit array 130 to sample the pixel signals from the IPs in the IP array 127), enabling the capture of the image or frame by the image sensor system. Similarly, in response to receiving a command to initialize or reset the image sensor system, the control logic may output reset signals configured to reset each IP in the IP array, causing each IP to disregard any accumulated charge. The control signals produced by the control logic identify particular IPs within the IP array for sampling, may control the functionality of read circuits associated with IPs, or may control any other functionality associated with the image sensor system. The control logic is shown in Figure 4 as external to the image sensor region 125, but as noted above, all or portions of the control logic may be implemented locally within the image sensor region.

[0077] The control logic 132 outputs control and reset signals for each IP in the image sensor region 125. As illustrated in the embodiment of Figure 4, each IP in an image pixel IP[X][Y] receives a row-parallel Cntrl[X] signal (corresponding to a “row” select control signal for each IP) and a row-parallel Reset[X] signal from the control logic to reset the IPs, wherein “X” and “Y” refer to the coordinates of the IP within the image sensor region. Although the control signal and reset signals received at any given IP are each only 1 bit as indexed in the embodiment of Figure 4, it is to be appreciated that such an indexing is done for the purposes of simplicity only, and that these signals may in practice be any width or dimension.

[0078] The read circuit array 130 includes M read circuits, each configured to receive pixel signals from a column of IPs in the IP array 127. It should be noted that in other embodiments, the read circuit array can include multiple read circuits configured to receive pixel signals from each IP column, as is discussed in figures 5a, 5b, and 5c. A pixel signal bus couples the IPs in each IP column in the IP array to the read circuit associated with the IP column within the read circuit array. Each IP is configured to output a pixel signal produced by the IP to the pixel signal bus, and each read circuit is configured to sample the pixel signals from the IPs in the IP column associated with the read circuit. For example, read circuit 0 is configured to sample pixel signals from pixel signal bus 0, and so forth. Each read circuit in the read circuit array can sample pixel

signals iteratively from IPs in the IP column associated with the read circuit (for instance, by sampling pixel signals from successive IPs in order over multiple passes), or can sample pixel signals according to a pre-determined non-sequential order. In one embodiment, read circuits can sample multiple pixel signals simultaneously. Although not illustrated in the embodiments of Figure 3 and Figure 4, the read circuits can additionally include memories configured to store accumulated digital values prior to outputting the accumulated values as image data.

[0079] A conditional reset bus couples the IPs in each IP column in the IP array 127 to the read circuit associated with each IP column. After sampling a pixel signal from an IP in an IP column, the read circuit associated with the IP column produces a conditional reset signal if the sampled pixel signal exceeds a sampling threshold. For example, if an IP in an IP column outputs a pixel signal to a read circuit associated with the IP column via the pixel signal bus coupling the IP to the read circuit, and if the read circuit determines that the pixel signal exceeds a sampling threshold, the read circuit outputs a conditional reset signal to the IP via the conditional reset bus coupling the read circuit to the IP and the IP resets the charge stored at the IP. As described above, the pixel signal bus and the conditional reset bus can be implemented in a shared bus with Cntrl[X] enabling pixel signals to be output from row X to the shared bus and Reset[X] enabling conditional reset for pixels in row X from the shared bus, though such embodiments are not described further herein for the purposes of simplicity.

[0080] The control logic 132 produces read control signals for the read circuits in the read circuit array 130. The read control signals can control the sampling of pixel signals from the IPs in the IP array 127 by the read circuits, the conversion of sampled pixel signals into digital values, the accumulation of the digital values, the outputting of the accumulated digital values, and the resetting of the adders. The read control signals can include a threshold signal, a sample signal, a compare signal, a residue signal, a readout signal, and a reset/add signal for each read circuit in the read circuit array as described in Figure 3.

[0081] The control logic 132 is configured to produce read control signals for the read circuit array 130 to enable the capture of an image over an image capture period. Prior to the image capture period or at the first use of a particular IP memory location for an image capture period, the control logic can produce a reset to cause the accumulator of each read circuit 110 to reset the IP memory location. At the beginning of the image capture period, the control logic can produce a threshold signal for each of the read circuits; as discussed above, the threshold signal is used by each read circuit to determine a threshold to which pixel signals are compared for the purposes of conditionally resetting IPs associated with the pixel signals and accumulating digital values associated with the pixel signals. During the image capture period, the control logic can

produce a series of sample signals configured to enable the read circuits to sample pixel signals from IPs associated with the read circuits. In one embodiment, the control logic produces sample signals according to one or more sampling policies. Sampling policies are described in greater detail below. At the end of the image capture period, the controlled logic produces a residue signal configured to enable each read circuit to accumulate a digital value representative of a pixel signal regardless of whether the pixel signal exceeds a sampling threshold. After the image capture period, the control logic produces a readout signal configured to enable each read circuit to output the accumulated digital values representative of sampled pixel signals that exceed an associated sampling threshold as image data. The control logic may also produce a reset signal after each image capture period to reset the accumulated digital values within each read circuit.

[0082] The control logic may also be configured to produce pause and resume signals configured to cause the IPs and the read circuits to pause and resume an image capture, and to produce any other signal necessary to control the functionality of the IPs and read circuits in the read circuit array. For each read circuit, the image data output by the read circuit is a digital representation of the light captured by each IP in an IP column associated with the read circuit. The image data is received by the physical signaling interface for subsequent output to a host IC.

[0083] Figure 5 illustrates an example image sensor system architecture with read circuit arrays located peripherally to an IP array, according to one embodiment. In the architecture of Figure 5, six read circuit arrays (140a, 140b, 140c, 140d, 140e, and 140f) are located around an image sensor region 145 including an IP array. Unlike the embodiment of Figure 4, in which one read circuit array 130 is located to one side of the image sensor region 125, the read circuit arrays 140 of Figure 5 are located on all sides of the image sensor region 145. The read circuit arrays can be located within an IC also containing the image sensor region, or can be located on one or more separate ICs. For example, each read circuit array could be located on the periphery of an image sensor IC, or could be located in dedicated read circuit array ICs located adjacent to the image sensor IC.

[0084] In the previous embodiment of Figure 4, each read circuit in the read circuit array 130 is coupled to an IP column in the IP array 127. In the embodiment of Figure 5, each read circuit array 140x is coupled to a set of six IPs from partial rows and partial columns of the image sensor region 145. For example, read circuit array 140a is coupled to IP1, IP2, IP3, IP7, IP8, and IP9. Each read circuit array 140x includes one or more read circuits. In one embodiment, each read circuit array includes 6 read circuits, with each read circuit in a read circuit array coupled to one IP. In such an embodiment, each read circuit samples only the IP to which it is coupled. More typically, each read circuit will be shared by a block of IPs comprising

a large number of rows and one or more columns. Although control logic is not illustrated in the embodiment of Figure 5, each read circuit array can be coupled to universal control logic, or each may be coupled to dedicated control logic. Further, although a physical signaling interface is not illustrated in the embodiment of Figure 5, each read circuit array may output image data via a common bus to a common physical signaling interface, or may output image data via a dedicated bus to a dedicated physical signaling interface coupled to each read circuit array.

[0085] Figure 6a illustrates a top view of a pixel array IC in an example two-layer image sensor system architecture, according to one embodiment. The pixel array IC of Figure 6a includes peripheral circuitry 162 surrounding an IP array. The IP array includes row control circuitry 164 and four row groups of IPs (IP Row Groups 0 through 3). Each IP row group is the width of the array and includes one-fourth of the rows in the array, and the row control circuitry provides control and reset signals needed for operation of the IPs (for instance, signals configured to cause the IPs to be enabled for reset and selected for readout, and any other signals discussed herein).

[0086] Figure 6b illustrates a top view of a preprocessor IC in an example two-layer image sensor system architecture, according to one embodiment. The preprocessor IC of Figure 6b includes peripheral circuitry 172 surrounding a read circuit array. The read circuit array includes a physical signaling interface 175 (which may alternately be on pixel array IC 160), read control circuitry 176, four read circuit arrays (read circuit array 0 through 3), and accompanying memory groups 0A/B, 1A/B, 2A/B, and 3A/B. Each read circuit array includes one or more read circuits (including an ADC, adder, and reset logic for each IP column) connected to corresponding rows in an associated memory group. When a particular IP row is selected in an IP row group of the pixel array IC, a corresponding row in the corresponding memory group is selected on the preprocessor IC.

[0087] Figure 6c illustrates a cross section of the pixel array IC of Figure 6a and the preprocessor IC of Figure 6b in an example two-layer image sensor system architecture, according to one embodiment. In the embodiment of Figure 6c, the pixel array IC 160 is located above the preprocessor IC 170 such that the bottom surface of the pixel array IC is coupled to the top surface of the preprocessor IC. A microlens array 180 and a color filter array 182 are located above the pixel array IC. The pixel array IC and the processor IC are coupled via pixel array IC wiring 184 and preprocessor IC wiring 186. By locating the pixel array IC above the preprocessor IC, the die size and percentage of surface area in the image sensor system capable of capturing light is increased. For instance, in a single-layer IC architecture including an IP array and one or more read circuit arrays, the portion of the single-layer IC including the one or

more read circuit arrays are incapable of capturing light; such an embodiment reduces the percentage of silicon die used to capture light incident upon the single-layer IC. This requires the camera module footprint to be larger than the lens and the imaging array, and increases the cost and size of the camera module. The top-layer of the embodiment of Figure 6c, in contrast, does not include read circuit arrays, so the die size of the top single layer IC is reduced to approximately the size of the IP array. Light incident upon the top-layer passes through the microlens array and the color filter array, is captured by the IPs in the IP array, and signals representative of the captured light are sampled by the read circuit arrays via the pixel array IC wiring and the preprocessor IC wiring.

[0088] Figure 7 illustrates the operation of an image sensor read circuit, such as the read circuit of Figure 3, according to one embodiment. In the example embodiment of Figure 7, an image is captured over the course of 16 sampling intervals. The ADC of the example embodiment of Figure 7 converts pixel signals to 5-bit digital values, and the accumulator accumulates 5-bit digital values into a 9-bit digital value during the image capture period. Further, in the embodiment of Figure 7, the ADC converts received pixel signals into digital values representing the pixel signals such that each additional photon detected by an IP results in an increase in the digital value by one. For example, if an IP detects 5 photons after being reset, the pixel signal produced by the IP will be converted by the ADC into the value “00101”. It should be emphasized that in other embodiments, the ADC converts received pixel signals into digital values representing the pixel signals such that multiple additional photons detected by an IP results in an increase in the digital value by one. In the embodiment of Figure 7, pixel signals are analog voltages, and thus aren’t shown in Figure 7 for the purposes of simplicity.

[0089] At the beginning of the image capture period (sampling interval 0), a control signal is received configured to configure an IP of the read circuit to be reset and begin exposure. In the embodiment of Figure 7, the “begin exposure” control signal also resets the value stored at the memory element corresponding to the IP to zero. In addition, a threshold signal is received to set the sampling threshold for the read circuit at a pixel signal equivalent to 20 photons.

[0090] During the first sampling interval, 4 photons are detected by the IP. The IP then produces a pixel signal representing the charge collected by a photosensitive element within the IP equivalent in response to detecting the 4 photons, and the ADC converts this pixel signal to the digital value “00100”. Since the 4 detected photons do not trigger the sampling interval of 20 photons (“10100”), the accumulator does not accumulate the digital value “00100”, and the charge stored by the IP is not dissipated (the IP is not reset). Note that the column “Photons (det.

– accum.)” indicates first the number of photons detected by the IP during a particular sampling interval and second the number of accumulated photons since the last conditional reset of the IP.

[0091] During sampling interval 2, 7 additional photons are detected by the IP. The charge stored by the IP increases from the charge produced in response to detecting 4 photons during sampling interval 1 to a charge produced in response to detecting 11 accumulated photons (4 photons during sampling interval 1 and 7 photons during sampling interval 2). The pixel signal produced by the IP in response to the stored charge is converted to the digital value “01011”. Since the total 11 photons do not trigger the sampling threshold of 20 photons, the accumulator does not accumulate the digital value “01011”, and the IP is not reset. Similarly, during sampling interval 3, 2 additional photons are detected by the IP, and the charge stored by the IP increases to a charge produced in response to detecting 13 accumulated photons (4 photons during sampling interval 1, 7 during sampling interval 2, and 2 during sampling interval 3). The pixel signal produced by the IP in response to this increased stored charge is converted to the digital value “01101”. Since the accumulated 13 photons do not trigger the sampling threshold of 20 photons, the accumulator does not accumulate the digital value “01101”, and the IP is not reset.

[0092] During sampling interval 4, 11 additional photons are detected by the IP. The charge stored by the IP increases to a charge equivalent to detecting 24 accumulated photons (4 during sampling interval 1, 7 during sampling interval 2, 2 during sampling interval 3, and 11 during sampling interval 4). The pixel signal produced by the IP in response to the stored charge is converted to the digital value “11000”. Since the accumulated 24 photons exceeds the sampling threshold of 20 photons, the adder accumulates the digital value “11000” into the memory element for the IP, and the IP is reset.

[0093] The 14 photons detected during sampling interval 5 do not exceed the sampling interval of 20, the digital value produced by the ADC, “01110” is not accumulated and the IP is not reset. The 8 photons detected during sampling interval 6 results in an accumulated detection of 22 photons by the IP (14 photons during sampling interval 5, and 8 during sampling interval 6), and the adder accumulates the digital value “10110” (resulting in a total accumulated value of “000101110” into the memory element), and the IP is reset.

[0094] This process is repeated for each of the 16 sampling intervals. The digital values produced by the ADC during sampling intervals 10, 14, and 15 are all accumulated in response to the sampling threshold of 20 photons being exceeded by the number of accumulated photons detected by the IP. Accordingly, the IPs are reset for the sampling intervals following these intervals (sampling interval 11, 15, and 16). During sampling interval 16, 19 photons are

detected by the IP, which does not exceed the sampling threshold of 20 photons. In addition, during sampling interval 16, a residue signal is received configured to instruct the accumulator to accumulate the digital value produced by the ADC (the residue value 190, "10011"). Accordingly, the adder accumulates the value "10011" to the maintained accumulation value "001111011" in the memory element to produce the image data 195, "010001110". Finally, a reset signal is received during sampling interval 16, which enables the read circuit to output the image data and which resets the values output by the ADC and stored at the accumulator to zero subsequent to outputting the image data.

[0095] Figure 8 illustrates pixel information flow in an image capture system, according to one embodiment. During the course of an image capture period, an IP 200 detects photons and outputs pixel signals 202 to the read circuit. In response, the read circuit 204 converts the received pixel signals to digital values representative of the receive pixel signals, and for each digital value associated with a pixel signal that exceeds a sampling threshold, accumulates the digital value and resets the IP. After the image capture period, the accumulated digital values are output as image data 206.

[0096] A post processing module 208 receives the image data 206 and performs one or more processing operations on the image data to produce the processed data 210. In one embodiment, a response function can be used to transform the image data 206 according to a desired response. For example, the image data can be transformed with a linear function or a logarithmic function based on the intensity of the light detected by the IP. The processed data is then stored in memory 212 for subsequent retrieval and processing. The IP 200, the read circuit 204, the post processing module, and the memory can be located within an IC, or can be located within separate coupled ICs.

[0097] Figure 9 illustrates various temporal sampling policies for use by an image sensor read circuit, such as the read circuit of Figure 3, according to one embodiment. In the embodiment of Figure 9, an image is captured over an image capture period 220 equivalent to 16 time units. For each of the three illustrated sampling policies, an "x" indicates the sampling of a given IP by a read circuit.

[0098] In sampling policy 1, the read circuit samples the IP after each of the 16 time units. In sampling policy 2, the read circuit samples the IP after every 4 time units. As the read circuit in sampling policy 2 samples the IP less frequently than the read circuit in sampling policy 1, the IP in sampling policy 2 is more likely to saturate than the IP in sampling policy 1. However, the resources (processing, bandwidth, and power) required to implement sampling policy 2 (4 total samples) may be lower than the resources required to implement sampling policy 1 (16 total

samples), since the read circuit in sampling policy 2 samples the IP only 25% as often as the read circuit in sampling policy 1.

[0099] In sampling policy 3, the read circuit samples the IP after time units 1, 2, 4, 8, and 16. The exponential spacing of the samplings of sampling policy 3 provide short sample intervals (for instance, the sample interval between time unit 0 and time unit 1) and long sample intervals (for instance, the sample interval between time unit 8 and time unit 16). Allowing for both short and long sampling intervals preserves the dynamic range of sampling policy 1 with nearly as few samplings as sampling policy 2 (5 samplings for sampling policy 3 vs. 4 samplings for sampling policy 2). Other sampling policies not illustrated in Figure 9 may also be implemented by read circuits in the image sensor systems described herein. Depending on the overall length of an exposure interval or other scene- or user-dependent factors, different sampling policies can be selected to meet desired power, SNR, dynamic range, or other performance parameters.

High-SNR Image Sensor with Non-Destructive Threshold Monitoring

[00100] While the three-transistor (3T) pixel architecture shown in Figure 2 is suitable for many applications, four-transistor (4T) designs having a “transfer gate” disposed between the photodiode and source follower (i.e., between node “ V_{DET} ” of photosensitive element 65 and element 74 in Figure 2) provide a number of advantages. First, the now-isolated floating diffusion at the gate of the source follower may be reset (e.g., coupled to V_{DD}) without disturbing the charge state of the photodiode, thereby enabling a correlated double-sampling (CDS) operation in which the noise floor of the floating diffusion is sampled prior to charge integration and then subtracted from the subsequent sampling of the photodiode potential, canceling the noise and significantly improving the SNR. Another advantage is, counterintuitively, a more compact pixel design as the switched connection between the photodiode and source follower (i.e., via the transfer gate) enables the source follower, reset and access transistors to be shared among multiple photodiodes. For example, only seven transistors are required to implement a set of four “4T” pixels having a shared source follower, reset transistor and access transistor (i.e., four transfer-gates plus the three shared transistors), thus effecting an average of 1.75 transistors per pixel (1.75T).

[00101] In terms of pixel read-out, the direct connection between photodiode and source follower in a 3T pixel permits the charge state of the photodiode to be read-out without disturbing ongoing photocharge integration. This “non-destructive read” capability is particularly advantageous in the context of the conditional reset operation described above as the 3T pixel may be sampled following an integration interval and then conditionally permitted to

continue integrating charge (i.e., not be reset) if the sampling operation indicates that the charge level remains below a predetermined threshold. By contrast, the charge transfer between photodiode and floating diffusion as part of a 4T pixel readout disrupts the state of the photodiode, presenting a challenge for conditional-reset operation.

[00102] In a number of embodiments described below in connection with Figures 10-14, a modified 4T pixel architecture is operated in a manner that dissociates the reset threshold from pixel sample generation to enable a non-destructive (and yet CDS) over-threshold determination. That is, instead of reading out the net level of charge accumulated within the photodiode (i.e., a pixel sampling operation) and conditionally resetting the photodiode based on that read-out (i.e., as in a 3T pixel sampling operation), a preliminary over-threshold sampling operation is executed to enable detection of an over-threshold state within the photodiode, with the full photodiode read-out (i.e., pixel sample generation) being conditionally executed according to the preliminary over-threshold detection result. In effect, instead of conditionally resetting the photodiode according to the pixel value obtained from full photodiode readout, full photodiode readout is conditioned on the result of a preliminary, non-destructive determination of whether the threshold has been exceeded; an approach enabled, in at least one embodiment, by dissociating the conditional-reset threshold from the pixel value generation.

[00103] Figure 10 illustrates an embodiment of a modified 4T pixel 250, referred to herein as a “progressive read-out pixel,” in which a non-destructive over-threshold detection operation is executed to enable conditional-reset operation in conjunction with correlated double sampling. As explained more fully below, the over-threshold detection involves a limited read-out of the photodiode state which, when determined to indicate an over-threshold condition, will trigger a more complete read-out of the photodiode state. That is, pixel 250 is read-out in a progression from a limited over-threshold detection read-out to a complete read-out (the latter being conditional according to the over-threshold detection result).

[00104] Still referring to Figure 10, progressive read-out pixel 250 includes a transfer gate 251 disposed between a photodiode 260 (or any other practicable photosensitive element) and floating diffusion node 262, and a transfer-enable transistor 253 coupled between a transfer-gate row line (TGr) and transfer gate 251. The gate of transfer-enable transistor 253 is coupled to a transfer-gate column line (TGc) so that, when TGc is activated, the potential on TGr is applied (minus any transistor threshold) via transfer-enable transistor 253 to the gate of transfer-gate 251, thus enabling charge accumulated within photodiode 260 to be transferred to floating diffusion 262 and sensed by the pixel readout circuitry. More specifically, floating diffusion 262 is coupled to the gate of source follower 255 (an amplification and/or charge-to-voltage

conversion element), which is itself coupled between a supply rail (V_{DD} in this example) and a read-out line, V_{out} , to enable a signal representative of the floating diffusion potential to be output to read-out logic outside the pixel.

[00105] As shown, a row-select transistor 257 is coupled between the source follower and the read-out line to enable multiplexed access to the read-out line by respective rows of pixels. That is, row-select lines (“RS”) are coupled to the control inputs of row-select transistors 257 within respective rows of pixels and operated on a one-hot basis to select one row of pixels for sense/read-out operations at a time. A reset transistor 259 is also provided within the progressive read-out pixel to enable the floating diffusion to be switchably coupled to the supply rail (i.e., when a reset-gate line (RG) is activated) and thus reset. The photodiode itself may be reset along with the floating diffusion by fully switching on transfer gate 251 (e.g., by asserting TGc while TGr is high) and reset transistor 259 concurrently, or by merely connecting the photodiode to a reset-state floating diffusion.

[00106] Figure 11 is a timing diagram illustrating an exemplary pixel cycle within the progressive read-out pixel of Figure 10. As shown, the pixel cycle is split into five intervals or phases corresponding to distinct operations carried out to yield an eventual progressive read-out in the final two phases. In the first phase (phase 1), a reset operation is executed within the photodiode and floating diffusion by concurrently asserting logic high signals on the TGr, TGc and RG lines to switch on transfer-enable transistor 253, transfer gate 251 and reset transistor 259, thereby switchably coupling photodiode 260 to the supply rail via transfer gate 251, floating diffusion 262 and reset transistor 259 (the illustrated sequence can begin with an unconditional reset (e.g., at the start of a frame), and can also begin from a preceding conditional read-out/reset operation). To conclude the reset operation, the TGr and RG signals (i.e., signals applied on like-named signal lines) are lowered, thereby switching off transfer gate 251 (and reset transistor 259) so that the photodiode is enabled to accumulate (or integrate) charge in response to incident light in the ensuing integration phase (phase 2). Lastly, although the row-select signal goes high during the reset operation shown in Figure 11, this is merely a consequence of an implementation-specific row decoder that raises the row-select signal whenever a given row address is decoded in connection with a row-specific operation (e.g., raising the TGr and RG signals during reset directed to a given row). In an alternative embodiment, the row decoder may include logic to suppress assertion of the row-select signal during reset as indicated by the dashed RS pulse in Figure 11.

[00107] At the conclusion of the integration phase, the floating diffusion is reset (i.e., by pulsing the RG signal to couple the floating diffusion to the supply rail) and then sampled by a

sample-and-hold element within the column read-out circuit. The reset and sample operation (shown as phase 3 in Figure 11), in effect, samples the noise level of the floating diffusion and is executed in the embodiment shown by asserting the row-select signal for the pixel row of interest (i.e., the “ith” pixel row, selected by RSi) while pulsing a reset-state sample-and-hold signal (SHR) to convey the state of the floating diffusion to the sample-and-hold element (e.g., a switch-accessed capacitive element) within the column read-out circuit via read-out line, Vout.

[00108] After acquiring the noise sample in phase 3, an over-threshold detection operation is executed in phase 4 by raising the TGr line to a partially-on, “over-threshold-detection” potential, VTG_{partial} , concurrently with switching on transfer-enable transistor 253 (i.e., by asserting a logic high TGc signal, although in this embodiment TGc is already on). By this operation, illustrated graphically in Figures 12 and 13, VTG_{partial} is applied to transfer gate 251 to switch the transfer gate to a “partial on” state (“TG partial on”). Referring to Figures 12 and 13, electrostatic potential diagrams for photodiode 260 (a pinned photodiode in this example), transfer gate 251 and floating diffusion 262 are shown below their corresponding schematic cross-section diagrams. Note that the depicted levels of electrostatic potential are not intended to be an accurate representation of the levels produced in an actual or simulated device, but rather a general (or conceptual) representation to illustrate the operation of the pixel read-out phases. Upon application of VTG_{partial} to transfer gate 251, a relatively shallow channel potential 271 is formed between photodiode 260 and floating diffusion 262. In the example of Figure 12, the level of charge accumulated within the photodiode at the time of the over-threshold detection operation (phase 4) does not rise to the threshold level required for charge to spill over (i.e., be transferred) to the floating diffusion via the shallow channel potential of the partially-on transfer gate. Accordingly, because the accumulated charge level does not exceed the spillover threshold established by application of VTG_{partial} to the control node of transfer gate 251, there is no spillover from the photodiode to the floating diffusion and the accumulated charge instead remains undisturbed within the photodiode. By contrast, in the example of Figure 13, the higher level of accumulated charge does exceed the spillover threshold so that a portion of the accumulated charge (i.e., that subset of charge carriers that are above the transfer gate partially-on electrostatic potential) spills over into floating diffusion node 262, with the residual accumulated charge remaining within the photodiode as shown at 272.

[00109] Still referring to Figures 11, 12 and 13, prior to conclusion of over-threshold detection phase 4, the charge level of the floating diffusion is sampled and held within a signal-state sample-and-hold element (i.e., in response to assertion of signal SHS) to yield a threshold-test sample -- the difference between the signal-state sample and the previously obtained reset-

state sample -- to be evaluated with respect to a conditional-reset threshold. In one embodiment, the conditional-reset threshold is an analog threshold (e.g., to be compared with the threshold-test sample in a sense amplifier in response to assertion of a compare/convert strobe signal) set or programmed to a setting above the sampling noise floor, but low enough to enable detection of minute charge spillover via the shallow transfer gate channel. Alternatively, the threshold-test sample may be digitized in response to assertion of the compare/convert signal (e.g., within an analog-to-digital converter that is also used to generate the finalized pixel sample value) and then compared with a digital conditional-reset threshold, again, set (or programmed to a setting) above the noise floor, but low enough to enable detection of trace charge spillover. In either case, if the threshold-test sample indicates that no detectable spillover occurred (i.e., threshold-test sample value is less than conditional-reset spillover threshold), then the photodiode is deemed to be in the under-threshold state shown in Figure 12 and the TGc line is held low in the ensuing conditional read-out phase (phase 5, the final phase) to disable transfer gate 251 for the remainder of the progressive read-out operation – in effect, disabling further read-out from the photodiode and thus enabling the photodiode to continue integrating charge without disruption for at least another sampling interval. By contrast, if the threshold-test sample indicates a spillover event (i.e., threshold-test sample greater than conditional-reset/spillover threshold), then the TGc line is pulsed during the conditional read-out phase concurrently with application of a fully-on, “remainder-transfer” potential, VTG_{full} , to the TGr line, thereby enabling the remainder of the charge (i.e., charge 272 as shown in Figure 13) within photodiode 260 to be transferred to floating diffusion 262 via the full-depth transfer-gate channel (273) so that, between the over-threshold transfer in phase 4 and the remainder transfer in phase 5, the charge accumulated within the photodiode since the hard reset in phase 1 is fully transferred to the floating diffusion where it may be sensed in a pixel read-out operation. In the embodiment shown, the pixel-readout operation is effected by pulsing the SHS signal and compare/convert strobe in sequence during conditional read-out phase 5, though either or both of those pulses may optionally be suppressed in absence of an over-threshold detection. Note that conditional read-out of the photodiode (i.e., effected by pulsing TGc in conjunction with application of VTG_{full} on TGr) effectively resets the photodiode (i.e., drawing off all charge to the floating diffusion), while suppression of the conditional read-out leaves the integration state of the photodiode undisturbed. Accordingly, execution of the conditional read-out operation in phase 5 conditionally resets the photodiode in preparation for integration anew in the succeeding sampling interval (subframe) or refrains from resetting the photodiode to enable cumulative integration in the subsequent sampling interval. Thus, in either case, a new integration phase

follows phase 5, with phases 2-5 being repeated for each subframe of the overall frame (or exposure) interval, before repeating the hard reset in a new frame. In other embodiments, where cumulative integration is permitted across frame boundaries, the hard reset operation may be executed to initialize the image sensor and omitted for an indeterminate period of time thereafter.

[00110] Figure 14 illustrates an embodiment of an image sensor 300 having a progressive-readout pixel array 301, sequencing logic 303, row decoder/driver 305 and column read-out circuit 307. While pixel array 301 is shown to include four rows and two columns of shared-element pixels, other embodiments may include many more pixel rows and columns to implement, for example, a multi-megapixel or gigapixel image sensor. The column read-out circuit 307 (for which two columns of read-out circuitry are depicted) and row decoder/driver 305 may likewise be scaled to meet the number of pixels in the pixel array.

[00111] In the embodiment shown, each column of the pixel array is populated by shared-element pixels in which every four pixels form a quad pixel cell 310 and contain respective photodiodes 260 (PD1-PD4), transfer gates 251, and transfer-enable transistors 253, but share a floating diffusion node 312, reset transistor 259, source follower 255 and row-select transistor 257. By this arrangement, the average transistor count per pixel is 2.75 (i.e., 11 transistors/4 pixels), thus effecting a relatively efficient, 2.75T-pixel image sensor.

[00112] As shown, row decoder/driver 305 outputs a shared row-select signal (RS) and reset-gate signal (RG) to each row of quad-pixel cells 310, and outputs independent row transfer-gate control signals (TGr1-TGr4) to drain terminals of respective transfer-enable transistors 253. In an embodiment in which row decoder/driver 305 sequences incrementally through the rows of the array (e.g., pipelining reset, integration and progressive read-out operations with respect to the rows of pixel array 301 such that one row is read-out after another), the row decoder/driver may include logic to assert the RG, RS and TGr signals at the appropriate time for each row (e.g., synthesizing those signals with respect to a row clock from sequencing logic 303). Alternatively, row decoder/driver 305 may receive individual timing signals corresponding to each or any of the RG, RS and TGr signals, multiplexing any individual enable pulse onto the corresponding RG, RS, or TGr lines of a selected row at the appropriate time. In one embodiment, the row decoder/driver receives transfer-gate control voltages corresponding to the off, partially-on and fully-on states shown in Figures 11, 12 and 13 (i.e., VTG_{off} , $VTG_{partial}$, VTG_{full}) from an on-chip or off-chip programmable voltage source 309, switchably coupling each of the different control voltages to a given transfer-gate row line at a deterministic time, for example, as shown in Figure 11. In alternative embodiments, more than one voltage source 309

may be provided within image sensor 300 to enable transfer-gate control voltages to be locally calibrated and thus compensate for control-voltage and/or performance variations (i.e., non-uniformity) across the pixel array.

[00113] Still referring to the embodiment of Figure 14, column read-out circuit 307 includes a bank of read-out circuits 315, each implementing a digital threshold comparator and a relatively low bit-depth analog-to-digital converter (e.g., a 4-10 bit ADC, though lower or higher bit depth ADCs may be employed) to execute the over-threshold detection and conditional sampling operations, respectively, discussed in connection with Figures 11-13. In one implementation, the threshold comparator and ADC are implemented by separate circuits so that the pixel sample value may be generated without regard to the conditional-reset threshold applied in the over-threshold determination. Through this approach, the conditional-reset threshold is dissociated from the reference signals (“ADC Vrefs”) used in the ADC conversion, freeing the conditional-reset threshold and ADC reference voltages to be independently adjusted (e.g., through reprogramming a threshold-reference generator) dynamically during or prior to sensor operation to achieve calibration and/or compensate for changing operating conditions or sub-optimal imaging results. In an alternative embodiment, the threshold comparator may be implemented as part of the ADC (e.g., using a reference applied in connection with resolving the digital sample value as the conditional-reset threshold), potentially reducing the footprint of the column read-out logic through more compact circuit design.

[00114] In the embodiment shown, the sequencing logic delivers a column clock, sample-and-hold strobes (SHR, SHS, which are applied to enable signal storage within sample-and-hold elements at the front-end of the ADC/threshold comparator), and compare/convert strobe to the column read-out logic to enable the operational timing shown, for example, in Figure 11. That is, during the over-threshold detection phase (i.e., phase 3), the read-out circuit for a given pixel column asserts (or maintains assertion of) the TGc line (e.g., in response to assertion of a TGcEn signal from sequencing logic 303 and logic OR gate 316) so that, when the row decoder/driver switches the TGr line for a given pixel row to the partially-on potential (e.g., VTG_{partial} , which is applied to the transfer gates of the pixel row), execution of the over-threshold detection operation described above is enabled. Accordingly, the threshold comparator within each read-out circuit evaluates the state of the threshold-test sample (which is generated according to the state of shared floating diffusion 312 following application of VTG_{partial} to the transfer gate of a given photodiode) with respect to the conditional-reset threshold to yield a binary over-threshold result. If an over-threshold condition is detected, the read-out circuit raises the TGc signal again a short time later (i.e., in conjunction with the fully-on TGr potential (VTG_{full}) to effect a

conditional read-out operation, enabling a full read-out of the photodiode state onto Vout and resetting the photodiode) and executes an analog-to-digital conversion operation in response to assertion of the compare/convert strobe to yield a digitized pixel sample.

Read-Out Circuitry

[00115] Figures 15A-15C illustrate alternative column read-out circuit embodiments that may be employed in connection with the exemplary progressive read-out pixels described above. Figure 15A, for example, illustrates a column read-out circuit 350 formed by sample-and-hold bank 351, analog-to-digital converter (ADC) 353, sense amplifier 355 and ADC-enable gate 357. Sample-and-hold (S/H) bank 351 includes switch elements and analog storage elements (e.g., capacitive elements) to enable the reset-state and signal-state of a selected pixel (delivered via column “Vout” line) to be sampled and held in response to assertion of reset-state and signal-state control signals. In one embodiment, the pixel reset-state and signal-state signals are output differentially (e.g., signal-state – reset-state) from S/H bank 351, thus enabling sense amplifier 355 and ADC 353 to receive measurement signals that reflect the state of the floating diffusion less a variable (i.e., noisy) reset level. In the embodiment shown, sense amplifier 355 and ADC 353 receive separate reference signals (“SA Ref” and “ADC Refs”) for application in over-threshold detection and ADC operations, respectively. More specifically, when a compare-strobe signal (“Compare”) is pulsed, a threshold comparison is triggered within sense amplifier 353, yielding a logic high or low comparison result according to whether the S/H signal output (and thus the noise-corrected pixel signal-state) exceeds the sense-amp reference signal (i.e., a spillover threshold or conditional-reset threshold as described above). The comparison result is fed back to the pixel column as the conditional-reset signal discussed above, and is also supplied to logic gate 357 to selectively enable an analog-to-digital conversion operation within ADC 353. That is, if sense amplifier 355 signals an over-threshold condition (a logic ‘1’ comparison result in this example), then an ensuing convert-strobe pulse (“Convert”) is enabled to pass through logic AND gate 357 (i.e., by virtue of the high sense-amp output) to a convert-enable input of ADC 353, thereby triggering the ADC operation. In one embodiment, a buffer 359 is provided to store the resulting N-bit ADC value (e.g., an 8-bit to 12-bit value in a number of embodiments, though higher or lower resolutions may apply in all cases), as well as the comparison result from sense amplifier 355, the latter forming a validity bit “V” that qualifies ADC content within buffer 359 as containing valid or non-valid data. Accordingly, if no detectable spillover has occurred within the pixel being read-out, the logic-low comparison result will not only suppress the ADC operation (saving power), but also qualify the content of the read-out buffer, thereby permitting compression of the outgoing data stream. This result is

indicated in the timing waveform at 360 by the dashed ADC data transmission -- showing generation and transmission of ADC data only if the pixel measurement exceeds the spillover threshold ($V=1$).

[00116] Figure 15B illustrates an alternative read-out circuit embodiment 365 that lacks a sense amplifier and instead applies ADC circuit 353 to perform both the threshold comparison and, if necessary, generation of ADC data corresponding to full pixel read-out. As before, S/H bank 351 outputs a measurement signal that reflects the difference between the signal-state and reset state during spillover (partial read-out) and full read-out operations. A compare-strobe (“Compare”), when asserted, is applied via logic OR gate 368 to an enable-convert input of the ADC to enable an ADC operation with respect to the measurement signal acquired during a partial-read operation (i.e., application of VTG_{Partial} to the transfer gate of a selected pixel as discussed above). If the ADC output exceeds a digital threshold value (i.e., a multi-bit digital value or digital number), comparator 367 asserts a conditional-reset/over-threshold signal (e.g., to a logic ‘1’ state in the example shown), thereby enabling an ensuing convert-strobe pulse (“Convert”) to pass through logic AND gate 369 (and logic OR gate 368) to trigger another ADC operation, this time with respect to a measurement signal acquired during a full read-out operation. As in the embodiment of Figure 15A, the conditional-reset signal is driven back to the pixel column to enable the full-read (and pixel reset) operation within the subject pixel, and is also output to read-out buffer 359 to be stored as a validity bit, qualifying the corresponding ADC data content of that buffer. Although the compare-strobe, convert-strobe and transmit-data waveforms in the embodiment of Figure 15B (i.e., shown at 370) are illustrated as matching those in Figure 15A, a somewhat larger delay may be imposed between the compare-strobe and convert-strobe pulses to account for the additional time required within ADC to digitize the S/H partial-read measurement. In both cases, the interval between the compare-strobe and convert-strobe pulses may be different from the intervals shown, for example, to align the read-out timing operations with the pixel operations described above (e.g., as shown in Figure 11).

[00117] Figure 15C illustrates a variation (375) of the read-out circuit embodiment of Figure 15B. In general, the sequence of read-out operations is as discussed in reference to Figure 15B except that the partial-read ADC output is latched within read-out buffer 377 and, if under-threshold (i.e., no conditional reset and thus no subsequent full-read ADC output), the digitized partial-read measurement is transmitted off chip together with an over-threshold bit (OT) that indicates whether the over-threshold condition has been detected. If the partial-read ADC output exceeds the spillover threshold, then the full-read measurement is digitized in a second ADC operation and stored within the read-out buffer, overwriting the partial-read ADC value.

By this operation, a valid pixel read-out value, reflecting either a partial read-out (OT=0) or a full read-out (OT=1) is transmitted to an external destination regardless of whether the spillover threshold is exceeded, thus permitting a sequence of partial-readout values to be accumulated (integrated) within the final pixel value. Note that storage and transmission of the OT bit may be omitted, particularly in embodiments in which ADC measurements are aggregated or otherwise combined without regard to whether their acquisition occurred in a full or a partial read-out operation.

Image Decimation and Pixel Binning

[00118] A number of conditional-reset image sensor embodiments described herein are operable in decimation modes that yield less than maximum image resolution. For example, in one embodiment an image sensor capable of generating an 8MP (8 megapixel) output in a still-image mode, yields a 2MP output in a decimated, high-definition (HD) video mode; a 4:1 decimation ratio (higher or lower resolutions may apply in each mode, and other decimation modes and ratios may be achieved in alternative embodiments; also, if the still and video frame aspect ratios differ, some areas of the sensor may not be used at all in one or the other modes).

[00119] While post-digitization logic may be provided to decimate full-resolution data (e.g., on-chip logic at the output of the ADC bank or off-chip processing logic), pixel charge aggregation or “binning” within the pixel array and/or voltage binning within sample-and-hold storage elements is applied in a number of embodiments to effect pre-digitization (i.e., pre-ADC and thus analog) decimation, obviating die-consuming and power-consuming digital binning logic and, in many cases, yielding improved signal-to-noise ratio in the decimated output.

[00120] Figure 16 illustrates a quad-pixel, shared floating diffusion image sensor architecture in which the row and column transfer-gate control lines (TGr and TGc) disclosed in the embodiments above are applied in a manner that enables multiple decimation modes without requiring additional array-traversing control lines. More specifically, by centralizing a shared floating diffusion 401 between four pixels (each including a respective photodiode, PD1-PD4, and transfer-enable transistor, 403.1-403.4, and transfer gate, 404.1-404.4) and splitting the column transfer-gate control line TGc into separate odd and even column-enable lines (TGc1 and TGc2, each coupled to a respective logic OR column-line driver 421, 423), it becomes possible to charge-bin all or any subset of the pixels in a decimation mode and also to operate and read-out each pixel individually a non-decimated (full-resolution) mode.

[00121] In the particular embodiment shown, the shared floating diffusion 401 (illustrated in two interconnected parts for drawing simplicity) is switchably coupled to photodiodes PD1-PD4 of the four pixels through respective transfer gates 404.1-404.4, with each transfer gate

controlled by a different pair of TGr and TGc signals within the control signal matrix. That is, transfer gate 404.1 is controlled by transfer-enable transistor 403.1 via control signals TGr1/TGc1, transfer gate 404.2 is controlled by transfer-enable transistor 403.2 via control signals TGr2/TGc1, transfer gate 404.3 is controlled by transfer-enable transistor 403.3 via control signals TGr1/TGc2 and transfer gate 404.4 is controlled by transfer-enable transistor 403.4 via control signals TGr2/TGc2. As in the shared-element pixel arrangements described above, the shared floating diffusion 401 is coupled to a shared source follower 405, row-select transistor 407 and reset transistor 409, thus enabling a more compact quad-pixel layout. Moreover, as shown in the exemplary physical-layout diagram of Figure 17, the four transfer gates (“TG”) may be physically disposed at the corners of a centralized floating diffusion (FD) with transfer-enable transistors, reset gate, source follower and row-select transistors formed at the periphery of the quad-pixel layout, thus effecting a highly compact quad-pixel footprint that may be repeated in row and column dimensions across a multi-megapixel array.

[00122] Figures 18A and 18B illustrate color filter array (CFA) patterns that may be employed with respect to the quad-pixel architecture of Figures 16 and 17 and that may dictate practical decimation modes. In the CFA pattern of Figure 18A, for example, the green corner pixels (G) that include photodiodes PD1 and PD4 (i.e., PD1 and PD4 are disposed beneath green color filter elements) may be binned in a 4:3 charge-binning decimation mode, while in the CFA pattern of Figure 18B, which includes, white, green, red and blue color filters, both pairs of corner pixels in each quad-pixel (i.e., the pixels that photodiodes PD1 and PD4, and the pixels that include photodiodes PD2 and PD3) may be charge-binned in a 4:2 decimation mode. Other charge-binning arrangements may be employed with respect to other CFA patterns and/or black & white (or grayscale) imaging.

[00123] Figures 19 and 20 present timing diagrams illustrating exemplary phases of full-resolution (non-binning) and binned-mode pixel read-out operations, respectively, within an image sensor containing the 2x2 quad-pixel arrangement shown in Figure 16. For purposes of example, different read-out gain configurations are assumed during partial read-out (threshold testing) and full-read out operations within each of the timing diagrams, with separate sets of sample and hold elements being applied to capture reset-state and signal-state samples during those read-out operations. Examples of different gain configuration circuits and their benefits are described below in reference to Figures 25A-25C, 26 and 27.

[00124] Turning first to the full-resolution read-out of Figure 19, a reset operation is performed in phase 1 (delineated at the bottom of the timing diagram) by fully asserting the transfer-gate row signal as shown at 420 for the row being read-out (TGri), together with the odd

and even transfer-gate column signals (TGc1, TGc2), thereby applying the full read-out potential to the transfer gates for the even and odd columns within the selected row to enable charge transfer from the corresponding photodiodes to the shared floating diffusion (i.e., resetting the photodiodes to an initial state in preparation for charge integration). After lowering the TGri signal, the reset-enable signal (RG) is pulsed at 422 to switch on the reset transistor and thus reset the floating diffusion. During integration phase 2 (duration not shown to scale), charge is integrated/accumulated within the photodiodes according to the intensity of the incoming light. During odd-column threshold-testing phase 3a, the RG signal is pulsed a second time at 424 to reset the floating diffusion, and reset-state sample-and-hold signals SHRsa and SHRadc are pulsed at 426 and 428 while row-select line RSi is high to enable the reset-state of the floating diffusion to be sampled within the sample-and-hold elements for the sense amplifier and ADC, respectively. After the reset-state of the floating diffusion is sampled, the even column transfer-gate signal (TGc2) is lowered (while TGc1 is held high) and TGri is raised to the VTG_{partial} potential to enable a threshold-test read-out with respect to the odd-column pixel. At 430, a signal-state sample-and-hold signal, SHSsa, is raised to enable a sample of the floating diffusion state (i.e., any spillover charge therein) to be captured within a sample-and-hold element for the sense-amplifier, and, at 432, the compare-strobe signal (“Compare”) is pulsed to enable the sense amplifier component of the read-out circuit to generate a comparison result between the floating diffusion signal state (less the reset state) and the conditional-reset (spillover) threshold.

[00125] The odd-column transfer-gate signal (TGc1) is lowered following capture of the floating diffusion signal-state at 432 and prior to raising the row transfer-gate signal to the fully-on (VTG_{full}) potential in odd-pixel, conditional read-out phase 4a. More specifically, if the comparison result indicates an under-threshold condition, the TGc1 line is held low while TGri is raised to the VTG_{full} potential, thereby suppressing the full pixel read-out and allowing the charge integrated within the photodiode during integration phase 2 to remain undisturbed and serve as the initial state during a subsequent integration interval (i.e., continued integration). By contrast, if the sense-amp comparison result indicates an over-threshold condition (i.e., the charge accumulated during integration phase 2 exceeds the conditional-reset threshold), then the TGc1 line is raised as shown by the dashed pulse at 434 concurrently with application of the VTG_{full} potential on TGri, thereby applying VTG_{full} to the odd-pixel transfer gate to enable a full pixel read-out operation. Shortly thereafter, just prior to the conclusion of the odd-pixel conditional read-out, signal-state sample-and-hold signal SHSadc is pulsed (as shown at 436) to capture a sample of the odd-pixel read-out signal within the signal-state sample-and-hold

element for the ADC. At 438, after capturing the odd-pixel read-out signal in the ADC sample-and-hold element, the convert-strobe is pulsed to trigger an ADC operation with respect to the differential between the reset-state and signal-state samples captured within the ADC sample-and-hold elements.

[00126] At the conclusion of the odd-pixel conditional read-out (i.e., phase 4a), the row transfer-gate signal is lowered so that, in the ensuing even-pixel threshold testing phase 3b, assertion of the odd-pixel column transfer-gate signal TGc1 at 440 drives the odd-pixel transfer gate low (ensuring isolation between the photodiode and floating diffusion), thus enabling the floating diffusion to be reset by the RG pulse at 442 without disturbing the odd-column pixel state. Still in phase 3b, the even-column transfer gate signal is raised at 446 concurrently with assertion of the SHRsa pulse at 448 to acquire a reset-state sample of the floating diffusion. As in the odd-pixel threshold test, the row transfer-gate signal TGri is raised to the partially-on potential (VTGpartial) at 450 (while TGc2 remains high), thereby enabling charge spillover from the even-pixel photodiode to the floating diffusion if an over-threshold condition exists within the photodiode. At 452, SHSsa is pulsed to sample the even-pixel signal-state and the compare-strobe is pulsed at 454 to enable an even-pixel over-threshold determination (even-pixel signal-state less floating diffusion reset-state) within the read-out sense-amplifier. As with the odd-pixel, if the comparison result from the sense amplifier indicates an over-threshold condition, the even-pixel column transfer gate signal is asserted at 456 concurrently with elevation of the TGri potential to the fully-on level (VTGfull), thus enabling a full read-out of the even-pixel signal state followed by assertion of the SHSadc and convert-strobe signals (at 458 and 460, respectively) to yield an even-pixel ADC result. If the comparison result from the sense amplifier indicates an under-threshold condition, the TGc2 pulse at 456 is suppressed to avoid disturbing the state of the even-pixel photodiode, thus leaving the charge on the photodiode intact for continued integration.

[00127] Still referring to Figure 19, in data-transfer phase 5, the row-i ADC values for the even and odd pixels are transmitted (e.g., to an off-chip image processing destination) one after another to an on-chip or off-chip image processing destination. As discussed above, in the case of an under-threshold condition with respect to a given pixel, analog-to-digital conversion with respect to that pixel may be suppressed and/or the ADC output omitted from the outgoing data stream. In any case, data transmission with respect to a selected pixel row may be pipelined with pixel read-out operations within subsequent rows as shown, for example, by the transmission of row i-1 data concurrently with phases of the read-out operation with respect to row i pixels.

[00128] In the binned-mode read-out timing diagram of Figure 20, hard-reset and integration operations (phases 1 and 2) are executed as described above in reference to Figure 19, as is the floating diffusion reset (i.e., asserting RG while TGc1 and TGc2 are high, and sampling the reset-state in response to assertion of the SHRsa and SHRadc signals) at the start of threshold-testing phase 3. Thereafter, partial read-out operations are executed one after another with respect to corner pixels (i.e., containing photodiodes PD1 and PD4, in the example shown), by driving TGr1 to the partially-on state at 476 concurrently with assertion of TGc1 and deassertion of TGc2, and then driving TGr2 to the partially-on state at 478 concurrently with assertion of TGc2 and deassertion of TGc1. By this operation, any spillover charge from photodiodes PD1 and PD4 is aggregated in the floating diffusion and thus captured within the sense amp sample-and-hold element when SHSsa is asserted at 480. Accordingly, assertion of the compare-strobe signal at 482 enables a comparison of the aggregated the spillover charge from PD1 and PD4 (less the reset-state of the floating diffusion) and the conditional reset/conditional read-out threshold. If the comparison result indicates an over-threshold condition, TGc1 and TGc2 are pulsed one after another at 484 and 486 (and each concurrently with assertion of the VTG_{full} potential on corresponding row lines TGr1 and TGr2, respectively) to enable the remainder of the charge accumulated within the corner photodiodes (PD1 and PD4) to be transferred to the floating diffusion, charge binning the pixel integration results and resetting each pixel in preparation for the next charge integration interval. Accordingly, when the SHSadc signal is pulsed at 488, the photodiode charge binned (or aggregated) within the floating diffusion is captured within the signal-state sample and hold element for the ADC, thus enabling an ADC operation with respect to the combined charge from the corner pixels (less the floating diffusion reset state) when the convert-strobe is pulsed at 490. The resulting digitized pixel value (i.e. ADC output) for row i may be transmitted to off-chip or on-chip processing logic during read-out of the following pair of pixel rows.

[00129] Still referring to Figure 20, if the comparison result output by the read-out sense amplifier indicates an under-threshold condition, the TGc1 and TGc2 signal assertions shown at 484 and 486 are suppressed to avoid disturbing the contents of the subject photodiodes, thereby permitting continued integration during a subsequent subframe interval. While the timing sequence shown yields the output of binned results from the corner pixels containing photodiodes PD1 and PD4 (i.e., northwest and southeast corners in the layout shown in Figures 16 and 18), the waveforms output onto signal lines TGc1 and TGc2 may be swapped to yield binned results from corner pixels containing photodiodes PD2 and PD3. Further, read-out of the aggregated (binned) charge within all four photodiodes may be effected by performing

additional partial-read operations in phase 3 (i.e., repeating the TGr1, TGr2 partial-on pulses, but reversing the assertion sequence of column transfer gate signals TGc1 and TGc2 to effect partial-reads of photodiodes PD2 and PD3), and then, if an over-threshold result is detected, performing additional full read-out operations in phase 4 (i.e., repeating the TGr1 and TGr2 fully-on pulses, but reversing the assertion sequence of column transfer gate signals TGc1 and TGc2).

[00130] Figure 21 illustrates an alternative binning strategy that may be executed with respect to a collection of 4x1 quad-pixel blocks 310 and the color filter array (CFA) fragment shown at 500. In the embodiment shown, each quad pixel block 310 (shown at 310.1-310.4 with respect to the CFA fragment) is implemented generally as described in reference to Figure 14 and may be read-out according to any of the read-out techniques described in reference to Figures 14 and 15A-15C. As shown, CFA fragment 500 (i.e., a sufficient portion of a sensor-wide CFA to demonstrate the CFA pattern) includes collections of like colored filter elements at the corner pixels of each 3x3 pixel group. Thus, green filter elements are disposed over shaded pixels 'G', blue filter elements are disposed over striped pixels 'B' and red filter elements are disposed over hashed pixels 'R'. In this arrangement, each pair of like-filtered pixels (i.e., subject to light filtered by same-color filter elements, R, G or B) disposed in the same quad-pixel block thus permit charge binning within their shared floating diffusion as detailed below. Further, referring to Figure 22, by fixing column offset between the pixel pair within each column and the like-filtered pair of pixels coupled to the same row lines (i.e., fixed at a spacing of two columns in the example shown) and by providing switching elements at the column read-out points of pixel array 551 (i.e., switching elements 561 and 562 within sample-and-hold circuitry 553), it becomes possible to "voltage-bin" the results of the two charge-binned pixel pairs within sample-and-hold circuitry 553, thus combining (i.e., aggregating, binning) the four corner pixels in each 3x3 pixel group prior to digitization within the ADC elements of SA/ADC block 555.

[00131] Figure 23 illustrates an exemplary timing diagram of binned-mode read-out operations within the 4x1 quad-pixel architecture of Figures 21 and 22. In the example shown, row lines for pixel rows i and $i+2$ are operated in lock step to achieve 2:1 charge binning within the shared floating diffusion of a given quad-pixel block. More specifically, row signals for pixel rows 1 and 3 of a 4x1 quad pixel block (or row of such quad pixel blocks) are asserted in unison, followed by locked-step assertion of row signals for pixel rows 2 and 4, before advancing to assert row signals for the next row of 4x1 quad pixel blocks. Transverse connections are established within sample-and-hold switch elements (e.g., at 561 and 562 of

sample-and-hold block 553 as shown in Figure 22) to achieve 2:1 voltage binning and thus an overall 4:1 analog signal summing and concomitant image decimation.

[00132] Referring more specifically to Figure 23, the row-select signals (RS), reset-gate signals (RG) and row transfer-gate signals (TGr1, TGr3 or “TGr1,3”) are operated in lock step to reset the photodiodes and shared floating diffusion of the selected pixel rows during hard-reset phase 1, permit charge integration during integration phase 2, determine whether the charge-binned and voltage-binned charge-accumulation results within each column-interleaved collection of four pixels (i.e., the 3x3 corner pixels as described in reference to Figures 21 and 22) exceed the conditional-reset threshold in threshold-test phase 3, and, if an over-threshold condition is detected, conditionally read-out and digitize the full charge-binned and voltage-binned accumulated charge within the subject pixel collections in conditional read-out phase 4 before transmitting the digitized pixel value to downstream (on-chip or off-chip) processing logic in output phase 5. Considering the phases one by one, during hard-reset phase 1, the row-transfer gate signals TGr1 and TGr3 are pulsed to VTG_{full} (as shown at 570) while simultaneously raising column transfer-gate signal TGc, thus transferring accumulated charge from photodiodes PD1 and PD3 to their shared floating diffusion node. After the photodiode-to-floating-diffusion charge transfer, reset signal RG is pulsed at 572 to clear charge from the floating diffusion in preparation for the ensuing charge integration in phase 2. At the start of threshold-test phase 3, the reset signal is pulsed again (574) to reset the floating diffusion and then signals SHRs_a and SHRs_{dc} are pulsed at 576 and 578 (while RSi is asserted) to capture samples of the reset-state of the floating diffusion within the sample-and-hold elements for the sense amplifier and ADC. At 580, TGr1 and TGr3 are raised to the partial-on transfer potential, $VTG_{partial}$, to enable charge spillover to the shared floating diffusion if an over-threshold condition exists in the photodiodes of the subject pixels. The SHS_a signal is then pulsed at 582 while the transverse-interconnect switch elements (e.g., transistors) are switched to a conducting state within the sample and hold bank to capture the signal-state of the floating diffusion nodes within related columns (i.e., column j and column j+2 in the embodiment shown) within a shared sample-and-hold element, thus voltage binning the two charge-binned spillover samples. The threshold-test phase is concluded by lowering the TGc signal and asserting the compare-strobe (584) to trigger a threshold comparison within the sense amplifier, comparing the aggregated spillover charge from the four charge/voltage binned pixels against a conditional-reset threshold. If the comparison result indicates an over-threshold condition, the TGc signal is pulsed at 586 during application of VTG_{full} on the TGr1 and TGr3 lines, (thus enabling a full read-out of photodiodes PD1 and PD3 to the shared floating diffusion within corresponding

quad pixel block), and then the SHSadc signal is raised at 588 to capture the signal-state of the floating diffusion nodes of switch-interconnected pixel columns within a signal-state sample-and-hold element for the ADC (i.e., voltage-binning the charge-binned floating diffusion contents). Thereafter, the convert-strobe is pulsed at 590 to trigger an ADC operation with respect to the voltage/charge-binned signal state captured within the sample-and-hold circuit (if any), followed by transmission of the ADC output in phase 5. As discussed above, the ADC operation and data transmission operations may be suppressed to save power and reduce signaling bandwidth if an over-threshold condition is not detected in threshold-test phase 4.

[00133] Figure 24 illustrates a more detailed embodiment of an image sensor 600 having an array of 4x1 quad pixel blocks 601 operable in the decimation (binning) mode described in reference to Figures 21-23. As in the embodiment of Figure 14, a row decoder/driver 605 receives transfer gate voltages (e.g., VTG_{partial} , VTG_{full} and VTG_{off}) from an on-chip or off-chip voltage source 309 and a row address value and row clock (used to control row signal timing) from sequencing logic 603, outputting row control signals, RG, RS and TGr1-TGr4 in response. Sequencing logic additionally outputs a set of read-out control signals to column read-out circuitry 607, including a column clock signal (which may be composed of multiple timing/control signals for timing operations within the sense amplifiers, ADCs, memory buffers, etc. with column read-out circuitry 607), compare-strobe and convert-strobe signals as described above, the column transfer-gate enable signal (TGcEn), SHR and SHS signals (which may include separate signals for sense amp and ADC sample-and-hold elements). Sequencing logic also outputs a decimation-mode signal (“Dec Mode”) to both column read-out circuitry 607 and row decoder/driver 605 to enable/disable the above-described charge and voltage binning operations. For example, in one embodiment, the decimation mode signal is configurable in one of at least two possible states (e.g., according to a decimation mode setting within a programmable configuration register 604), including a binning-disabled state in which pixel rows and columns are operated individually to enable full-resolution image read-out, and a bin-enable state in which the row decoder/driver asserts row signal pairs (e.g., TGr1/TGr3 and then TGr2/TGr4) in locked-step to achieve charge binning within the shared floating diffusion, and in which column read-out lines (Vout) for even and odd column pairs are transversely coupled (e.g., as shown in Figure 22) to enable voltage binning within sample-and-hold elements.

[00134] Still referring to the embodiment of Figure 24, column read-out circuitry 607 includes, in addition to sense amplifiers 617 and TGc logic gates 619 (which operate generally as described above), a set of column eclipse detect circuits 615, each coupled to receive a pixel reset signal from sample-and-hold block 609, and having circuitry to determine whether the

photodiode measurement (whether binned or at full resolution) exceeds a saturation threshold. If a given eclipse-detector 615 (e.g., implemented by a threshold comparator) detects a saturation condition (i.e., saturation threshold exceeded), the eclipse detector raises an eclipse signal at a secondary enable input of ADC circuit 611 to disable ADC operation therein. The eclipse signal is also output to a line memory element 621 to qualify the ADC output, being recorded therein as a logic '1' eclipse bit if a saturation condition was detected (thus indicating that the ADC output is invalid and in fact should be represented by a maximum read-out value) and a logic '0' eclipse bit otherwise. By this operation, the eclipse bit and under-threshold bit recorded for each pixel column serve jointly to qualify the corresponding ADC output as follows (where 'X' indicates a don't care status):

Under-Threshold	Eclipse	ADC Value	Interpretation
0	0	Invalid	Under-Threshold: ADC output assumed to be 0
X	1	Invalid	Saturation:, ADC output assumed to be all '1's
1	0	Valid	Over-Threshold without Saturating

Table 1

[00135] Still referring to Figure 24, when the binning mode is set to enable voltage binning between column pairs (e.g., even numbered columns voltage binned and odd-numbered columns voltage binned), the sense amplifier and ADC within one column in each binned column pair may be disabled to save power, with the transmitted data stream decimated according to the binning mode.

Dynamic-Gain Pixel Read-Out

[00136] As briefly mentioned in connection with Figures 19 and 20, different gains may be applied during partial and full read-out operations. That is, because the spillover charge during a partial read-out may be exceedingly small (i.e., where the charge integration level barely exceeds the conditional-reset threshold), it may be beneficial to apply a higher gain during the partial read-out. By contrast, because the full read-out may range between minimum and maximum charge integration levels, a significantly lower gain may be applied to normalize those charge levels to the minimum and maximum ADC output values. Accordingly, in a number of embodiments herein (including those described above in reference to Figures 19-24), different gains are applied by the column read-out circuitry during partial read-out and full read-out operations.

[00137] Figure 25A illustrates an embodiment of a selectable-gain (or multi-gain) read-out circuit that may be used to effect a high-gain partial read-out and near-unity gain full read-out

within a pixel column. More specifically, in the implementation shown, multiplexers 651 and 653 are used to establish either a common-source amplifier configuration (gain = transconductance of transistor M1 * load resistance R_L , where '*' denotes multiplication) or a source-follower configuration (unity gain or near-unity gain) according to the state of multiplexer control signals CS and SF. In the common-source amplifier configuration, (CS=1, SF=0), multiplexer 653 couples column line Col2 to voltage supply rail Vdd via load resistance R_L (655), while multiplexer 651 couples column line Col1 to ground. As shown, Col2 is coupled to the drain terminal of row-select transistor 683 so that Vout1 will vary according to the current flow through transistor M1; a function of the applied gate voltage (floating diffusion charge level) and transconductance of that transistor. More specifically, as can be understood from Figure 25B (which illustrates the common source gain configuration), Vout1 is given by $V_{DD} - I_{M1} * R_L$ so that V_{out1}/V_{FD} is approximately $g_m * R_L$, where g_m represents the transconductance of transistor M1. Accordingly, by appropriately sizing M1 and/or R_L , a common-source gain substantially greater than unity may be achieved, thus improving sensitivity to the relatively small level of charge that may spillover to the floating diffusion during partial read-out operations. Note that reset transistor 685 is also coupled to the Col2 line, thus enabling the floating diffusion to be pulled up to CS mode Vout (i.e., reset) in response to RG signal assertion while in the common-source gain configuration.

[00138] In the source-follower configuration (SF=1, CS=0), multiplexer 653 couples a current source 657 to the Col2 line, and multiplexer 651 couples column line Col1 to Vdd, thus establishing M1 as a source-follower amplifier (i.e., output voltage at M1 source and thus Vout2 follows the floating-diffusion voltage applied at the gate of M1) as shown at Figure 25C. More specifically, in order to maintain a substantially constant current through the Col2 line, the feedback loop that maintains the constant current source raises the potential at Vout2 as necessary to counteract any conductance change in transistor M1. Accordingly, assuming a substantially linear transconductance within M1, the current source raises and lowers Vout2 in a substantially linear correspondence to increase and decrease in the floating diffusion potential, thus effecting substantially constant proportionality between Vout2 and V_{FD} . In the embodiment shown, the constant of proportionality is slightly less than unity (e.g., 0.85 in the specific example depicted, though other proportionality constants, including unity, may be achieved in alternative embodiments or other programmed configurations) in the source follower configuration.

[00139] Still referring to Figure 25A, separate sets of sample-and-hold elements (e.g., capacitive elements and switch elements) 669 and 671 are coupled to the Vout1 and Vout2

nodes, respectively, to accommodate the different gain configurations applied during partial read-out and full read-out operations, with correspondingly separate sets of reset-state and signal-state sample-enable signals applied to the two sample-and-hold circuits. In the example shown, the partial read-out sample-and-hold circuit 669 (i.e., controlled by signals SRCs and SSCs in the common-source gain configuration) provides a differential output (i.e., signal-state sample less reset-state sample) to a sense amplifier circuit 675, while the full read-out sample-and-hold circuit 671 (controlled by signals SRsf and SSsf in the source-follower gain configuration) provides a differential output to ADC 677. As in all embodiments having both a sense amplifier and ADC, the sense amplifier may be omitted and the ADC applied during both the partial and full read-out operations as discussed in reference to Figures 15B and 15C. In such ADC-only implementations, the outputs of sample-and-hold circuits 669 and 671 may be multiplexed to the input of ADC 677 according to the state of the CS and SF signals. In an embodiment in which the CS and SF signals always have complementary states, a single signal may alternatively be used to switch between common-source and source-follower gain configurations.

[00140] Figure 26 presents an exemplary timing diagram illustrating the alternating application of common-source and source-follower gain configurations during hard-reset, integration, partial read-out and (conditional) full read-out operations within the multi-gain architecture of Figure 25A. As shown, the common-source enable signal (CS) is asserted at 686 concurrently with the hard-reset RG pulse (i.e., asserted in preparation for charge integration) and at 688 (floating diffusion reset in preparation for reset-state sampling). During at least a portion of the charge integration interval, signal gain may be disabled altogether to save power (i.e., lowering both the SF and CS control signals as shown), though in actuality one or both gain modes may be applied during that interval to enable operations in other pixel rows. During reset-state sampling, the common-source and source-follower gain configurations are enabled one after another as shown at 690 and 692 (i.e., initially holding CS high while SF is low and then reversing that configuration), with reset-state sampling signals SRCs and SRsf being pulsed at 694 and 696 while in the common-source and source-follower gain configurations, respectively, to capture reset-state samples within the different sample-and-hold circuits provided for the two gain configurations. Thereafter, CS is raised at 698 (and SF lowered) to apply the common-source gain configuration during the partial read-out operation (effected by raising TGr to the partially-on state at 700 while TGc is held high and concluding with assertion of the SSCs and compare-strobe signals), and then SF is raised at 702 (and CS lowered) to apply the source-follower gain configuration during the ensuing conditional full read-out operation

(effected by raising TGr to the full read-out potential at 704 concurrently with conditional pulsing of the TGc signal and concluding with assertion of the SSSf and convert-strobe signals).

[00141] Reflecting on the multi-gain architecture described in reference to Figures 25A-25C and Figure 26, it should be noted that other gain configurations or combinations of gain configurations may be used in alternative embodiments. For example, as shown in Figure 27, two different common-source gain configurations, may be effected by coupling different pull-up resistances (RL1 and RL2) to the col2 line via multiplexer 701, and thereafter selecting one gain or the other (i.e., through appropriate assertion of control signals CS1 and CS2) generally as described in reference to Figure 26. In another embodiment, a programmable gain amplifier may be coupled to the Col2 and/or Col1 line and switched between programmed settings to effect different partial read-out and full read-out gains. More generally, any practicable configuration or architecture that enables adjustment of the gain applied during partial read-out and full read-out operations may be employed in alternative embodiments.

Image Sensor Architecture, System Architecture

[00142] Figure 28 illustrates an embodiment of an image sensor having a pixel array 731 disposed between upper and lower read-out circuits 732.1 and 732.2. The read-out circuits are coupled to respective halves of the pixel rows in the array and are operable in parallel, thereby halving the time required to scan through the rows of the pixel array. In one embodiment, the pixel rows are allocated between the upper and lower read-out circuits according to the physical half of the pixel array in which the pixel rows reside. For example, all upper pixel rows (i.e., above a physical midpoint) may be coupled to the upper read-out circuit, and all lower pixel rows may be coupled to the lower read-out circuit, thereby reducing the overall column line length (reducing capacitance, noise, required drive power, etc. with respect to each Vout and reset feedback (TGc) line). In other embodiments, the pixel row interconnections to the upper and lower read-out circuits may be interleaved across the rows of pixel arrays, with the connection alternating between upper and lower read-out circuits for each successive row of pixel blocks (e.g., every fourth row in a pixel array populated by the 4x1 quad-pixel block shown in Figure 21, or every second row in a pixel array populated by the 2x2 quad-pixel block shown in Figures 16 and 17, or every other row in a pixel array populated by pixels having dedicated Vout interconnects). In the embodiment shown, each read-out circuit (732.1 and 732.2) includes a sample-and-hold bank 733 (e.g., including per-column capacitive storage elements and switching elements as described above), a sense amplifier bank 735 including per-column sense amplifier circuits (or latches) and reset-feedback logic, a per-column ADC bank 737 and a digital line memory 739. In embodiments that apply the per-column ADCs to digitize

partial read-out samples, the sense amplifier bank 735 may be omitted and the per-column ADC bank outfitted with digital comparators to generate reset-feedback signals (i.e., conditional-reset signals, TGc). Also, the sample-and-hold bank may include transverse switching elements as described in reference to Figure 22 to support voltage binning operations. More generally, the various circuit blocks of the upper and lower read-out circuits may be operated and/or configured as described above to support various decimation modes and read-out options. Though not specifically shown, the upper and lower digital line memories 739 may feed a shared physical output driver (PHY), for example, disposed to the left or right of the pixel array and coupled to receive data in parallel from each of the digital line memories. Alternatively, separate PHYs may be provided with respect to the two digital line memories, with the PHYs being disposed, for example, at an opposite edges of the image sensor IC. Further, while the upper and lower read-out circuits may be implemented on the same physical die as pixel array 731 (e.g., at the periphery of the die (sandwiching the pixel array) or in the center of the die between respective halves of the pixel array, the read-out circuits may alternatively be located on another die (e.g., coupled to the pixel array die in a stacked configuration that may additionally include other imaging-related dies).

[00143] Figure 29 illustrates an embodiment of an imaging system 800 having an image sensor 801, image processor 803, memory 805 and display 807. The image sensor 801 includes a pixel array 811 constituted by temporally-oversampled conditional-reset pixels according to any of the embodiments disclosed herein, and also includes pixel control and read-out circuitry as described above, including row logic 815, column logic 817, line memory 819 and PHY 821. Image processor 803 (which may be implemented as a system-on-chip or the like) includes an image signal processor (ISP) 831 and application processor 833, coupled to one another via one or more interconnect buses or links 836. As shown, ISP 831 is coupled to receive imaging data from the pixel array via PHY 827 (and signaling link(s) 822, which may implemented, for example, by a Mobile Industry Processor Interface (“MIPI” bus) or any other practicable signaling interface), and the ISP and application processor are coupled to a memory control interface 835 and user-interface port 837 via interconnect 836. Further, as explained below, interconnect 836 may also be coupled to the image sensor interface of ISP 831 (i.e., the ISP’s interface to PHY 827) via side-channel 838 to enable the application processor to deliver data to the ISP in a manner that emulates an image sensor.

[00144] Still referring to Figure 29, imaging system 800 further includes one or more memory components 805 coupled to the memory control interface 835 of image processor 803. In the example shown, and in the discussion below, the memory components are assumed to

include a dynamic random access memory (DRAM) which may serve as a buffer for image subframe data and/or as a frame buffer for other functions. The memory components may additionally include one or more non-volatile memories for long-term storage of processed images.

[00145] User-interface port 837 is coupled to a user display 807 which may itself include a frame memory (or frame buffer) to store an image to be displayed for a user (e.g., a still image frame or video frame). Though not shown, user-interface port 837 may also be coupled to a keypad, touchscreen or other user-input circuitry capable of providing information to image processor 803 corresponding to user-input, including operating mode information that may be used to configure decimation modes within the image sensor 801. Although also not shown, image processor 803 may be coupled to image sensor 801 through a sideband channel or other control interface to permit transmission of operating mode, configuration information, operation-triggering instructions (including image capture instructions, configuration-programming instructions, etc.) and the like to the image sensor.

[00146] Figure 30 illustrates an exemplary sequence of operations that may be executed within the imaging system of Figure 29 in connection with an image processing operation. Starting at 851, the application processor configures ISP 831 for DMA (direct-memory-access) operation with respect to memory control interface 835 and thus memory IC 805. By this arrangement, the ISP is enabled to operate as DMA controller between image sensor 801 and memory IC 805, receiving subframe data from image sensor 801 row by row (as shown at 853) and transferring the subframe data to the memory IC. Thus, the subframe data generated by temporal oversampling within image sensor 801 are, in effect, piped through the ISP directly to memory IC (e.g., a DRAM) where they may be accessed by the application processor. Note that, in the embodiment shown, subframes are loaded into the memory one after another until a final subframe has been received and stored (i.e., the frame-by-frame storage loop and its eventual termination being reflected in decision block 855). This process may be optimized in an alternative embodiment by omitting storage of the final subframe in memory IC 805 and instead delivering the final subframe data directly to application processor 833. That is, as shown at 857, the application processor retrieves and combines (e.g., sums) the stored subframes to produce a consolidated (integrated) image frame so that, instead of storing the final subframe in memory and then reading it right back out, the final subframe may be delivered directly to the application processor to serve as a starting point for subframe data consolidation. In any case, at 859 the application processor configures ISP 831 for operation in image-processing mode and, at 861, outputs the image frame data (i.e., the consolidation of the temporally oversampled

image sensor data) to the image-sensor interface of the ISP (i.e., to the front-end of the ISP via channel 838), thereby emulating image sensor delivery of a full image frame to ISP 831. At 863, the ISP processes the image frame delivered by the application processor to produce a finalized image frame, writing the completed (processed) image frame, for example, to DRAM or non-volatile memory (i.e., one or both of memory ICs 805), and/or directly to the frame buffer within display 807 to enable the image to be displayed to the system user.

Split-Gate Architecture

[00147] Figure 31 contrasts embodiments of the conditional-reset pixel 250 of Figure 10 and a modified pixel architecture 870, referred to herein as “split-gate” conditional-reset pixel or split-gate pixel. In the embodiment shown, split-gate pixel 870 includes a photodiode 260 together with the same floating diffusion 262, reset transistor 259, source-follower 255, and read-select transistor 257 as pixel 250, but omits transfer-enable transistor 253 and single-control transfer-gate 251 in favor of a split, dual-control transfer-gate 871. Referring to detail view 880, dual-control transfer gate (or “dual-gate”) includes distinct (separate) row and column transfer gate elements 881 and 883 disposed adjacent one another over the substrate region between photodetector 260 (PD) and floating diffusion 262 (FD). The row and column transfer gate elements (881 and 883) are coupled to row and column control lines, respectively, to receive row and column control signals, TGr and TGc and thus are independently (separately) controlled. As discussed in further detail below, by omitting the source/drain implant ordinarily required between series-coupled transistors (and thus between adjacent gate terminals), the row and column transfer gate elements may be disposed closely enough to one another that the resulting overlapping electrostatic fields will form a continuous enhancement channel 885 when both TGr and TGc are asserted, (at a signal level to provide charge transfer), while maintaining an ability to interrupt the channel when either of TGr and TGc are deasserted, (at a signal level to prevent charge transfer). Accordingly, the logic-AND function effected by the combined operation of transfer-gate 251 and transfer-enable transistor 253 in pixel 250 may be achieved within the substantially more compact dual-control gate 871, reducing the pixel footprint (i.e., die area consumption) by a transistor or a significant portion of a transistor relative to pixel 250. In the case of a quad pixel layout, for example, the dual-gate arrangement lowers the per-pixel transistor count from 2.75T (i.e., when pixel 250 is employed) to approximately 1.75T to 2T, depending on the dual-gate implementation. In addition to the reduced pixel footprint, the dual-gate design permits a negative potential to be applied to the transfer gate or transfer gates during the charge-integration (light accumulation) interval to reduce PD to FD leakage current and transfer gate dark current, a function not readily available in embodiment 250 as a negative TGr

voltage may disruptively forward-bias the source/drain to substrate diodes in transfer-enable transistor 253. Further, in contrast to the floating potential that results at transfer gate 251 of pixel 250 whenever TGc is lowered, row and column transfer gate elements 881 and 883 are continuously coupled to signal driving sources and thus continuously driven to the driver output voltage (i.e., not floating), potentially reducing noise in the pixel read-out operation.

[00148] Figure 32 is a timing diagram illustrating an exemplary pixel cycle (reset/charge integration/read-out) within the split-gate pixel of Figure 31. As in embodiments described above, the pixel cycle is split into five intervals or phases corresponding to distinct operations carried out to yield an eventual progressive read-out in the final two phases (the pixel can also provide an unconditional readout sequence that skips phase four). Referring to both Figure 32 and split-gate pixel 870 in Figure 31, a reset operation is executed within the photodiode and floating diffusion in phase one by concurrently raising the TGr and TGc signals to establish a conduction channel between photodiode 260 and floating diffusion 262 (i.e., as shown at 885 in Figure 31), and thereby reset the photodiode by enabling residual or accumulated charge within the photodiode to be transferred to the floating diffusion. After (or concurrently with) the charge transfer operation, the reset-gate signal (RG) is pulsed to switch on reset transistor 259 and thus evacuate/empty charge from the floating diffusion by switchably coupling the floating diffusion to V_{dd} or other supply voltage rail. In the embodiment shown, TGr is driven to a negative potential following the photodetector reset operation (e.g., immediately after concurrent assertion with TGc or at the conclusion of the reset phase), thereby establishing a low-leakage isolation between the photodetector and floating diffusion, and reducing dark current from the region below TGr. Also, because the row and column control signals are jointly applied to adjacent transfer gate elements, TGc may be raised and lowered as necessary following the photodetector reset operation and during the ensuing integration phase (phase 2) without undesirably floating the transfer gate. Thus, TGc is lowered following pixel reset and, while shown as remaining low throughout the ensuing integration and noise sampling phases (phases 2 and 3), will toggle between high and low states during those phases to support reset and read-out operations in other pixel rows.

[00149] The noise or reset sampling operation within phase 3, overthreshold detection within phase 4 and conditional read-out (or conditional transfer) within phase 5 are carried out generally as discussed in reference to Figure 11, except that TGc need only be raised in conjunction with the TGr pulses (i.e., to VTGpartial and VTGfull) during the partial-transfer and conditional-transfer operations. In the embodiment shown, a quad-potential TGr driver is provided within the row decoder/driver (e.g., within element 305 of Figure 14) to maintain TGr

at the negative potential throughout the integration phase, and then step TGr up to a pre-read potential (zero volts in the example shown) at the start of the noise sampling phase before raising TGr further to VTG_{partial} and finally to VTG_{full} in the overthreshold detection and conditional read-out operations, respectively. In alternative embodiments, a three-potential driver may be used to maintain TGr at the negative potential except when pulsed to VTG_{partial} or VTG_{full} (i.e., no pre-read potential).

[00150] Figure 33 illustrates exemplary low-light and high-light operation of the split-gate pixel of Figure 31, showing electrostatic potential diagrams in each case beneath schematic cross-section diagrams of the photodetector (photodiode 260 in this example), row and column transfer gate elements 881 and 883 (i.e., forming a dual-control transfer gate) and floating diffusion 262. As in preceding examples, the depicted levels of electrostatic potential are not intended to be an accurate representation of the levels produced in an actual or simulated device, but rather a general (or conceptual) representation to illustrate the operation of the pixel read-out phases. Starting with the low-light example, a relatively low level of charge is accumulated within the photodiode during the integration phase (phase 2) so that, when TGc is asserted and TGr is raised to the partial-on potential (VTG_{partial}) during overthreshold detection phase 4 (i.e., after noise sample acquisition in phase 3), the charge level is insufficient to be transferred via the relatively shallow channel formed between photodiode 260 and floating diffusion 262. Because the accumulated charge level does not exceed the spillover threshold established by application of VTG_{partial} to the gate element couple to the TGr line, there is no spillover from the photodiode to the floating diffusion and the accumulated charge instead remains undisturbed within the photodiode. Because no spillover is detected during the overthreshold phase, TGc is deasserted during conditional transfer (conditional read-out) phase 5. Although some charge will migrate to the well under the row gate during TGr assertion, that charge will move back to the photodiode well when TGr is deasserted, thus maintaining the charge level within the photodiode as a starting point for further charge accumulation in a subsequent integration interval. By contrast, in the high-light example, the higher level of accumulated charge does exceed the spillover threshold during overthreshold detection phase 4 so that a portion of the accumulated charge (i.e., that subset of charge carriers that are above the transfer gate partially-on electrostatic potential) spills over into floating diffusion node 262, with the residual accumulated charge remaining within the photodiode as shown at 918. Accordingly, during overthreshold phase 5, TGr is raised to the VTG_{full} potential concurrently with assertion of TGc, thus establishing a full conduction path through the channel formed by the dual-gate structure to transfer the entirety of the accumulated charge from photodiode 260 to floating diffusion 262.

[00151] Figure 34 illustrates an alternative overthreshold detection operation within the split-gate pixel of Figure 31. As shown, instead of driving the TGr line to a partial potential (i.e., VTG_{partial}), a fractional (i.e., reduced-width) TGr pulse 920 is applied in conjunction with the TGc pulse (which may also have a fractional pulse width) thus limiting the time available for charge transfer between the photodetector and floating diffusion. In one embodiment, for example, fractional pulse 920 is a short-duration pulse having a time constant shorter than required to transfer all charge above the threshold defined by the voltage applied to the dual-control transfer gate and therefore transfers the charge only partially, in contrast to a full-width pulse which is long enough to transfer all of that charge. Accordingly, due to the time constant and sub-threshold characteristics of the photodetector-to-diffusion charge transfer, below-threshold charge integration within the photodetector will yield little or no charge transfer during the fractional pulse interval, while over-threshold charge integration will yield a detectable charge transfer, analogous, in effect, to application of VTG_{partial} for the full pulse interval. Pulse width control may provide superior performance (i.e., relative to voltage-level control) in terms of repeatability and/or threshold precision, particularly in noisy environments (e.g., where switching noise may couple to the TGr line) or where programmable threshold trimming or calibration may be needed. As shown at 921, the partial-readout control, whether pulse-width or voltage-level controlled, alternatively (or additionally) may be applied to the TGc line, particularly where the TGc signal is used to control the gate element nearest the photodetector. Also, pulse-width control and voltage control may be combined, for example, by driving a fractional pulse having a reduced voltage onto the TGc or TGr line. Further, the full pulse applied to the TGr and/or TGc line during a conditional read-out operation (and/or during a reset operation) may be replaced by a burst of fractional pulses as shown at 922, thus establishing a uniform (fractional) width for each pulse applied. In one embodiment, the full pulse width during conditional-readout phase 5 is on the order of 200 to 1000 nanoseconds (nS), while the fractional pulse width is on the order of 2 to 200 nanoseconds, though other fractional and/or full pulse widths may apply in alternative embodiments. Although shown as operative for a split-gate embodiment, similar fractional pulse methods are also applicable to the operation of, for example, a Figure 14 or Figure 16 embodiment.

[00152] Figure 35 illustrates an exemplary implementation of the dual-control gate 871 shown in Figure 31. In the implementation shown, two distinct polysilicon features 925 and 927 are formed in immediate proximity to one another over the substrate region between photodiode 260 and floating diffusion 262 with a separation distance (" d_{sep} ") shorter than the minimum inter-poly distance specified for polysilicon lines of drain-to-source-coupled transistors, but long

enough to ensure electrical isolation between the two polysilicon features (i.e., sufficient separation to avoid shorting the features to one another). In one fabrication technique, the two polysilicon features are formed separately to enable a distance d_{sep} that is less than the minimum lithographic feature size. In an alternative embodiment, a single polysilicon feature is formed and then etched or otherwise split/divided into two distinct polysilicon features (e.g., with d_{sep} set to the minimum lithographic feature size or smaller). In the implementation shown, sidewall spacers 929, 931 are formed with respect to each polysilicon line, with spacer structures formed within separation region merging as shown at 933 (i.e., due to the narrow d_{sep} dimension) so that subsequent doping to form source/drain implant structures is blocked within the separation region, thus avoiding formation of such a carrier trapping structure in the otherwise continuous substrate region between photodiode 260 and floating diffusion 262, yielding the dual-gate control described above. While polysilicon feature 925 (Poly 1) is shown as the gate element coupled to TGr and polysilicon feature 927 (Poly 1') as the gate element coupled to TGc, that interconnection arrangement may be reversed in alternative embodiments.

[00153] Figure 36 illustrates an alternative manner of implementing the dual-control gate structure 871 of Figure 31. In this embodiment, a first polysilicon feature 941 is formed (e.g., lithographically printed and etched), covered with a layer of insulating material 945, and then a second polysilicon feature 943 is formed over the top of the first. A portion of the second polysilicon feature (not shown) is etched away to expose and enable metal-layer contact to the initial polysilicon feature 941 without removing the (insulating) material 945 that remains in the separation region (i.e., the region marked by " d_{sep} "). By this operation, d_{sep} may be made arbitrarily small (i.e., as small as possible while maintaining integrity of the insulating material within the separation region and thus electrical isolation between the two polysilicon features) and the overall footprint of the dual-control gate is similar to a single-control gate. Various alternative and/or supplemental fabrication techniques may be employed in other embodiments to form the dual-gate structure between photodiode 260 and floating diffusion 262.

[00154] Figure 37 illustrates a quad-pixel, shared floating diffusion image sensor architecture in which pairs of row and column transfer-gate control lines (TGr1/TGr2 and TGc1/TGc2) are coupled to a dual-gate structure (957.1-957.4) within each of four split-gate pixels in the manner described above. More specifically, by centralizing a shared floating diffusion 955 between four pixels (each also including a respective one of photodiodes PD1-PD4 and one of dual-control transfer gates 957.1-957.4, together with shared reset-gate transistor 409, source follower 405 and read-select transistor 407) and splitting the column transfer-gate control line TGc into separate odd and even column-enable lines (TGc1 and TGc2, each coupled to a respective

column-line driver), a highly compact pixel layout may be achieved. Figures 38 and 39 illustrate exemplary physical layouts of the quad-pixel of Figure 37, showing the four photodiodes disposed about and switchably coupled to a centralized floating diffusion (“FD”) via respective dual-control gate structures. In the embodiment of Figure 38, row lines (TGr1, TGr2) are coupled to respective gate elements 961 nearest the photodiodes and column lines are coupled to gate elements 962 nearest the floating diffusion (i.e., gate elements 961 and 962 collectively forming a dual-gate), while that interconnect order is reversed in the embodiment of Figure 39, with row lines coupled to gate elements 972 nearest the floating diffusion and column lines coupled to gate elements 971 nearest the photodiodes. In both layouts, each row line may be coupled to the gate elements for photodiodes in the same row (e.g., PD1/PD3 or PD2/PD4 in the example shown) via a single metal-to-poly contact and each column line may likewise be coupled to the gate elements for photodiodes in the same column (e.g., PD1/PD2 or PD3/PD4) via a single contact, thus halving the contact area as compared to implementations that require two interconnects per signal line per quad pixel. Also, in the embodiments of both Figures 38 and 39, the shared reset gate transistor, read-select transistor and source follower transistor are disposed at the periphery of the photodiode cell as shown at 964, 965 and 966 in Figure 38 and 974, 975 and 976 in Figure 39 (each transistor being shown as a polysilicon line over a diffusion region, omitting interconnect lines to avoid obscuring other features of the drawing). In both layouts, the transistors may be disposed in positions/locations other than those shown. For example, all three shared transistors may be co-located at the same edge of a given pixel, or all or one or more of the transistors may be disposed in a central region of the quad pixel between rows or columns of the photodiodes. Also, while a consolidated diffusion region is shown, the diffusion region may alternatively be split into two or more interconnected diffusion regions. The structures shown allow both individual and selective charge-binned readout of pixels with the quad group.

[00155] Figures 40 and 41 illustrate a split-gate pixel architecture and corresponding timing diagram according to an alternative embodiment that lacks a dedicated row transfer-gate (TGr) line. More specifically, the read-select and row transfer-gate control functions are merged within a single read-select (or row-select) signal coupled to row gate element 881 and to read-select transistor 257 as shown, thus reducing the number of row signal lines per pixel row from three to two (column transfer gate element 883 and the remaining shared transistors (255, 259) are connected as described above). This row line reduction may be particularly beneficial in front-side illuminated implementations as the 33% row metal reduction increases the overall fill factor of the pixel array. Even in backside illuminated embodiments, the row line reduction may

simplify per-cell signal line interconnection, possibly reducing the number of metal layers required or otherwise reducing fabrication complexity and cost. Note that frontside or backside illumination may be employed with respect to any of the embodiments disclosed herein.

[00156] Referring to Figure 41, reset, integration, noise-sampling, overthreshold detection and conditional read-out operations are carried out generally as described in reference to Figure 32, except that row transfer gate element 981 is switched to conducting and non-conducting states through assertion and deassertion of the read-select signal (RS), and overthreshold and conditional read-out operations are managed by asserting partial potential (and/or pulse width) and full potential (and/or full pulse sequence) on the column control line (TGc). Thus, a photodiode reset is effected by asserting TGc concurrently with read-select signal assertion, overthreshold detection is carried out by raising TGc to the VTG_{partial} potential (and/or applying a reduced-width TGc pulse) concurrently with read-select signal assertion, and conditional read-out is executed by conditionally (selectively) raising TGc to the VTG_{full} potential as shown. In the embodiment of Figure 40, row gate element 981 is disposed nearest the floating diffusion and the column gate element 983 is disposed nearest the photodiode. This disposition may be reversed in alternative embodiments.

[00157] Figure 42A illustrates an alternative dual-control gate arrangement in which the gate elements of a dual-control gate are formed by respective p-doped and n-doped regions of a transfer gate diode 987. The doping is achieved by depositing a lightly or intrinsically doped polysilicon, and using the pinning implants and FD implants to dope the PD and FD sides of the TG respectively. Alternate methods can also be employed. With this structure the TGr signal is connected to the p-type side of the diode 987 via a first contact (not shown), and the TGc signal is connected to the n-type side of the diode 987 via a separate, second contact (also not shown). Electrical isolation of the two gate control signals is achieved by diode isolation and does not require two physically separate polysilicon structures. As a result the dual-control gate is smaller.

[00158] Figure 42B illustrates another alternative dual-control gate arrangement in which the gate elements of a dual-control transfer gate 990 are formed by respective p-doped regions of back-to-back diodes having a shared n-doped region 991. The doping is achieved by depositing a lightly or intrinsically doped polysilicon, and using the pinning implants, FD implants and/or specific transfer gate doping implants to dope the PD and FD sides and center n-type region (991) of the dual-control transfer gate, respectively. As with all embodiments disclosed herein, alternative fabrication methods can be employed. With this structure the TGr signal is connected to the p-type side of the diode adjacent to the PD via a separate contact, (not shown),

and the TGc signal is connected to the p-type side of the diode 990 adjacent to the FD via a separate contact, (not shown). Electrical isolation of the two gate control signals is achieved by diode isolation (intervening n-type region 991) and does not require two physically separate polysilicon structures.

[00159] Figure 43 illustrates a 4x1 block of split-pixels (a quad, split-pixel block) that may be operated in binned or independent-pixel modes as described above, for example, in reference to Figure 21. As shown, floating diffusion regions FD₁₂ and FD₃₄ for upper and lower pixel pairs, respectively, are interconnected via conductor 992 (or alternatively formed by a single floating diffusion region), thus permitting, for example, the states of photodiodes PD1 and PD3 or photodiodes PD2 and PD4 to be read conjunctively (i.e., read concurrently or as one). Each photodiode in the 4x1 pixel block is switchably coupled to a floating diffusion node via a dual-control gate, with a row gate element 993 coupled to a respective one of the four row lines (i.e., TGr1-TGr4 for photodiodes PD1-PD4, respectively) and a column gate element 994 coupled to the per block column line. In the implementation shown, a shared column-line contact is coupled to each of the two column gate elements adjacent a given floating diffusion, thus halving the required number of column line interconnects. Shared transistors 995, 996 and 997 (i.e., reset-gate, source follower and read-select transistors) are disposed in regions between photodiodes PD1-PD4, though any or all of those transistors may be disposed at other positions. Also, while the row line is coupled to the dual-control gate element nearest the photodiode and column line coupled to the gate element nearest the floating diffusion, that arrangement may be reversed in alternative implementations.

[00160] When received within a computer system via one or more computer-readable media, such data and/or instruction-based expressions of the above described circuits can be processed by a processing entity (e.g., one or more processors) within the computer system in conjunction with execution of one or more other computer programs including, without limitation, net-list generation programs, place and route programs and the like, to generate a representation or image of a physical manifestation of such circuits. Such representation or image can thereafter be used in device fabrication, for example, by enabling generation of one or more masks that are used to form various components of the circuits in a device fabrication process.

[00161] In the foregoing description and in the accompanying drawings, specific terminology and drawing symbols have been set forth to provide a thorough understanding of the disclosed embodiments. In some instances, the terminology and symbols may imply specific details that are not required to practice those embodiments. For example, any of the specific numbers of bits, signal path widths, signaling or operating frequencies, component circuits or devices and

the like can be different from those described above in alternative embodiments. Additionally, links or other interconnection between integrated circuit devices or internal circuit elements or blocks may be shown as buses or as single signal lines. Each of the buses can alternatively be a single signal line, and each of the single signal lines can alternatively be buses. Signals and signaling links, however shown or described, can be single-ended or differential. A signal driving circuit is said to “output” a signal to a signal receiving circuit when the signal driving circuit asserts (or de-asserts, if explicitly stated or indicated by context) the signal on a signal line coupled between the signal driving and signal receiving circuits. The term “coupled” is used herein to express a direct connection as well as a connection through one or more intervening circuits or structures. Integrated circuit device “programming” can include, for example and without limitation, loading a control value into a register or other storage circuit within the integrated circuit device in response to a host instruction (and thus controlling an operational aspect of the device and/or establishing a device configuration) or through a one-time programming operation (e.g., blowing fuses within a configuration circuit during device production), and/or connecting one or more selected pins or other contact structures of the device to reference voltage lines (also referred to as strapping) to establish a particular device configuration or operation aspect of the device. The term “light” as used to apply to radiation is not limited to visible light, and when used to describe sensor function is intended to apply to the wavelength band or bands to which a particular pixel construction (including any corresponding filters) is sensitive. The terms “exemplary” and “embodiment” are used to express an example, not a preference or requirement. Also, the terms “may” and “can” are used interchangeably to denote optional (permissible) subject matter. The absence of either term should not be construed as meaning that a given feature or technique is required.

[00162] The section headings in the above detailed description have been provided for convenience of reference only and in no way define, limit, construe or describe the scope or extent of the corresponding sections or any of the embodiments presented herein. Also, various modifications and changes can be made to the embodiments presented herein without departing from the broader spirit and scope of the disclosure. For example, features or aspects of any of the embodiments can be applied, at least where practicable, in combination with any other of the embodiments or in place of counterpart features or aspects thereof. Accordingly, the specification and drawings are to be regarded in an illustrative rather than a restrictive sense.

CLAIMS

What is claimed is:

1. An integrated-circuit image sensor, comprising a pixel array having:
 - a first photodetector formed within a substrate;
 - a floating diffusion formed within the substrate;
 - first and second gate elements disposed adjacent one another over a first charge transfer region of the substrate between the first photodetector and the floating diffusion, the first and second gate elements respectively controlling first and second serial sections of the first charge transfer region;
 - a first row line extending in a row direction within the pixel array and coupled to the first gate element; and
 - a first column line extending in a column direction within the pixel array and coupled to the second gate element.
2. The integrated-circuit image sensor of claim 1, the pixel array further comprising:
 - a second photodetector formed within the substrate;
 - third and fourth gate elements disposed adjacent one another over a second charge transfer region of the substrate between the second photodetector and the floating diffusion, the third and fourth gate elements respectively controlling third and fourth serial sections of the second charge transfer region, the third gate element being coupled to the first row line; and
 - a second column line extending in a column direction within the pixel array and coupled to the fourth gate element.
3. The integrated-circuit image sensor of claim 2 wherein the first and third gate elements are formed by a continuous conductive feature.
4. The integrated-circuit image sensor of claim 2 wherein the first photodetector and second photodetector are constituents of respective pixels within a first row of pixels.
5. The integrated-circuit image sensor of claim 4, the pixel array further comprising:
 - a third photodetector formed within the substrate;
 - fifth and sixth gate elements disposed adjacent one another over a third charge transfer region of the substrate between the third photodetector and the floating diffusion, , the fifth and sixth gate elements respectively controlling fifth and sixth serial sections of the third charge transfer region, the sixth gate element being coupled to

- the first column line; and
a second row line extending in a row direction within the pixel array and coupled to the fifth gate element.
6. The integrated-circuit image sensor of claim 5 wherein the second and sixth gate elements are formed by a continuous conductive feature.
 7. The integrated-circuit image sensor of claim 5 wherein the first photodetector and third photodetector are constituents of respective pixels within a first column of pixels.
 8. The integrated-circuit image sensor of claim 1 wherein the first gate element is disposed over the first charge transfer region nearer the first photodetector than the second gate element and the second gate element is disposed over the first charge transfer region nearer the floating diffusion than the first gate element.
 9. The integrated-circuit image sensor of claim 1 wherein a spacing between the first and second gate elements is less than a minimum distance specified for implementing a source/drain implant between gate terminals of adjacent transistors under a fabrication process employed to fabricate the integrated-circuit image sensor.
 10. The integrated-circuit image sensor of claim 1 wherein the first and second gate elements constitute field-effect gate elements such that, when row and column control signals are asserted on the first row line and first column line, respectively, overlapping electrostatic fields are formed within the first charge transfer region, the overlapping electrostatic fields effecting formation of a charge-conducting channel within the first charge transfer region.
 11. The integrated-circuit image sensor of claim 10 further comprising row circuitry to assert, as at least part of the row control signal on the first row line, a partial-transfer pulse at a first time and a full-transfer pulse at a second time, the partial-transfer pulse enabling a partial transfer of charge from the first photodetector to the floating diffusion if charge accumulated within the first photodetector exceeds a threshold level, and the full-transfer pulse conditionally enabling a full transfer of charge from the first photodetector to the floating diffusion, the full transfer of charge effecting a reset of the photodetector.
 12. The integrated-circuit image sensor of claim 11 wherein the partial-transfer pulse and full transfer pulse differ from one another in respect to at least one of amplitude or duration.
 13. An integrated circuit image sensor comprising:
a substrate;
a plurality of row control signal lines and a plurality of column control signal lines;

- a plurality of photosensitive elements disposed within the substrate to accumulate charge in response to incident light;
- a shared floating diffusion disposed within the substrate to enable read-out of each of the photosensitive elements; and
- a plurality of dual-control transfer gates each disposed over a region of the substrate between a respective one of the photosensitive elements and the shared floating diffusion, each of the dual-control transfer gates including first and second gate elements controlled by a respective unique combination of one of the row control signal lines and one of the column control signal lines.
14. The integrated circuit image sensor of claim 13 wherein the first and second gate elements constitute field-effect gate elements such that, when first and second control signals are asserted concurrently on the respective unique combination of control signal lines, overlapping electrostatic fields are formed within the region of the substrate between the respective one of the photosensitive elements and the floating diffusion, the overlapping electrostatic fields effecting formation of a charge-conducting channel within the region of the substrate between the respective one of the photosensitive elements and the floating diffusion that enables charge accumulated within the one of the photosensitive elements to be transferred to the shared floating diffusion.
 15. The integrated circuit image sensor of claim 13 further comprising control circuitry to concurrently assert control signals on the respective unique combination of control signal lines during a first interval to enable determination of whether charge accumulated within the one of the photosensitive elements during integration interval exceeds a first threshold.
 16. The integrated circuit image sensor of claim 15 wherein the control circuitry further comprising circuitry to concurrently assert control signals on the respective unique combination of control signal lines during a second interval if the first threshold is determined to be exceeded, wherein concurrent assertion of control signals on the control signal lines during the second interval enables generation of a read-out signal corresponding to a level of charge accumulated within the one of the photosensitive elements during the integration interval.
 17. The integrated circuit image sensor of claim 15 wherein, in addition to enabling generation of the read-out signal, concurrent assertion of control signals on the respective unique combination of control signal lines resets the one of the photosensitive elements to an initial state in preparation for subsequent charge integration within the one of the

- photosensitive elements, and wherein, if the first threshold is determined not to be exceeded, subsequent charge integration is cumulative with respect to the charge accumulated within the one of the photosensitive elements during the integration interval.
18. The integrated circuit image sensor of claim 13 wherein a spacing between the first and second gate elements is less than a minimum distance specified for implementing a source/drain implant between gate terminals of adjacent transistors under a fabrication process employed to fabricate the integrated circuit image sensor.
 19. A method of operation within a pixel array having a photosensitive element and floating diffusion disposed within a substrate, the method comprising:
accumulating charge within the photosensitive element in response to incident light; and concurrently asserting a row control signal and a column control signal at respective gate elements disposed serially over a charge transfer region of the substrate between the photosensitive element and the floating diffusion to enable charge carriers to be conducted through the charge transfer region of the substrate from the photosensitive element to the floating diffusion, the row control signal being conveyed on a row line that extends in a row direction within the pixel array and the column control signal being conveyed on a column line that extends in a column direction within the pixel array.
 20. The method of claim 19 wherein concurrently asserting the row control signal and column control signal comprises:
concurrently asserting the row and column control signals during a first interval, after an exposure interval in which the charge is accumulated within the photosensitive element; and
when a quantity of the charge carriers conducted through the charge transfer region of the substrate during the first interval indicates that charge accumulated within the photosensitive element exceeds a first threshold, concurrently asserting the row and column control signals during a second interval to enable further charge carriers to be conducted through the charge transfer region of the substrate and generation of a read-out signal corresponding to a level of charge accumulated within the one of the photosensitive elements during the exposure interval.
 21. The method of claim 20 wherein concurrently asserting the row and column control signals during the first interval comprises asserting at least one of the row and column control signals at a partial potential that is lower than a full potential to which the at least one of

the row and column control signals is asserted during the second interval.

22. The method of claim 20 wherein concurrently asserting the row and column control signals during the first interval comprises asserting at least one of the row and column control signals for a fractional duration that is shorter than a full duration for which the at least one of the row and column control signals is asserted during the second interval.

FIG. 1

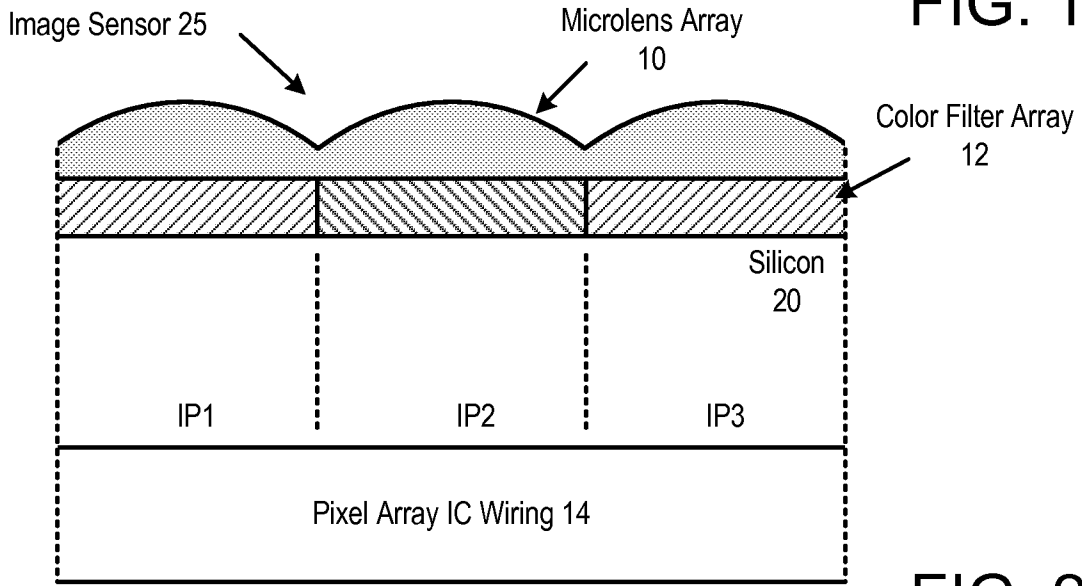
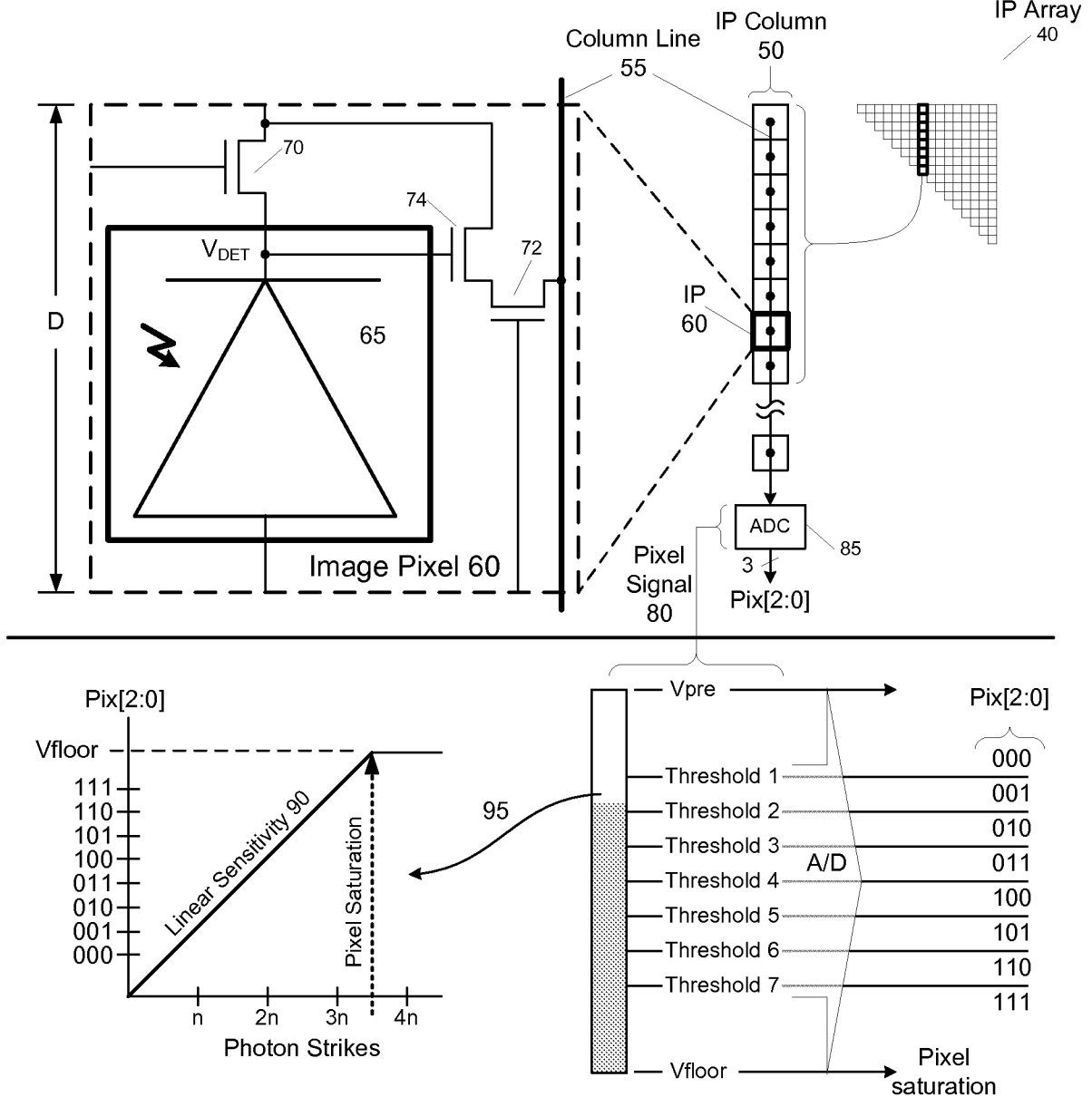


FIG. 2



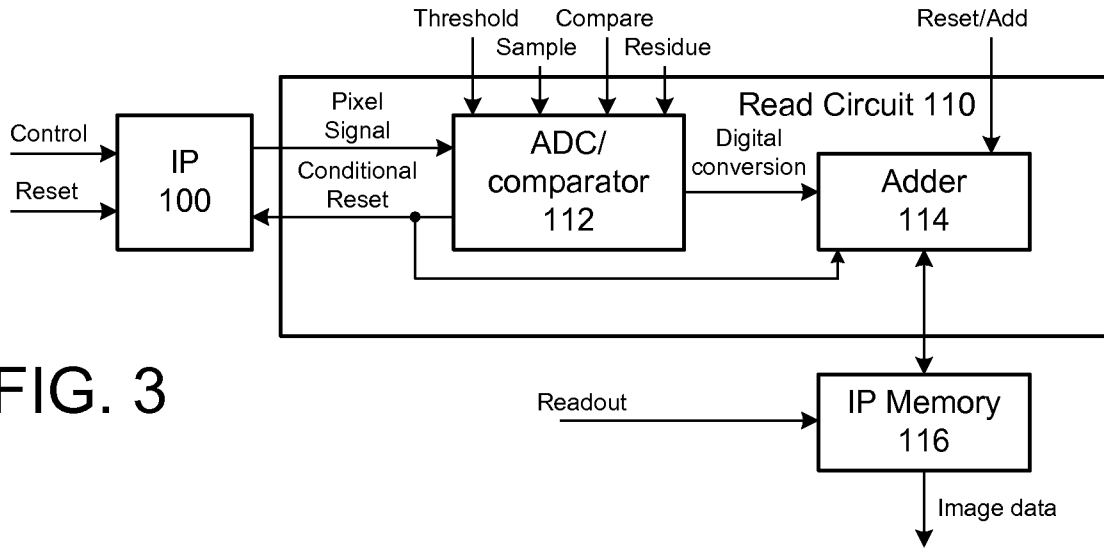
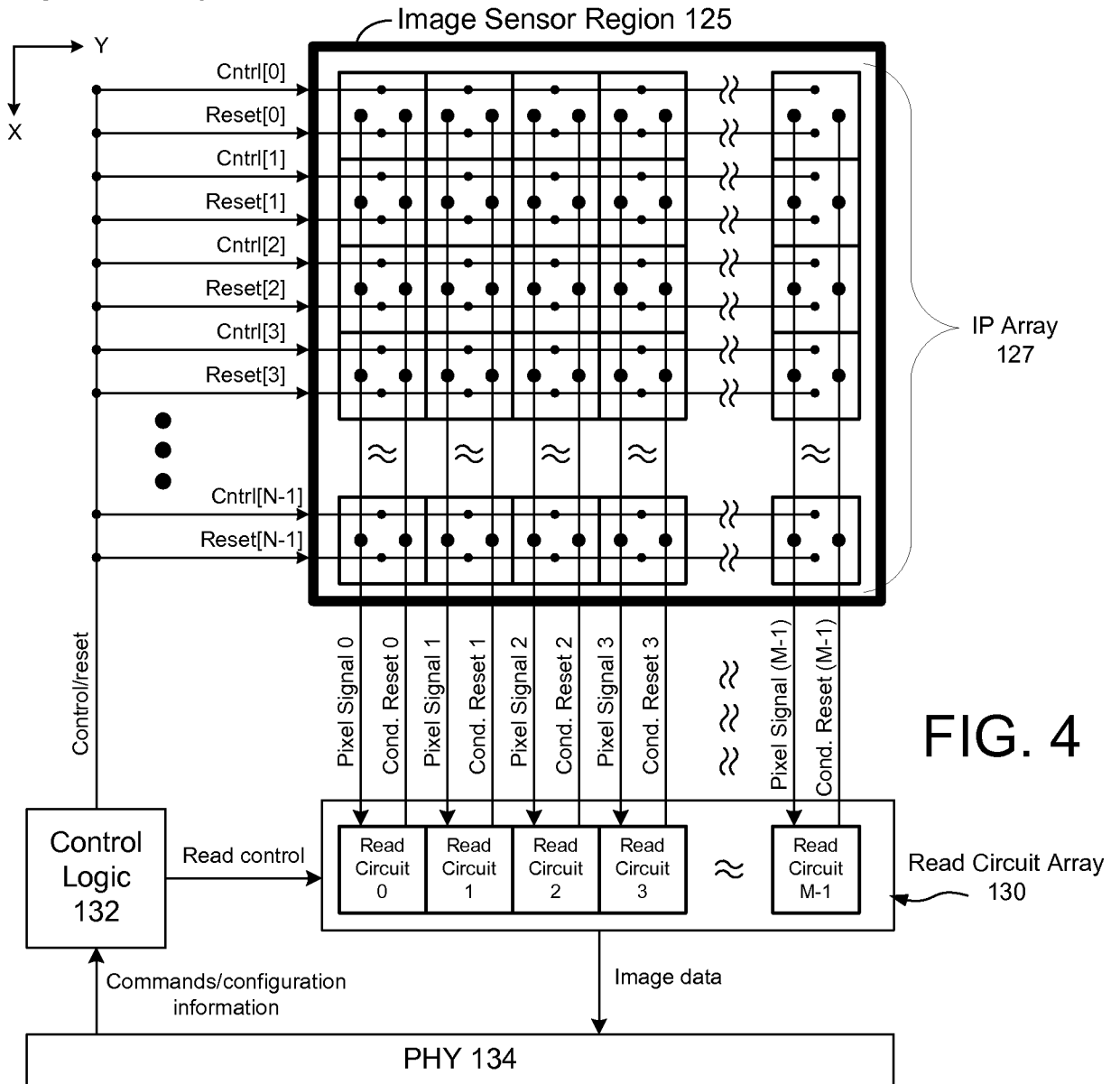
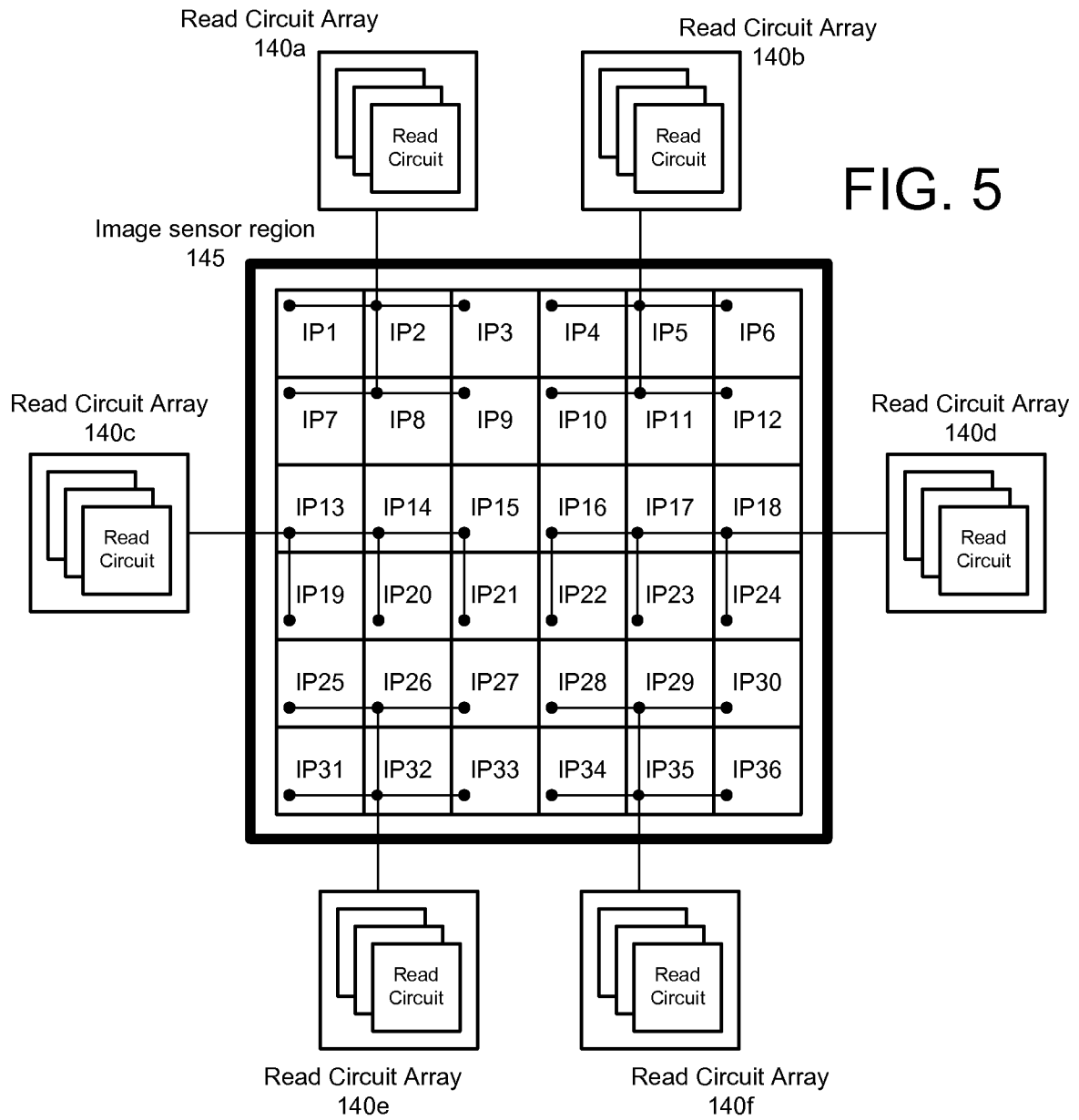


Image Sensor System 120





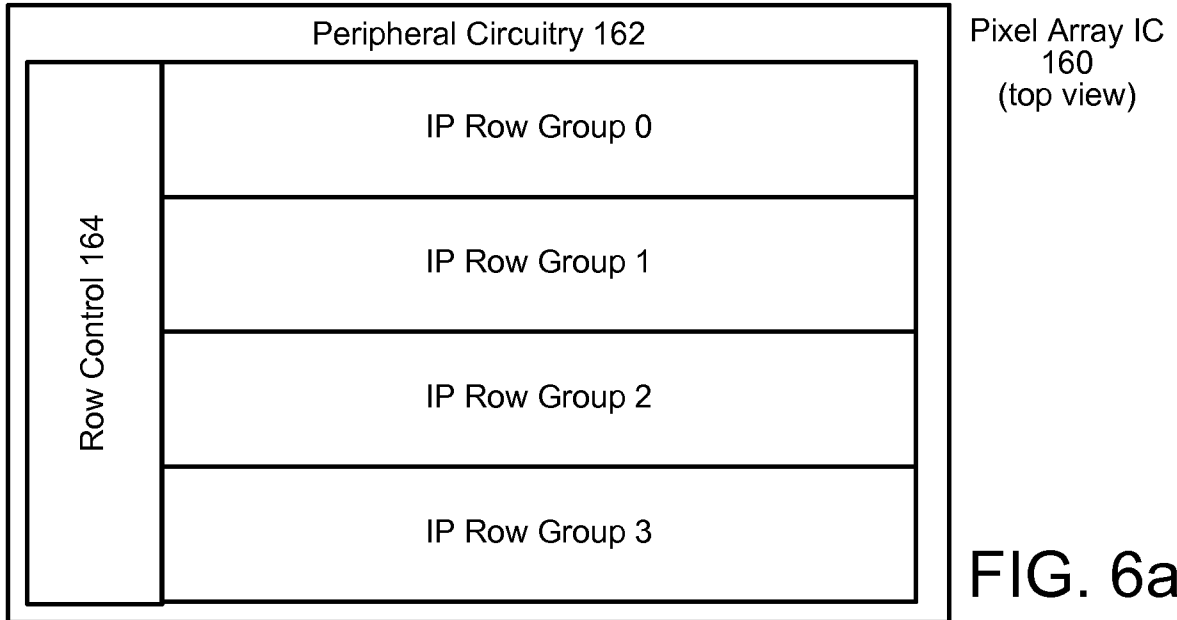


FIG. 6a

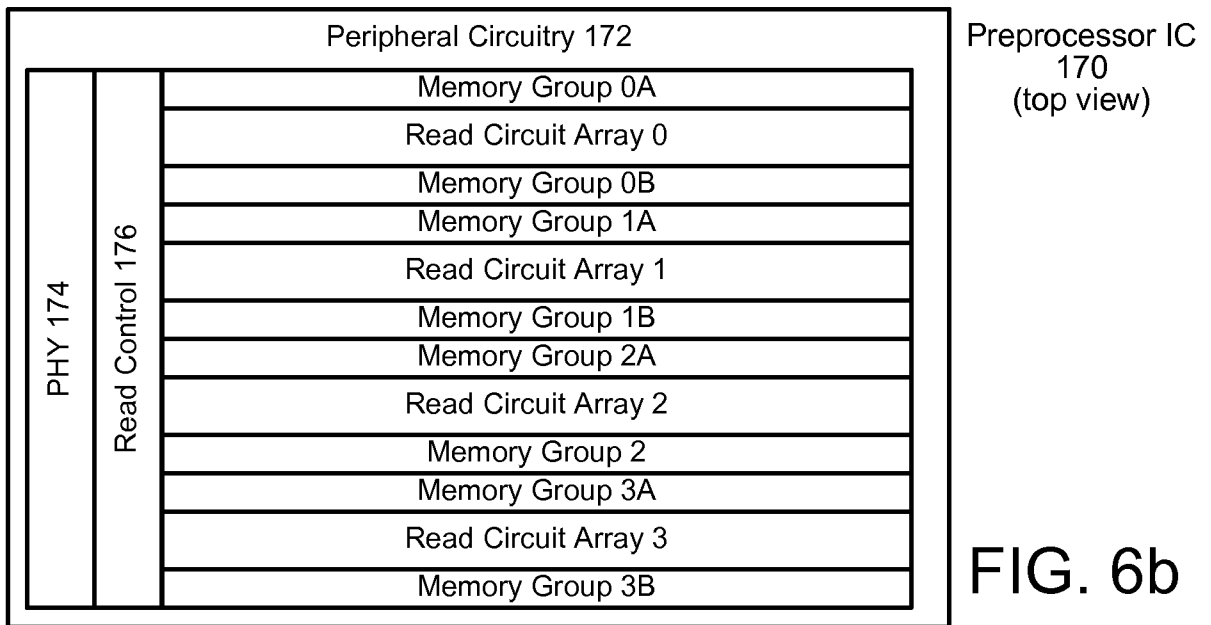


FIG. 6b

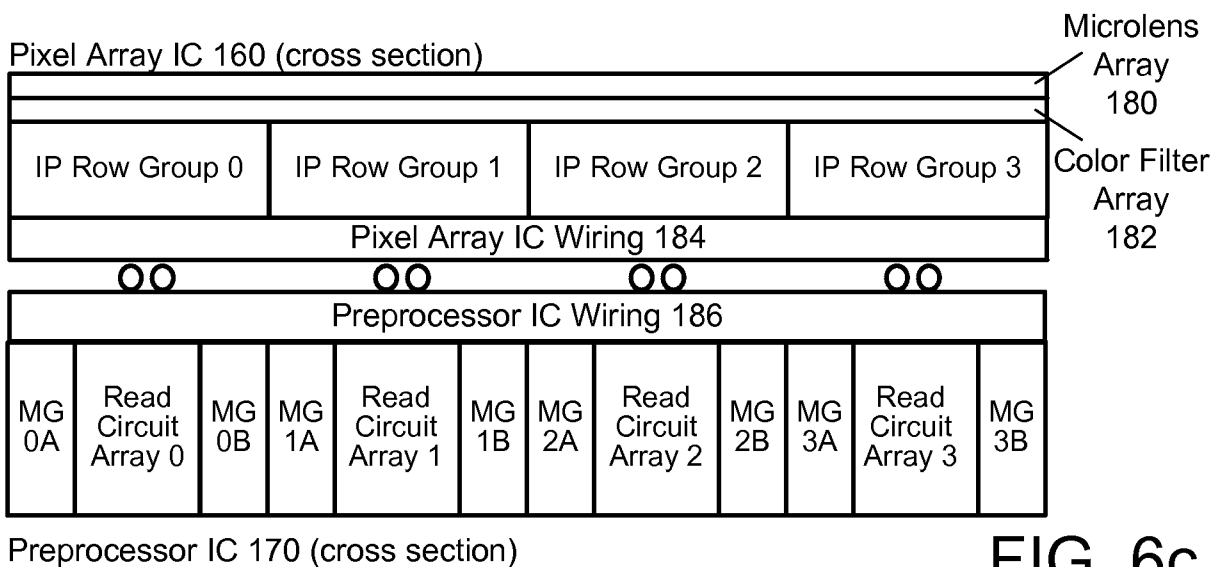


FIG. 6c

Control	Sampling interval	Photons (det. - accum.)	Threshold met?	ADC value	Memory Element
Begin exposure, Threshold = 20	0	N/A	N/A	X X X X X	X X X X X X X X X
	1	4 - 4	n	0 0 1 0 0	0 0 0 0 0 0 0 0 0
	2	7 - 11	n	0 1 0 1 1	0 0 0 0 0 0 0 0 0
	3	2 - 13	n	0 1 1 0 1	0 0 0 0 0 0 0 0 0
	4	11 - 24	y	1 1 0 0 0	0 0 0 0 1 1 0 0 0
	5	14 - 14	n	0 1 1 1 0	0 0 0 0 1 1 0 0 0
	6	8 - 22	y	1 0 1 1 0	0 0 0 1 0 1 1 1 0
	7	4 - 4	n	0 0 1 0 0	0 0 0 1 0 1 1 1 0
	8	0 - 4	n	0 0 1 0 0	0 0 0 1 0 1 1 1 0
	9	6 - 10	n	0 1 0 1 0	0 0 0 1 0 1 1 1 0
	10	13 - 23	y	1 0 1 1 1	0 0 1 0 0 0 1 0 1
	11	1 - 1	n	0 0 0 0 1	0 0 1 0 0 0 1 0 1
	12	2 - 3	n	0 0 0 1 1	0 0 1 0 0 0 1 0 1
	13	12 - 15	n	0 1 1 1 1	0 0 1 0 0 0 1 0 1
	14	13 - 28	y	1 1 1 0 0	0 0 1 1 0 0 0 0 1
	15	26 - 26	y	1 1 0 1 0	0 0 1 1 1 1 0 1 1
Reset, Residue	16	19 - 19	n	1 0 0 1 1	0 1 0 0 0 1 1 1 0

Residue 190
Image data 195

FIG. 7

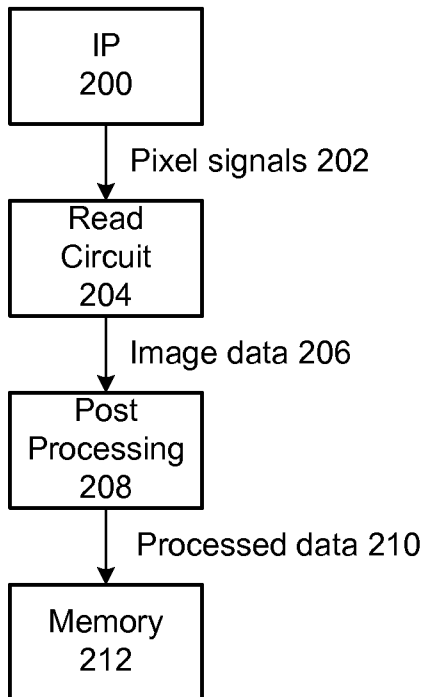


FIG. 8

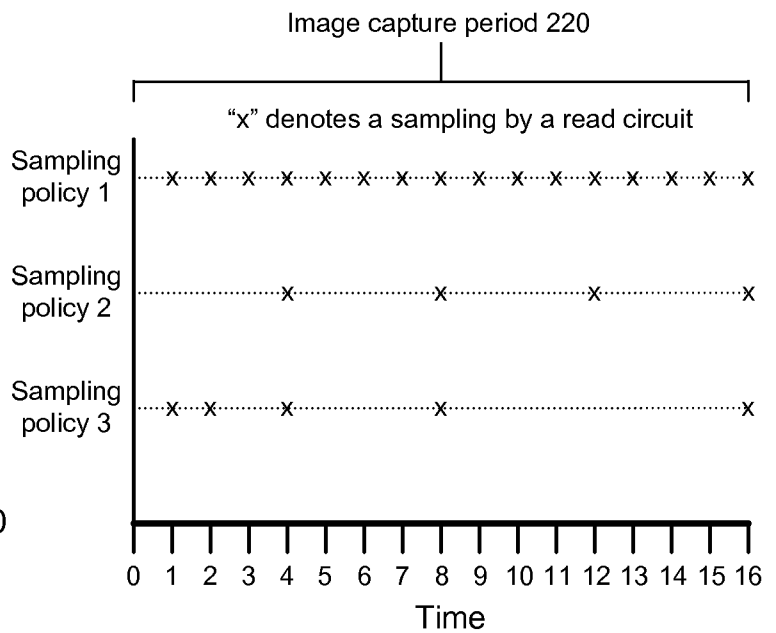
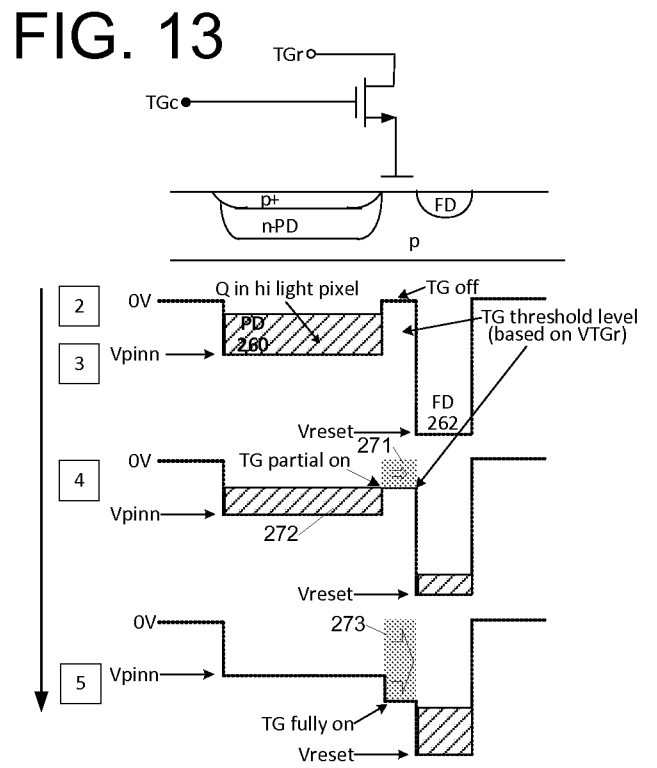
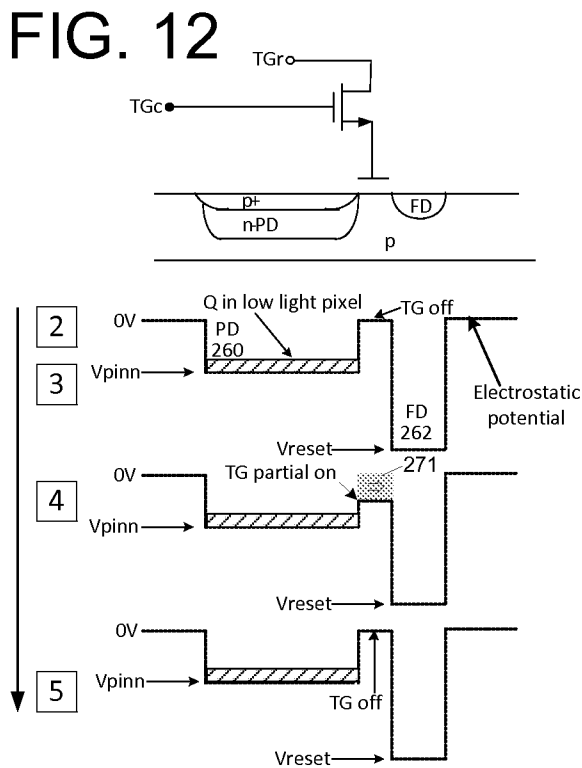
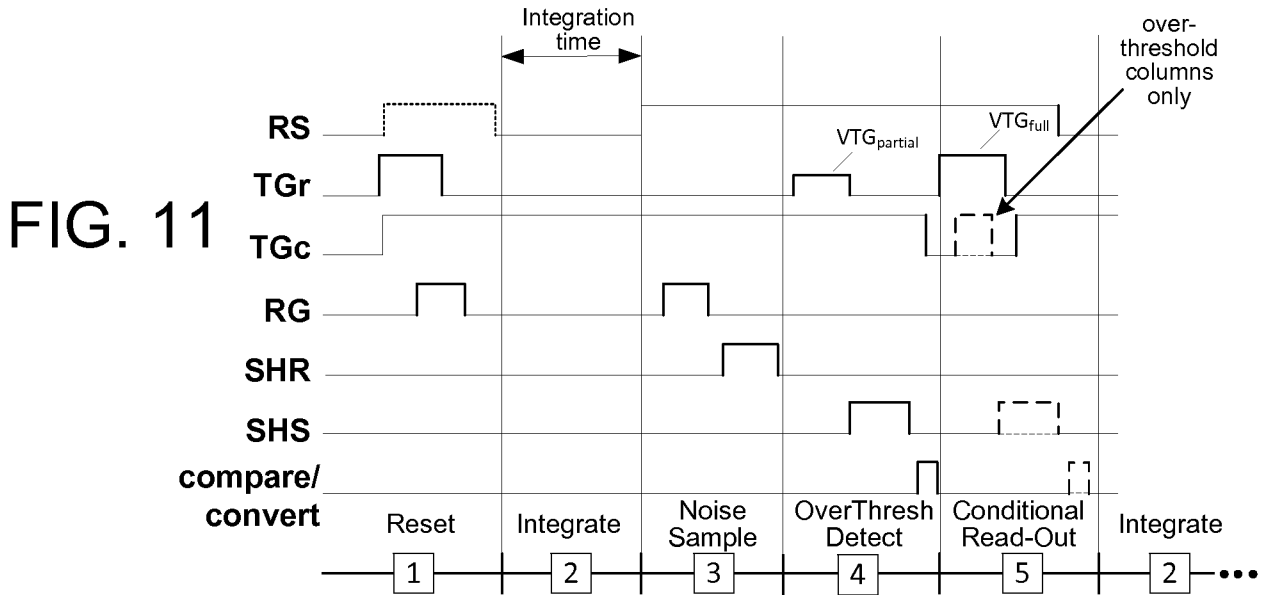
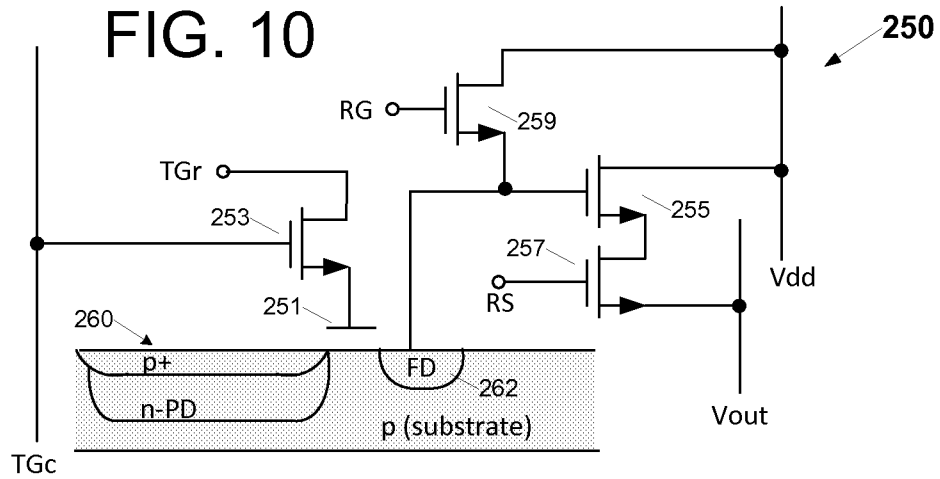


FIG. 9



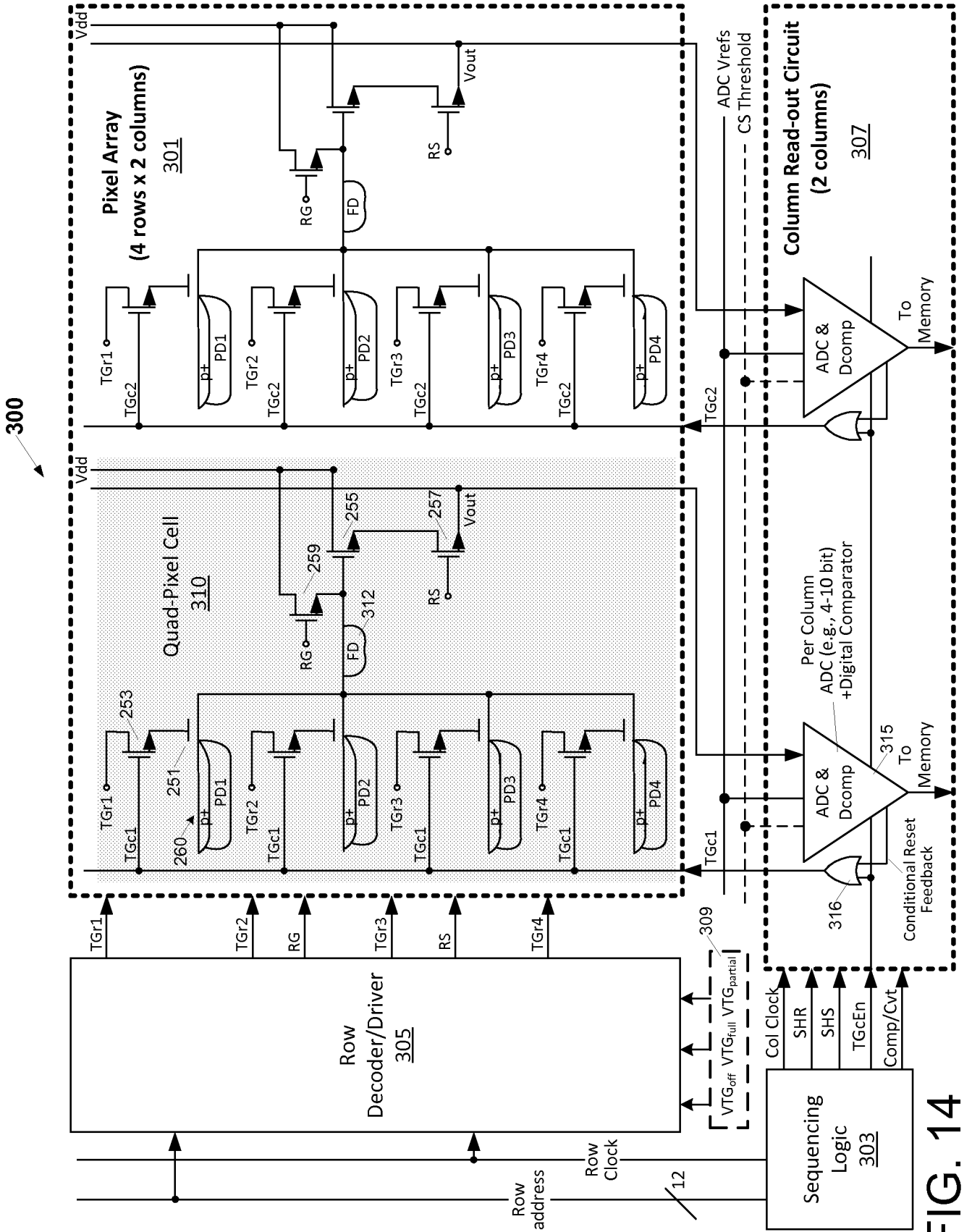


FIG. 14

FIG. 15A

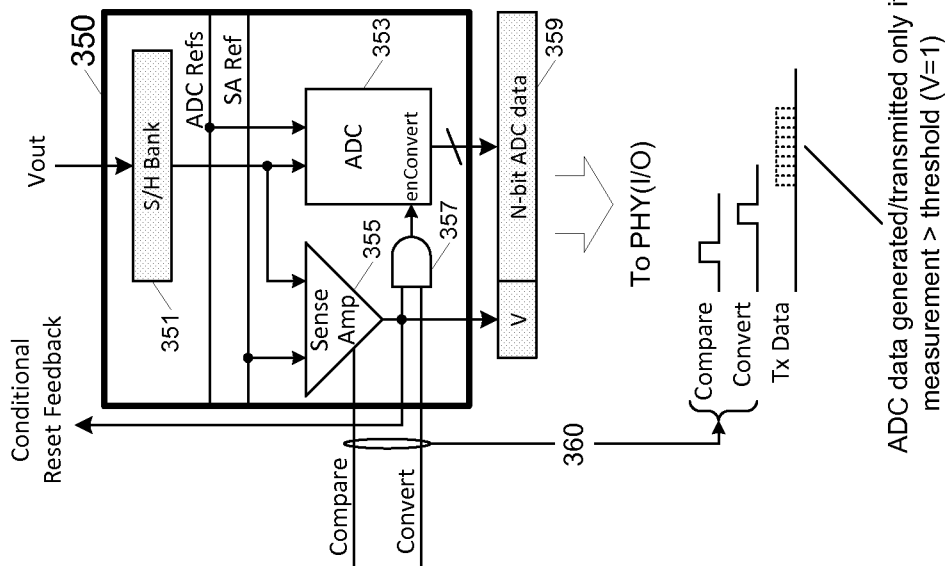


FIG. 15B

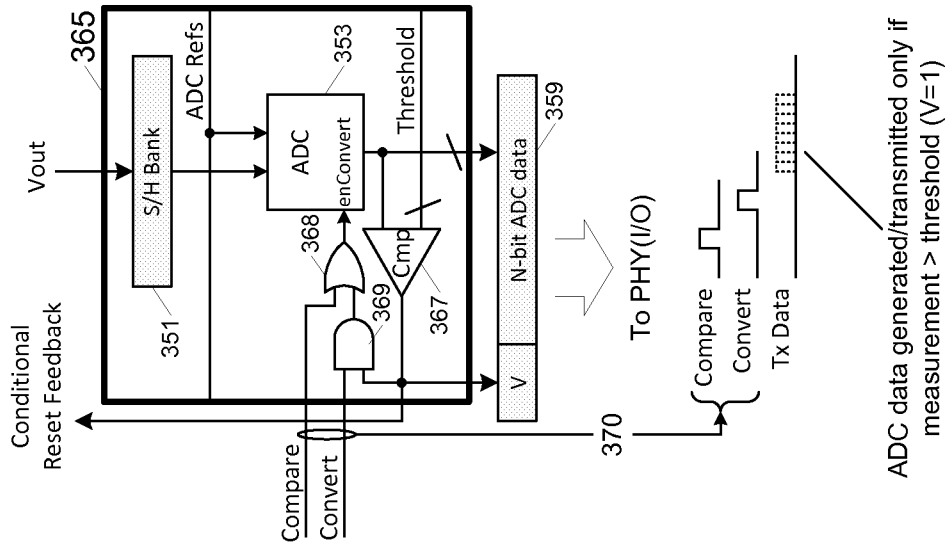


FIG. 15C

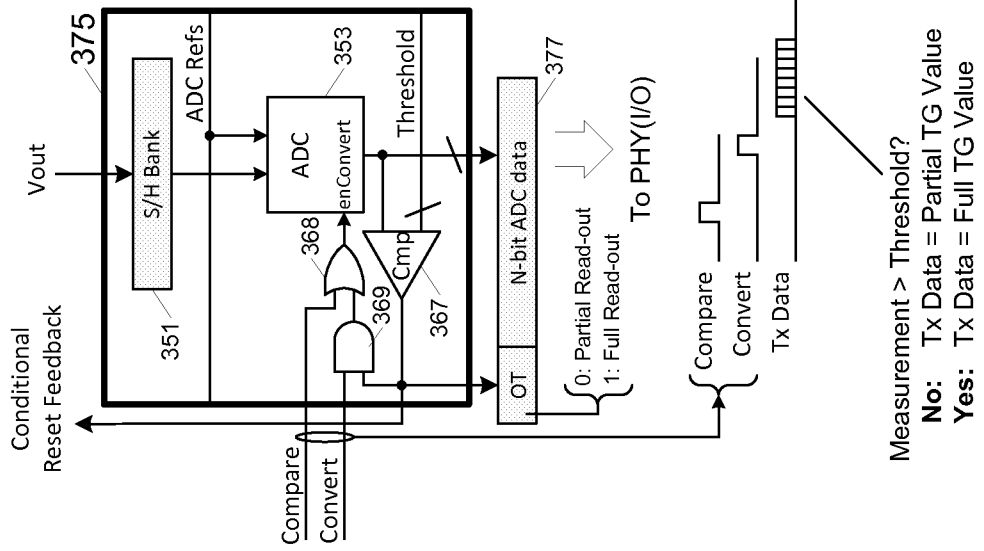


FIG. 19 Full Resolution Read-Out

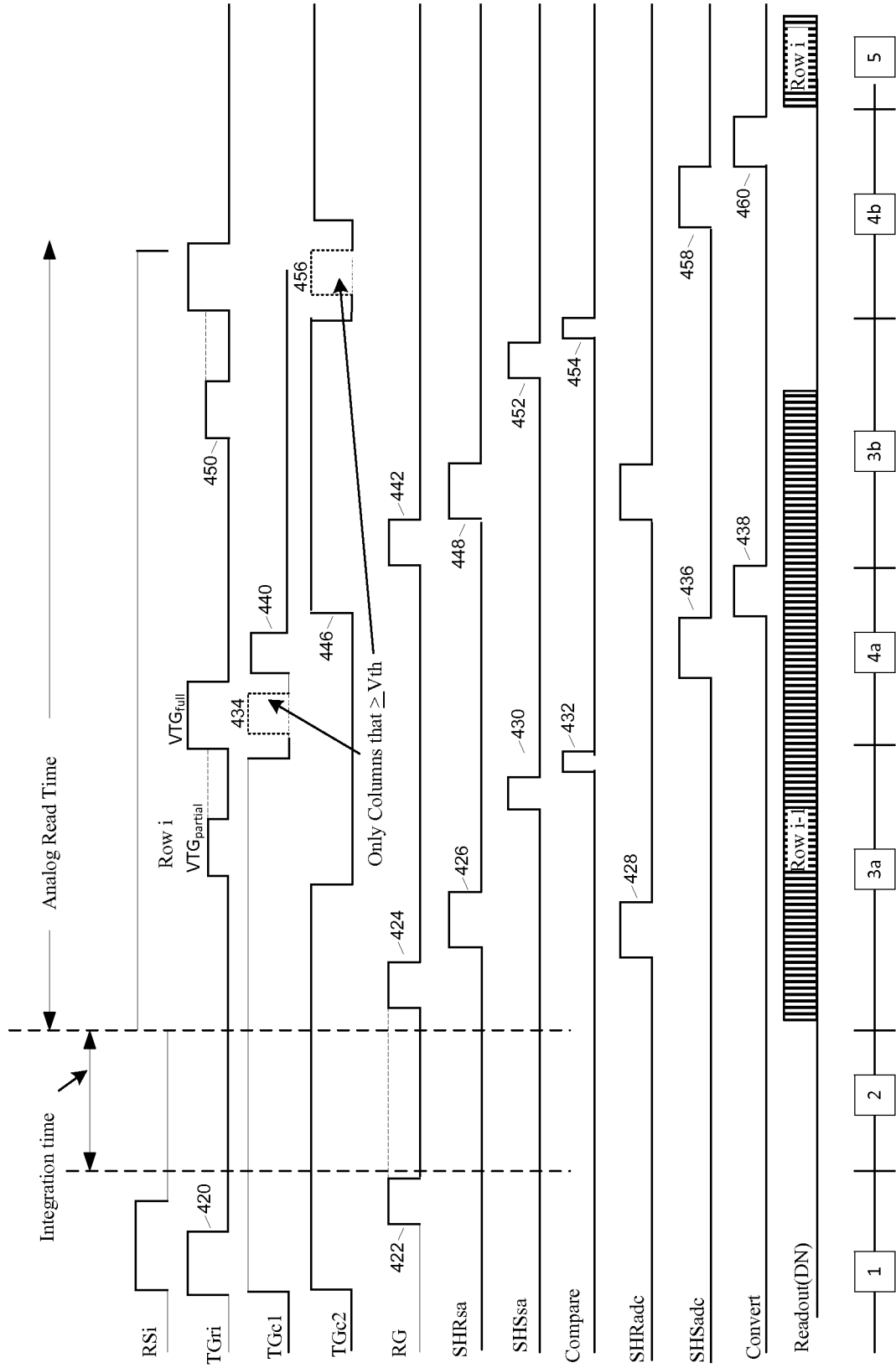


FIG. 20 Decimated (Binned) Read-Out

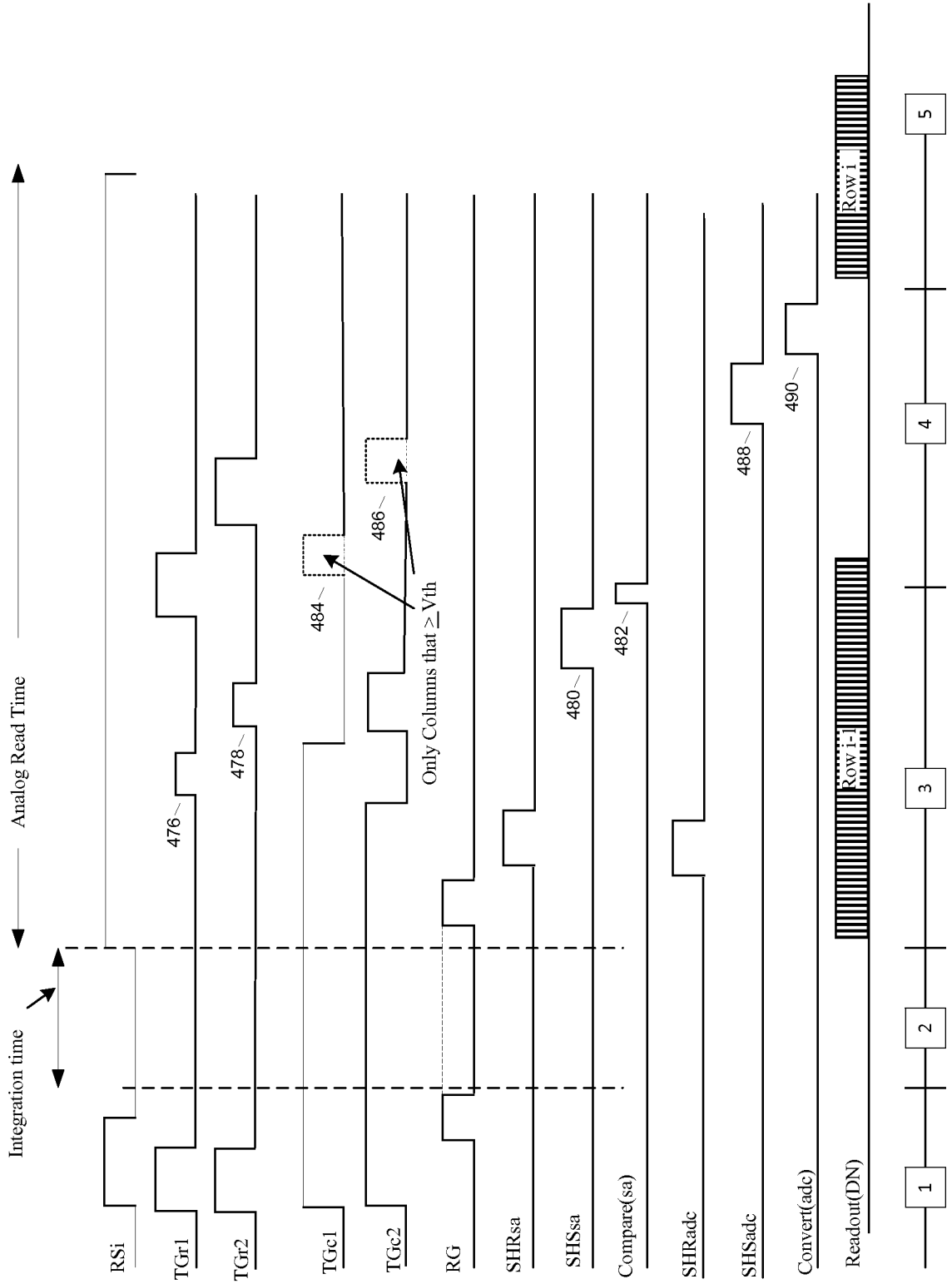


FIG. 21

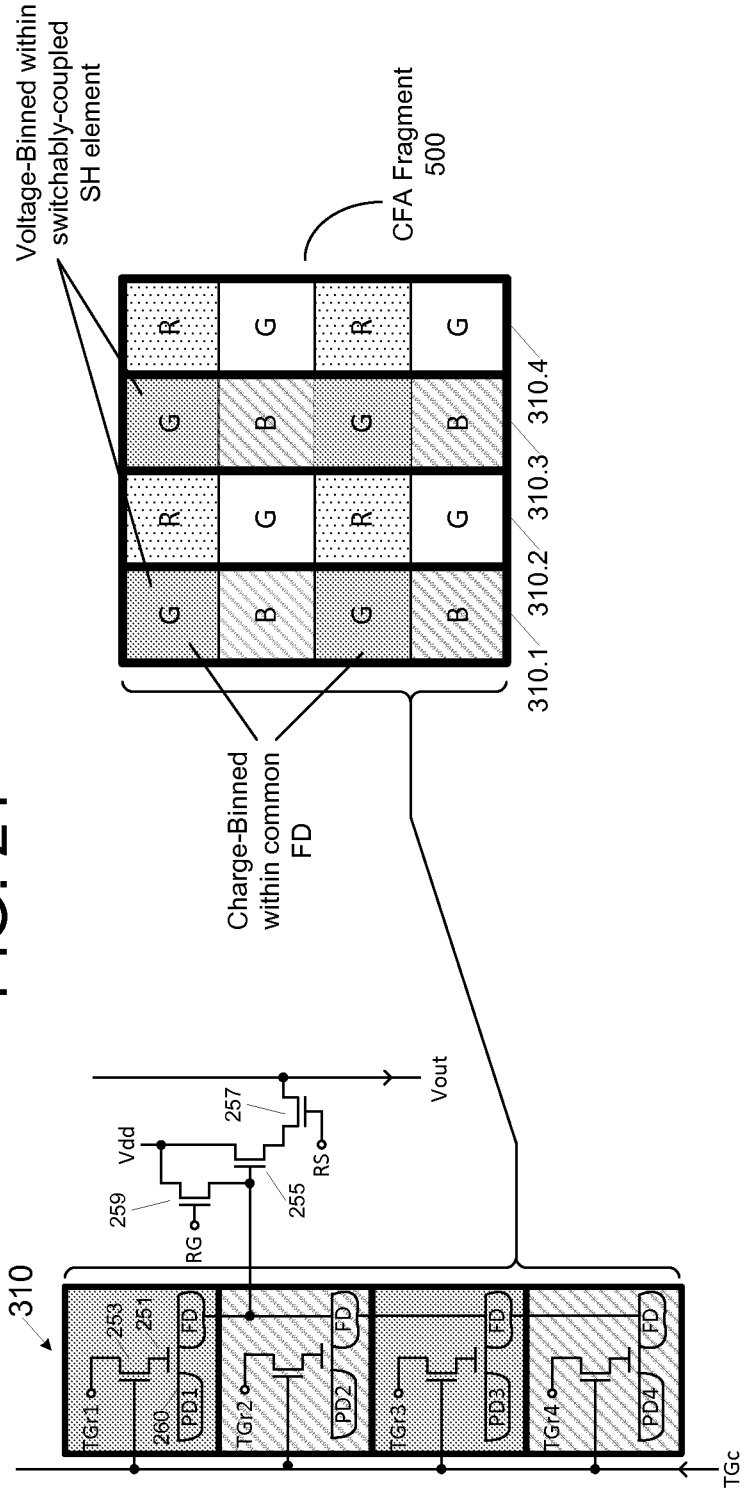
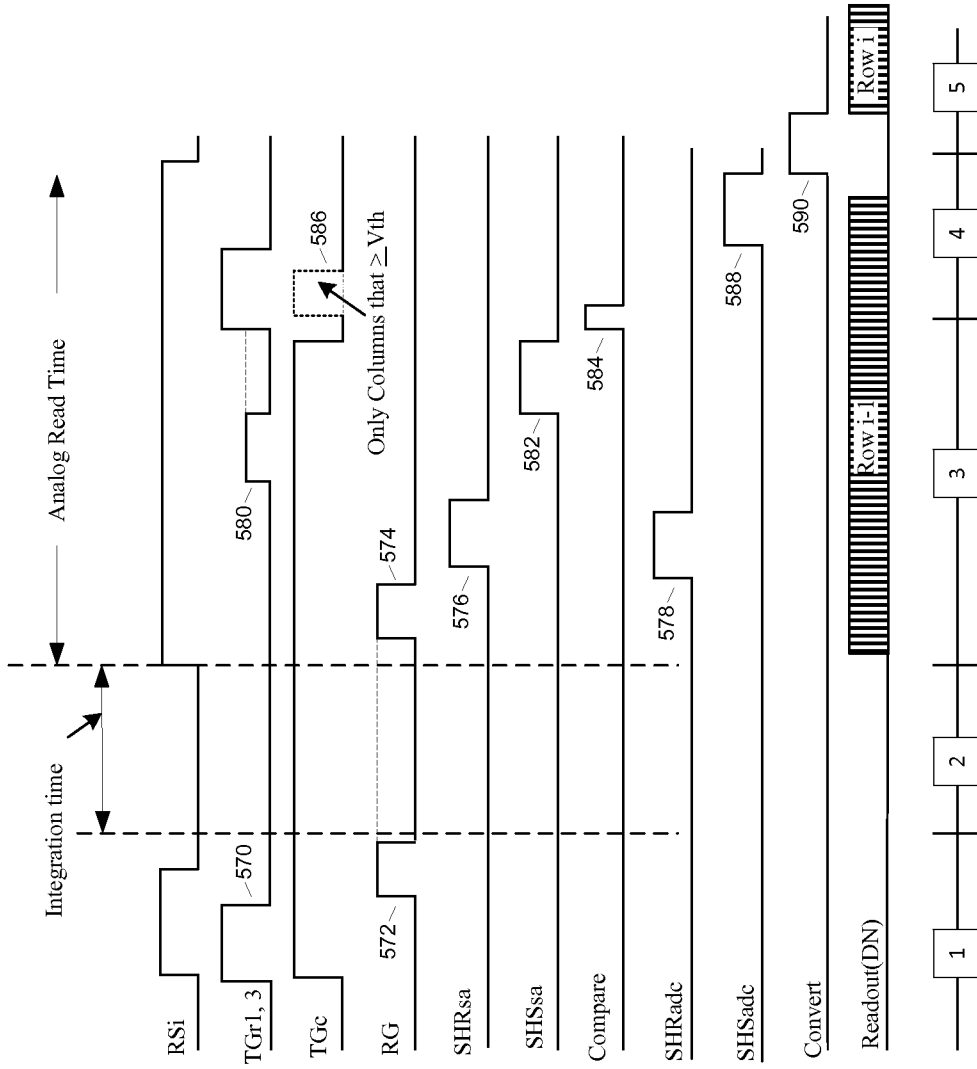


FIG. 23



Version 5 - 4x1 Shared Pixel Q-Binning

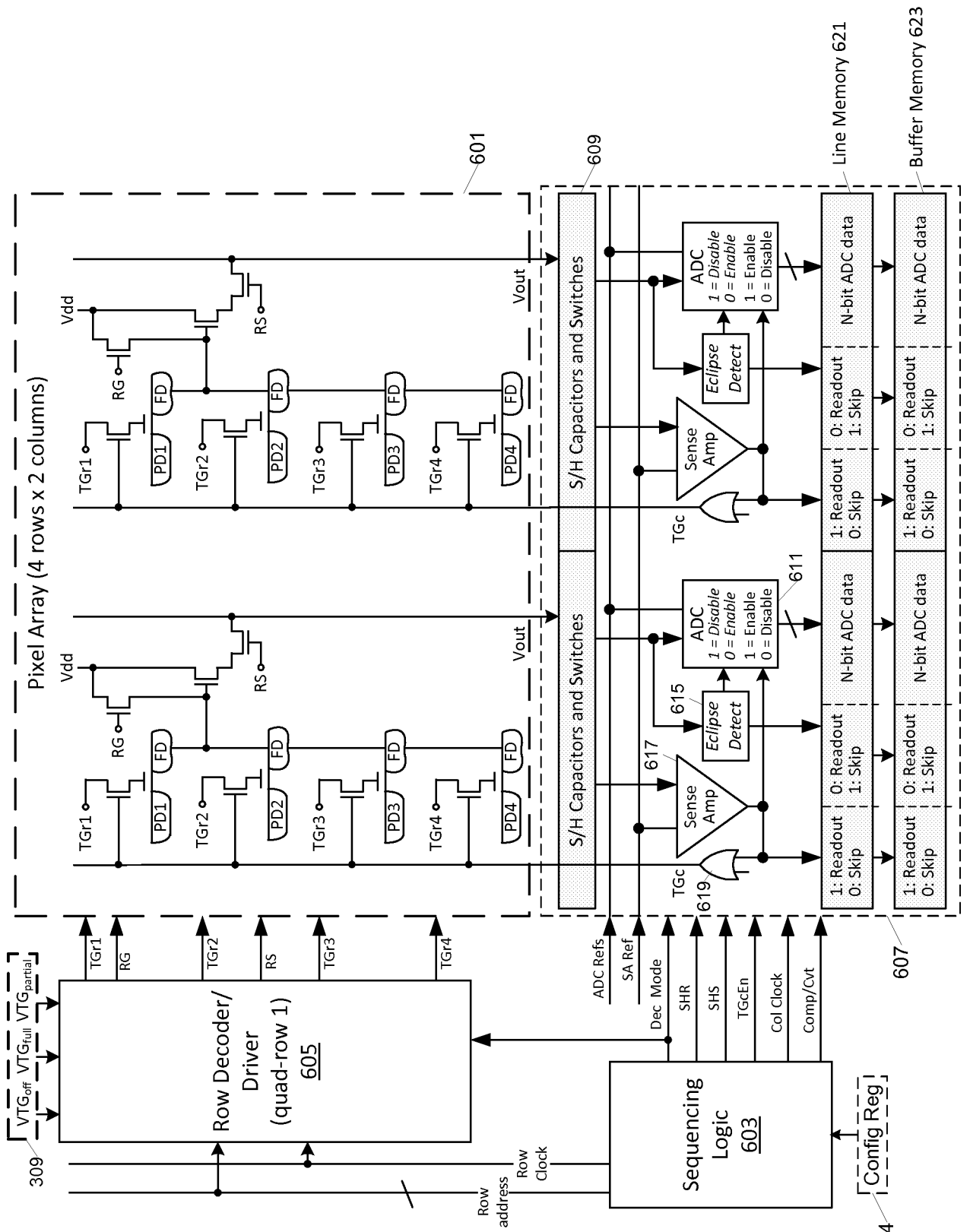


FIG. 24

600

FIG. 25A

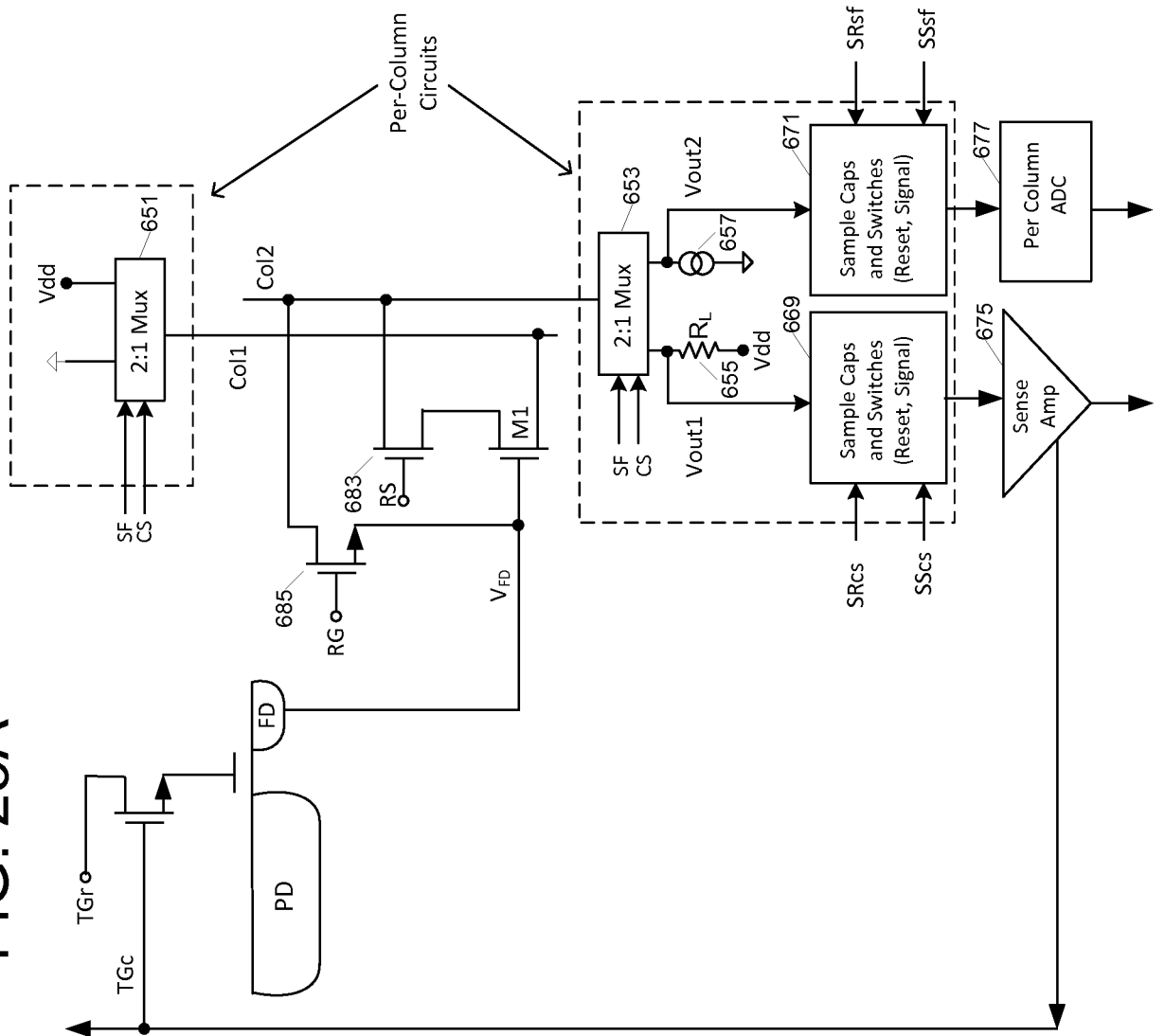


FIG. 25B

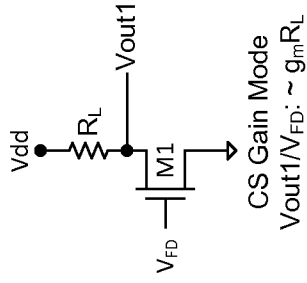


FIG. 25C

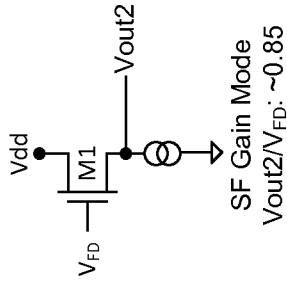


FIG. 27

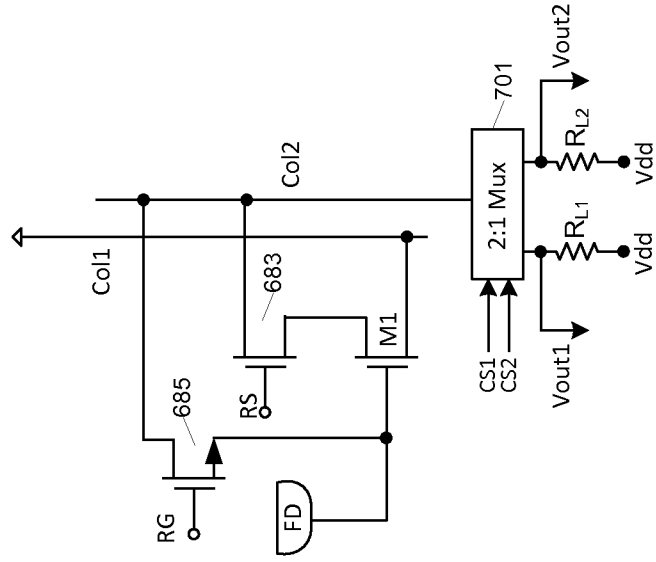
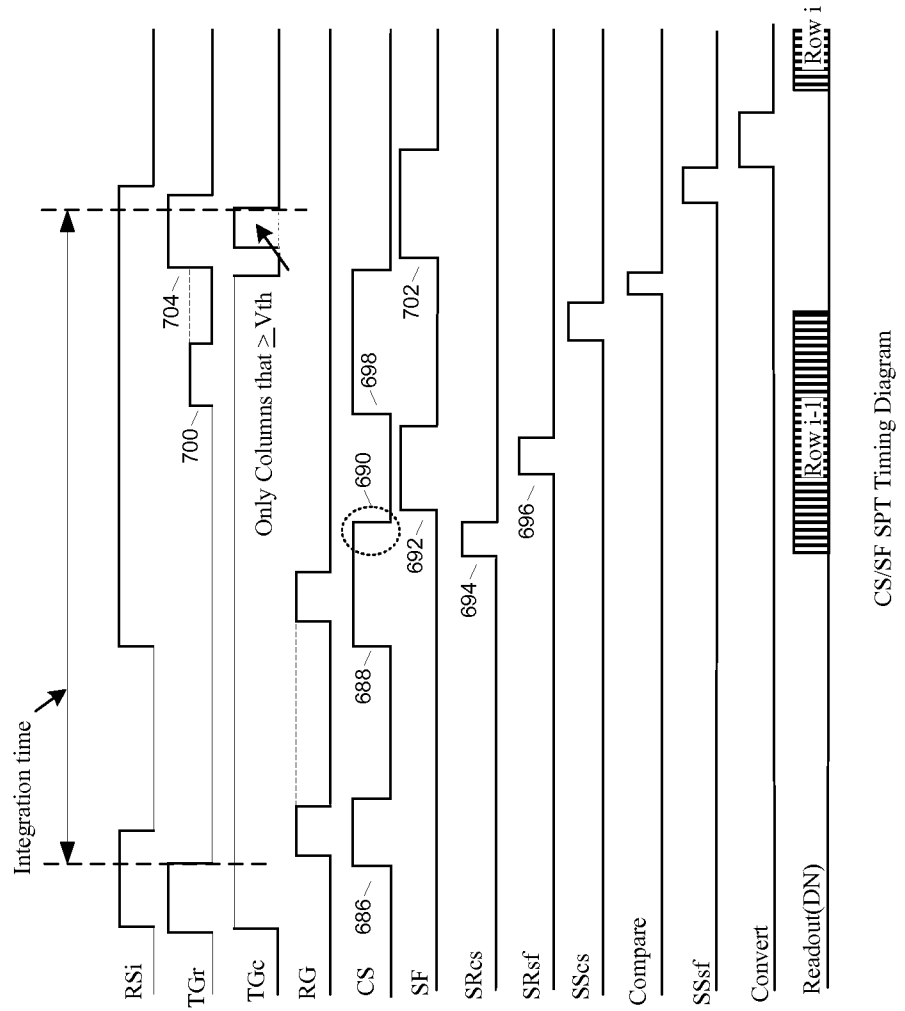


FIG. 26



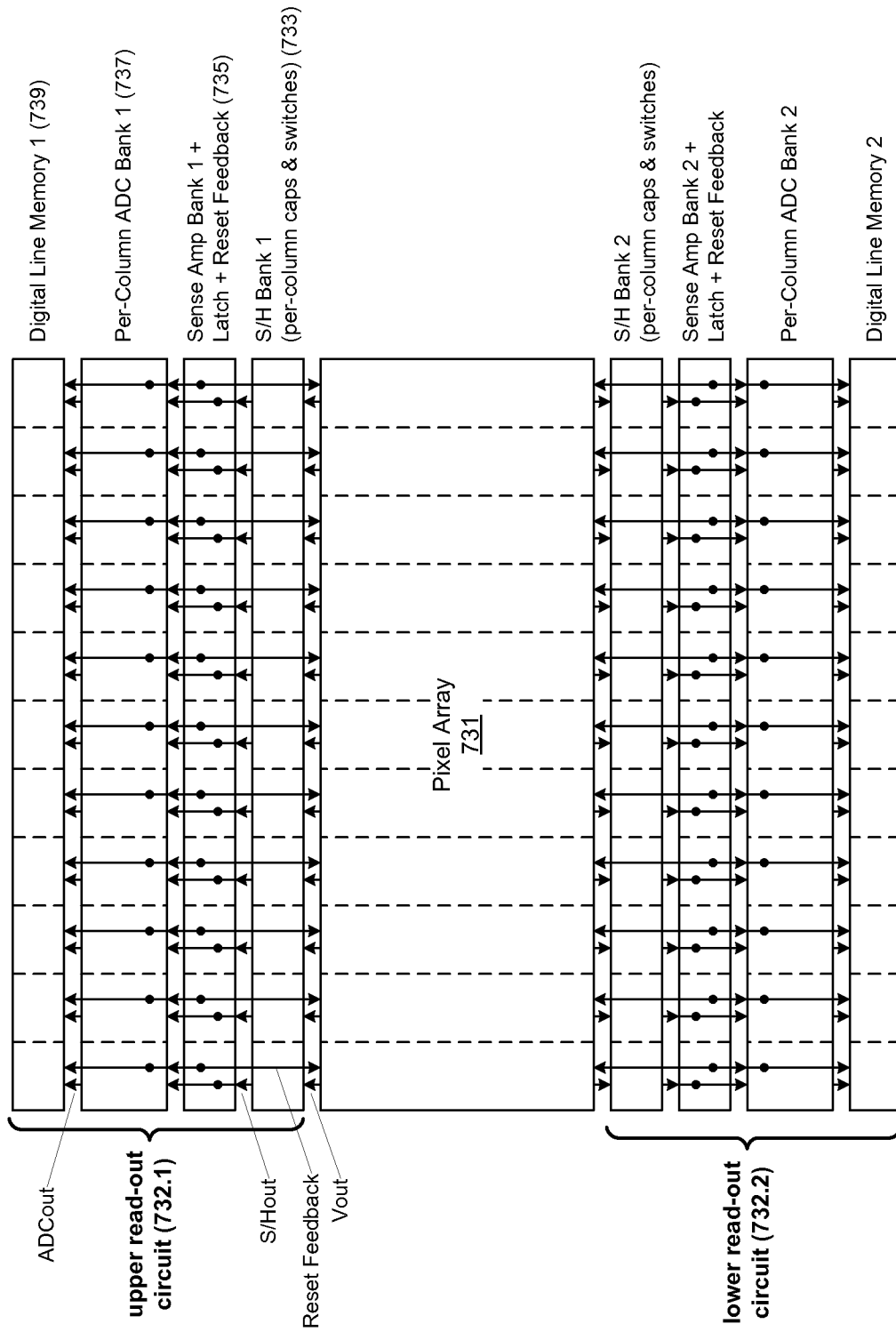


FIG. 28

FIG. 30

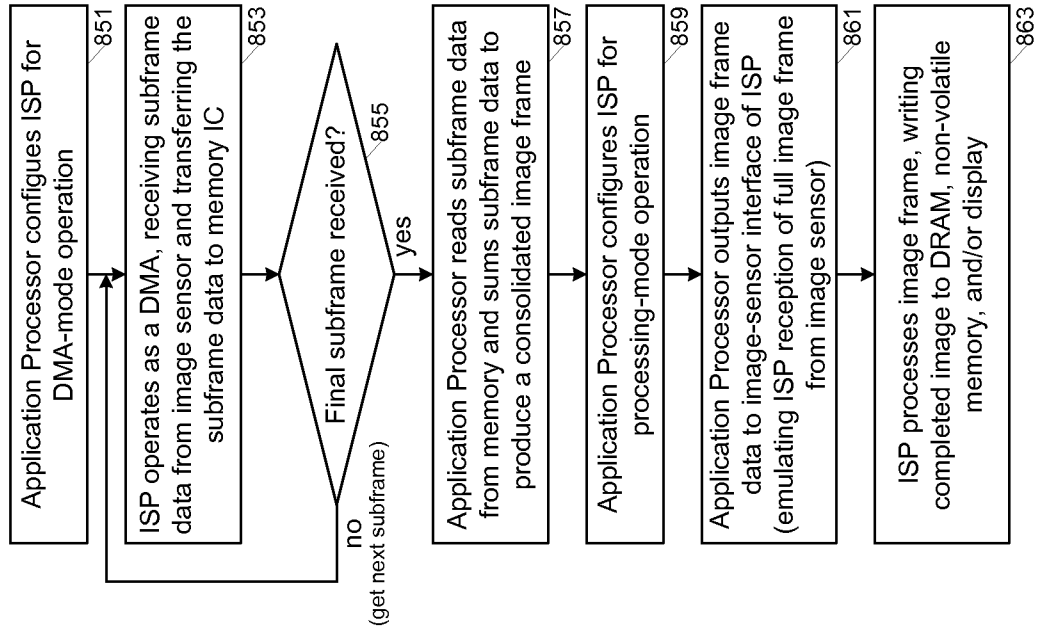
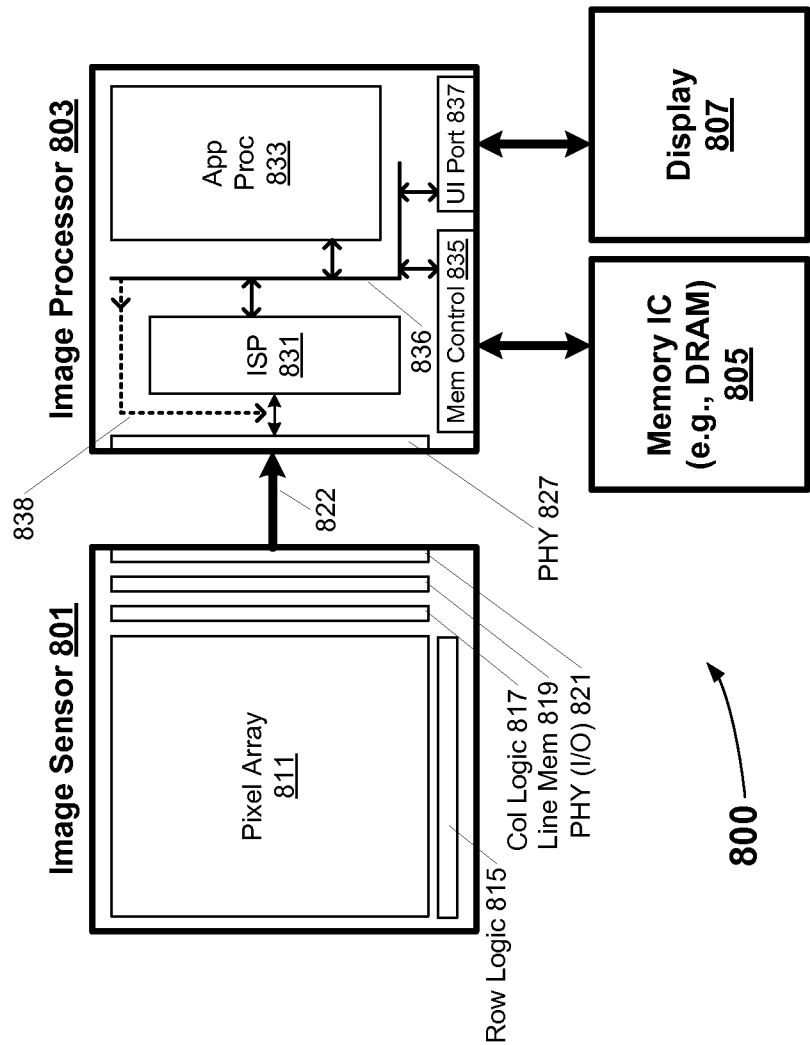


FIG. 29



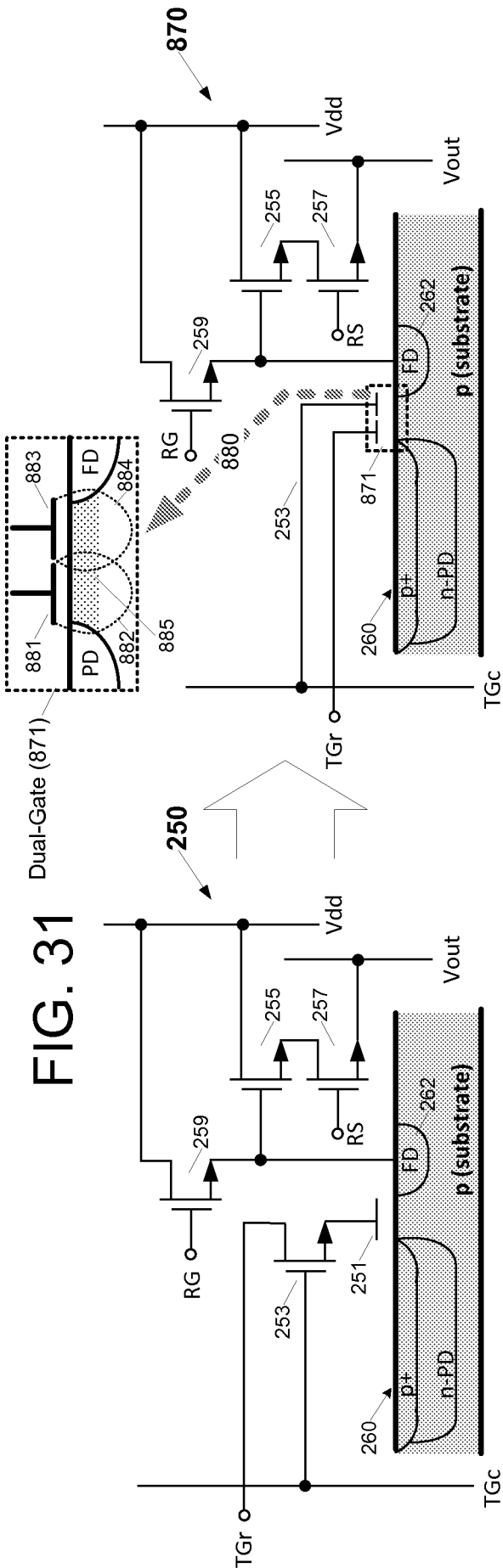


FIG. 31

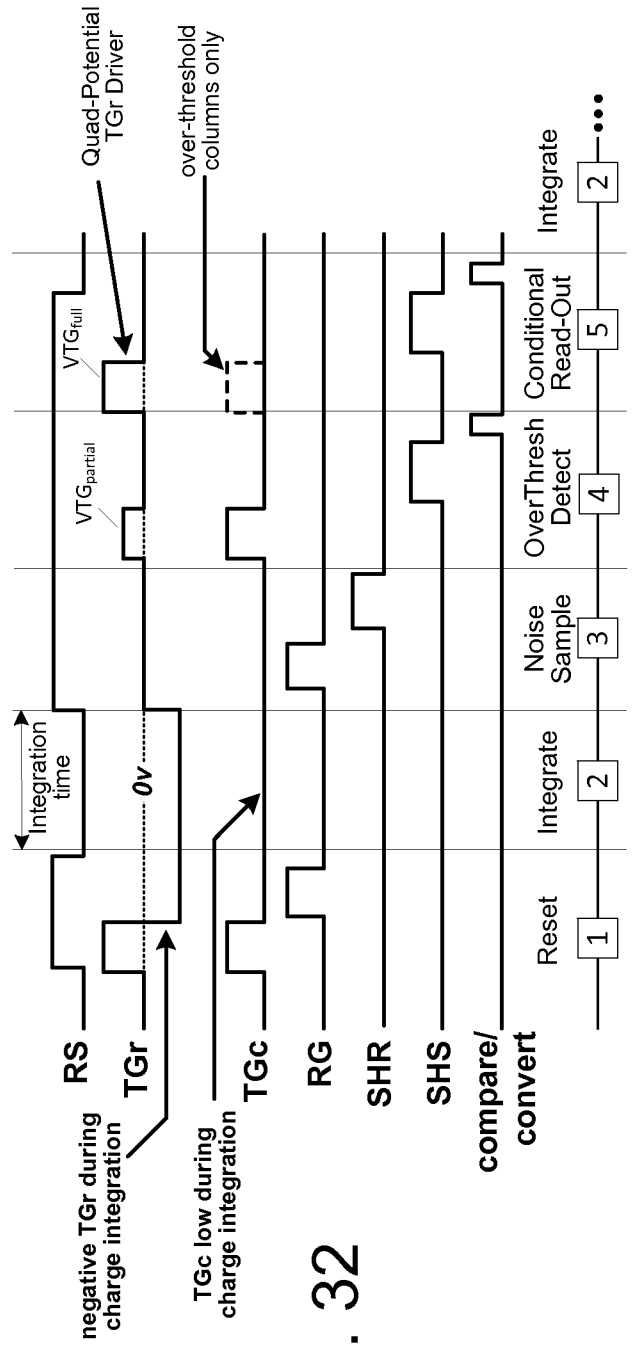
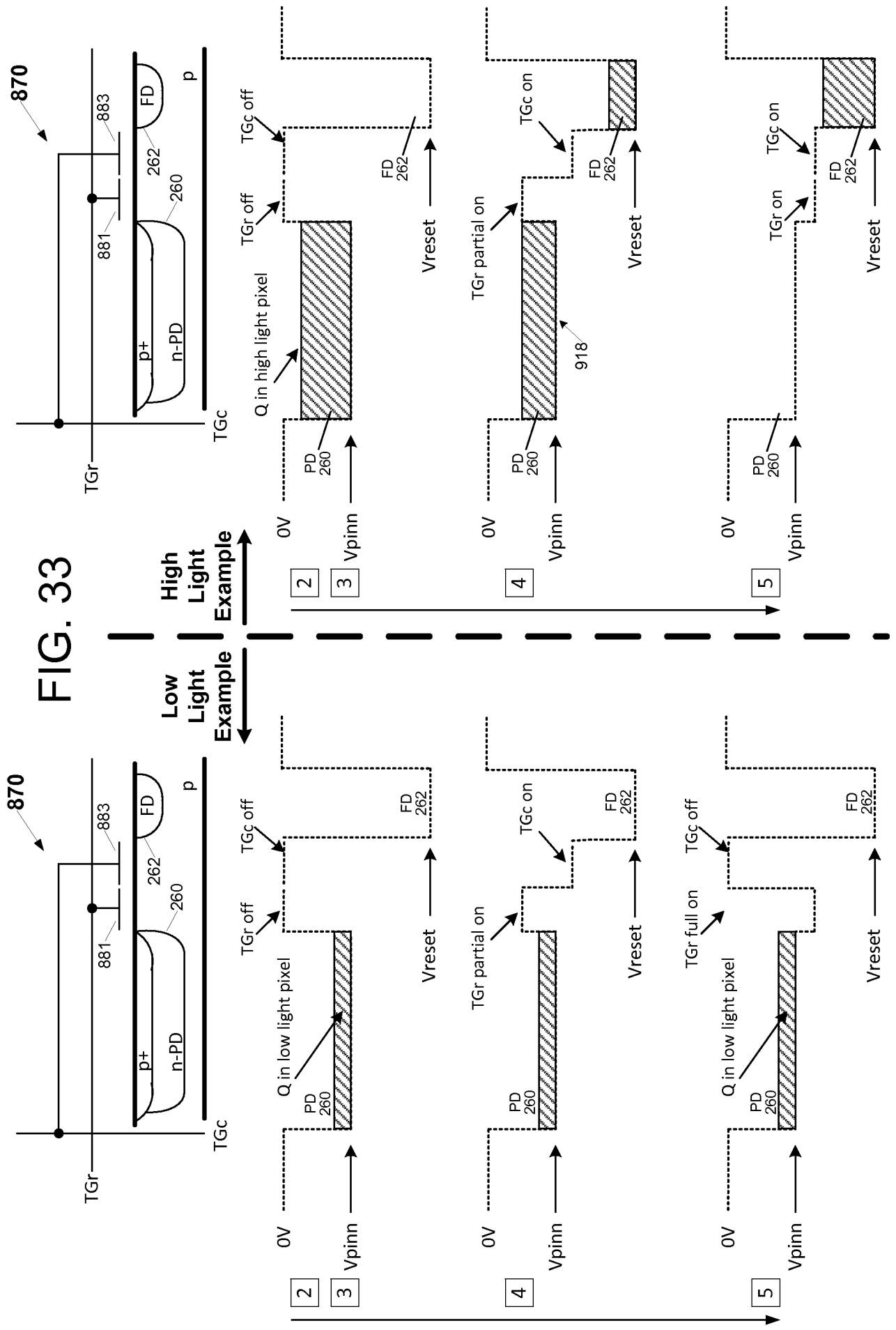


FIG. 32



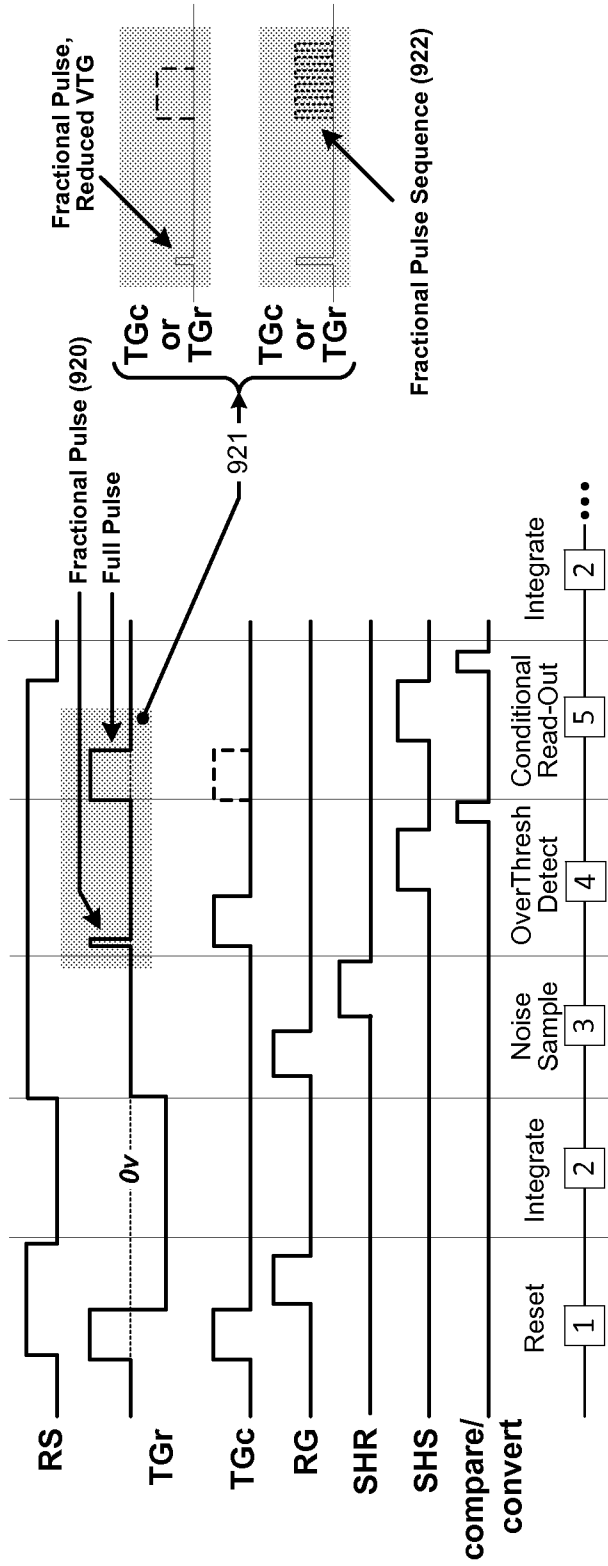


FIG. 34

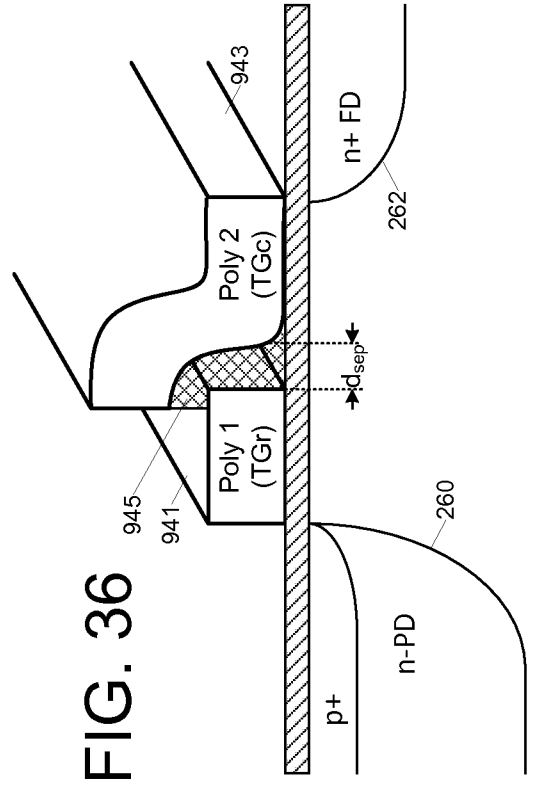


FIG. 36

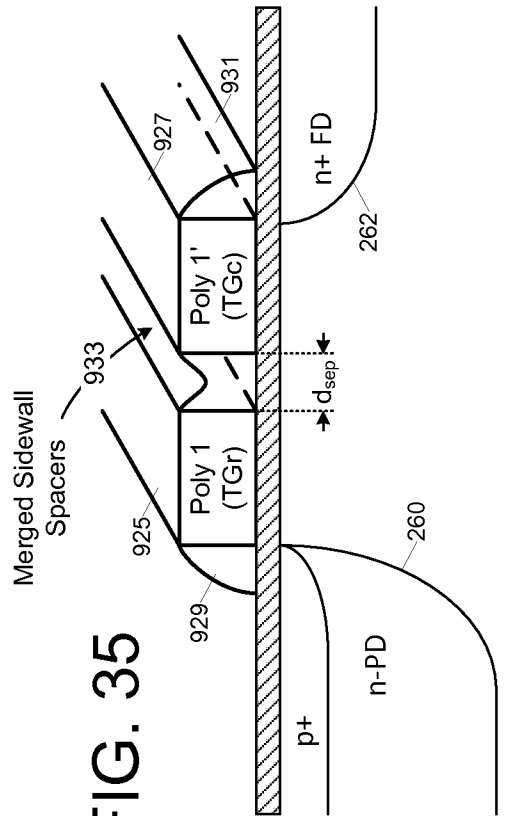


FIG. 35

FIG. 41

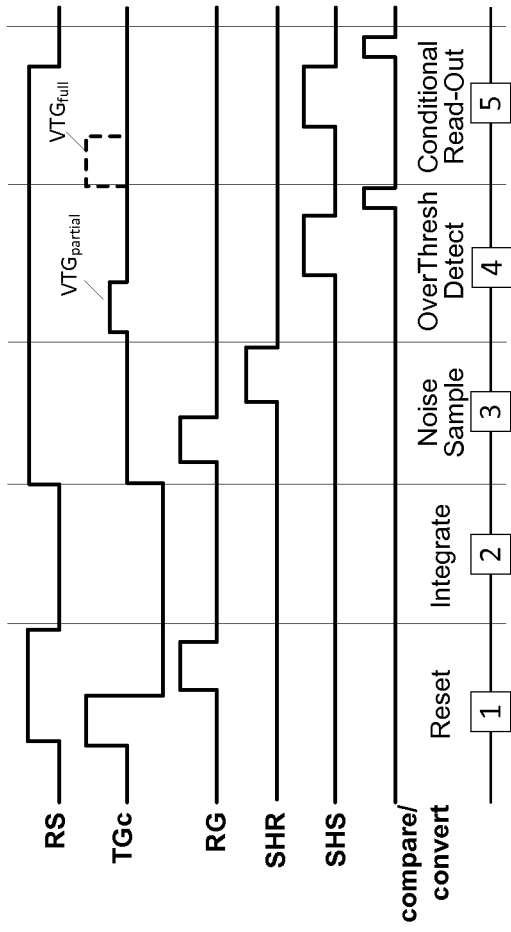


FIG. 40

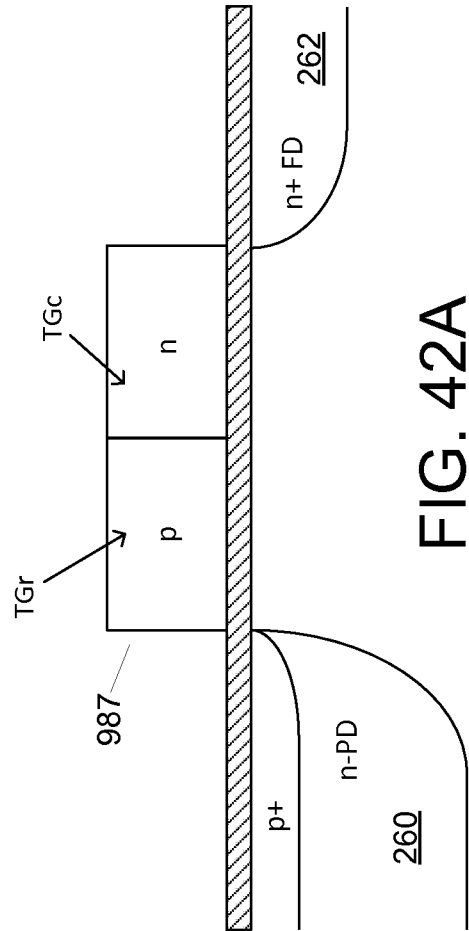
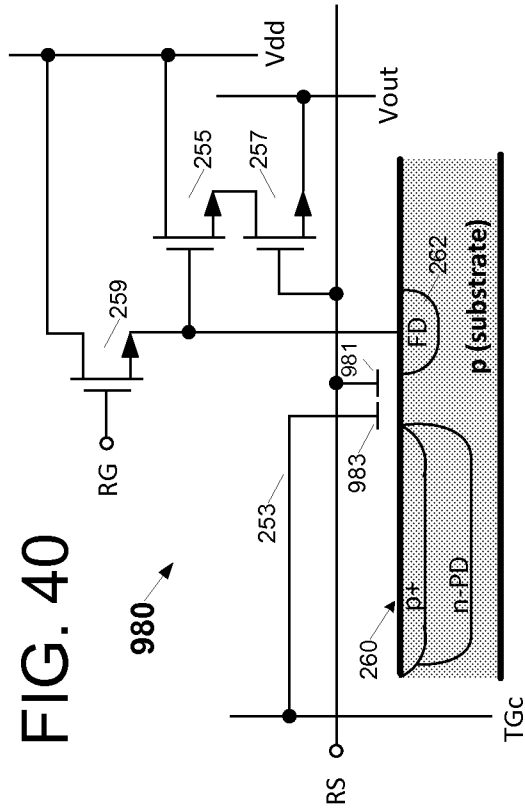


FIG. 42A

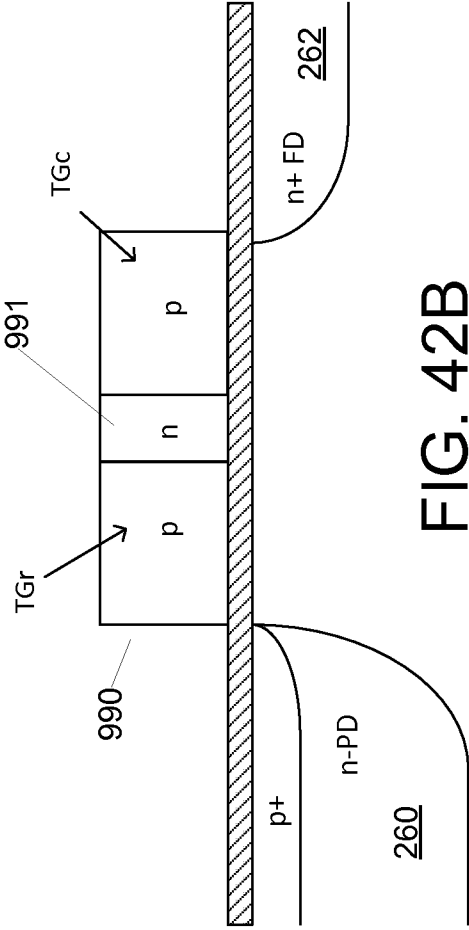


FIG. 42B

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2014/041596

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L27/146
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED
Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2006/138581 A1 (LADD JOHN [US]) 29 June 2006 (2006-06-29) paragraphs [0035] - [0037], [0047] figures 3, 10 -----	1,8,9
X	US 2009/179232 A1 (ADKISSON JAMES W [US] ET AL) 16 July 2009 (2009-07-16) paragraphs [0060], [0061] figures 3, 4 -----	1,8,9
X	US 2008/111170 A1 (KIM MI JIN [KR] ET AL) 15 May 2008 (2008-05-15) paragraphs [0093] - [0097] figure 8 -----	1,8,9
X	US 2006/138489 A1 (AHN JUNG-CHAK [KR] ET AL) 29 June 2006 (2006-06-29) paragraphs [0055] - [0066] figure 2a -----	1,8,9

Further documents are listed in the continuation of Box C.

See patent family annex.

* Special categories of cited documents :

- "A" document defining the general state of the art which is not considered to be of particular relevance
- "E" earlier application or patent but published on or after the international filing date
- "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
- "O" document referring to an oral disclosure, use, exhibition or other means
- "P" document published prior to the international filing date but later than the priority date claimed

- "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
- "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
- "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
- "&" document member of the same patent family

Date of the actual completion of the international search 7 August 2014	Date of mailing of the international search report 05/11/2014
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Name and mailing address of the ISA/ European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Authorized officer Markmann, Markus
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INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2014/041596

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.

3. As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

1, 8, 9

Remark on Protest

- The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
- The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
- No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No PCT/US2014/041596

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2006138581 A1	29-06-2006	US 2006138581 A1	29-06-2006
		US 2007102781 A1	10-05-2007
		US 2009322913 A1	31-12-2009

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		JP 2008125084 A	29-05-2008
		US 2008111170 A1	15-05-2008
		US 2012187279 A1	26-07-2012

US 2006138489 A1	29-06-2006	JP 2006186355 A	13-07-2006
		US 2006138489 A1	29-06-2006

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1, 8, 9

Split-gate transfer gate

2. claims: 2-7, 13-18

Shared floating diffusion

3. claims: 10-12, 19-22

Control circuitry for applying control signals
