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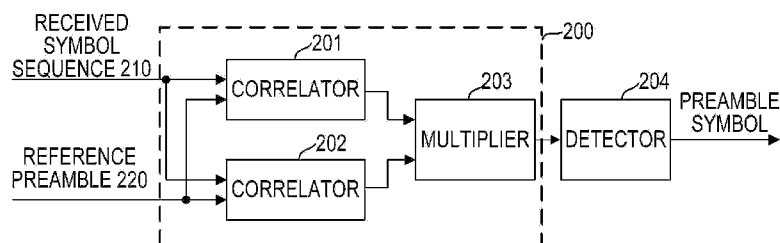


FIG.2

(57) Abstract: A method and apparatus for time synchronization and an OFDMA receiver thereof are provided. The preamble timing is obtained by a two-stage correlation in time domain between the sequence of a received symbol and a reference preamble. The two-stage correlation is further simplified to perform a conjugate multiplication between a one-stage correlation and its correspondingly delayed result. The preamble boundary is adaptively determined by the peak value from the result of the two-stage correlation. In this way, the time synchronization is achieved with a robust performance in a low SNR, high frequency offset or large delay spread fading channel.



METHOD AND APPARATUS FOR ACCURATE TIME SYNCHRONIZATION IN WIRELESS COMMUNICATION SYSTEM

FIELD OF THE INVENTION

[0001] The present invention relates to Orthogonal Frequency Division Multiple Access (OFDMA) wireless communication, and more specifically, to a time synchronization method for Worldwide Interoperability for Microwave Access (WiMAX) system.

BACKGROUND

[0002] Orthogonal frequency division multiplexing (OFDM) as a promising technology is widely used in wireless communication system, which converts a frequency selective channel to a collection of frequency-flat subchannels achieved by splitting the input high-rate data stream into a number of low-rate substreams. In order to enhance the efficiency of the frequency allocation, the technique of Orthogonal Frequency Division Multiple Access (OFDMA) is proposed to allow multiple users to access a same channel, by dividing available subcarriers into mutually exclusive clusters assigned to distinct users for simultaneous transmission. The orthogonality of the subcarriers guarantees intrinsic protection against multiple access interference, while the adoption of a dynamic subcarrier assignment strategy provides the system with high flexibility in resource management. OFDMA has become a part of IEEE 802.16 standards for wireless metropolitan area networks as a promising candidate for next generation broadband wireless networks.

[0003] With more fine frequency allocation, OFDMA signal demodulation is extremely sensitive to timing errors and carrier frequency offsets. Inaccurate compensation of the frequency offset destroys the orthogonality among subcarriers and produces inter-carrier interference (ICI). Timing errors result in inter-symbol interference (ISI) and produce severe error rate degradations.

[0004] OFDMA uses a cyclic extension between adjacent symbols to provide intrinsic protection against the time dispersion and timing offset. In the WiMAX standard, IEEE 802.16e, the cyclic prefix (CP) is adopted. As soon as the symbol timing is detected within the cyclic extension, the received spectrum will keep the constant magnitude and only lead to

a phase rotation. But if the symbol timing is detected out of the cyclic extension, both magnitude and phase of current symbol are interfered by the adjacent symbols, which leads to unrecoverable errors in received frequency spectrum.

[0005] In an OFDMA downlink process, the OFDMA symbols are generated after an Inverse Fast Fourier Transform (IFFT) and converted from the tones in frequency domain to the signal in time domain in a base station (BS), while in a mobile station (BS) or subscriber station (SS) the symbols should be detected and converted to the tones in the frequency domain after a FFT unit. The preamble is the first symbol modulated with the predetermined pseudo random sequence and highest power in a time division duplex (TDD) frame. Hence, it is a good signal for detecting the start position of an OFDMA frame and the frequency offset over the channel.

[0006] Existing techniques based on preamble detection as time synchronization have some drawbacks.

[0007] A popular scheme of preamble detection adopts delay-correlation mechanism, which utilizes the repetitive property of the signal in time domain. The typical algorithm is CP auto-correlation or M-correlation based on the modulo-3 periodic property in WiMAX preamble, where M is a number equal to one third of the FFT length. But these correlation results may have a plateau, which affects the position of symbol boundary and also leads to the inaccurate estimation of the fractional frequency offset at that location. In another words, it could lead to ICI error. Moreover, the M-correlation works badly in multi-cell deployment of WiMAX system because of the repetition degradation in the preamble. Therefore, the delay-correlation only offers coarse time synchronization under the low signal to noise ratio (SNR) or the time-variant fading channels.

[0008] Another technique based on preamble cross-correlation in time domain can offer fine time synchronization, while it is quite sensitive to the carrier frequency offset and should better be processed after the frequency offset compensation. Moreover, this method will produce multi-peaks in WiMAX preamble because of modulo-3 property, which makes the peak detection difficult.

[0009] Besides above techniques, the conjugate symmetric property of a BPSK modulated preamble can also be used to perform symbol timing. This method produces several sharp peaks with the biggest peak located at the preamble boundary, but its

implementation requires a lot of complex multipliers and delay taps which adds heavy burden to the system.

SUMMARY

[0010] The invention disclosed herein includes a method, an apparatus for accurate time synchronization and a receiver thereof. The method, apparatus and receiver are applicable in WiMAX communication system or Long Term Evolution (LTE) program. Based on the characteristics of time-domain correlation and the periodic property of symbol sequence, the robust and accurate preamble synchronization is obtained by performing a simplified two-stage correlation based on a symbol sequence and a reference preamble. The preamble boundary is determined based on an obvious target peak which is detected by an adaptive peak detector. Advantageously, the present disclosure allows for an easy detection of the start position of an OFDMA frame and at the same time reduces the system complexity and offers a robust performance in the low SNR, high frequency offset or large delay spread fading channel.

[0011] In one embodiment of the present invention, a method for time synchronization is provided. The method may include receiving a sequence of symbols; performing a two-stage correlation in time domain based on the sequence of symbols and a reference preamble; and detecting a preamble symbol from the result of the two-stage correlation.

[0012] In another embodiment of the present invention, an apparatus for time synchronization is provided. The apparatus may include a two-stage correlator configured to perform a two-stage correlation in time domain based on a received sequence of symbols and a reference preamble; and a detector coupled to the two-stage correlator, wherein the detector is configured to detect a preamble symbol from the result of the two-stage correlation.

[0013] In yet another embodiment of the present invention, an OFDMA receiver is provided. The receiver may include an apparatus for time synchronization and an apparatus for frequency synchronization coupled to the apparatus for time synchronization, configured to estimate and compensate the carrier frequency offset of the received sequence of symbols. The apparatus for time synchronization may include a two-stage correlator configured to perform a two-stage correlation in time domain based on a received sequence of symbols and

a reference preamble; and a detector coupled to the two-stage correlator, wherein the detector is configured to detect a preamble symbol from the result of the two-stage correlation.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] In the drawings, each identical or nearly identical component that is illustrated in various figures is represented by a like numeral. For purposes of clarity, not every component may be labeled in every drawing. In the drawings:

[0015] Fig. 1 is a block diagram of an OFDMA receiver;

[0016] Fig. 2 is a diagram of an apparatus for time synchronization according to one embodiment of the present invention;

[0017] Fig. 3 is a diagram of a two-stage correlator according to one embodiment of the present invention;

[0018] Fig. 4 is a diagram of a simplified real multiplier according to one embodiment of the present invention;

[0019] Fig. 5 is a diagram of a peak detector according to one embodiment of the present invention;

[0020] Fig. 6 is a flowchart of a method for time synchronization and peak detection according to one embodiment of the present invention;

[0021] Fig. 7A is a plot of a simulated result in a normal channel for the output of the first correlator 201 shown in Fig. 2;

[0022] Fig. 7B is a plot of a simulated result in a normal channel for the output of the second correlator 202 shown in Fig. 2;

[0023] Fig. 7C is a plot of a simulated final result in a normal channel for output of the two-stage correlator shown in Fig. 2;

[0024] Fig. 8A is a plot of a simulated result in a poor delay spread channel for the output of the first correlator 201 shown in Fig. 2;

[0025] Fig. 8B is a plot of a simulated result in a poor delay spread channel for the output of the second correlator 202 shown in Fig. 2;

[0026] Fig. 8C is a plot of a simulated final result in a poor delay spread channel for the output of the two-stage correlator shown in Fig. 2;

[0027] Fig. 9 is a plot of the time synchronization failure rate in different channels; and

[0028] Fig. 10 is a plot of the time synchronization failure rate according to different frequency offset.

DETAILED DESCRIPTION

[0029] The purposes, technical solutions and advantages concerning the embodiments of the present invention will become more readily appreciated by reference to the following description of the embodiments, when taken in conjunction with the accompanying drawings.

[0030] Fig. 1 illustrates a block diagram of an OFDMA receiver. As shown in Fig. 1, the OFDMA receiver typically includes a time synchronization module 10, a frequency synchronization module 12, a symbol windowing module 14, a Fast Fourier Transform (FFT) processor 16, a Pilot extractor 18, a channel estimator and equalizer 20, a demapper 22, a demodulator 24, and a channel decoder 26.

[0031] The time synchronization module is configured to estimate the timing offset and determines an OFDMA frame boundary. The frequency synchronization module 12 is configured to estimate and compensate the carrier frequency offset of the received signal. In particular, in the frequency synchronization module 12, a fractional carrier frequency offset may be estimated in time domain and the integer carrier frequency offset may be estimated in frequency domain. The symbol windowing module 14 is configured to determine the FFT window timing by removing the cyclic prefix of an OFDMA symbol. The FFT processor 16 is configured to convert a time-domain signal to a frequency-domain signal. The channel estimator 20 is configured to estimate the amplitude and phase shift caused by the wireless channel from the available pilot information, which is obtained by a pilot extractor 18. The channel equalizer 20 removes the effect of the wireless channel and allows subsequent symbols to be demapped and demodulated. The demapper 22 allows a subcarrier permutation and converts the subcarrier order from physical subcarrier to logical subcarrier. The demodulator 24 is configured to recover the OFDMA tone to the information bits based on the phase shifting keying (PSK) or quadrature amplitude modulation (QAM) scheme used in IEEE802.16e. At last, the information bit stream is decoded by a channel decoder 26 which often includes the mirror operations of randomization, forward error correction coding and interleaving.

[0032] Generally, time synchronization is the first step in the entire OFDMA synchronization process and the preamble is the first symbol in OFDMA frame with highest power and used to perform time synchronization.

[0033] Fig. 2 illustrates a diagram of a time synchronization apparatus for accurate time estimation according to one embodiment of the invention. As illustrated in Fig. 2, the time synchronization apparatus may include a two-stage correlator 200 and a detector 204 (also referred to as a peak detector) coupled to the two-stage correlator 200. The two-stage correlator 200 may include a first correlator 201, a second correlator 202 and a multiplier 203.

[0034] The correlators 201 and 202 are two one-stage correlators for realizing cross correlation between a received sequence of symbols 210 (e.g., OFDMA symbol sequence) and a reference preamble 220, which may be represented in equation (1) and (2).

$$R_1(m) = \sum_{k=0}^{L-1} x(m+k) \cdot c^*(k) \quad (1)$$

$$R_2(m) = \sum_{k=0}^{L-1} x(m+N-M+k) \cdot c^*(N-M+k) \quad (2)$$

[0035] In equation (1) and (2), x is a complex sequence 210 of the received OFDMA symbols generated by an analog to digital converters (ADC) in a receiver, c is a sequence 220 for reference preamble symbol, (.)^{*} denotes a complex conjugate operator, m is the sampling index, L is the correlation length, N is FFT size and M is predetermined time period equal to one third of N in mobile WiMAX. R₁ refers to the first one-stage correlator 201 and R₂ refers to the second one-stage correlator 202. Their correlation results are recorded as $\overline{R}_1$ and $\overline{R}_2$, which are the absolute value of R₁ and R₂.

[0036] In the WiMAX specification, there are 114 pseudo-noise (PN) sequences used for different base station and sectors, which are often stored in a memory of a mobile station. Before synchronizing with a base station, the mobile station may read a reference preamble from the memory based on a known preamble index which is obtained by a conventional cell search process in cellular system.

[0037] The preamble defined in IEEE802.16e has three types of carrier-sets with different allocation of subcarriers, which may be modulated using a boosted BPSK with a specific pseudo-noise code. Because the tones of preamble align every three subcarriers, it shows a

property of three pseudo periodic signals in time domain with the length of M , where M is equal to floor ($N/3$).

[0038] Accordingly, the correlation result $\bar{R}_1$ in equation (1) will possibly produce three obvious sharp peaks, which locates at 0, 1/3 and 2/3 symbol length of the preamble.

[0039] To suppress the useless peaks, the two-stage correlator 200 may further include a multiplier 203. The multiplier 203 multiplies R_1 with the result of conjugate operation of R_2 to emphasize the target peak. The final result of the multiplier 203 is denoted in equation (3).

$$R(m) = R_1(m) \cdot R_2^*(m) \quad (3)$$

[0040] Advantageously, instead of three obvious sharp peaks generated according to conventional arts, only one obvious sharp peak is produced in the above-described embodiment, thereby facilitating the peak detection process. This obvious sharp peak may then be used to determine the accurate symbol timing, where the peak value is the maximum value of $\bar{R}$ denoted as $\bar{R}_{\max}$.

[0041] Moreover, the conjugate multiplier between two repetitive parts of preamble used in equation (3) can increase the resistance on a common phase rotation in time domain, which usually results from the carrier frequency offset.

[0042] Since the reference preamble exhibits the property of M periodicity, the $R_2(m)$ in equation (2) is equivalent to $R_1(m)$ time shifted by $N-M$ taps, which is shown in equation (4).

$$R_2(m) \approx \sum_{k=0}^{L-1} x(m+N-M+k) \cdot c^*(k) = R_1(m-N+M) \quad (4)$$

[0043] Consequently, $R(m)$ in the equation (3) can be rewritten as shown in equation (5), and the $\bar{R}(m)$ is given in the equation (6).

$$R(m) = R_1(m) \cdot R_1^*(m-N+M) \quad (5)$$

$$\bar{R}(m) = |R_1(m) \cdot R_1^*(m-N+M)| = |R_1^*(m) \cdot R_1(m-N+M)| \quad (6)$$

[0044] In equation (5), as can be seen, two correlation operations are simplified to one correlation operation, one delay operation and one conjugate multiplication, where the hardware complexity is nearly reduced by half.

[0045] The corresponding reference power in equation (6) can be represented in the equation (7), and it is calculated once the cell is specified.

$$P = \sum_{k=0}^{L-1} |c(k)|^2 \cdot \sum_{k=0}^{L-1} |c(N-M+k)|^2 \quad (7)$$

[0046] Fig. 3 illustrates a diagram of a simplified two-stage correlator according to one embodiment of the present invention. The first correlator 201 includes one complex conjugate operator 300, L complex multipliers 301 and an accumulator 302. The second correlator 202 is implemented with a delayer 303 having (N-M) taps which delays the output of the first correlator 201 by N-M. In one embodiment, the delayer 303 is implemented with a First In First Out memory (FIFO). Advantageously, with this simplified structure, the number of complex multipliers may be reduced from 2*L+1 to L+1.

[0047] In the correlator 201, most of the operations are multiplications, where the number of complex multipliers is L. It is understood that one complex multiplier is comprised of four real multipliers and two adders. Minimizing the data width of multipliers can reduce the operations of multipliers greatly. In the present invention, only the most two significant bits of the received sequence take part in the correlation operations, whose correlation performance degrades slightly if the L is not too small. The first bit is a sign bit, and the second bit is used to distinguish between 0 and 1. By this method, the reference power in equation (7) is equal to $4L^2$. Furthermore, an equivalent combinational logic may be used to replace the function of the real multiplier, which is shown in Fig. 4. Advantageously, this simplified real multiplier 400 is easy to be implemented in the Programmable Logic Devices (PLD) or Application Specific Integrated Circuits (ASIC).

[0048] Fig. 5 is a diagram of an adaptive detector 204 according to one embodiment of the present invention. The detector 204 includes a first comparators 503 and a second comparator 504, and a dynamic threshold generator 500. The first comparator 503 compares the present maximum correlation value $\bar{R}_{\max}$ with a preset threshold TH1 505. It is noted that TH1 505 is a fixed value chosen to meet with the normal requirement under different SNR or channel quality, based on the reference power P. In one embodiment, the ratio of TH1 versus the reference power may be chosen at 0.5. In a normal situation, if the present maximum correlation value $\bar{R}_{\max}$ is greater than a preset threshold TH1 505, the position of the peak value can be located immediately. The second comparator 504 is not enabled in this case. However, if the channel condition is severely poor, the correlation degree may be degraded resulting from the uncertain interferences and the peak cannot be detected by the threshold TH1. In this case, the dynamic threshold generator 500 is in

charge of the detection of weak peak. The dynamic threshold generator 500 includes a peak preserver 501 and a coefficient controller 502. The peak preserver 501 is configured to preserve the present peak value detected by the comparator 503. The coefficient controller 502 is used to generate a new threshold named TH2 506 by multiplying the previous peak value with a certain coefficient, normally using 0.5. The first comparator 503 has the priority to determine the running of the second comparator 504. The second comparator 504 is triggered only when the correlation degree becomes very low. The second comparator 504 then compares the present maximum correlation value $\bar{R}_{\max}$ with TH2. In this way, the peak can be effectively detected regardless the signal channel is in a good condition or in a poor condition.

[0049] Fig. 6 is a flowchart of a method for time synchronization and peak detection according to one embodiment of the invention. Upon Start, the complex sequence of OFDMA symbols which are converted by the ADCs is obtained at step 601. Next, at step 602, a previous peak value which denotes maximum correlation value in a previous frame is loaded, and the dynamic threshold TH2 506 used in present frame is then generated. Note that at the startup the previous peak value may not exist and the TH2 should be initialized with a preset threshold. At step 603, a two-stage correlation for the present frame is computed, and the correlation result $\bar{R}$ is then sent into the comparators. At step 604, the maximum value of $\bar{R}$ is compared with TH1. If the maximum value ($\bar{R}_{\max}$) is greater than the preset threshold TH1, the process proceeds to step 606 where the position of this peak is output directly and the peak value is stored in memory which is used for the detection of next frame. Otherwise, the process proceeds to step 605 where $\bar{R}_{\max}$ is compared with TH2. The synchronization process is terminated when $\bar{R}_{\max}$ is detected and its position has output.

[0050] In one embodiment, the two-stage correlation at step 603 includes correlating the received sequence of symbols with the reference preamble and thereby obtaining the result of one-stage correlation; delaying the result of one-stage correlation; performing a conjugate operation on the result of the one-stage correlation; and multiplying the delayed result and the conjugate result and thus obtaining the result of the two-stage correlation.

[0051] Fig. 7A, Fig. 7B and Fig. 7C are plots of simulated results in a normal channel for the output of the first correlator 201, the second correlator 202 and the two-stage correlator 200 respectively according to one embodiment of the invention. In one embodiment, the

simulation is performed in additive white Gaussian noise (AWGN) channel where SNR is 6dB and the frequency offset is zero. As can be seen, the result of one-stage correlation as shown in Fig. 7A and Fig. 7B has several peaks, while the two-stage correlation shown in Fig. 7C generates only one obvious sharp peak and the peak detector uses the threshold TH1 to handle the comparison.

[0052] According to the foregoing embodiments of the present invention, the full width at half maximum (FWHM) of the peak is narrowed within a sampling spacing. Therefore, the methods of threshold comparison or maximum value search can achieve the same accuracy within one sampling point.

[0053] Fig. 8A, Fig. 8B and Fig. 8C are plots of simulated results in a poor delay spread fading channel for the first correlator 201, the second correlator 202 and the two-stage correlator 200 respectively according to one embodiment of the invention. In one embodiment, the simulation is performed in the International Telecommunication Union (ITU) Vehicular-A channel where SNR is -6dB and the mobile speed is 120 kilometers per hour. In this case, the result of one-stage correlation shown in Fig. 8A, Fig. 8B has several peak groups 801, where peak group 801 includes the peaks of multi-paths. The main peak 802 is not so outstanding comparing with the noise and other path peak. But in Fig. 8C the main peak 802 is distinct and the peaks of other paths are suppressed, where the peak detector uses the threshold TH2 to handle the comparison.

[0054] Fig. 9 is a plot of time synchronization failure rate according to different SNR and channels. The curves in Fig. 9 are simulated in additive white Gaussian noise (AWGN) channel, ITU Pedestrian B channel with speed of 3kmph and ITU Vehicular-A channel with speed of 120kmph individually. It is seen that present invention offers the robust time detection under low SNR and high mobility conditions in time-variant fading channels.

[0055] Fig. 10 is a plot of time synchronization failure rate according to the different frequency offsets. The curves in Fig. 10 are simulated in ITU Vehicular-A channel with speed of 120kmph when an initial frequency offset is 0, 0.2, 0.5 and 1.0 subcarrier frequency spacing. The result has shown the good performance in present invention even if the frequency offset is not compensated completely, i.e. the two-stage correlation is insensitive to the phase rotation in time domain.

[0056] All or part of the embodiments in present invention may be implemented or performed with a general purpose processor, a digital signal processor (DSP), an application

specific integrated circuit (ASIC), a field programmable gate array (FPGA) or other programmable logic device (PLD), discrete gate or transistor logic, discrete hardware components or any combination thereof designed to perform the functions described herein.

[0057] Although the invention has been described in language specific to structural features and/or methodological acts, it is to be understood that the invention defined in the appended claims is not necessarily limited to the specific features or acts described. Rather, the specific features and acts are disclosed as exemplary forms of implementing the claimed invention.

CLAIMS

What is claimed is:

1. A method for time synchronization, comprising:
receiving a sequence of symbols;
performing a two-stage correlation in time domain based on the sequence of symbols and a reference preamble; and
detecting a preamble symbol from the result of the two-stage correlation.
2. The method of claim 1, wherein performing a two-stage correlation further comprises:
performing a one-stage correlation in time domain based on the sequence of symbols and the reference preamble and obtaining a result of the one-stage correlation;
delaying the result of the one-stage correlation by a predetermined time period;
performing a conjugate operation on the result of the one-stage correlation; and
multiplying the delayed result and the conjugate result and obtaining the result of the two-stage correlation.
3. The method of claim 2, wherein the predetermined time period is associated with the period of the reference preamble.
4. The method of claim 2, further comprising:
performing a complex multiplication with four real multipliers based on the most two significant bits of the received sequence of symbols and a conjugate reference preamble in time domain.
5. The method of claim 1, wherein detecting the preamble symbol comprises:
comparing a peak value of the result of the two-stage correlator with a preset threshold; and
directly locating the preamble symbol if the peak value is greater than the preset threshold;

comparing the peak value of the result of the two-stage correlator with a dynamic threshold if the peak value is equal to or less than the preset threshold;

locating the preamble symbol if the peak value is greater than the dynamic threshold.

6. The method of claim 5, wherein the dynamic threshold is determined based on a previous peak value by multiplying the previous peak value with a coefficient.

7. The method of claim 1, wherein the sequence of symbols are repeated periodically.

8. The method of claim 1, wherein the sequence of symbols is received from an Orthogonal Frequency Division Multiple Access wireless communication system based on IEEE 802.16e specification.

9. An apparatus for time synchronization, comprising:

a two-stage correlator configured to perform a two-stage correlation in time domain based on a received sequence of symbols and a reference preamble; and

a detector coupled to the two-stage correlator, the detector configured to detect a preamble symbol from the result of the two-stage correlation.

10. The apparatus of claim 9, wherein the two-stage correlator is configured to perform a one-stage correlation in time domain based on the sequence of symbols and the reference preamble and obtain a result of the one-stage correlation, delay the result of the one-stage correlation by a predetermined time period, perform a conjugate operation on the result of the one-stage correlation; and multiply the delayed result and the conjugate result and obtain the result of the two-stage correlation.

11. The apparatus of claim 9, wherein the two-stage correlator comprises:

a one-stage correlator configured to perform a one-stage correlation in time domain based on the sequence of symbols and the reference preamble and obtain a result of the one-stage correlation;

a delayer configured to delay the result of the one-stage correlation by a predetermined time period;

a complex conjugate operator configured to perform a conjugate operation on the result of the one-stage correlation; and

a multiplier configured to multiply the delayed result and the conjugate result and obtain the result of the two-stage correlation.

12. The apparatus of claim 11, wherein the predetermined time period is associated with the period of the reference preamble.

13. The apparatus of claim 11, wherein the one-stage correlator comprises:

a complex conjugate operator configured to perform a conjugate operation on the reference preamble;

a simplified complex multiplier configured to multiply the most two significant bits of the received sequence of symbols and a conjugate reference preamble in time domain; and

a complex accumulator configured to perform additions of complex multiplication results.

14. The apparatus of claim 9, wherein the detector comprises:

a first comparator configured to compare a peak value of the result of the two-stage correlator with a preset threshold;

a second comparator coupled to the first comparator, the second comparator configured to compare the peak value of the result of the two-stage correlator with a dynamic threshold if the peak value is equal to or less than the preset threshold; and

a dynamic threshold generator coupled to the second comparator, the dynamic threshold generator configured to generate the dynamic threshold based on a previous peak value.

15. The apparatus of claim 14, wherein the dynamic threshold generator comprises:

a peak preserver configured to save the previous peak value; and

a coefficient controller coupled to the peak preserver, the coefficient controller configured to determine a magnitude of the dynamic threshold by multiplying the previous peak value with a coefficient.

16. The apparatus of claim 9, wherein the sequence of symbols are repeated periodically.

17. The apparatus of claim 9, wherein the sequence of symbols is received from an Orthogonal Frequency Division Multiple Access wireless communication system based on IEEE 802.16e specification.

18. A receiver, comprising:
an apparatus for time synchronization comprising:
a two-stage correlator configured to perform a two-stage correlation in time domain based on a received sequence of symbols and a reference preamble; and
a detector coupled to the two-stage correlator, the detector configured to detect a preamble symbol from the result of the two-stage correlation; and
an apparatus for frequency synchronization coupled to the apparatus for time synchronization, configured to estimate and compensate the carrier frequency offset of the received sequence of symbols.

19. The receiver of claim 18, wherein the two-stage correlator is configured to perform a one-stage correlation in time domain based on the sequence of symbols and the reference preamble and obtain a result of the one-stage correlation, delay the result of the one-stage correlation by a predetermined time period, perform a conjugate operation on the result of the one-stage correlation; and multiply the delayed result and the conjugate result and obtain the result of the two-stage correlation.

20. The receiver of claim 18, wherein the two-stage correlator comprises:
a one-stage correlator configured to perform a one-stage correlation in time domain based on the sequence of symbols and the reference preamble and obtain a result of the one-stage correlation;

a delayer configured to delay the result of the one-stage correlation by a predetermined time period;

a complex conjugate operator configured to perform a conjugate operation on the result of the one-stage correlation; and

a multiplier configured to multiply the delayed result and the conjugate result and obtain the result of the two-stage correlation.

21. The receiver of claim 20, wherein the predetermined time period is associated with the period of the reference preamble.

22. The receiver of claim 20, wherein the one-stage correlator comprises:

a complex conjugate operator configured to perform a conjugate operation on the reference preamble;

a simplified complex multiplier configured to multiply the most two significant bits of the received sequence of symbols and a conjugate reference preamble in time domain; and

a complex accumulator configured to perform additions of complex multiplication results.

23. The receiver of claim 18, wherein the detector comprises:

a first comparator configured to compare a peak value of the result of the two-stage correlator with a preset threshold;

a second comparator coupled to the first comparator, the second comparator configured to compare the peak value of the result of the two-stage correlator with a dynamic threshold if the peak value is equal to or less than the preset threshold; and

a dynamic threshold generator coupled to the second comparator, the dynamic threshold generator configured to generate the dynamic threshold based on a previous peak value.

24. The receiver of claim 23, wherein the dynamic threshold generator comprises:

a peak preserver configured to save the previous peak value; and

a coefficient controller coupled to the peak preserver, the coefficient controller configured to determine the magnitude of the dynamic threshold by multiplying the previous peak value with a coefficient.

25. The receiver of claim 18, wherein the sequence of symbols are repeated periodically.

26. The receiver of claim 18, wherein the sequence of symbols is received from an Orthogonal Frequency Division Multiple Access wireless communication system based on IEEE 802.16e specification.

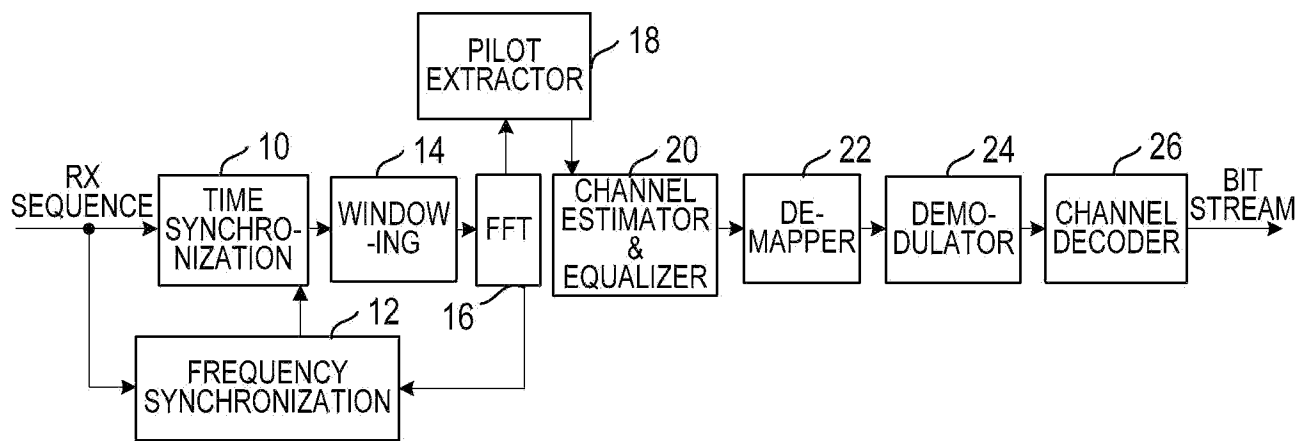


FIG. 1

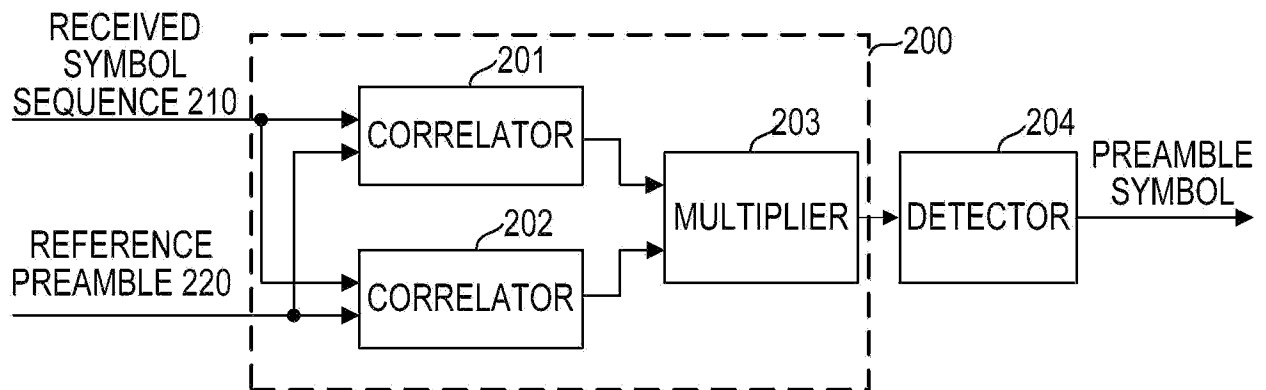


FIG. 2

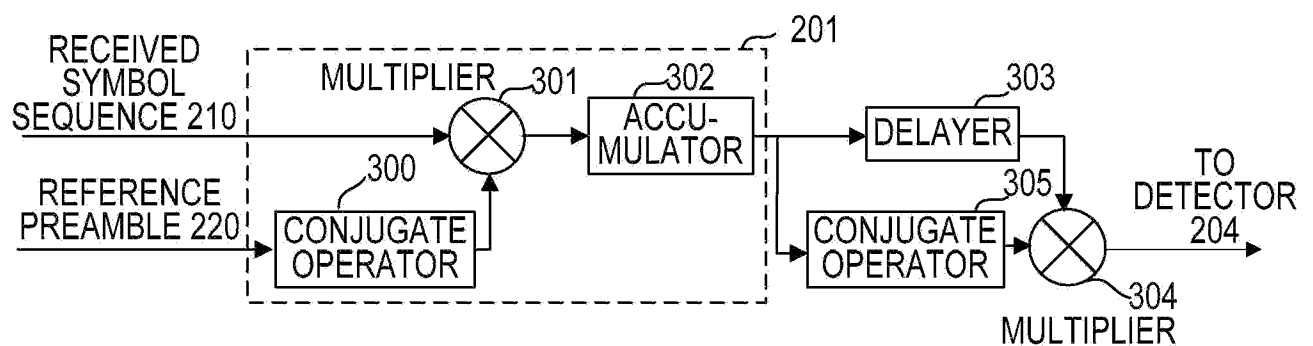


FIG. 3

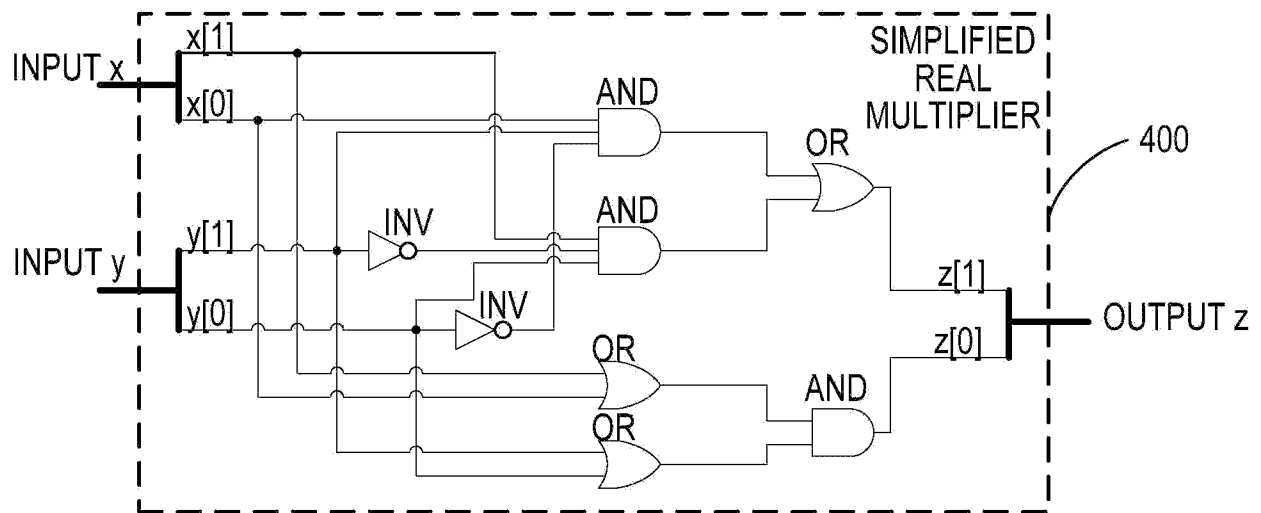


FIG. 4

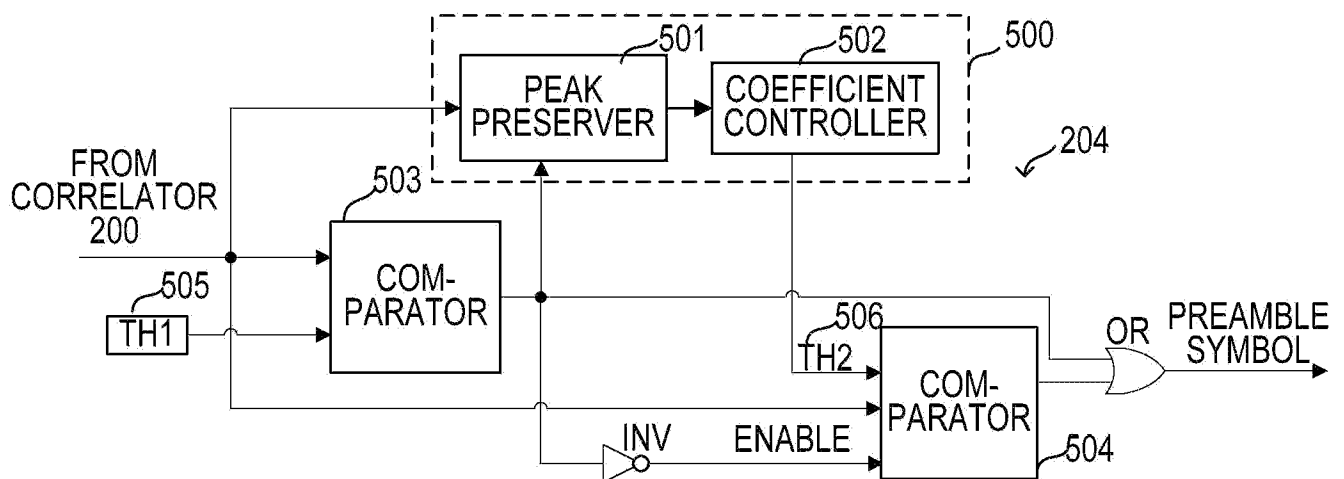


FIG. 5

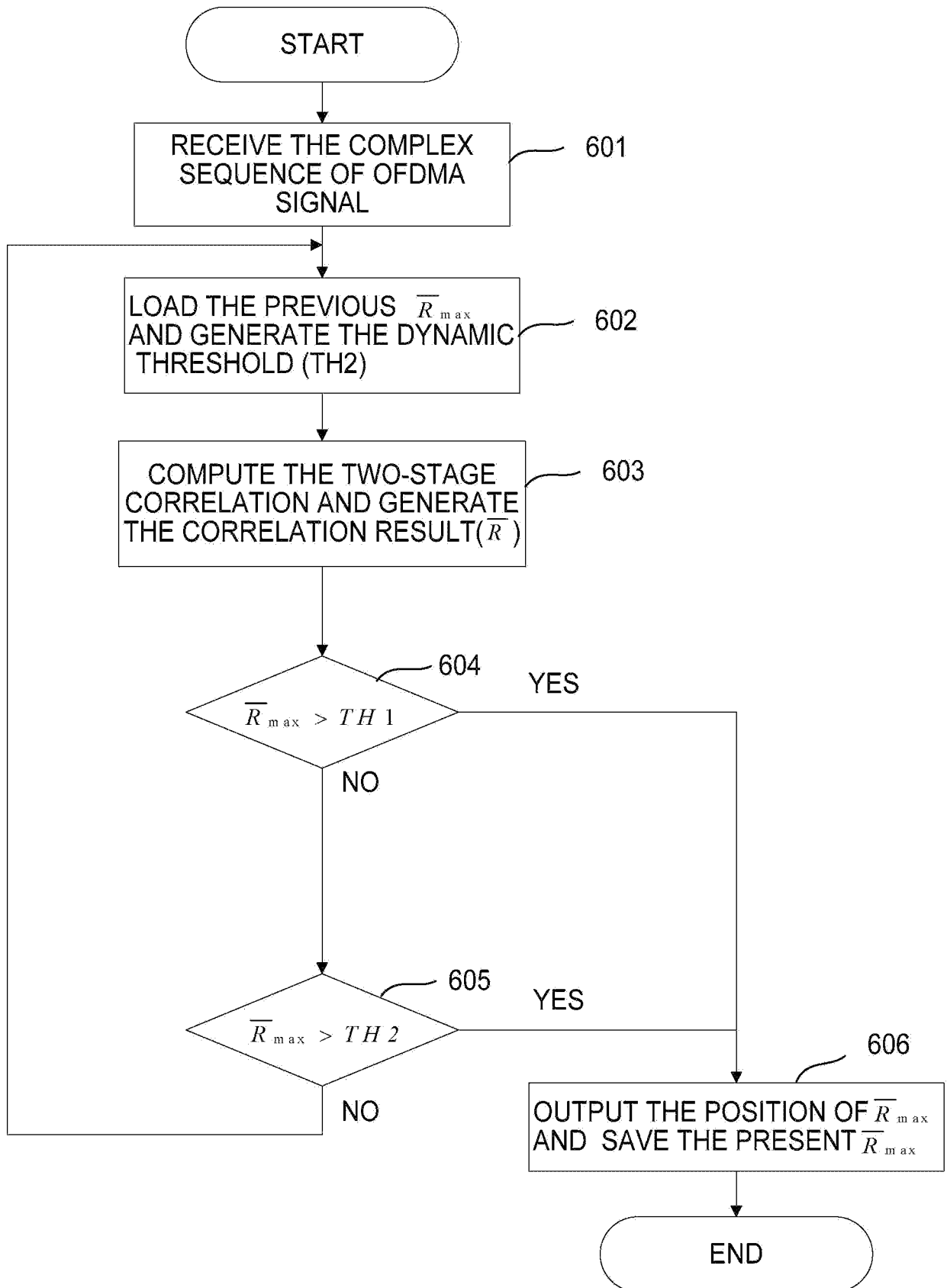


FIG.6

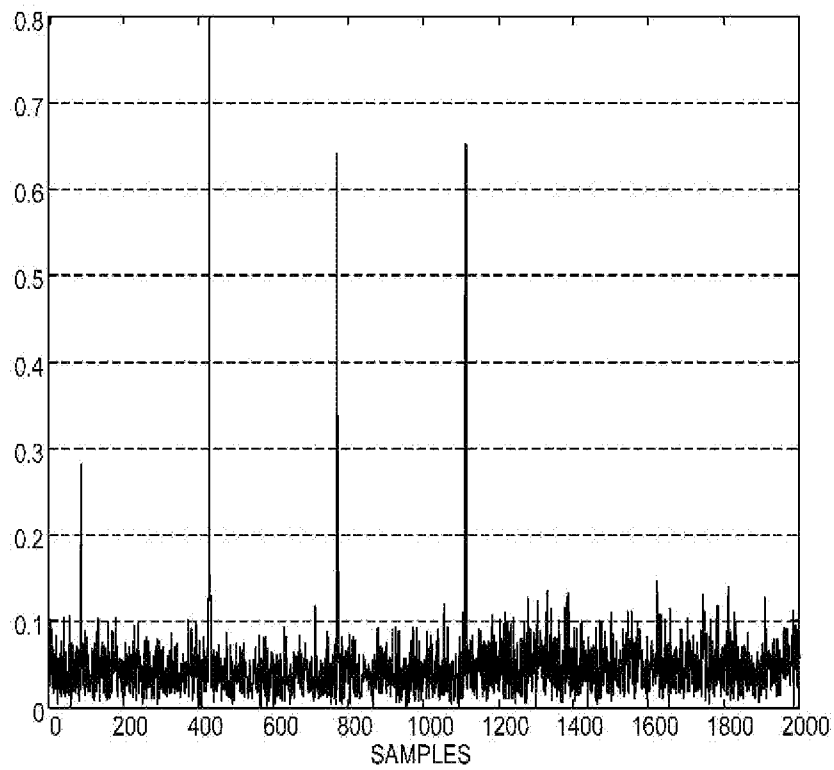


FIG. 7A

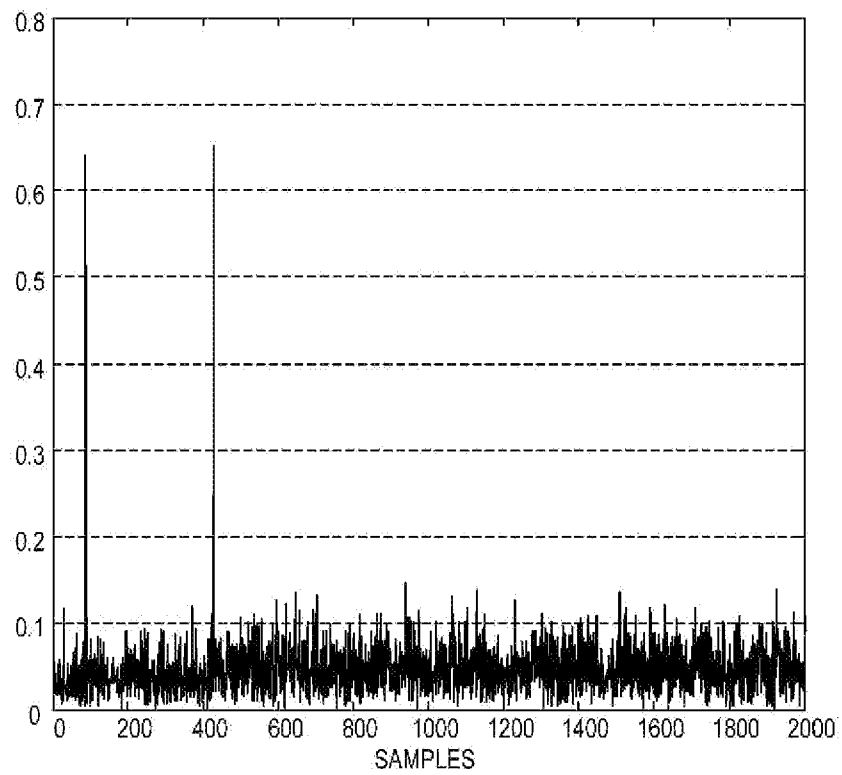


FIG. 7B

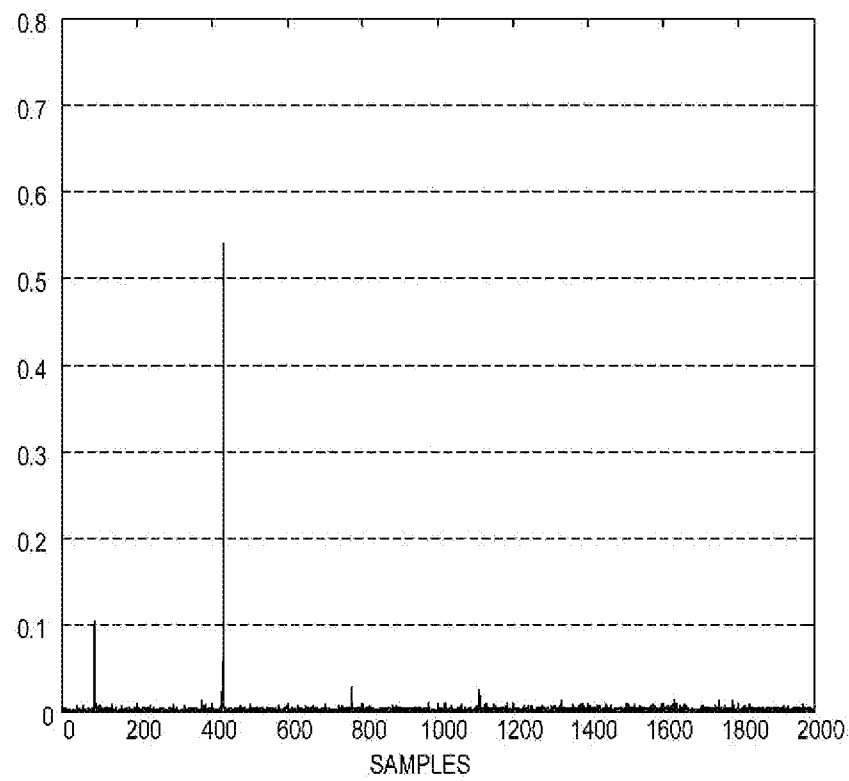


FIG.7C

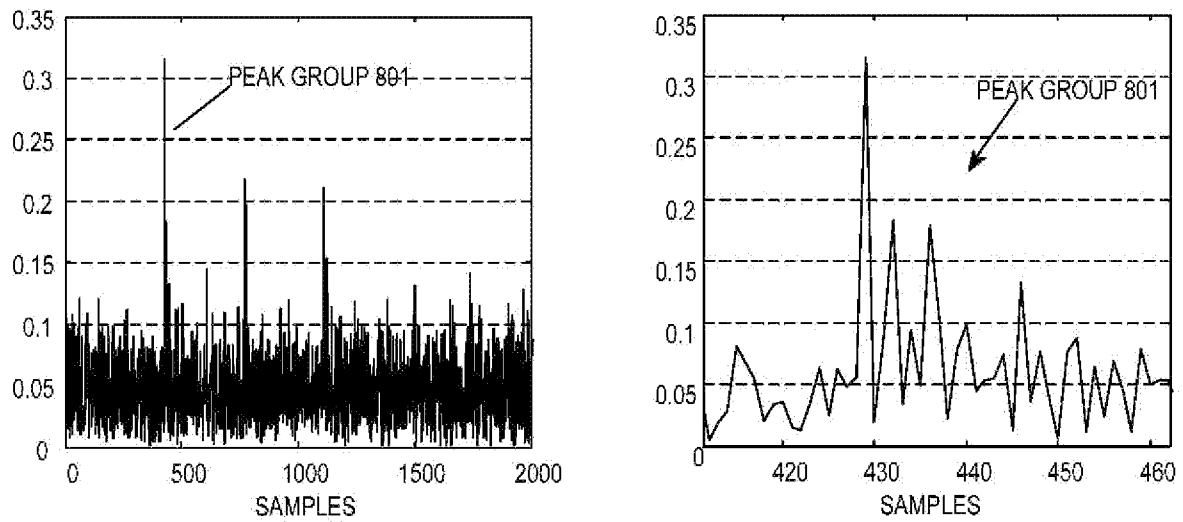


FIG.8A

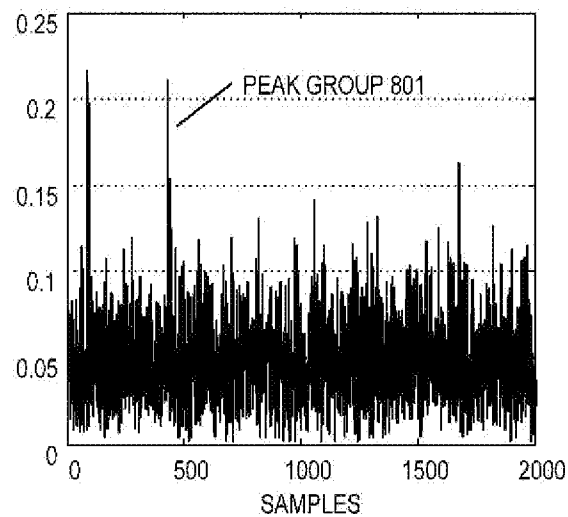


FIG.8B

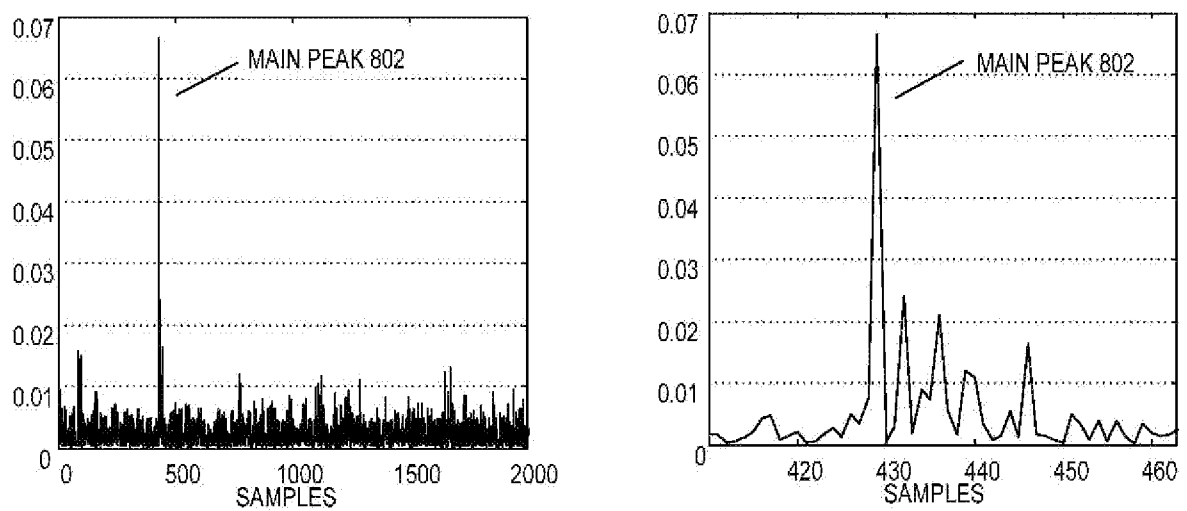


FIG.8C

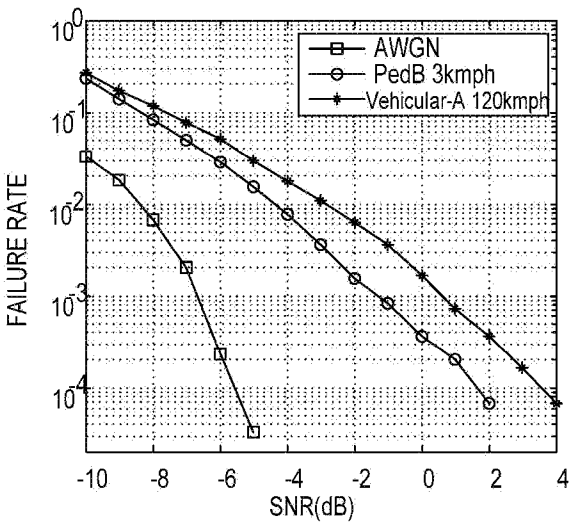


FIG.9

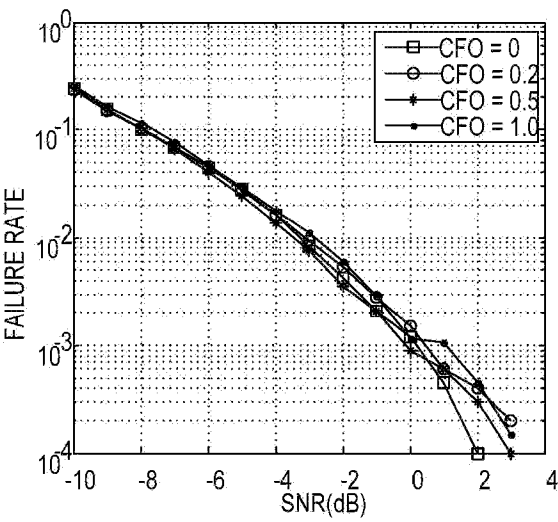


FIG.10

INTERNATIONAL SEARCH REPORT

International application No.

PCT/CN2010/071380

A. CLASSIFICATION OF SUBJECT MATTER

H04L 27/14(2006.01) i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC: H04L 27/-

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

Database: WPI; EPODOC; CNPAT; CNKI

Search terms: time, synchronization, synchronous, correct, two, preamble, compensate

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	CN1842981A(SONY CORP) 04 Oct. 2006 (04.10.2006) See the whole document	1-26
A	CN1893407A(SAMSUNG ELECTRO-MECHANICS CO., LTD) 10 Jan. 2007 (10.01.2007) See the whole document	1-26
A	CN101115036A(SAMSUNG ELECTRONICS CO., LTD) 30 Jan. 2008 (30.01.2008) See the whole document	1-26

☐ Further documents are listed in the continuation of Box C.☒ See patent family annex.

* Special categories of cited documents:	“T” later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
“A” document defining the general state of the art which is not considered to be of particular relevance	“X” document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
“E” earlier application or patent but published on or after the international filing date	“Y” document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
“L” document which may throw doubts on priority claim (S) or which is cited to establish the publication date of another citation or other special reason (as specified)	“&” document member of the same patent family
“O” document referring to an oral disclosure, use, exhibition or other means	
“P” document published prior to the international filing date but later than the priority date claimed	

Date of the actual completion of the international search 13 Dec. 2010 (13.12.2010)	Date of mailing of the international search report 06 Jan. 2011 (06.01.2011)
Name and mailing address of the ISA/CN The State Intellectual Property Office, the P.R.China 6 Xitucheng Rd., Jimen Bridge, Haidian District, Beijing, China 100088 Facsimile No. 86-10-62019451	Authorized officer WANG, YAN Telephone No. (86-10)62411625

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CN2010/071380

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