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(71) Applicant: **SEOUL OPTO DEVICE CO., LTD.** [KR/KR]; 1B-36, 727-5, Wonsi-dong, Danwon-gu, Ansan-si, Gyeonggi-do 425-85 1 (KR).

(72) Inventors: **SUH, Dae Woong;** 1B-36, 727-5, Wonsi-dong, Danwon-gu, Ansan-si, Gyeonggi-do 425-85 1 (KR). **LEE, Kyu Ho;** 1B-36, 727-5, Wonsi-dong, Danwon-gu, Ansan-si, Gyeonggi-do 425-85 1 (KR). **JANG, Jong Min;** 1B-36, 727-5, Wonsi-dong, Danwon-gu, Ansan-si, Gyeonggi-do 425-85 1 (KR). **IN, Chi Hyun;** 1B-36, 727-5, Wonsi-dong, Danwon-gu, Ansan-si, Gyeonggi-do 425-851 (KR).

(74) Agent: **AIP PATENT & LAW FIRM;** Shinwon Building 8F, 813-14, Yeoksam-dong, Gangnam-gu, Seoul 135-933 (KR).

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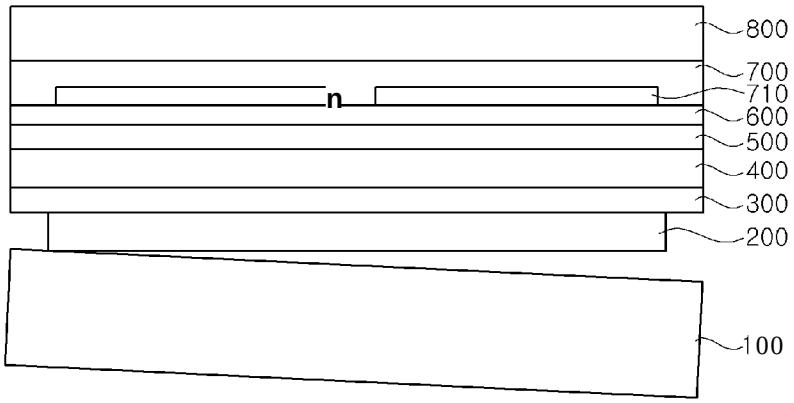
(54) Title: METHOD FOR SEPARATING EPITAXIAL LAYER FROM GROWTH SUBSTRATE

[Fig. 5]



(57) Abstract: The present invention relates to a method for separating an epitaxial layer from a growth substrate. The present invention provides a method for separating an epitaxial layer from a growth substrate, comprising growing an epitaxial layer including a plurality of layers on a growth substrate; etching an edge of at least one layer in the epitaxial layer to form a notch; forming a bonding layer on the epitaxial layer, contacting a bonding substrate onto the bonding layer, and then heating the bonding layer to a bonding temperature for joining the epitaxial layer and the bonding substrate; and cooling the bonding layer after the heating of the bonding layer, so that the epitaxial layer and the bonding substrate are joined by the bonding layer, and the epitaxial layer is separated from the growth substrate, wherein the separating the epitaxial layer from the growth substrate starts with separation from the at least one layer where the notch is formed.

Description

Title of Invention: METHOD FOR SEPARATING EPITAXIAL LAYER FROM GROWTH SUBSTRATE

Technical Field

[1] The present invention relates to a method for separating an epitaxial layer from a growth substrate.

Background Art

[2] A light emitting diode (LED) is an optical semiconductor device using a principle that when a voltage is applied to a junction of a P-type semiconductor and an N-type semiconductor, energy released upon recombination of electrons in an N-region with holes in a P-region is emitted as light. Such LEDs have characteristics of environmental friendliness, low driving voltages, long lifespan, low costs, etc. Conventionally, the LEDs have been frequently applied to lamps for display or to display of simple information such as numbers. However, with development of industrial technologies, particularly information display and semiconductor technologies, the LEDs have been recently used in various fields such as displays, vehicle headlamps and projectors.

[3] Particularly, an LED using a Group III-V based semiconductor such as gallium nitride (GaN) has a direct transition energy band structure, so that it has an advantage of high internal quantum efficiency. Accordingly, the GaN semiconductor has recently come into the spotlight as a material for LEDs.

[4] In a fabrication of the LED, it is difficult to make a homogeneous substrate on which an epitaxial layer of the LED can be grown. Therefore, the epitaxial layer is grown on a heterogeneous growth substrate having a similar crystal structure by means of a process such as metal organic chemical vapor deposition (MOCVD) or molecular beam epitaxy (MBE). Generally, a sapphire substrate with a hexagonal system is mainly used as a growth substrate. However, since the sapphire substrate is electrically non-conductive, it restricts the structure of an LED formed thereon.

[5] Accordingly, studies have been conducted to develop a technique for fabricating a vertical LED by growing epitaxial layers on a growth substrate such as a sapphire substrate and then separating the growth substrate.

[6] A method for removing a substrate by means of a substrate polishing process may be used as a method for separating the growth substrate. However, the removal of the growth substrate by polishing the growth substrate requires much time and high costs.

[7] Therefore, a laser lift-off (LLO) method, a stress lift-off (SLO) method or a chemical lift-off (CLO) method is mainly used as the method for separating the epitaxial layer

from the growth substrate.

[8] Here, the LLO method is a method in which an epitaxial layer is grown on a growth substrate, a support substrate is bonded onto an epitaxial layer, and a laser beam then irradiates through the growth substrate to separate the epitaxial layer from the growth substrate. The SLO method is a method in which a convexo-concave pattern is formed on one surface of a growth substrate, a passivation layer such as an insulation film is formed on some regions of the growth substrate such that an epitaxial layer is grown on only other regions of the growth substrate, and a thick epitaxial layer is grown and then cooled to separate the epitaxial layer from the growth substrate due to surface stress. The CLO method is a method in which a pattern is formed by using a material, which is susceptible to chemical damage, on a surface of a growth substrate, an epitaxial layer is grown, and the material that is susceptible to chemical damage is electrochemically or chemically removed to separate the epitaxial layer from the growth substrate.

[9] However, in the LLO method among the aforementioned methods for separating the growth substrate, heat generated by irradiation of a laser beam has influence on the epitaxial layer, thereby deteriorating characteristics of the epitaxial layer. In the SLO method or CLO method, a separate process of processing the surface of the growth substrate is required before the epitaxial layer is grown, which results in complicated processes as well as problems with mass production due to much time that is taken to separate the epitaxial layer. In the SLO method, the epitaxial layer can be separated without damage thereto only when it is grown to be thick, and thus, it is not easy to apply this method to actual processes.

Disclosure of Invention

Technical Problem

[10] An object of the present invention is to provide a method capable of easily separating an epitaxial layer from a growth substrate without having influence on the epitaxial layer.

Solution to Problem

[11] To achieve the object, a method for separating an epitaxial layer from a growth substrate according to one embodiment of the present invention comprises growing an epitaxial layer comprising a plurality of layers on a growth substrate; etching an edge of at least one layer in the epitaxial layer to form a notch; forming a bonding layer on the epitaxial layer, contacting a bonding substrate onto the bonding layer, and then heating the bonding layer to a bonding temperature for joining the epitaxial layer and the bonding substrate; and cooling the bonding layer after the heating of the bonding layer, so that the epitaxial layer and the bonding substrate are joined by the bonding

layer and the epitaxial layer is separated from the growth substrate. The separation of the epitaxial layer from the growth substrate starts with separation from the at least one layer where the notch is formed.

[12] The growth of the epitaxial layer comprising the plurality of layers may comprise growing a heavily doped semiconductor layer on the growth substrate; growing an undoped semiconductor layer on the heavily doped semiconductor layer; and sequentially growing a first semiconductor layer, an active layer and a second semiconductor layer on the undoped semiconductor layer.

[13] Alternatively, the growth of the epitaxial layer comprising the plurality of layers may comprise growing an undoped semiconductor layer on the growth substrate; growing a heavily doped semiconductor layer on the undoped semiconductor layer; and sequentially growing a first semiconductor layer, an active layer and a second semiconductor layer on the heavily doped semiconductor layer.

[14] The notch may be formed in an edge region of the heavily doped semiconductor layer.

[15] Meanwhile, the heavily doped semiconductor layer may comprise n-GaN doped with silicon, and the undoped semiconductor layer may comprise u-GaN.

[16] The notch may be formed by using electro-chemical etching.

Advantageous Effects of Invention

[17] According to the present invention, there is an advantage of providing a method capable of easily separating an epitaxial layer from a growth substrate without having a negative influence on the epitaxial layer.

Brief Description of Drawings

[18] Figs. 1 to 6 are sectional views illustrating a method for separating an epitaxial layer from a growth substrate according to an embodiment of the present invention.

[19] Figs. 7 to 9 are sectional views illustrating a method for separating an epitaxial layer from a growth substrate according to another embodiment of the present invention.

Mode for the Invention

[20] Hereinafter, exemplary embodiments of the present invention will be described in detail with reference to the accompanying drawings. These embodiments described below are provided by way of example so that the spirit of the present invention can be fully understood by those skilled in the art. Therefore, the present invention is not limited to the embodiments described below but may be implemented into different forms. In the drawings, the widths, lengths, thicknesses and the like of elements may be exaggerated for convenience. Further, an expression that an element is placed "on" or "above" another element indicates not only a case where the element is placed "directly on" or "directly above" the other element but also a case where a further

element is interposed between the element and the other element. Like reference numerals are used to designate like elements throughout the specification and drawings.

[21] Figs. 1 to 6 are sectional views illustrating a method for separating an epitaxial layer from a growth substrate according to an embodiment of the present invention.

[22] Referring to Fig. 1, a growth substrate 100 is first prepared.

[23] The growth substrate 100 may be any substrate, e.g., a sapphire substrate, a silicon carbide substrate, a silicon substrate or the like, on which a semiconductor layer described later, particularly a layer of a Group III nitride can be epitaxially grown. Preferably, the growth substrate 100 may be a sapphire substrate.

[24] Subsequently, an epitaxial layer including a plurality of layers is grown on one surface of the growth substrate 100.

[25] A heavily doped semiconductor layer 200 is grown on the one surface of the growth substrate 100. Subsequently, an undoped semiconductor layer 300 is grown on the heavily doped semiconductor layer 200. A first semiconductor layer 400, an active layer 500 and a second semiconductor layer 600 may be sequentially grown on the undoped semiconductor layer 300.

[26] Although not shown in this figure, a superlattice layer (not shown) may be further grown between the first semiconductor layer 400 and the active layer 500, and an electron blocking layer (not shown) may be further grown between the active layer 500 and the second semiconductor layer 600.

[27] The heavily doped semiconductor layer 200 may include n-GaN doped with silicon (Si) at a high concentration. The heavily doped semiconductor layer 200 may be formed to have a thickness of 0.1 to 20㎛, and preferably a thickness of 3㎛.

[28] The undoped semiconductor layer 300 may include u-GaN undoped with impurities.

[29] The first semiconductor layer 400 may include a semiconductor layer of a Group III nitride such as (Al, Ga, In)N. The first semiconductor layer 400 may be a GaN layer doped with N-type impurities such as Si, i.e., an N-GaN layer. The first semiconductor layer 400 may be formed as a single layer or multilayer. In a case where the first semiconductor layer 400 is formed as a multilayer, the first semiconductor layer 400 may include a superlattice layer.

[30] The active layer 500 may include a semiconductor layer of a Group III nitride such as (Al, Ga, In)N. The active layer may include a single layer or a plurality of layers. The active layer 500 may be a layer that at least emits light of a wavelength, e.g., ultraviolet light. The active layer 500 may have a single quantum well structure including one well layer (not shown), or may have a multiple quantum well structure in which well layers (not shown) and barrier layers (not shown) are alternately laminated. In this case, one or both of the well layers and the barrier layers may be formed to have a su-

perlattice structure.

[31] The second semiconductor layer 600 may include a semiconductor layer of a Group III nitride such as (Al, Ga, In)N. The second semiconductor layer 600 may be a GaN layer doped with P-type impurities such as Mg, i.e., a P-GaN layer. The second semiconductor layer 600 may be formed as a single layer or multilayer. For example, the second semiconductor layer 600 may include a superlattice layer.

[32] The superlattice layer (not shown) may be positioned between the first semiconductor layer 400 and the active layer 500, and may have a structure in which a plurality of Group III-N based compound semiconductor layers are laminated, e.g., InN layers and InGaN layers are repetitively laminated. The superlattice layer (not shown) can be grown earlier than the active layer 500 so as to prevent a dislocation, defect or the like from diffusing or propagating to the active layer 500. Thus, the superlattice layer (not shown) can serve to reduce formation of a defect such as a dislocation in the active layer 500 and also to improve crystallinity of the active layer 500.

[33] The electron blocking layer (not shown) may be positioned between the active layer 500 and the second semiconductor layer 600 so as to improve the efficiency of recombination of electrons and holes, and may include a semiconductor layer formed of a material having a relatively wide bandgap. The electron blocking layer (not shown) may include an (Al, In, Ga)N-based Group III nitride semiconductor layer. For example, the electron blocking layer may include a P-AlGaN layer doped with Mg.

[34] Referring to Fig. 2, after the epitaxial layer including the plurality of layers including the high-concentration semiconductor layer 200, the undoped semiconductor layer 300, the first semiconductor layer 400, the active layer 500 and the second semiconductor layer 600 is grown on the growth substrate 100, a notch 210 is formed by etching an edge region of any one of the plurality of layers in the epitaxial layer.

[35] In this case, at least one layer of the plurality of layers in the epitaxial layer may be the heavily doped semiconductor layer 200.

[36] The notch 210 may be formed by etching the heavily doped semiconductor layer 200, and the etching may be, for example, an electro-chemical etching (ECE). The electro-chemical etching of the heavily doped semiconductor layer 200 includes immersing the growth substrate 100 on which the epitaxial layer including the plurality of layers has been grown into an electrolyte solution and then applying a voltage to the heavily doped semiconductor layer 200. Accordingly, the edge region of the heavily doped semiconductor layer 200 exposed to a side surface of the growth substrate 100 is electro-chemically etched inwardly, so that the notch 210 can be formed.

[37] Referring to Fig. 3, a bonding layer 700 is formed on the epitaxial layer including the plurality of layers.

[38] In this case, before the bonding layer 700 is formed, a metallic reflective pattern

layer 710 may be further formed on the epitaxial layer including the plurality of layers. The metallic reflective pattern layer 710 may reflect light, and/or may serve to electrically connect the epitaxial layer including the plurality of layers, particularly the second semiconductor layer 600, to the bonding layer 700 and/or a bonding substrate 800 described later.

[39] The bonding layer 700 joins the bonding substrate 800 described later and the second semiconductor layer 600 or the metallic reflective pattern layer 710. The bonding layer 700 may be formed of a conductive material that performs bonding by being heated to a bonding temperature, e.g., a temperature of 100 to 500°C and then cooled. Preferably, the bonding layer 700 may be formed of an alloy containing zinc (Sn) or an alloy containing copper, gold, silver or the like. However, the present invention is not limited thereto.

[40] Although not shown in this figure, when all or some of the plurality of layers in the epitaxial layer, e.g., the first semiconductor layer 400, the active layer 500 and the second semiconductor layer 600, are patterned by etching, an etching stop pattern (not shown) used as an etching stop layer may be further formed between segments of the metallic reflective pattern layer 710.

[41] The metallic reflective pattern layer 710 may be formed of a material including a metal capable of reflecting light. Preferably, the metallic reflective pattern layer 710 may be formed of a reflective and conductive metallic material, e.g., a material including nickel (Ni), platinum (Pt), palladium (Pd), rhodium (Rh), tungsten (W), titanium (Ti), silver (Ag) or gold (Au).

[42] The etching stop pattern (not shown) may be formed of an insulating material including a silicon oxide film, a silicon nitride film or the like.

[43] Referring to Fig. 4, the bonding substrate 800 is prepared separately from the process of preparing the growth substrate 100 and growing the epitaxial layer including the plurality of layers on the growth substrate 100.

[44] The bonding substrate 800 may include a conductive material, e.g., copper, having a thermal expansion coefficient considerably different from that of the epitaxial layer including the plurality of layers.

[45] The bonding substrate 800 is brought into contact with the bonding layer 700.

[46] Subsequently, the bonding layer 700 and the bonding substrate 800 are heated while they are in contact with each other. At this time, they are heated to a bonding temperature at which the bonding layer 700 joins the epitaxial layer including the plurality of layers and the bonding substrate 800, and are then cooled so that the bonding layer 700 can join the epitaxial layer including the plurality of layers and the bonding substrate 800.

[47] That is, in a case where the bonding layer 700 is made of an alloy including Zn, e.g.,

a solder, the bonding layer 700 is heated to a temperature of about 450°C such that the bonding layer 700 is reflowed, and then cooled so that the epitaxial layer including the plurality of layers and the bonding substrate 800 are joined.

[48] Referring to Fig. 5, the epitaxial layer including the plurality of layers and the bonding substrate 800 are separated from the growth substrate 100 by heating the bonding layer 700 to the bonding temperature and then cooling the bonding layer 700.

[49] At this time, for the separation of the epitaxial layer including the plurality of layers from the growth substrate 100, upon performing the heating to the bonding temperature and the subsequent cooling, the epitaxial layer including the plurality of layers and the bonding substrate 800 are also heated to the same temperature and then cooled. Since the epitaxial layer including the plurality of layers and the bonding substrate 800 have a large difference in thermal expansion coefficient therebetween, thermal stress is generated so that the epitaxial layer including the plurality of layers is separated from the growth substrate 100.

[50] This separation may start with separation from the heavily doped semiconductor layer 200 where the notch 210 is formed. Particularly, the separation may start from the notch 210 formed in an edge region of the heavily doped semiconductor layer 200. That is, the thermal stress generated by the difference in thermal expansion coefficient between the epitaxial layer including the plurality of layers and the bonding substrate 800 is concentrated on the notch 210, and a crack is created from the notch 210 on which the thermal stress is concentrated. Thus, the epitaxial layer including the plurality of layers can be separated from the growth substrate 100.

[51] In this case, the separation can be further facilitated by applying an impact to the notch 210 using a sharp tool.

[52] Referring to Fig. 6, after the growth substrate 100 is separated, the exposed heavily doped semiconductor layer 200 and the undoped semiconductor layer 300 positioned beneath the heavily doped semiconductor layer 200 can be removed, thereby completing the process of separating the epitaxial layer including the plurality of layers from the growth substrate 100.

[53] The removal of the exposed heavily doped semiconductor layer 200 and the undoped semiconductor layer 300 may be made by a planarization process or an etching process.

[54] When the growth substrate 100 is separated, the exposed heavily doped semiconductor layer 200 might have been damaged due to concentration of the thermal stress. The damaged heavily doped semiconductor layer 200 may be a cause that lowers light emitting efficiency when an LED device is fabricated using the epitaxial layer including the plurality of layers and the bonding substrate 800. Therefore, the heavily doped semiconductor layer 200 may be removed after the separation process is

finished.

[55] In a case where an LED device is fabricated using the epitaxial layer including the plurality of layers and the bonding substrate 800, the undoped semiconductor layer 300 may be removed to expose a surface of the first semiconductor layer 400 in the epitaxial layer including the plurality of layers after the separating process is finished.

[56] At this time, although it is illustrated in this figure that the exposed heavily doped semiconductor layer 200 and the undoped semiconductor layer 300 have been removed, they may be left without being removed.

[57] Figs. 7 to 9 are sectional views illustrating a method for separating an epitaxial layer from a growth substrate according to another embodiment of the present invention.

[58] The method according to this embodiment will be described with reference to Fig. 7. First, a growth substrate 100 is prepared. The growth substrate 100 has been described in the method according to the embodiment described with reference to Figs. 1 to 6, and therefore, a detailed description thereof will be omitted.

[59] Subsequently, an epitaxial layer including a plurality of layers is epitaxially grown on one surface of the growth substrate 100.

[60] At this time, the epitaxial layer including the plurality of layers is formed by first growing an undoped semiconductor layer 300 on the surface of the growth substrate 100, growing a heavily doped semiconductor layer 200 on the undoped semiconductor layer 300, and then sequentially growing a first semiconductor layer 400, an active layer 500 and a second semiconductor layer 600 on the heavily doped semiconductor layer 200.

[61] At this time, although not shown in this figure, a superlattice layer (not shown) may be further grown between the first semiconductor layer 400 and the active layer 500, and an electron blocking layer (not shown) may be further grown between the active layer 500 and the second semiconductor layer 600.

[62] Therefore, this embodiment is different from the embodiment described with reference to Figs. 1 to 6 in that the undoped semiconductor layer 300 rather than the heavily doped semiconductor layer 200 is first grown on the growth substrate 100, and the heavily doped semiconductor layer 200 is then grown.

[63] At this time, the heavily doped semiconductor layer 200, the undoped semiconductor layer 300, the first semiconductor layer 400, the active layer 500, the second semiconductor layer 600, the superlattice layer (not shown) and the electron blocking layer (not shown) have been described in connection with the method according to the embodiment described with reference to Figs. 1 to 6, and thus, detailed descriptions thereof will be omitted.

[64] Subsequently, a notch 210 is formed in an edge region of the heavily doped semiconductor layer 200 through the same process as that described in connection with the

method according to the embodiment described with reference to Figs. 1 to 6.

[65] Subsequently, a bonding layer 700 including metallic reflective pattern layer 710 may be formed on the epitaxial layer including the plurality of layers. Although not shown in this figure, an etching stop pattern (not shown) may be further formed between segments of the metallic reflective pattern layer 710.

[66] Since the metallic reflective pattern layer 710, the bonding layer 700 and the etching stop pattern (not shown) have been described in connection with the method for separating the epitaxial layer from the growth substrate according to the embodiment described with reference to Figs. 1 to 6, detailed descriptions thereof will be omitted.

[67] Referring to Fig. 8, a bonding substrate 800 is prepared separately from the process of growing the epitaxial layer including the plurality of layers on the growth substrate 100.

[68] At this time, the bonding substrate 800 has been described in the method for separating the epitaxial layer from the growth substrate according to the embodiment described with reference to Figs. 1 to 6, and thus, a detailed description thereof will be omitted.

[69] Subsequently, the bonding substrate 800 is brought into contact with the bonding layer 700, and heating and subsequent cooling are performed while the bonding layer 700 and the boding substrate 800 are in contact with each other, thereby separating the epitaxial layer including the plurality of layers from the growth substrate 100.

[70] At this time, since the undoped semiconductor layer 300 is first grown on the growth substrate 100 and the heavily doped semiconductor layer 200 is then grown on the undoped semiconductor layer 300 as shown in Fig. 8, upon separation of the growth substrate 100, the undoped semiconductor layer 300 is separated together with the growth substrate 100.

[71] Since the separation of the epitaxial layer including the plurality of layers from the growth substrate 100 has been described in the method for separating the epitaxial layer from the substrate according to the embodiment described with reference to Figs. 1 to 6, a detailed description thereof will be omitted.

[72] Referring to Fig. 9, after the growth substrate 100 is separated, the exposed heavily doped semiconductor layer 200 can be removed to expose the first semiconductor layer 400, thereby completing the process of separating the epitaxial layer including the plurality of layers from the growth substrate 100.

[73] The exposed heavily doped semiconductor layer 200 may be removed by performing an etching process or a planarization process. Although it is illustrated in this figure that the exposed heavily doped semiconductor layer 200 has been removed, the exposed heavily doped semiconductor layer 200 may be left without being removed.

[74] Thus, in the method for separating the epitaxial layer from the growth substrate, the

epitaxial layer including the plurality of layers is epitaxially grown on the growth substrate 100, and the notch 210 is formed in an edge region of any one layer of the plurality of layers in the epitaxial layer, e.g., the heavily doped semiconductor layer 200. Then, the bonding layer 700 is formed on the epitaxial layer including the plurality of layers, and the bonding substrate 800 having a thermal expansion coefficient considerably different from that of the epitaxial layer including the plurality of layers is brought into contact with the bonding layer 700. Preferably, the thermal expansion coefficient of the bonding substrate 800 is greater than that of the epitaxial layer including the plurality of layers. Thereafter, the epitaxial layer including the plurality of layers, the bonding layer 700 and the bonding substrate 800 are heated and then cooled to cause the bonding layer 700 to join the epitaxial layer including the plurality of layers and the bonding substrate 800. Subsequently, the thermal stress generated due to the difference in thermal expansion coefficient is caused to be concentrated on the notch 210 formed at any one layer of the plurality of layers in the epitaxial layer, so that the epitaxial layer including the plurality of layers can be separated from the growth substrate 100, starting from the notch 210.

[75] According to the present invention, there is an advantage of providing a method capable of easily separating an epitaxial layer from a growth substrate without having a negative influence on the epitaxial layer.

[76] Although the present invention has been described in connection with the aforementioned embodiments, the present invention is not limited thereto. It will be understood by those skilled in the art that various changes and modifications can be made thereto without departing from and also fall within the spirit and scope of the present invention.

Claims

[Claim 1] A method for separating an epitaxial layer from a growth substrate, the method comprising:
growing an epitaxial layer comprising a plurality of layers on a growth substrate;
etching an edge of at least one layer in the epitaxial layer to form a notch;
forming a bonding layer on the epitaxial layer, contacting a bonding substrate onto the bonding layer, and then heating the bonding layer to a bonding temperature for joining the epitaxial layer and the bonding substrate;
cooling the bonding layer after the heating of the boding layer, so that the epitaxial layer and the bonding substrate are joined by the bonding layer and the epitaxial layer is separated from the growth substrate,
wherein the separating the epitaxial layer from the growth substrate starts with separation from the at least one layer where the notch is formed.

[Claim 2] The method of claim 1, wherein the growing the epitaxial layer comprising the plurality of layers comprises:
growing a heavily doped semiconductor layer on the growth substrate;
growing an undoped semiconductor layer on the heavily doped semiconductor layer; and
sequentially growing a first semiconductor layer, an active layer and a second semiconductor layer on the undoped semiconductor layer.

[Claim 3] The method of claim 1, wherein the growing the epitaxial layer comprising the plurality of layers comprises:
growing an undoped semiconductor layer on the growth substrate;
growing a heavily doped semiconductor layer on the undoped semiconductor layer; and
sequentially growing a first semiconductor layer, an active layer and a second semiconductor layer on the heavily doped semiconductor layer.

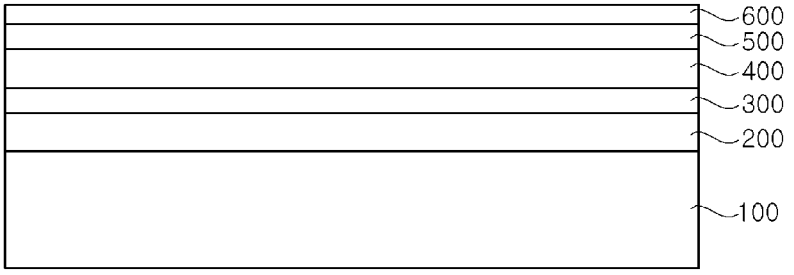
[Claim 4] The method of claim 2 or 3, wherein the notch is formed in an edge region of the heavily doped semiconductor layer.

[Claim 5] The method of claim 2 or 3, wherein the heavily doped semiconductor layer comprises n-GaN doped with silicon, and the undoped semiconductor layer comprises u-GaN.

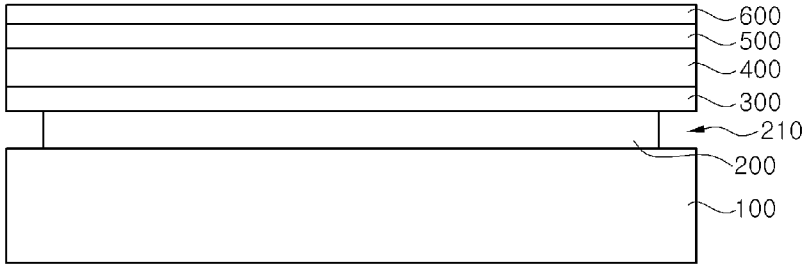
[Claim 6] The method of claim 2 or 3, wherein the notch is formed by using

electro-chemical etching.

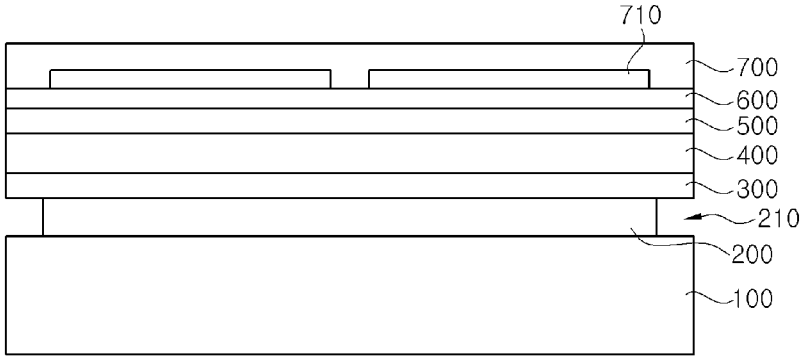
[Fig. 1]



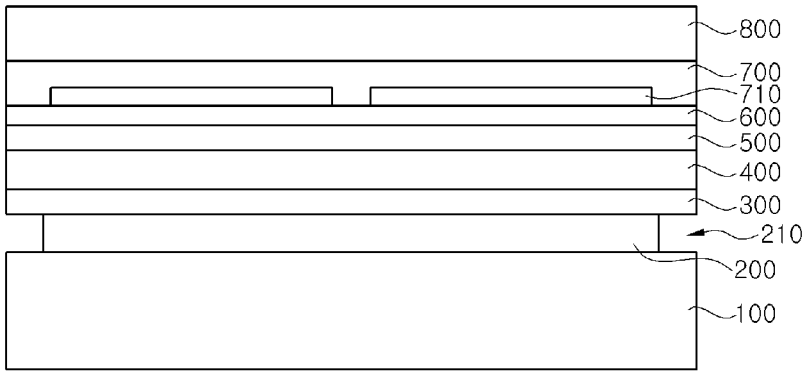
[Fig. 2]



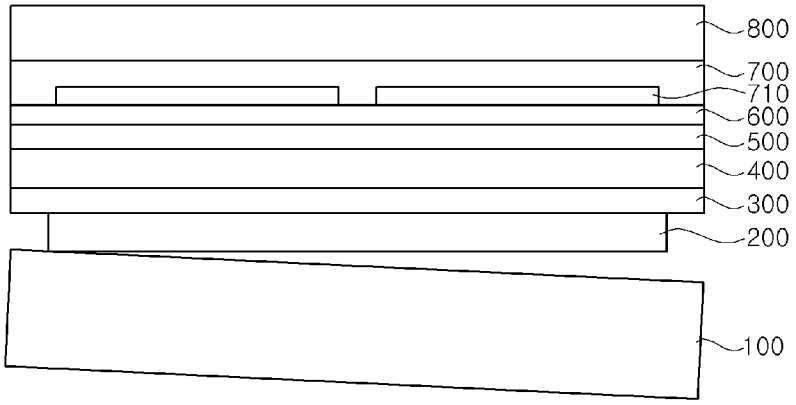
[Fig. 3]



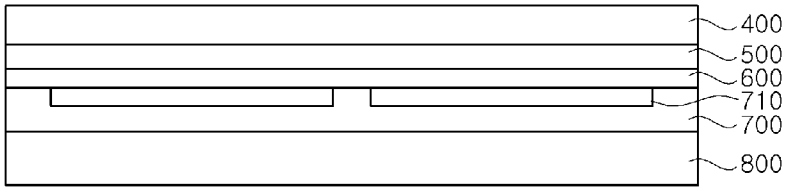
[Fig. 4]



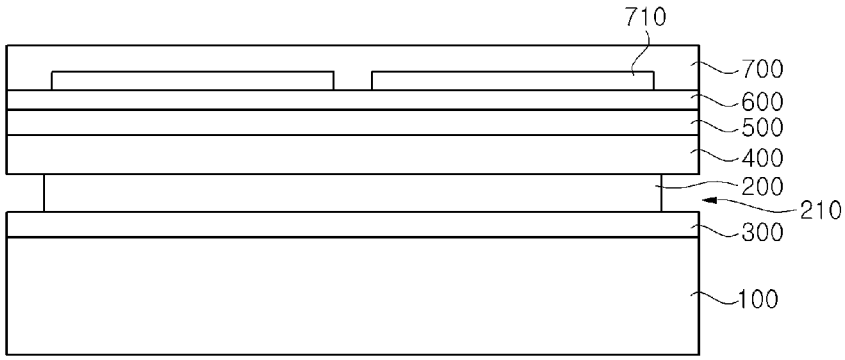
[Fig. 5]



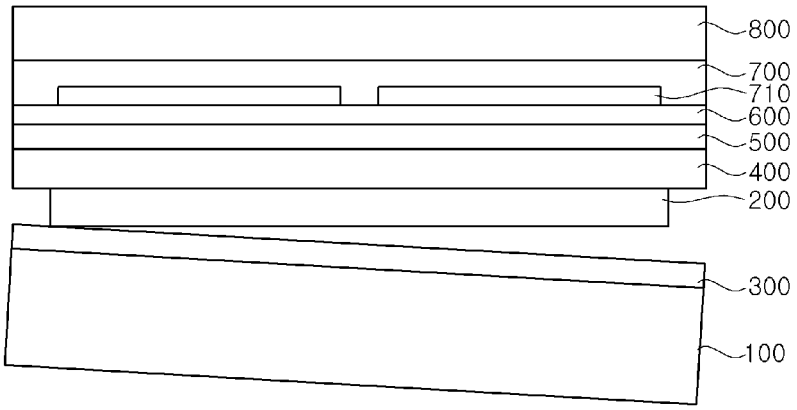
[Fig. 6]



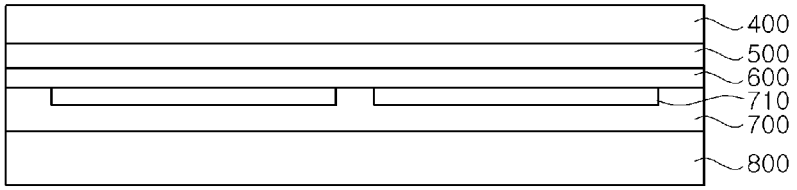
[Fig. 7]



[Fig. 8]



[Fig. 9]



INTERNATIONAL SEARCH REPORT

International application No.
PCT/KR2012/010096

A. CLASSIFICATION OF SUBJECT MATTER

H01L 33/12(2010.01)i, H01L 21/20(2006.01)1

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 33/12; H01L 21/46; H01L 29/739; H01L 33/14

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: free standing, vertical, separating, notch, bonding

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
19 FEBRUARY 2013 (19.02.2013)	**20 FEBRUARY 2013 (20.02.2013)**

Name and mailing address of the ISA/KR
Korean Intellectual Property Office
189 Cheongsa-ro, Seo-gu, Daejeon Metropolitan City, 302-70 1, Republic of Korea
Facsimile No. 82-42-472-7140

Authorized officer
LEE Young Bae
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INTERNATIONAL SEARCH REPORT

Information on patent family members

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