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(54) Title: FAULT TOLERANT VOLTAGE REGULATOR

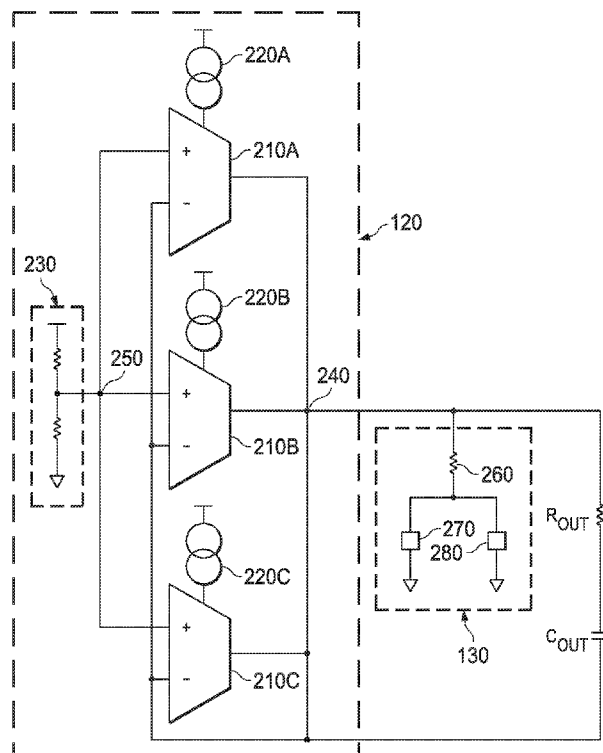


FIG. 2

(57) Abstract: A fault tolerant voltage regulator (120) may include a plurality of operational transconductance amplifiers (210A, 210B, 210C). The operational transconductance amplifiers (210A, 210B, 210C) may be configured according to a unity-gain configuration. The operational transconductance amplifiers (210A, 210B, 210C) may be configured to couple in parallel to a load (130). The operational transconductance amplifiers (210A, 210B, 210C) may be configured to load share a load current associated with the load (130) approximately equally among the operational transconductance amplifiers (210A, 210B, 210C).



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FAULT TOLERANT VOLTAGE REGULATOR

BACKGROUND

[0001] Some electrical circuits may have a single point of failure, so the circuit might fail entirely (e.g., cease to function in a desired or intended manner) when a single component or portion of the electrical circuit fails. For example, such failures may be caused by a current and/or voltage exceeding an operational range or threshold of the electrical circuit. One cause of an excessive current and/or voltage may be charged particles striking an electrical circuit. For example, an ionizing radiation particle strike may create electron-hole pairs in an electrical circuit that cause an excessive current to flow through the circuit (e.g., similar to coupling an unwanted current source into the circuit in parallel). Such a failure mode might cause the electrical circuit to fail and thus might be intolerable to other electrical circuits or devices utilizing the failed electrical circuit.

SUMMARY

[0002] In some embodiments, a plurality of operational transconductance amplifiers may be configured according to a unity-gain configuration. The operational transconductance amplifiers may be configured to couple in parallel to a load. The operational transconductance amplifiers may be configured to load share a load current associated with the load approximately equally among the operational transconductance amplifiers.

[0003] In another implementation, a fault tolerant voltage regulator may include a first operational transconductance amplifier, a second operational transconductance amplifier coupled in parallel with the first operational transconductance amplifier, and a third operational transconductance amplifier coupled in parallel with the first operational transconductance amplifier and the second operational transconductance amplifier. Each of the first operational transconductance amplifier, the second operational transconductance amplifier and the third operational transconductance amplifier may be configured to couple to a load. Each of the first operational transconductance amplifier, the second operational transconductance amplifier and the third operational transconductance amplifier may include an input stage that may include a plurality of metal oxide semiconductor field effect transistors (MOSFETs). The MOSFETs may

be configured to operate in accordance with a class B transfer function to approximately equally share a load current associated with the load.

[0004] In a further implementation, a method of sourcing or sinking a load current of a load. The method may include receiving a voltage from a power supply. The voltage may be based on a voltage provided by the power supply to the load. The method may also include transmitting a voltage based on the voltage received from the power supply to a plurality of amplifiers. The amplifiers may be configured as low-gain amplifiers and may operate in accordance with class B transfer function characteristics. The method may also include generating, by the amplifiers, an output current based on the voltage received from the power supply. Each of the amplifiers may contribute approximately equally to the output current. The method may also include generating, by a plurality of unaffected amplifiers, the output current based on the voltage received from the power supply when one of the amplifiers experiences an upset event. The unaffected amplifiers may be a subset of less than all of the plurality of amplifiers. Each of the unaffected amplifiers may contribute approximately equally to the output current.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] FIG 1 is a block diagram of an electronic device in accordance with various embodiments.

[0006] FIG 2 is a schematic diagram of the fault tolerant voltage regulator in accordance with various embodiments.

[0007] FIG 3 is a block diagram of an operational transconductance amplifier in accordance with various embodiments.

[0008] FIG 4 is a schematic diagram of a physical implementation of a transistor of the fault tolerant voltage regulator in accordance with various embodiments.

[0009] FIG 5 is a graph of a class B transfer function in accordance with various embodiments.

[0010] FIG 6 is a flowchart of a method for servicing a load current of a load in accordance with various embodiments.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0011] In some applications fault tolerance is beneficial so that the system can continue to operate normally in the face of a failure with a component of the system. Many electronic systems include a voltage regulator that generates regulated voltages for the various circuits comprising the system. Failure of the voltage regulator may render the entire system inoperative.

[0012] Disclosed herein are various embodiments directed to a fault tolerant voltage regulator. The disclosed fault tolerant voltage regulator may be a low dropout regulator (LDO) driven by a plurality of operational transconductance amplifiers configured to drive a load. In some embodiments, the load may be one or more resistors (or groups of resistors coupled together in series or parallel to create a desired resistance level). Each resistor may be used to terminate a respective double data rate (DDR) memory line coupled between processing and memory components of an electrical device. The disclosed fault tolerant voltage regulator may be redundant and, as such, may be able to continue operating in an expected manner when a portion of the fault tolerant voltage regulator fails. As used herein, if an electrical component fails, it may be: temporarily unable to function in a normal and expected manner but, after a period of time, is able to recover from the failure to again function in the normal and expected manner; or a catastrophic failure in which the electrical component fails to function in the normal and expected manner and is unable to recover from the failure. For example, when the fault tolerant voltage regulator is struck by ionizing radiation (or more generally, affected by any upset event that causes a failure or unacceptably large deviation in an output voltage of the fault tolerant voltage regulator), a deviation in the output voltage of the fault tolerant voltage regulator may vary, for example, within an approximately 80 millivolt (mV) range approximately centered on an optimal output voltage of the fault tolerant voltage regulator (e.g., an approximately +/- 40 mV tolerance of the optimal output voltage). In other embodiments, a deviation in the output voltage of the fault tolerant voltage regulator may vary within an approximately 50 mV range approximately centered on an optimal output voltage of the fault tolerant voltage regulator (e.g., an approximately +/- 25 mV tolerance of the optimal output voltage).

[0013] Redundancy of the fault tolerant voltage regulator may be implemented, such as by a plurality of operational transconductance amplifiers coupled in parallel. Each operational transconductance amplifier of the fault tolerant voltage regulator may be configured to provide a portion of the drive current for a load. For example, each operational transconductance amplifier may be configured to share support for the load with each other operational transconductance amplifier such that a current requirement of the load (e.g., sourcing or sinking current) may be split approximately evenly among each operational transconductance amplifier that is functioning properly in the fault tolerant voltage regulator. As a result, embodiments of the fault tolerant voltage regulator may provide increased reliability relative to conventional regulator

circuits while providing equivalent or improved performance at a lesser degree of topological or circuit complexity relative to conventional redundant regulator circuits.

[0014] FIG 1 shows a block diagram of an electronic device 100 in accordance with various embodiments. The electronic device 100 may include a power supply 110, a fault tolerant voltage regulator 120, and a load 130. The power supply 110 may be any suitable power supply included within, or coupled to, the electronic device 100. The power supply 110 may include, for example, any one or more electrical components (e.g., a transformer, an integrated circuit, or other suitable power supplying components) configured to output one or more direct current (DC) or alternating current (AC) voltages for use by the fault tolerant voltage regulator 120 or the load 130 for powering at least some components of the fault tolerant voltage regulator 120 or the load 130.

[0015] The load 130 may be any combination of electrical components or circuits that may be coupled to the fault tolerant voltage regulator 120 to be driven by the fault tolerant voltage regulator 120. For example, in some embodiments the load 130 may include one or more termination resistors coupled between the multiply redundant regulator 120 and a data line coupled between a processing circuit and a memory circuit such as a DDR circuit.

[0016] The fault tolerant voltage regulator 120 may comprise a plurality of regulator stages 121, each configured to couple to the load 130 to help drive the load 130. For example, each regulator stage 121 of the fault tolerant voltage regulator 120 may be configured to generate one or more regulated DC voltage outputs based on a voltage provided by the power supply 110 and source current to, or sink current from, the load 130. The fault tolerant voltage regulator 120 may have a number of regulator stages 121 corresponding to a desired level of redundancy determined of the fault tolerant voltage regulator 120. In some embodiments, the regulator stages 121 may be low (or approximately no) attenuation regulator stages (e.g., such as regulator stage configured according to a unity-gain configuration and/or configured without additional electrical components configured for gain or attenuation in a feedback path of the regulator stage). For example, the fault tolerant voltage regulator 120 may be a triple redundant fault tolerant voltage regulator having three regulator stages 121 such that when one regulator stage 121 of the fault tolerant voltage regulator 120 fails, the fault tolerant voltage regulator 120 may still operate to adequately drive the load using the remaining two regulator stages 121. As another example, the fault tolerant voltage regulator may be quadruple redundant having four

regulator stages 121 such that when one or two regulator stages 121 of the fault tolerant voltage regulator 120 fail, the fault tolerant voltage regulator 120 may still continue operating to adequately drive the load 130. A greater level of fault tolerance provides the fault tolerant voltage regulator 120 with greater protection against failure than a regulator with a smaller level of fault tolerance. The above examples are non-limiting, and the fault tolerant voltage regulator 120 may be configured, based on the teachings of the various embodiments disclosed herein, to include any number of regulator stages 121 to provide any desired level of redundancy, each implementation of which is intended to fall within the scope of this disclosure. In some embodiments, each regulator stage 121 may comprise a plurality of transistors, such as MOSFETs.

[0017] When one of the regulator stages 121 fails, the remaining regulator stages 121 may compensate for the failure and maintain adequate operation of the fault tolerant voltage regulator 120 to drive the load 130. For example, the fault tolerant voltage regulator 120 may include a plurality of independently biased operational transconductance amplifiers, each configured to source or sink an approximately equal portion of load current associated with the load 130. The operational transconductance amplifiers of the fault tolerant voltage regulator 120 may be configured to share the approximately equal portion of support for sourcing or sinking the load current associated with the load 130 when all operational transconductance amplifiers of the fault tolerant voltage regulator 120 are functioning properly, and when less than all operational transconductance amplifiers of the fault tolerant voltage regulator 120 are functioning properly.

[0018] FIG 2 shows a schematic diagram of the fault tolerant voltage regulator 120 in accordance with various embodiments. The fault tolerant voltage regulator 120 may include a plurality of operational transconductance amplifiers 210A, 210B, and 210C. Although three amplifiers are shown in the embodiment of FIG 2, the fault tolerant voltage regulator 120 may include any number of operational transconductance amplifiers 210 in other embodiments to provide a desired level of redundancy. Each operational transconductance amplifier 210A, 210B, and 210C may be individually biased by a respective current source 220A, 220B, and 220C. Because each of the operational transconductance amplifiers 210A, 210B, and 210C is biased by a separate current source 220A, 220B, and 220C, none of the current sources 220A, 220B, or 220C is a potential point of failure for more than one operational transconductance amplifier 210A, 210B, or 210C. Each of the current sources 220A, 220B, and 220C may

generate a bias current proportional (or approximately proportional) to a temperature, such as an environmental temperature in which the electronic device 100 is configured to operate.

[0019] Based on an intended application of the fault tolerant voltage regulator 120, the fault tolerant voltage regulator 120 may further include additional components such as a voltage divider 230 which may be configured to manipulate a voltage received by the fault tolerant voltage regulator 120 from the power supply 110 before the voltage is received by the operational transconductance amplifiers 210A, 210B, and 210C. For example, when the fault tolerant voltage regulator 120 is utilized as a driver for a termination resistor 260 that terminates DDR communication lines between processing circuitry 270 and memory circuitry 280, the voltage divider 230 may divide the voltage received by the fault tolerant voltage regulator 120 from the power supply 110 (e.g., a voltage approximately equal to a voltage provided to the memory circuitry) before the voltage is received by the operational transconductance amplifiers 210A, 210B, and 210C. For example, the voltage divider 230 may divide the voltage received by the fault tolerant voltage regulator 120 from the power supply 110 by a factor of two (e.g., the voltage divider 230 may be an “R by R” voltage divider in which each resistor of the voltage divider 230 has an approximately equal magnitude of resistance and thus the power supply voltage is divided in half). Additionally, the fault tolerant voltage regulator 120 may further include, or be configured to couple to, additional components such as an output resistor R_{out} and an output capacitor C_{out} , as shown. For example, the fault tolerant voltage regulator 120 may be configured to couple to the output capacitor C_{out} to select or program certain characteristics (e.g., a frequency response and/or a bandwidth) of the fault tolerant voltage regulator 120. In such embodiments, the output resistor R_{out} may be an inherent resistance of the output capacitor C_{out} rather than a separate electrical component. In other embodiments, the output resistor R_{out} may be a separate electrical component that may be included in addition to the inherent resistance of the output capacitor C_{out} .

[0020] Each operational transconductance amplifier 210A, 210B, and 210C may include a positive differential input and a negative differential input, and an output. In some embodiments, the positive differential input may be referred to as a non-inverting input of a differential input pair and the negative differential input may be referred to as an inverting input of the differential input pair. The output of each operational transconductance amplifier 210A, 210B, and 210C may be coupled to a common output node 240 that may also be coupled to the load 130 and the

output resistor R_{out} . The negative differential input of each operational transconductance amplifier 210A, 210B, and 210C may be coupled to the common output node 240 as shown. Accordingly, each operational transconductance amplifier 210A, 210B, and 210C may be configured according to a unity gain configuration in which components are not placed in a feedback loop of the operational transconductance amplifiers 210A, 210B, or 210C to provide an attenuation or gain to an output of any of the operational transconductance amplifiers 210A, 210B, or 210C. Alternatively, in other embodiments, one or more of the operational transconductance amplifiers 210A, 210B, and 210C may include one or more electrical components in a feedback loop to provide a desired gain or scaling factor for an output of the respective operational transconductance amplifiers 210A, 210B, or 210C. The positive differential input of each operational transconductance amplifier 210A, 210B, and 210C may be coupled to a common input node 250 that is coupled to an output of the voltage divider 230 (or alternatively, a power or signal supply with the voltage divider 230 is not included in the fault tolerant voltage regulator 120).

[0021] Each operational transconductance amplifier 210A, 210B, and 210C may be configured to load share a load current associated with the load 130 approximately equally between the amplifiers. For example, for a load 130 that sources or sinks a current of 3 amps, each operational transconductance amplifier 210A, 210B, and 210C may be configured to source or sink 1 amp of the load current. To provide redundancy, each operational transconductance amplifier 210A, 210B, and 210C may be configured such that a maximum sourceable or sinkable current (e.g., a current limit) of each operational transconductance amplifier 210A, 210B, and 210C is approximately one half of a maximum load current associated with the load 130. For example, for the load 130 that sources or sinks a current of 3 amps, each operational transconductance amplifier 210A, 210B, and 210C may be capable of servicing (e.g., sourcing or sinking) 1.5 amps of the load current. In this way, fewer than all of the operational transconductance amplifiers 210A, 210B, and 210C (e.g., only two of the operational transconductance amplifiers 210A, 210B, or 210C) may be capable of servicing the load current if an output current of a third of the operational transconductance amplifiers 210A, 210B, or 210C is unable to load share the load current. For example, in an embodiment in which one of the operational transconductance amplifiers (e.g., operational transconductance amplifier 210A for the sake of discussion) experiences an upset event (e.g., a failure or shutdown) that renders

the operational transconductance amplifier 210A unable to load share the load current, the remaining two operational transconductance amplifiers 210B and 210C may compensate for the lack of output from the operational transconductance amplifier 210A. The operational transconductance amplifiers 210B and 210C may compensate for the lack of output by load sharing between only the operational transconductance amplifiers 210B and 210C the load current that was previously load shared among operational transconductance amplifiers 210A, 210B, and 210C. Such compensation may result in a greater amount of the load current being serviced by each of the operational transconductance amplifiers 210B and 210C than before the upset event affecting the operational transconductance amplifier 210A.

[0022] In another embodiment in which the operational transconductance amplifier 210A experiences the upset event, the upset event may not render the operational transconductance amplifier 210A unable to load share the load current. Instead, the upset event may contribute additional current to the output current of the operational transconductance amplifier 210A. The additional current may be a transient current that may dissipate over a period of time. However, a magnitude of the additional current may be subject to certain compliance specifications (e.g., Joint Electron Device Engineering Council (JEDEC) specifications) that limit an output current or voltage range of the fault tolerant voltage regulator 120. Because each operational transconductance amplifier 210A, 210B, and 210C is configured to load share the load current approximately equally, each operational transconductance amplifier 210A, 210B, and 210C is responsible for and contributes only approximately one-third of an output current of the fault tolerant voltage regulator 120. Accordingly, the additional current resulting in the output current of the operational transconductance amplifier 210A as a result of the upset event may have approximately one-third of an effect on an output of the fault tolerant voltage regulator 120 than an effect on an output of conventional regulator implementations suffering from a similar upset event. As a result, in some embodiments the fault tolerant voltage regulator 120 may be capable of experiencing an upset event of an approximately three times greater magnitude than conventional regulator implementations while maintaining an output current or voltage that complies with applicable specifications.

[0023] Each of the operational transconductance amplifiers 210A, 210B, and 210C may have an approximately equal transconductance value. For example, the transconductance value of each of the operational transconductance amplifiers 210A, 210B, and 210C may be determined

according to $g_m = I_{out}/\Delta V$, where g_m is the transconductance value of the operational transconductance amplifiers 210A, 210B, and 210C, I_{out} is $1/x$ of the load current with x being the number of operational transconductance amplifiers having outputs coupled to the common output node 240 (e.g., illustrated as three in FIG 2), and ΔV is a difference between voltages present at the positive differential input and the negative differential input of each of the operational transconductance amplifiers 210A, 210B, and 210C (e.g., a difference between a voltage present at the common input node 250 and a voltage present at the common output node 240). In some embodiments, the transconductance value of each of the operational transconductance amplifiers 210A, 210B, and 210C may be determined based on a desired ΔV of approximately 40 mV, approximately 25 mV, or another suitable voltage. In some embodiments, the transconductance value of each of the operational transconductance amplifiers may be determined according to a minimum number of operational transconductance amplifiers that may support a load current of the load 130 instead of a total number of operational transconductance amplifiers having outputs coupled to the common output node 240. Alternatively, the transconductance value may be determined according to any suitable technique based on a particular topology, implementation, or configuration of the fault tolerant voltage regulator 120.

[0024] FIG 3 shows an illustrative block diagram of an operational transconductance amplifier 300, such as may be as any one or more of the operational transconductance amplifiers 210A, 210B, or 210C. In the example of FIG 3, the amplifier 300 may include an input stage 310, a class B function stage 320, and an output stage 330. The input stage 310 may comprise a plurality of transistors (e.g., transistors 340A and 340B) that may be configured as a differential input pair 350 that may be configured to receive a differential input. For example, a positive differential input of the differential input pair 350 (e.g., an input or gate terminal of the transistor 340A) may be coupled to the node 250 and a negative differential input of the differential input pair 350 (e.g., an input or gate terminal of the transistor 340B) may be coupled to the node 240, both as discussed above. Although the input stage 310 is illustrated as having transistors 340A and 340B, the input stage 310 may in fact include any number of transistors suitable for use in the amplifier 300. The transistors 340A and 340B may be, in some embodiments, p-type MOSFETs that may be coupled to a bias current I_{bias} (e.g., such as one of the bias currents 220A, 220B, or 220C, as discussed above). Based on the input received by the differential input

pair 350, the differential input stage 310 may be configured to transmit a current of approximately $\frac{I_{bias}}{2} \pm \frac{\Delta I_d}{2}$ to the class B transfer function stage 320, where $\Delta I_d = \frac{k_p * W}{L} * V_{id} * \sqrt{\frac{4 * I_{bias} * L}{k_p} - V_{id}^2}$, k_p is a transconductance gain of the transistors 340A and 340B, W is a width of the transistors 340A and 340B, L is a length of the transistors 340A and 340B, I_{bias} is a magnitude of the bias current, and V_{id} is a different between the positive differential input and the negative differential input of the differential input pair 350.

[0025] The class B transfer function stage 320 may include a plurality of transistors (e.g., n-type or p-type MOSFETs) that may be configured to generate a signal characteristic of a class B transfer function, as discussed below. For example, the class B transfer function stage 320 may include a first plurality of transistors that may be configured to cause the amplifier 300 to source current to a load when V_{id} is greater than a first threshold and a second plurality of transistors that may be configured to cause the amplifier 300 to sink current from the load when $-V_{id}$ is less than a second threshold (e.g., the first and second thresholds being determined with respect to a nominal output voltage of the amplifier 300). The transistors of the class B transfer function stage 320 may be implemented in any configuration that may be suitable for causing the amplifier 300 to source current to, or sink current from, the load based on an output of the input stage 310.

[0026] The output stage 330 may include a plurality of transistors configured as one or more current mirrors and may be coupled to an input power supply 370. For example, the output stage 330 may include transistors 340C and 340D that may be configured to form a current mirror 360A, and transistors 340E and 340F that may be configured to form a current mirror 360B. The current mirrors 360A and 360B may be configured to scale a current received by the output stage 330 from the class B transfer function stage 320 into an output current that is greater than the received current. Although the output stage 330 is illustrated as having current mirrors 360A and 360B, the output stage 330 may in fact include any number of current mirrors or other transistors suitable for use in sourcing or sinking current by the amplifier 300. Also, each of the transistors 340A, 340B, 340C, 340D, 340E and 340F may be individually implemented according to any suitable semiconductor technology, topology, or doping characteristic and may include additional electrical components and/or may be arranged in any suitable configuration to support such implementation.

[0027] FIG 4 shows a schematic diagram of a physical implementation of a transistor 410 of the fault tolerant voltage regulator 120 in accordance with various embodiments. The fault tolerant voltage regulator 120 may be implemented, in some embodiments, as an integrated circuit constructed on a semiconductor. For example, one or more transistors of the fault tolerant voltage regulator 120 (e.g., such as one or more of the transistors that comprise the input stage and/or the output stage of the operational transconductance amplifiers 210A, 210B, or 210C) may be implemented by a variety of semiconductor regions, some of which may be doped (e.g., made impure through an introduction of impurities to effect electrical properties of the semiconductor). As illustrated in FIG 4, the transistor 410 may be implemented, in some embodiments, by forming an epitaxial layer 420 on a substrate 430 and doping the epitaxial layer according to a desired semiconductor configuration (e.g., by doping the regions 460 to form n-doped regions and doping the region 470 to form a p-doped region). For example, the epitaxial layer may be doped in one or more areas with one or more concentrations of impurities that may cause an abundance of electrons or an abundance of holes, the combination and/or orientation of which may determine the electrical characteristics of the semiconductor. The transistor 410 may be isolated by an isolation region 440 such that the transistor 410 exists within an isolated well 450 of the semiconductor. In some embodiments, the isolation region 440 may be heavily doped with a first dopant (e.g., such that the isolation region is deeply n-doped) and both the epitaxial layer and the isolated well 450 may be doped with a second dopant (e.g., such that the epitaxial layer and the isolated well 450 may be p-doped). In this way, when an undesirable charge or current is introduced to the isolated well 450, for example, as a result of an ionizing radiation particle strike, the undesirable charge or current introduced to the transistor 410 and/or the isolated well 450 may be limited to the isolated well 450 by way of the isolation region 440. Such an isolation of the undesirable charge or current may inhibit charge sharing between the transistor 410 and/or the isolated well 450 and other transistors or electrical structures or components that may be formed on, or otherwise coupled to, the substrate 430 or the epitaxial layer 420.

[0028] FIG 5 shows an example of a graph 500 of a class B transfer function in accordance with various embodiments. The class B transfer function illustrated in graph 400 may illustrate minimum requirements for a fault tolerant voltage regulator 120 that is configured to operate within an approximately ± 40 mV tolerance of an optimal output voltage. The x-axis represents

the differential input voltage of the fault tolerant voltage regulator 120 and the y-axis represents the output current of the fault tolerant voltage regulator 120. Electrical components that share a common design and/or are fabricated in a common production run may nonetheless vary with regard to any one or more electrical characteristics. Such a variation may cause an undesirable complexity or difficulty in creating fault tolerant regulator circuits according to conventional. The fault tolerant voltage regulator 120 may be configured to compensate for such variations to reduce an effect of the variations on performance of the fault tolerant voltage regulator 120. In some embodiments, such a compensation may be performed by configuring components of the fault tolerant voltage regulator 120 (e.g., transistors coupled together to form the operational transconductance amplifiers 210A, 210B, and 210C) to operate in accordance with certain desired electrical characteristics. For example, a transfer function may describe a relationship between an input voltage and an output current of an electrical component. Certain transfer functions may be characteristic of certain electrical component responses. For example, a class A transfer function may describe an approximately linear or x:y relationship between an input voltage and an output current of an electrical component, where for approximately x volts in input voltage, approximately y amps of output current are generated. As another example, a class B transfer function may describe a relationship between an input voltage and an output current in terms of a polynomial function wherein the output may not be linearly proportional to the input voltage across an operational range of the electrical component. For example, the electrical component may be configured to operate in accordance with a class B transfer function that includes a transition zone where minimal to no change in output current may occur in response to a change in input voltage.

[0029] Electrical components of the fault tolerant voltage regulator 120 may be configured to advantageously utilize a particular embodiment of a class B transfer function to compensate for the inherent variations among electrical components, as discussed above. For example, without such compensations, a first of the operational transconductance amplifiers 210A, 210B, or 210C may output x current for z differential input voltage while a second of the operational transconductance amplifiers 210A, 210B, or 210C may output y current for the same z differential input voltage, where x and y are current magnitudes that are not equal and z is the differential input voltage. Such variations may inhibit approximately equal load sharing of the operational transconductance amplifiers 210A, 210B, and 210C. By configuring the electrical

components of the fault tolerant voltage regulator 120 to advantageously utilize a particular embodiment of a class B transfer function, the fault tolerant voltage regulator may utilize the transition zone of the class B transfer function to compensate for variations among the electrical components. For example, by utilizing the transition zone of the class B transfer function, a system-wide “on” and “off” may be configured such that the electrical components may each respond to an approximately equal input voltage with an approximately equal output current. For example, in some embodiments, operating in accordance with the class B transfer function of graph 500 may enable the operational transconductance amplifiers 210A, 210B, and 210C to compensate for an offset between the positive differential input and the negative differential input of each of the operational transconductance amplifiers 210A, 210B, and 210C to enable the operational transconductance amplifiers 210A, 210B, and 210C to each service an approximately equal portion of the load current, as discussed above.

[0030] As shown in graph 500, when the fault tolerant voltage regulator 120 sinks current from the load 130, for example, as illustrated by a current between zero and negative load current, current may flow from the load 130 to the fault tolerant voltage regulator 120. When the multiple redundant regulator 120 sources current to the load 130, for example, as illustrated by a current between zero and positive load current, current may flow from the fault tolerant voltage regulator 120 to the load 130.

[0031] FIG 6 shows a flowchart of a method 600 for servicing (e.g., sourcing or sinking) a load current of a load in accordance with various embodiments. The method 600 may be implemented in a regulator of an electronic device, for example, by the fault tolerant voltage regulator 120. The method 600 may be implemented to, for example, service a load current via a plurality of parallel-coupled amplifiers (such as, for example, operational transconductance amplifiers) performing load sharing before and after an upset event inhibits an ability of one of the amplifiers to participate in the load sharing. The load may include, for example, one or more DDR memory communication line terminations resistors.

[0032] At step 610, the regulator receives a voltage from a power supply (e.g., the power supply 110). The voltage received from the power supply may be, in some embodiments, based on a voltage provided by the power supply to another circuit (e.g., the load 130), or may be a unique or independent voltage not provided by the power supply to another circuit. Upon receipt of the voltage from the power supply, the regulator may scale the voltage, or may utilize the

voltage without scaling. For example, in some embodiments the regulator may scale the voltage received from the power supply (e.g., to a scaled voltage approximately one-half of the voltage received from the power supply) through the use of a voltage divider.

[0033] At step 620, a voltage based on the voltage received from the power supply (e.g., the voltage received from the power supply or the scaled voltage) may be transmitted to a plurality of amplifiers (e.g., the operational transconductance amplifiers 210A, 210B, or 210C) to cause the amplifiers to output a current based on the scaled voltage. The amplifiers may be low-gain amplifiers (e.g., configured according to a unity gain configuration) and may be configured to operate in accordance with class B transfer function characteristics, as discussed above. The amplifiers may further receive a second voltage (e.g., a feedback voltage such that the scaled voltage and the feedback voltage for a differential input voltage comprise a differential input voltage that may be received by each respective amplifier at differential input ports) from, for example, an output of each respective amplifier. A coupling between the output an input of each respective amplifier may comprise a feedback path or feedback loop.

[0034] At step 630, the amplifiers generate an output current based on the voltage received from the power supply and, optionally, the second voltage. The output current may be determined, for example, according to a desired load current of a load to which the regulator may be coupled. The amplifiers may load share the load current such that each of the amplifiers provides an approximately equal portion of the output current of the regulator. For example, when the regulator includes three amplifiers, each amplifier may provide approximately one-third of the output current when the regulator is operating normally. As another example, when the regulator includes four amplifiers, each amplifier may provide approximately one-fourth of the output current when the regulator is operating normally.

[0035] At step 640, one of the amplifiers of the regulator experiences an upset event that alters or affects an output of the effected amplifier. The upset event may be, for example, an ionizing radiation particle strike that alters operation of the effected amplifier. For example, the upset event may introduce an additional amount of current into an output of the effected amplifier (e.g., as may be represented or understood as an additional current source coupled across the output of the effected amplifier). In some embodiments, the additional amount of current may dissipate over a period of time and have limited to no effect on normal operations of the regulator. In other embodiments, the upset event and/or the additional amount of current may

render the effected amplifier inoperable or inhibit the effected amplifier from outputting sufficient current to approximately equally participate in load sharing with a remainder of the amplifiers that may be unaffected by the upset event.

[0036] At step 650, when the effected amplifier is inoperable or otherwise unable to output sufficient current to approximately equally participate in load sharing, the unaffected amplifiers (e.g., a subset of all amplifiers in the regulator that is fewer in number than a total number of amplifiers in the regulator) may compensate for the effected amplifier by performing load sharing between the unaffected amplifiers. When the unaffected amplifiers compensate for the loss of the effected amplifiers, the unaffected amplifiers may output a greater amount of current to contribute to the output of the regulator that the unaffected amplifiers output before the upset event occurring at step 540.

[0037] Although the above steps of method 600 have been discussed in the context of generating an output current for servicing a load (e.g., sourcing current), the disclosed techniques may be equally adaptable to sinking current from the load, and embodiments of both usage scenarios are within the scope of this disclosure.

[0038] Different companies may refer to a component by different names. Also, the term “couple” or “couples” is intended to mean either an indirect or direct wired or wireless connection. Thus, if a first device couples to a second device, that connection may be through a direct connection or through an indirect connection via other devices and connections. Unless otherwise stated, “approximately” means +/- 10 percent of the stated value.

[0039] Modifications are possible in the described embodiments, and other embodiments are possible, within the scope of the claims.

CLAIMS

What is claimed is:

1. A fault tolerant voltage regulator comprising:
a plurality of operational transconductance amplifiers configured according to a unity-gain configuration and to couple in parallel to a load, wherein the operational transconductance amplifiers are configured to load share a load current associated with the load approximately equally among the operational transconductance amplifiers.
2. The fault tolerant voltage regulator of claim 1, wherein an output of each of the operational transconductance amplifiers is coupled to a common output node, and wherein a negative input of each of the operational transconductance amplifiers is coupled to the common output node.
3. The fault tolerant voltage regulator of claim 2, wherein the load comprises a termination resistor coupled between the output node and a communication line coupled between a processing circuit and a memory circuit.
4. The fault tolerant voltage regulator of claim 1, wherein each of the operational transconductance amplifiers is further configured to generate an output characteristic of a class B transfer function.
5. The fault tolerant voltage regulator of claim 1, where a positive input of each of the operational transconductance amplifiers is coupled to a common input node, and wherein the common input node is an output of a voltage divider.
6. The fault tolerant voltage regulator of claim 1, wherein the load current is distributed approximately equally among a remainder of the operational transconductance amplifiers when one or more of the operational transconductance amplifiers is incapable of sharing the load current associated with the load approximately equally.
7. The fault tolerant voltage regulator of claim 1, wherein a first of the operational transconductance amplifiers is coupled to a first current source configured to bias the first of the operational transconductance amplifiers, and wherein the first current source is independent of a second current source coupled to a second of the operational transconductance amplifiers and configured to bias the second of the operational transconductance amplifiers.
8. A fault tolerant voltage regulator comprising:
a first operational transconductance amplifier;
a second operational transconductance amplifier coupled in parallel with the first

operational transconductance amplifier; and

a third operational transconductance amplifier coupled in parallel with the first operational transconductance amplifier and the second operational transconductance amplifier,

wherein each of the first operational transconductance amplifier, the second operational transconductance amplifier and the third operational transconductance amplifier is configured to couple to a load and comprises an input stage that comprises a plurality of metal oxide semiconductor field effect transistors (MOSFETs), and

wherein the MOSFETs are configured to operate in accordance with a class B transfer function to approximately equally share a load current associated with the load.

9. The fault tolerant voltage regulator of claim 8, wherein the second operational transconductance amplifier and the third operational transconductance amplifier are configured to load share the load current of the load approximately equally when the first operational transconductance amplifier fails.

10. The fault tolerant voltage regulator of claim 8, wherein the load is a double data rate (DDR) termination resistor.

11. The fault tolerant voltage regulator of claim 8, wherein a transconductance value of each of the first operational transconductance amplifier, the second operational transconductance amplifier and the third operational transconductance amplifier is approximately equally.

12. The fault tolerant voltage regulator of claim 8, wherein each of the first operational transconductance amplifier, the second operational transconductance amplifier and the third operational transconductance amplifier is independently biased by a bias current.

13. The fault tolerant voltage regulator of claim 8, wherein each of the first operational transconductance amplifier, the second operational transconductance amplifier and the third operational transconductance amplifier is configured according to a unity gain configuration.

14. The fault tolerant voltage regulator of claim 8, wherein an output voltage of the fault tolerant voltage regulator is within an approximately 80 millivolt (mV) range that is approximately centered on an optimal output of the fault tolerant voltage regulator.

15. The fault tolerant voltage regulator of claim 14, wherein the output voltage of the fault tolerant voltage regulator is within an approximately 50 mV range that is approximately centered on the optimal output of the fault tolerant voltage regulator.

16. A method of sourcing or sinking a load current of a load, comprising:
- receiving a voltage from a power supply, the voltage based on a voltage provided by the power supply to the load;
 - transmitting a voltage based on the voltage received from the power supply to a plurality of amplifiers, the amplifiers configured as low-gain amplifiers operating in accordance with class B transfer function characteristics;
 - generating, by the amplifiers, an output current based on the voltage received from the power supply, wherein each of the amplifiers contributes approximately equally to the output current; and
 - generating, by a plurality of unaffected amplifiers, the output current based on the voltage received from the power supply when one of the amplifiers experiences an upset event, wherein the unaffected amplifiers is a subset of less than all of the plurality of amplifiers, and wherein each of the unaffected amplifiers contributes approximately equally to the output current.
17. The method of claim 16, wherein the upset event is an ionizing radiation particle strike that renders the one of the amplifiers that experiences the upset event incapable of contributing approximately equally to the output current.
18. The method of claim 16, wherein a contribution to the output current of each of the unaffected amplifiers is greater after the upset event than a contribution to the output current of each of the unaffected amplifiers before the upset event.
19. The method of claim 16, wherein the voltage based on the voltage received from the power supply is an output of a voltage divider that scales the voltage received from the power supply.
20. The method of claim 16, wherein the load is a double data rate (DDR) memory communication line termination resistor.

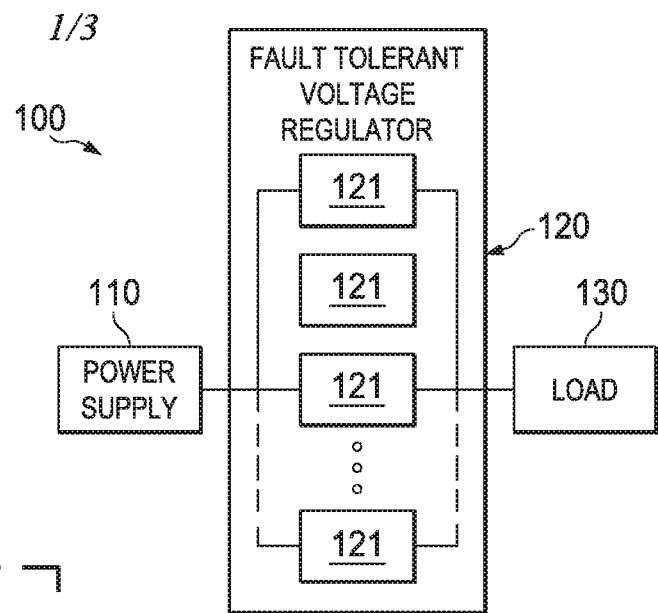


FIG. 1

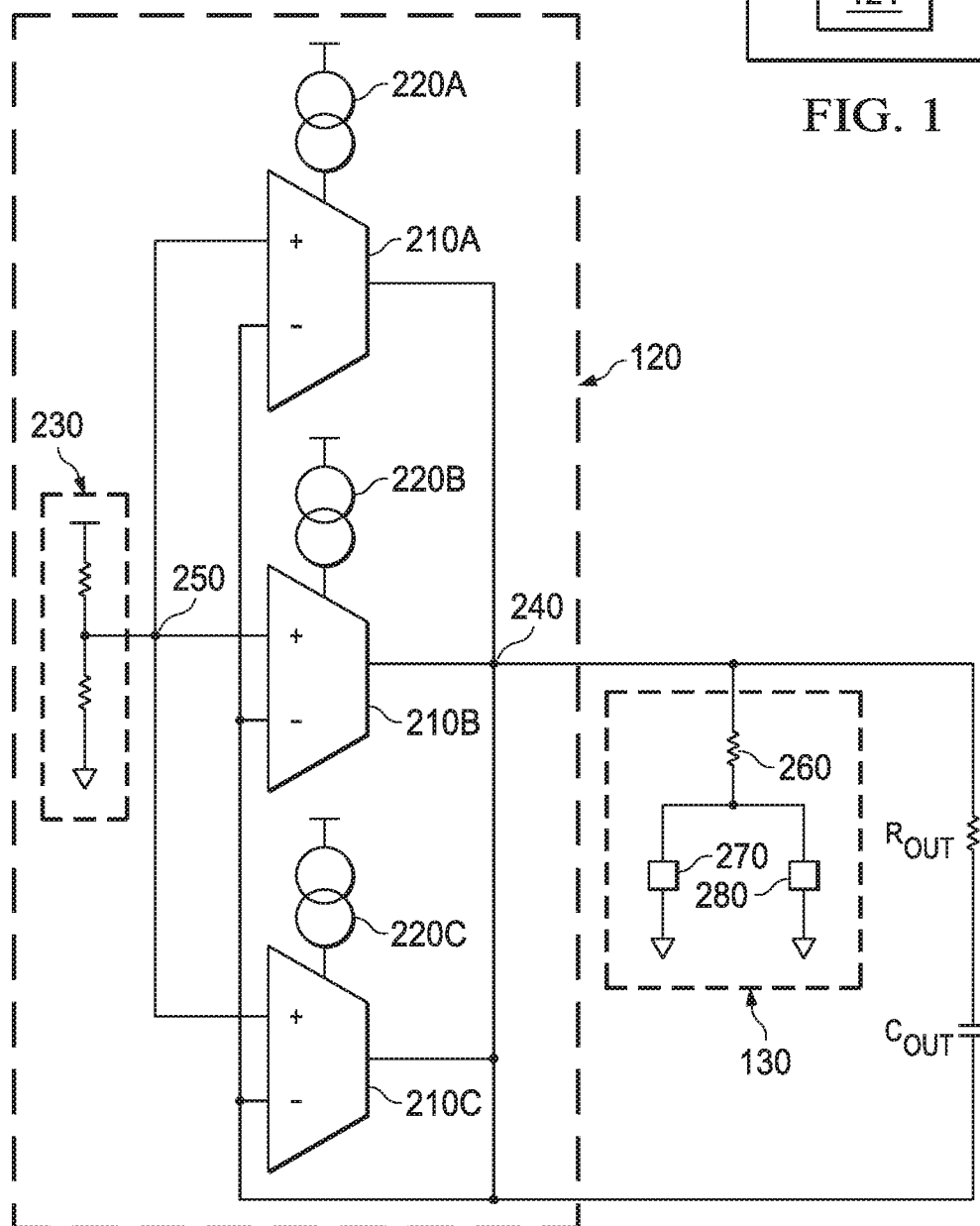
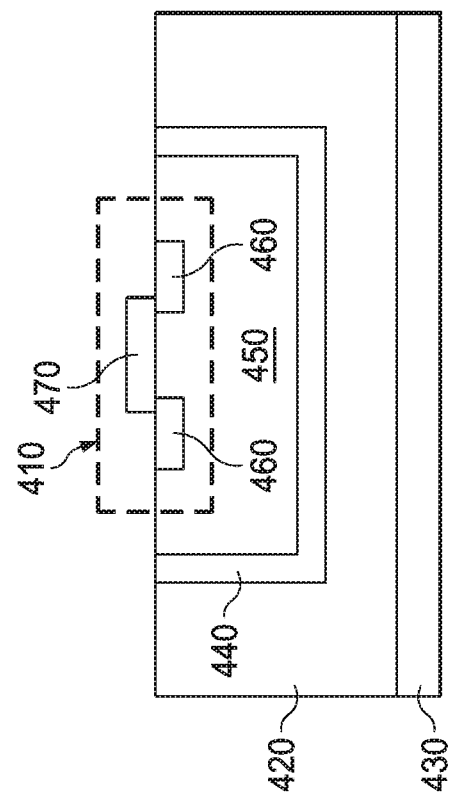
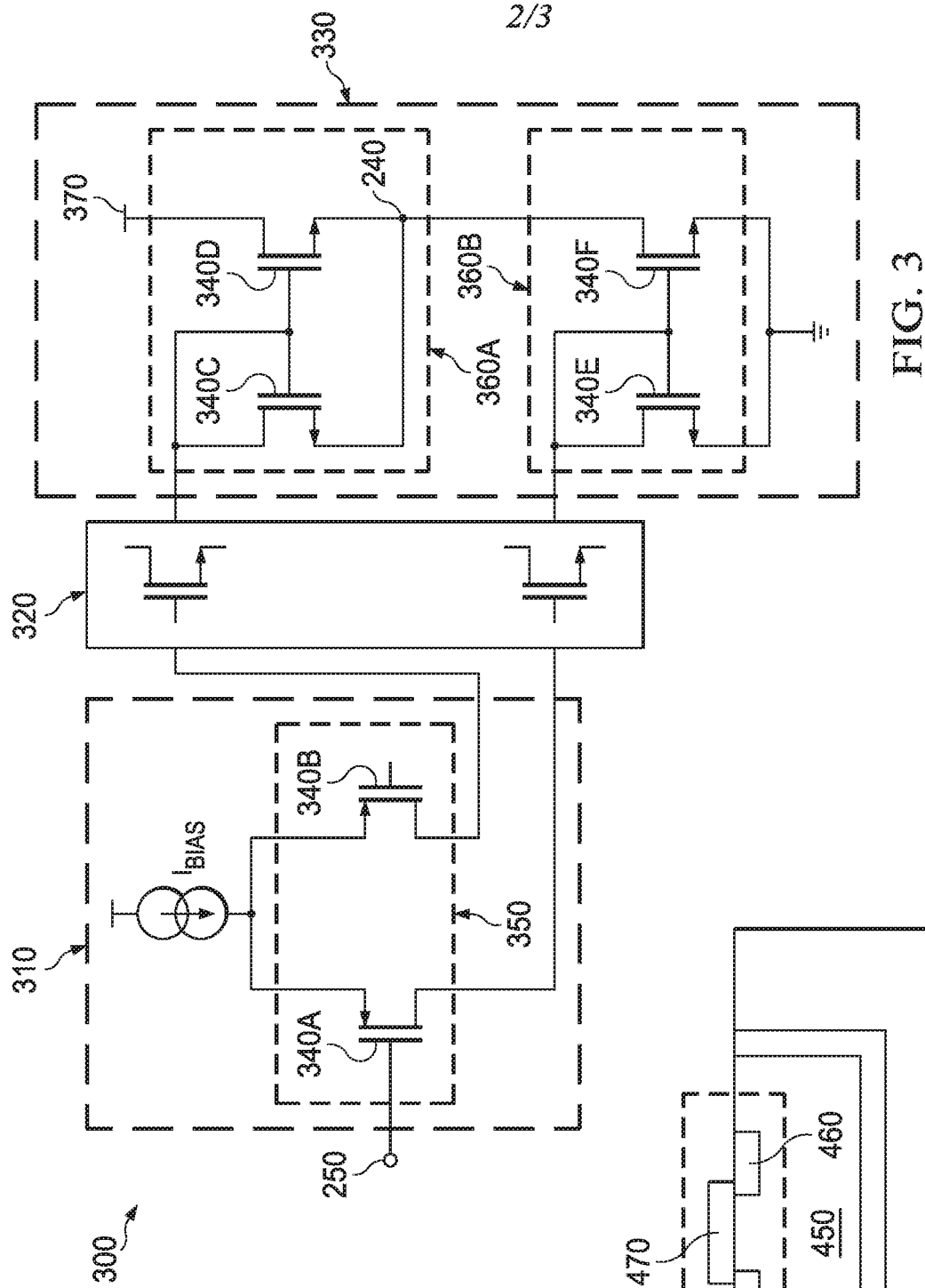


FIG. 2



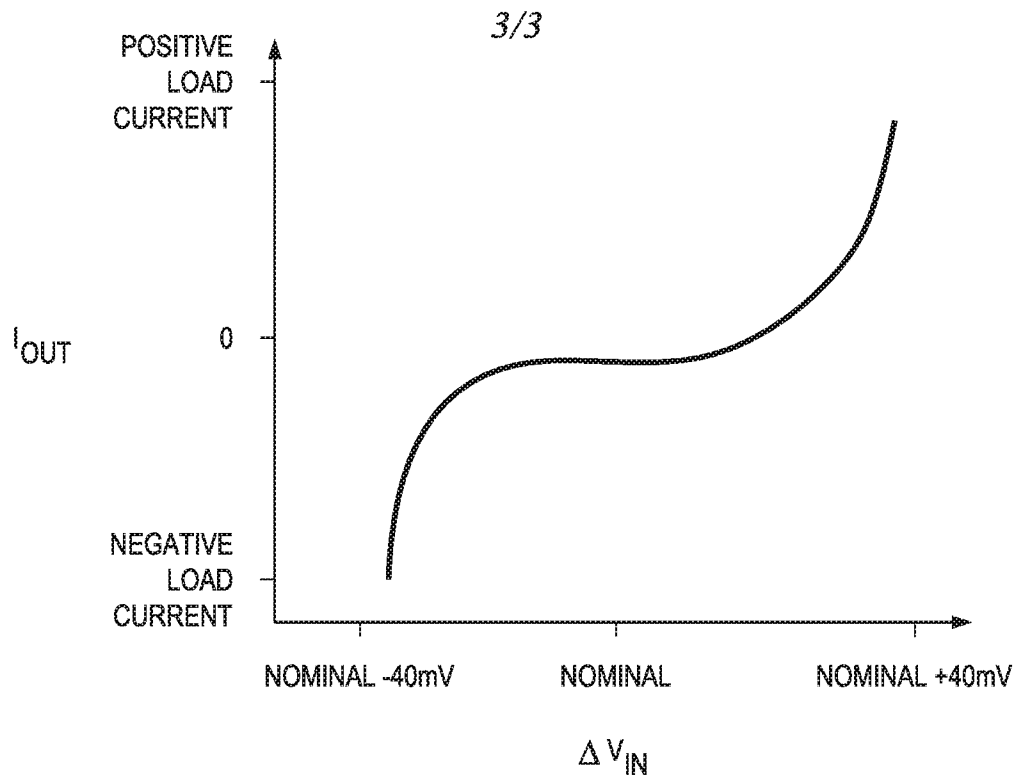


FIG. 5

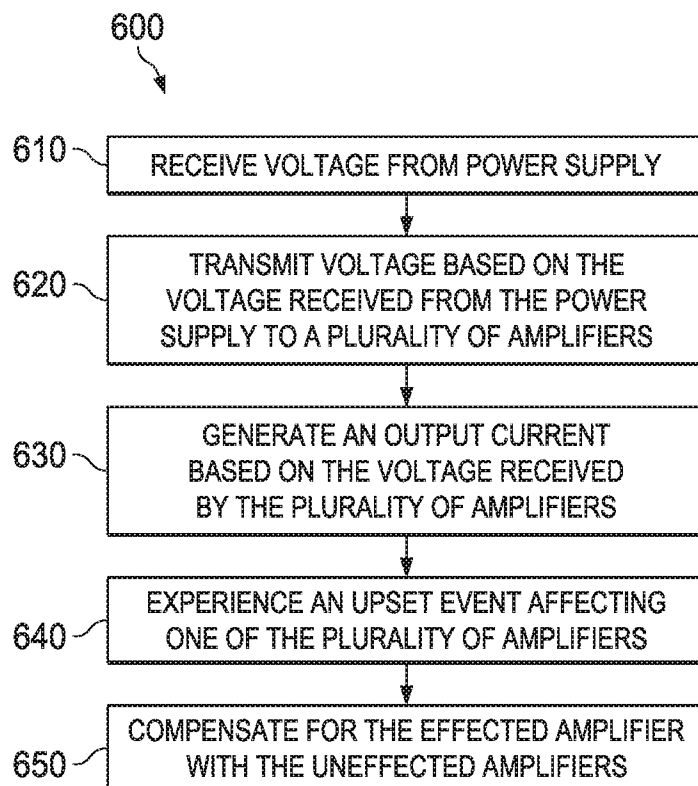


FIG. 6

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 2016/053778

A. CLASSIFICATION OF SUBJECT MATTER		
G05F 3/02 (2006.01) H03F 3/20 (2006.01) According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED		
Minimum documentation searched (classification system followed by classification symbols)		
G05F 1/00, 1/10, 1/46, 3/00, 3/02, H02M 3/00-3/158, H03F 3/00, 3/20, 3/21, 3/217, 3/45, H03B 1/00, G06F 1/00, 1/26, 1/32		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched		
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)		
PAJ, Espacenet, USPTO DB, Information Retrieval System of FIPS		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 4920309 A (NATIONAL SEMICONDUCTOR CORPORATION) 24.04.1990, abstract, claim 1, col. 1, line 28 - col. 2, line 29, col. 3, line 46 - col. 5, line 28, fig. 2, 4	1-3, 5, 7
Y		8, 10-15
A		4, 6, 9, 16-20
Y	US 7187233 B1 (JOSEPH NORMAN BERRY) 06.03.2007, col. 4, lines 41-57, fig. 1	8, 10-15
Y	US 2002/0144166 A1 (NAI-SHUNG CHANG et al.) 03.10.2002, abstract	10
A	US 7091785 B2 (MICROCHIP TECHNOLOGY INC.) 15.08.2006	1-20
A	US 2009/0224829 A1 (MICRON TECHNOLOGY, INC.) 10.09.2009	1-20
☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.		
* Special categories of cited documents:	"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art "&" document member of the same patent family	
"A" document defining the general state of the art which is not considered to be of particular relevance		
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"O" document referring to an oral disclosure, use, exhibition or other means		
"P" document published prior to the international filing date but later than the priority date claimed		
Date of the actual completion of the international search	Date of mailing of the international search report	
20 October 2016 (20.10.2016)	10 November 2016 (10.11.2016)	
Name and mailing address of the ISA/RU: Federal Institute of Industrial Property, Berezhkovskaya nab., 30-1, Moscow, G-59, GSP-3, Russia, 125993 Facsimile No: (8-495) 531-63-18, (8-499) 243-33-37	Authorized officer P. Volkov Telephone No. (495)531-64-81	