(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
13 February 2003 (13.02.2003)

PCT

(10) International Publication Number
WO 03/011747 A1

(51) International Patent Classification[7]: B81B 3/00, G01F 1/684, H05B 1/00

(21) International Application Number: PCT/GR02/00008

(22) International Filing Date: 18 February 2002 (18.02.2002)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
20010100378 31 July 2001 (31.07.2001) GR

(71) Applicant *(for all designated States except US)*: **NCSR "DEMOKRITOS"** [GR/GR]; Institute of Microelectronics, P.O. Box 60228, GR-153 10 Aghia Paraskevi, Athens (GR).

(71) Applicants and
(72) Inventors: **TSAMIS, Christos** [GR/GR]; NCSR "Demokritos", Institute of Microelectronics, P.O. Box 60228, GR-153 10 Aghia Paraskevi, Athens (GR). **TSEREPI, Angeliki** [GR/GR]; NCSR "Demokritos", Institute of Microelectronics, P.O. Box 60228, GR-153 10 Aghia Paraskevi, Athens (GR). **NASSIOPOULOU, Androula, G.** [GR/GR]; NCSR "Demokritos", Institute of Microelectronics, P.O. Box 60228, GR-153 10 Aghia Paraskevi, Athens (GR).

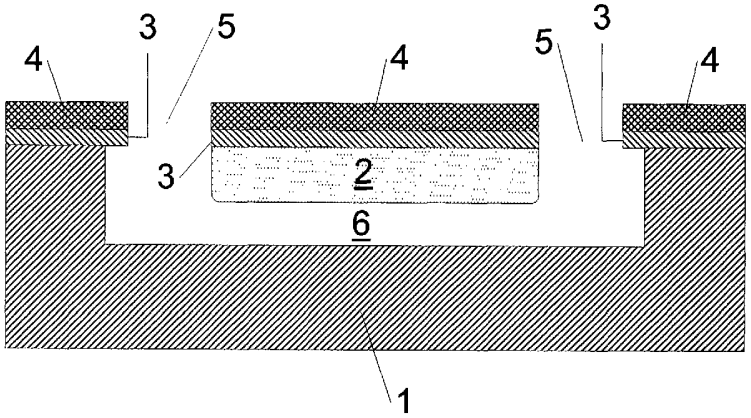
(74) Common Representative: **TSAMIS, Christos**; NCSR "Demokritos", Institute of Microelectronics, P.O. Box 60228, GR-153 10 Aghia Paraskevi, Athens (GR).

(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZM, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR,

[Continued on next page]

(54) Title: METHOD FOR THE FABRICATION OF SUSPENDED POROUS SILICON MICROSTRUCTURES AND APPLICATION IN GAS SENSORS



(57) Abstract: This invention provides a front-side silicon micromachining process for the fabrication of suspended Porous Silicon membranes in the form of bridges or cantilevers and of thermal sensor devices employing these membranes. The fabrication of the suspended Porous Silicon membranes comprises the following steps: (a) formation of a Porous Silicon layer (2) in, at least one, predefined area of a Silicon substrate (1), (b) definition of etch windows (5) around or inside said Porous Silicon layer (2) using standard photolithography and (c) selective etching of the Silicon substrate (1), underneath the Porous Silicon layer (2), by using dry etching techniques to provide release of the Porous Silicon membrane and to form a cavity (6) under the said Porous Silicon layer. Furthermore, the present invention provides a method for the fabrication of thermal sensors based on Porous Silicon membranes with minimal thermal losses, since the proposed methodology combines the advantages that result from the low thermal conductivity of Porous Silicon and the use of suspended membranes. Moreover, the front-side micromachining process proposed in the present invention simplifies the fabrication process. Various types of thermal sensor devices, such as calorimetric-type gas sensors, conductometric-type gas sensors and thermal conductivity sensors are described utilizing the proposed methodology.

WO 03/011747 A1

GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declaration under Rule 4.17:

— *of inventorship (Rule 4.17(iv)) for US only*

Published:

— *with international search report*

— *with amended claims*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

Title : METHOD FOR THE FABRICATION OF SUSPENDED POROUS SILICON MICROSTRUCTURES AND APPLICATION IN GAS SENSORS.

DESCRIPTION OF THE INVENTION

Field of the Invention

This invention relates to a method of fabricating suspended porous silicon membranes and to devices made employing this method.

Description of the related art

For the fabrication of micromachined gas sensors, a lot of effort has focused on the development of methodologies for the formation of membranes used as support for the heater. In particular, two different structures have been utilized (Simon et al., Sensor and Actuator B 73, p.1, 2001): The closed-type membrane, where the membrane overlaps the silicon substrate along its periphery and the suspended-type membrane (also called spider-type and micro hot-plate). In the latter, the membrane element is connected to the Si substrate by means of supporting beams, and the central portion of the membrane is suspended over a cavity that is etched in the substrate.

The closed-type membrane is formed by means of anisotropic (crystallographic) etching of silicon from the back side of the wafer. Wet etchants like KOH and EDP are typically used. Appropriate etch stops for these etchants are silicon nitride, silicon oxide or Boron- doped silicon. For the formation of the membrane, two different techniques have been utilized. The first, which is more popular, uses silicon oxide and/or silicon nitride as membrane and insulation materials to obtain membranes of typical thickness between 1 and 2 μm [(a) G. Sberveglieri et al. Microsyst. Technolog., p.183, 1997, (b) J. Gardner, Sens. Actuators B 26/27, p. 135, 1995 and (c) D. Lee, Sens. Actuators B 49, p.147, 1996]. The second method, which has been applied recently, uses nitrided porous silicon of thickness between 25 and 30 μm (Maccagnani et al., Proceed. of the 13th European Conference on Solid-State Transducers, The Netherlands 1999) that can be obtained by silicon anodization and subsequent nitridation. Silicon oxide, silicon nitride and nitrided porous silicon all possess low thermal conductivities and can provide good thermal isolation between the heated active area and the membrane rim.

On the other hand, the suspended-type membrane is completely processed from the front-side. Therefore, the suspended membrane is often said to be more compatible with CMOS processing (Gaitan et al., US Patent. 5,464,966). The suspended membrane is either formed by anisotropic wet etching with KOH or EDP from the front side or by sacrificial etching of oxide layers. Sacrificial etching of porous silicon is another possibility to obtain suspended membranes (Nassiopoulou et al., Patent No PCT/GR/00040, published by WIPO 12/11/1998, Greek Patent OBI 1003010). Suspended polycrystalline and monocrystalline membranes have been fabricated using this technique by Kaltsas and Nassiopoulou [(α) G. Kaltsas and A.G. Nassiopoulou, Mat. Res. Soc. Symp. Proc., 459, p. 249, 1997, (β) G. Kaltsas and A. G. Nassiopoulou, Sens. Actuators: A65, p.175, 1998] and suspended nitride membranes by Gardeniers et al (J. G. E. Gardeniers et al., Sens. Actuators A60, p. 235, 1997). The typical lateral dimensions of suspended membranes range between 100 and 200 μm.

The use of suspended membranes is generally preferred compared to the closed-type

membranes. The reason is that the thermal losses from the suspended-type membrane are minimized, since they occur only through the supporting beams of the membrane, compared to the closed membrane where thermal losses occur along its periphery.

Highly porous silicon (with porosity ~65%) has very good thermal properties similarly to silicon oxide. In sensor applications, it has been used in two ways: as a material for local thermal isolation on a silicon substrate [(a) Nassiopoulou et al., Patent No PCT/GR/00040, published by WIPO 12/11/1998, Greek Patent OBI 1003010, (b) G. Kaltsas and A.G Nassiopoulou, Sens. Actuators A 76, p. 133, 1999] and as sacrificial layer for the formation of suspended membranes. Recently, nitrided porous silicon membranes were fabricated using backside etching. Maccagnani et al. (Maccagnani Proc. of the 13th European Conference on Solid-State Transducers, The Netherlands, 1999) fabricated closed-type, nitrided porous silicon membrane, by using backside etch with KOH. The disadvantages of the proposed method are the need for double-side alignment before the bulk silicon etching from the back side and the need for more space due to the sloped side-walls (lateral dimension needed to form a membrane is larger by 40%). Plasma etching techniques like high aspect ratio silicon etching which is capable of forming vertical walls might therefore be an alternative to wet etching, allowing for a higher number density of sensors on a wafer compared to wet etching techniques. An alternative process for the fabrication of closed type membranes using front side micromachining technique is proposed by Baratto et al. (C. Baratto, Thin Solid Films, p. 261, 2001), based on the electropolishing of the silicon substrate after the formation of the porous silicon layer in order to form a cavity beneath the porous silicon. However in the case of closed type membranes, the thermal losses due to the membrane support area are increased compared to suspended membranes which have reduced contact area with the substrate, as stated previously [(a) G. Kaltsas and A.G. Nassiopoulou, Mat. Res. Soc. Symp. Proc., 459, p. 249, 1997, (b) J. G. E. Gardeniers et al., Sens. Actuators A60, p. 235, 1997].

Bulk silicon micromachining by plasma etching has been successfully used for the release of lightly doped Si structures overlaying a buried heavily doped n^+ layer. The method is based on the high lateral etching rate of the n^+ layer in contrast to the anisotropic etching of lightly doped Si in Cl_2/BCl_3 plasmas (Y.X. Li, *et. al.*, Sensors and Actuators A57, p. 223, 1996). However, due to the relatively slow lateral etching of heavily doped n^+ layer and the relatively small selectivity of the process with respect to masking material (PECVD oxide layer), the lateral dimension of the released structure was limited to about 4 μm. In addition, a combination of high aspect ratio anisotropic and isotropic etching in F-based plasmas has been employed for the release of free-standing microcantilevers and bridges from multi-layer substrates (Si-SiO_2-polySi-SiO_2-Si sandwiched wafers) (C. Cui et al., Sensors and Actuators A70, p.61, 1998). In this case, the released structures remain intact from the isotropic etching process, as they are protected by SiO_2 layers or fluorocarbon plasma deposited layers. Although this method offers the possibility of fabrication and release of high aspect ratio microstructures, it is based on the complicated process of fabrication of multi-layer substrates. Generally speaking, the release of single-crystal silicon structures from the substrate through the front side of the wafer can be achieved by means of a combined directional and isotropic silicon dry etch if the structures are protected on the sides by a Si-etching selective mask such as for example SiO_2 (F. Ayazi, et. al. JMEMS 9(3), p. 288, 2000). In the present invention, the released structure is made of porous Si, which simplifies extremely the process : The high selectivity of the used isotropic Si etching process with

respect to porous Si makes unnecessary any protection of the structure to be released.

Summary of the invention

It is an object of this invention to provide a method of fabricating suspended porous silicon membranes in the form of bridges or cantilevers, based on front side micromachining by means of dry etching techniques for the membrane release.
It is yet another object of this invention to provide a method for the fabrication of gas sensors, using suspended porous silicon membranes.
It is yet another object of this invention to provide a method for the fabrication of thermal conductivity sensors, using a heater on top of suspended porous silicon membranes.
The methodology that is described in the present invention gives the ability to utilize membranes for thermal sensors that combine two major innovations:

a) The ability to fabricate suspended Porous Silicon membranes, in the form of bridges or cantilevers, with good mechanical strength (compared to SiO_2 or Si_3N_4 membranes) and minimal thermal losses compared to the closed-type membranes.
b) The use of front side micromachining techniques for the fabrication of the suspended porous silicon structures with maximum device density.

Brief description of drawings

Figs. 1A through 1C are cross sectional schematic drawings illustrating the method for the fabrication of suspended Porous Silicon Membranes.

Figs. 2A to 2C are plan view schematic drawings of various Porous Silicon membranes.

Figs. 3A through 3C are cross sectional schematic drawings illustrating the process for the fabrication of a calorimetric type gas sensor, using a heater and/or a resistor as a thermal sensing element.

Fig. 4 Plan view schematic of a calorimetric type sensor.

Figs. 5A through 5C are cross sectional schematic drawings illustrating the process for the fabrication of a conductometric type gas sensor

Fig 6 is cross sectional schematic drawings illustrating a thermal conductivity sensor.

Description of the preferred embodiments

Figs. 1A through 1C are schematic drawings illustrating the fabrication process of suspended Porous Silicon membranes. As the base material (1), doped monocrystalline or polycrystalline silicon is used. The dopant concentration in the substrate can be either n type or p type with concentrations greater that $10^{14}cm^{-2}$. Porous silicon (2) is formed in predefined areas of the said substrate. Various masking techniques have been used for the local formation of porous silicon. These techniques include deposition and patterning of various layers such as Si_3N_4, SiO_2, SiGe, SiC, polycrystalline silicon and

combination of them as well as ion implantation techniques. The masking material or method for the local patterning of porous silicon is not a limiting factor for the method described in this invention.

Fig. 1A shows the substrate (1) and the defined Porous Silicon area (2). The mask for the local formation of Porous Silicon (not shown in figure 1A), may consist of a silicon dioxide layer and a polysilicon layer, according to one of the embodiments of the present invention. After the formation of the porous silicon areas, an insulating layer (3) is deposited on top of porous silicon (Fig 1B). The insulating layer (3) can be SiO_2, or Si_3N_4 or any combination of them. Subsequently, photoresist (4) is deposited on top of the wafer and etch windows (5) are opened using standard photolithography techniques. Depending on the design and the geometrical characteristics of the Porous Silicon membrane (2), the etch windows (5) are placed at the periphery of the porous silicon membrane (2) or at predefined places inside the membrane (Fig 1B). The removal of the insulating layers (3) and the mask, that is used for the local formation of porous silicon (2) can be achieved either by wet or dry etching techniques. Then the etch windows (5) extend down to the silicon substrate (1) adjacent to the porous silicon membrane (2). At this point, the silicon material from underneath the porous structure is removed by a combination of anisotropic / isotropic dry etching processes. Experiments that have been performed by the inventors showed that the etching rate of thermally treated porous silicon is about 100 times slower compared to the etching rate of silicon substrate for anisotropic and even slower for isotropic etching. For this reason the porous membrane remains virtually unaffected during the lateral plasma etching of the silicon substrate. Fig. 1C shows a cross section schematic of the released Porous Silicon membrane where the cavity (6) formed under the porous silicon (2) is shown. Figs. 2A to Fig 2C show various top view designs of suspended Porous Silicon structures, where we can see the silicon substrate (1), the porous silicon membrane (2) and the porous silicon supporting beams (7). The membrane is suspended over the cavity (6).

One of the key parameters for the successful implementation of the methodology that is described in the present invention is the optimization of dry etching conditions. Various processes can be used provided that the etching conditions are selected in such a way that the process is highly selective to silicon etching compared to Porous Silicon etching. For example, an F-rich gas as sulfur hexafluoride is used which has a flow of between 100-300 sccm and a processing pressure between 1 and 10 Pa. The plasma generation preferably takes place with a high frequency supply (13.56 MHz) at outputs between 500 W and 2000 W. At the same time, a low substrate voltage for ion acceleration is supplied to the substrate electrode. The substrate voltage is preferably between 30 and 60 V.

One of the phenomena that is observed during dry etching, is that the etch rate depends on the dimensions of the etch windows. This phenomenon has been observed in the past in high aspect ratio Si etching and is known as RIE lag. Experiments that were performed by the inventors demonstrated that this influence exists also for lateral etching of Si. However this influence of the dimension of the etch window on the Si etch rate does not impose any constraints on the method that is described in the present invention. On the contrary, by carefully designing the position and the dimensions of the etch windows, it is possible to benefit from this dependence and release selectively suspended microstructures of certain shapes, and sizes.

Another key parameter for the successful implementation of the proposed methodology is the optimization of mechanical properties of the characteristics of the Porous Silicon

layer. It is obvious that the structural characteristics of the Porous Silicon membranes (porosity, thickness, pore size) and the subsequent thermal treatment have to be optimized according to the design and geometrical characteristics of the layer. With the aid of the methodology proposed in the present invention, suspended Porous Silicon membranes have been formed with thickness ranging from few nm to several micrometers and with size up to several millimeters.

In another embodiment of the present invention, a calorimetric type gas sensor is fabricated. In that case, after the local formation of the Porous Silicon areas (2) an insulating layer (3) is deposited, as shown in Fig. 3A. The insulating layer can be either SiO_2, or Si_3N_4 or any combination of them. However, it is desirable to use an insulating material with very low thermal conductivity. A heater (8) is formed on top of the said insulating layer (3) (Fig. 3A). The heater is made either of doped polycrystalline silicon or any conducting layer or layer combination, as for example Pt/Ti. An insulating layer 9 is then deposited on top of the heater (8) (Fig. 3B). The deposition method of the said insulating layer (9) depends on the nature of the heater. For example if the heater is made from polycrystalline silicon, the insulating layer can be SiO_2 deposited by LPCVD or LTO techniques. A catalytic layer (10) is then deposited on top of the said insulating layer (9) (Fig. 3B). For the particular embodiment described, the selection of the catalytic material can be made over a vast range of materials, such as Pt, Pd for example. The choice of the catalytic material will depend on the properties of the gas to be detected. The only limitation for the catalytic material, according to the methodology described in the present invention, is to remain unaffected by the processes that follow, and particularly by the removal of the photoresist, which can be performed either by using wet techniques (for example by exposure to organic solvents such as acetone) or dry etching techniques (for example O_2 plasma). The patterning of the catalytic layer can be achieved either by the lift-off technique or by standard photolithography techniques combined with wet etching, if needed. The temperature change from the heat that is generated or absorbed from the catalytic reaction of the gases on the surface of the catalytic layer (10) can be detected, either by the heated resistor (8) or by a second resistor, a sensing resistor, that is implemented in the device (not shown on Fig. 3). Alternatively, integrated thermopiles can be used to detect the temperature changes due to the catalytic reaction.

After the deposition and patterning of the said catalytic material (10), photoresist (4) is deposited on top of the wafer and etch windows (5) are opened using standard photolithography techniques, as shown in Fig. 3C. The release of the Porous Silicon membrane is performed as described previously. Fig. 3C shows a cross section schematic drawing of the gas sensor, where we can see the cavity (6) that is formed under the porous silicon (2). Fig. 4 shows a plan view drawing of the device, where we can see the silicon substrate (1), the porous silicon membrane (2), the porous silicon supporting beams (7) and an indicative design of the heater (8).

In another embodiment of the present invention, a conductometric type gas sensor is fabricated. The fabrication process for the formation of the porous silicon area (2) and the heater (8) is similar to the process described above (Fig 5A). After the deposition of the isolation layer (9) on top of the heater, conductive electrodes (11) are deposited and patterned (Fig. 5B). The catalytic material (10) is deposited on top of the electrodes (Fig. 5B). The choice of the catalytic material depends on the gas to be detected and can be selected by a large range of materials (SnO_2 for example) or any material whose electrical characteristics depend on the ambient gas. The release of the porous silicon

membrane is performed in the way described previously. Fig. 5C shows a cross sectional schematic drawing of the gas sensor after the release of the porous silicon membrane, where we can see the cavity (6) formed under the porous silicon membrane (2).

In another embodiment of the present invention, a thermal conductivity sensor can be formed by depositing a Pt resistor (12) on top of a Porous Silicon membrane (2) suspended over the cavity (6), as illustrated in Fig. 6. An insulating layer (3) may exist between the resistor and the Porous Silicon membrane (2). The dimensions of the suspended porous silicon membrane (2) can be changed in order to modulate the response time of the sensor.

Although the description we have provided up to now has focused on the release of porous silicon membranes, it is possible to use the method described in this invention for the release of suspended membranes that are made of silicon oxide, nitride or any stack of these materials, due to the high selectivity of dry etching of Si with respect to SiO_2/Si_3N_4. With a slightly modified fabrication process, polycrystalline silicon membranes can be also released.

The present invention has been described in terms of a number of preferred embodiments. The invention is not limited to the embodiments depicted and described. The scope of the invention is defined by the appended claims.

Claims

What is claimed is:

1. A front-side silicon micromachining process for the fabrication of suspended Porous Silicon membranes in the form of bridges or cantilevers, comprising the following steps : (a) Formation of a Porous Silicon layer in, at least one, predefined area of a Silicon substrate, (b) Definition of etch windows around or inside said Porous Silicon area using standard photolithography, (c) Selective etching of the Silicon substrate, underneath the Porous Silicon layer, by using dry etching techniques to provide release of the Porous Silicon membrane and to form a cavity under the said Porous Silicon layer.

2. The front side silicon micromachining process of claim **1** for the fabrication of suspended Porous Silicon membranes in the form of bridges or cantilevers, further comprising the formation of a patterned conductive layer on top of said porous silicon membrane. The said patterned conductive layer is used as a heater for the fabrication of thermal sensor devices.

3. The use of the patterned conductive layer on porous silicon membrane of claim **2** as a heater for the fabrication of thermal sensors, such as gas or thermal conductivity sensors.

4. A gas sensor device comprising: (a) a silicon substrate with at least one Porous Silicon area, (b) a suspended membrane of said Porous Silicon area, in the form of a bridge or cantilever, said suspended membrane of porous silicon fabricated by the front-side dry etching of said silicon substrate (c) a patterned conductive layer on said suspended membrane (d) an insulating layer on top of said conductive layer (e) a catalytic material on top of said insulating layer (f) a thermal sensing element to sense the temperature change due to the reaction of the ambient gas with the catalytic material.

5. The gas sensor of claim **4** wherein said thermal sensing element is a Pt resistor.

6. The gas sensor device of claim **4** wherein said thermal sensing element consists of a number of thermocouples, one contact of said thermocouples being on the suspended porous silicon membrane, the other contact being on bulk silicon.

7. A gas sensor device comprising : (a) a silicon substrate with at least one Porous Silicon area, (b) a suspended membrane of said Porous Silicon area, in the form of a bridge or cantilever, said suspended membrane of porous silicon fabricated by the front-side dry etching of said silicon substrate (c) a patterned conductive layer on said suspended membrane (d) an insulating layer on top of said conductive layer (e) metal electrodes on top of said insulating layer and (f) a catalytic material on top of said electrodes, the resistivity of the said catalytic material being dependent on the ambient gas.

8. A thermal conductivity sensor comprising: (a) a silicon substrate with at least one Porous Silicon area, (b) a suspended membrane of said Porous Silicon area, in the

form of a bridge or cantilever, said suspended membrane of porous silicon fabricated by the front-side dry etching of said silicon substrate (c) a patterned conductive layer on said suspended membrane, where said patterned conductive layer is a Pt resistor. The dimensions of the said porous silicon membrane can be changed in order to modulate the response time of the sensor.

AMENDED CLAIMS

[Received by the International Bureau on 29 November 2002 (29.11.02): original claims 1, 2, 5, 6 are unchanged, Claim 3 is cancelled and Claims 4, 7 and 8 are replaced by amended claims claims bearing the same numbers (2 pages)]

1. A front-side silicon micromachining process for the fabrication of suspended Porous Silicon membranes in the form of bridges or cantilevers, comprising the following steps : (a) Formation of a Porous Silicon layer in, at least one, predefined area of a Silicon substrate, (b) Definition of etch windows around or inside said Porous Silicon area using standard photolithography, (c) Selective etching of the Silicon substrate, underneath the Porous Silicon layer, by using dry etching techniques to provide release of the Porous Silicon membrane and to form a cavity under the said Porous Silicon layer.

2. The front side silicon micromachining process of claim **1** for the fabrication of suspended Porous Silicon membranes in the form of bridges or cantilevers, further comprising the formation of a patterned conductive layer on top of said porous silicon membrane. The said patterned conductive layer is used as a heater, for the fabrication of thermal sensor devices.

4. A gas sensor device based on Porous Silicon suspended membranes in the form of bridges or cantilevers fabricated by the front side micromachining process of claim **1** and composed of : (a) a silicon substrate, (b) a suspended membrane on top of a cavity on the silicon substrate to provide local thermal isolation, (c) a patterned conductive layer on said suspended membrane, (d) an insulating layer on top of said conductive layer, (e) a catalytic material on top of said insulating layer (f) a thermal sensing element to sense the temperature change due to the reaction of the ambient gas with the catalytic material.

5. The gas sensor of claim **4** wherein said sensing element is a Pt resistor.

6. The gas sensor device of claim **4** wherein said thermal sensing element consists of a number of thermocouples, one contact of said thermocouples being on the suspended porous silicon membrane, the other contact being on bulk silicon.

7. A gas sensor device based on Porous Silicon suspended membranes in the form of bridges or cantilevers fabricated by the front side micromachining process of claim **1** and composed of: (a) a silicon substrate, (b) a suspended membrane on top of a cavity on the silicon substrate to provide local thermal isolation, (c) a patterned conductive layer on said suspended membrane (d) an insulating layer on top of said conductive layer (e) metal electrodes on top of said insulating layer and (f) a catalytic material on top of said electrodes, the resistivity of the said catalytic material being dependent on the ambient gas.

8. A thermal conductivity sensor based on Porous Silicon suspended membranes in the form of bridges or cantilevers fabricated by the front side micromachining process of claim **1** and composed of : (a) a silicon substrate, (b) a suspended membrane on top of a cavity on the silicon substrate to provide local thermal isolation, (c) a patterned conductive layer on said suspended membrane, where said patterned conductive layer is a Pt resistor. The dimensions of the said porous silicon membrane can be changed in

order to minimize thermal losses and modulate the response time of the sensor.

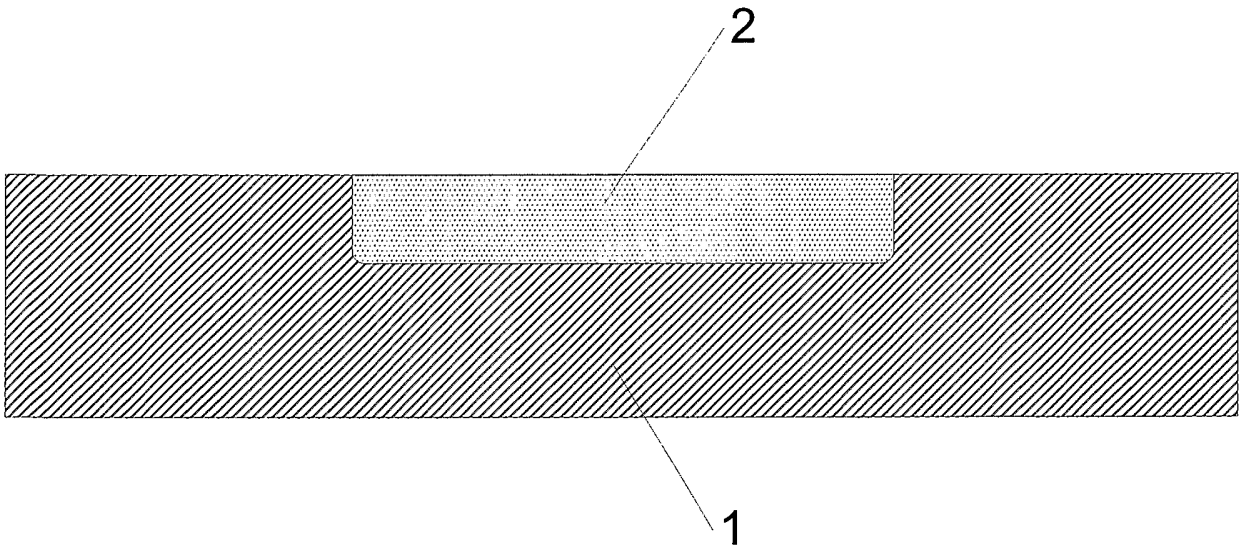


Figure 1A

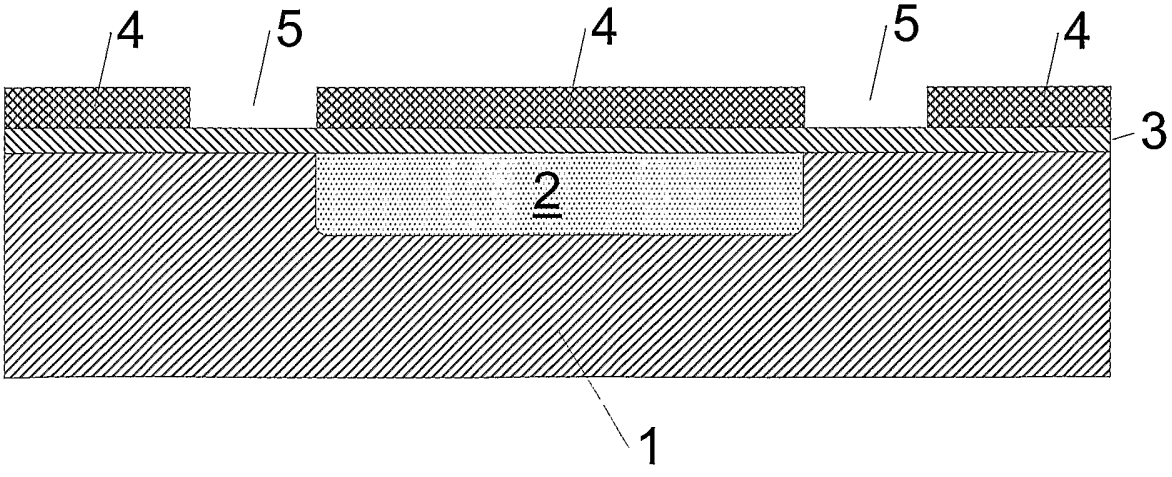


Figure 1B

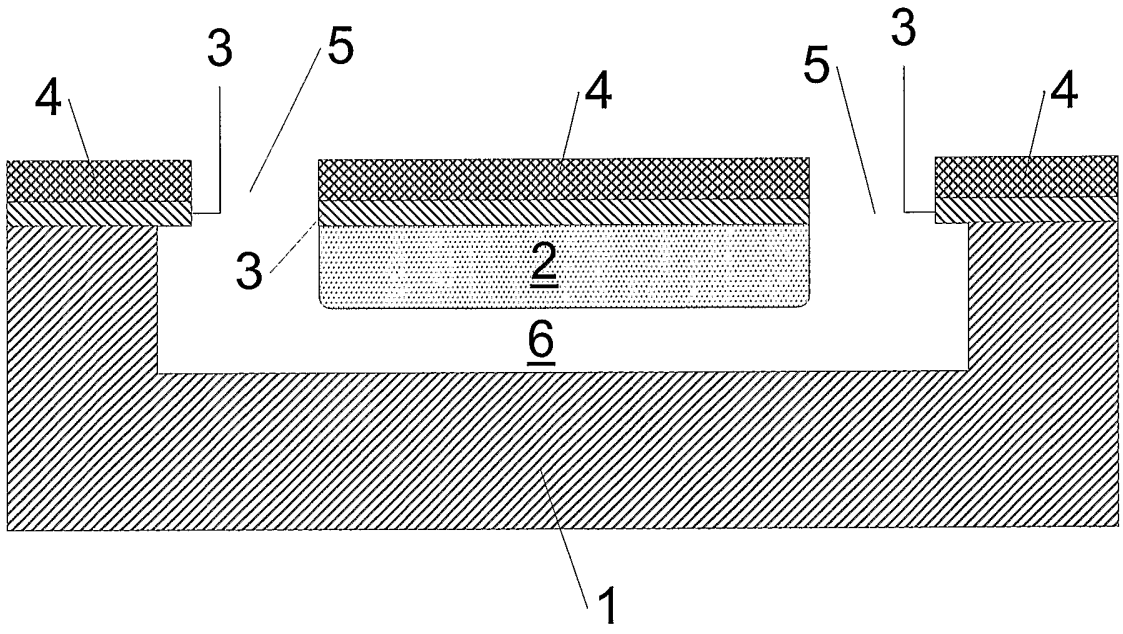


Figure 1C

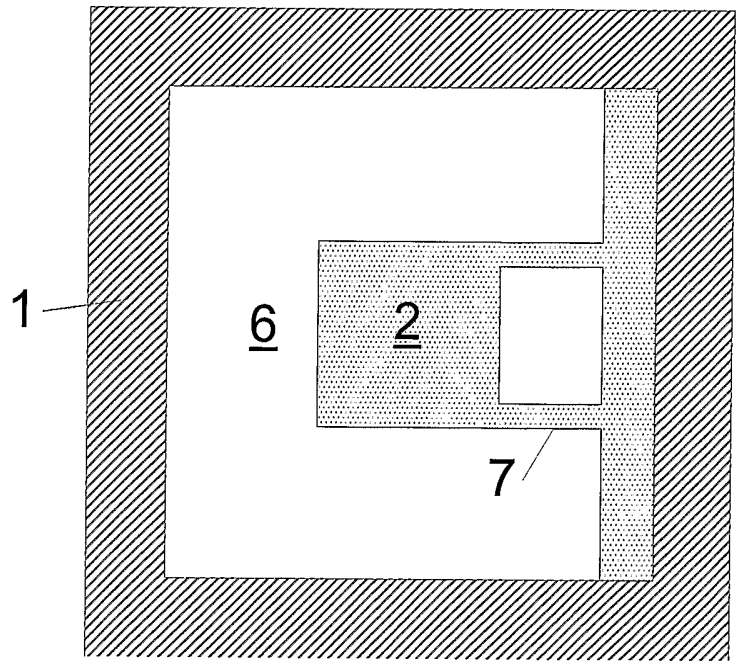


Figure 2A

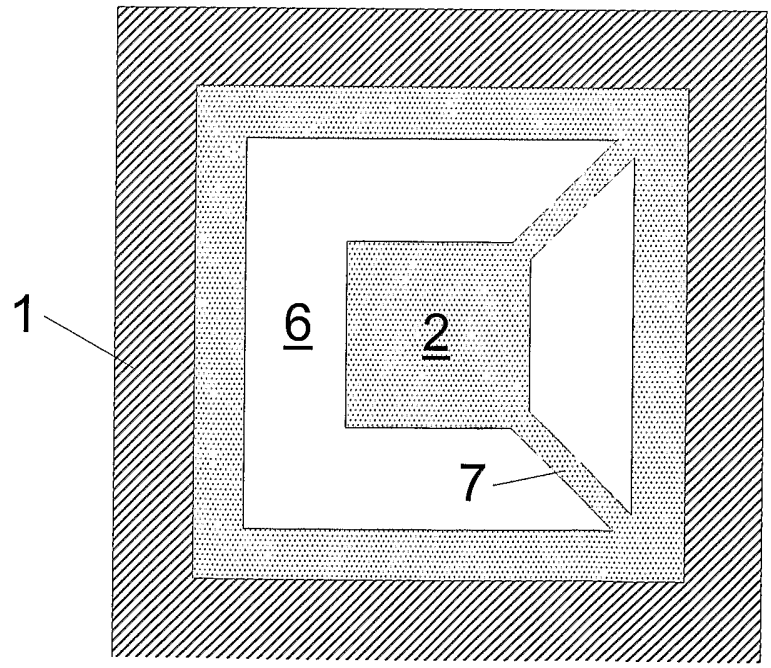


Figure 2B

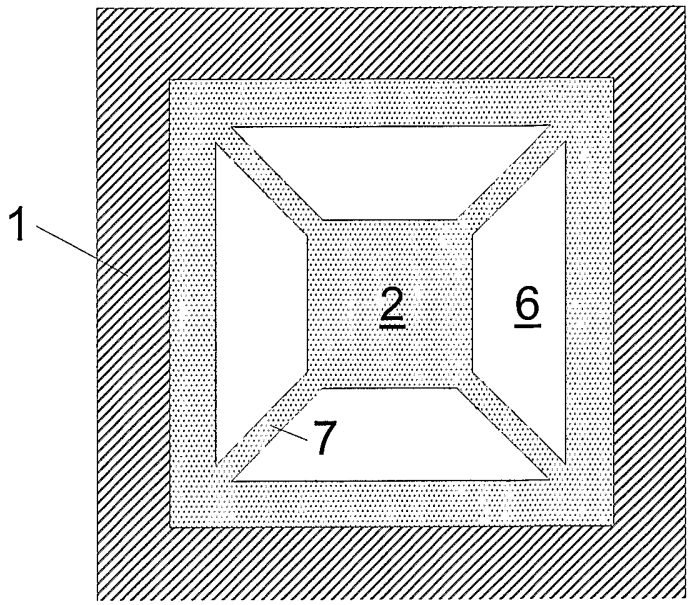


Figure 2C

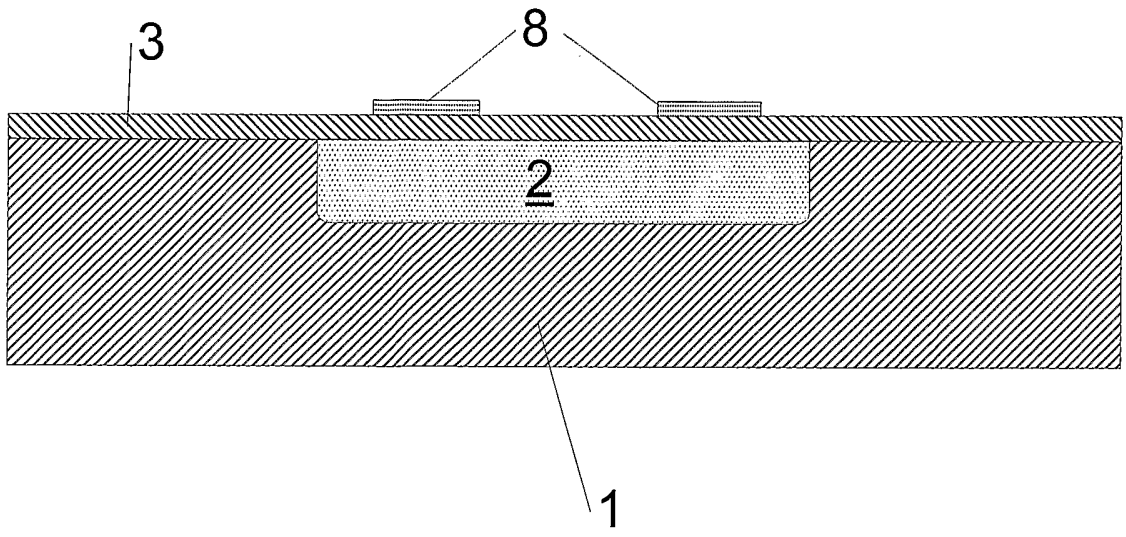


Figure 3A

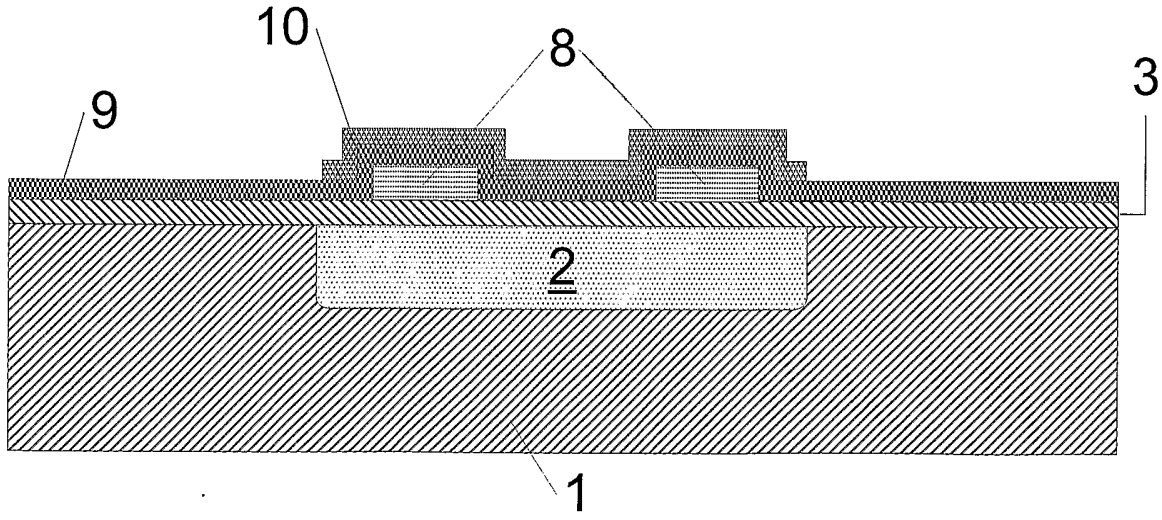


Figure 3B

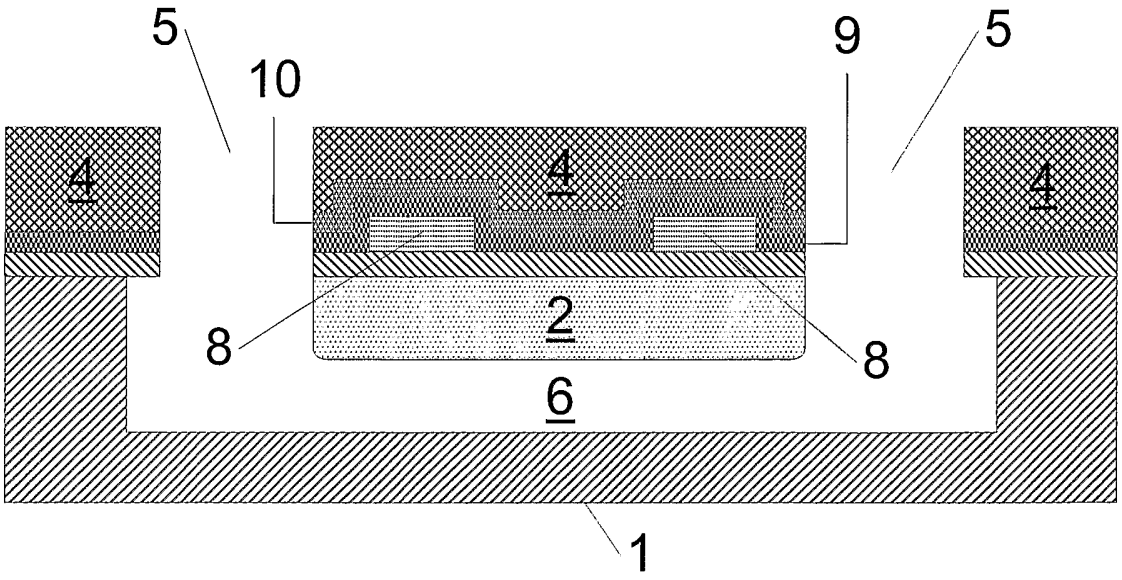


Figure 3C

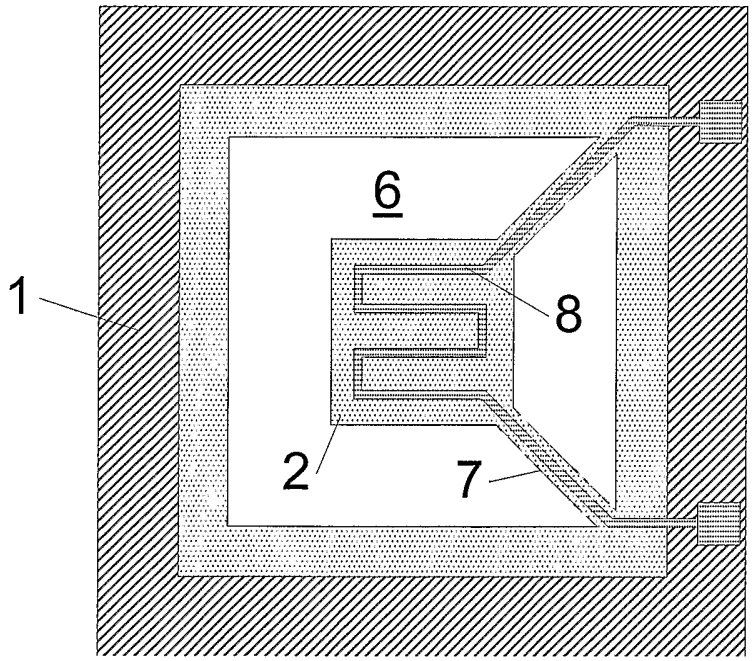


Figure 4

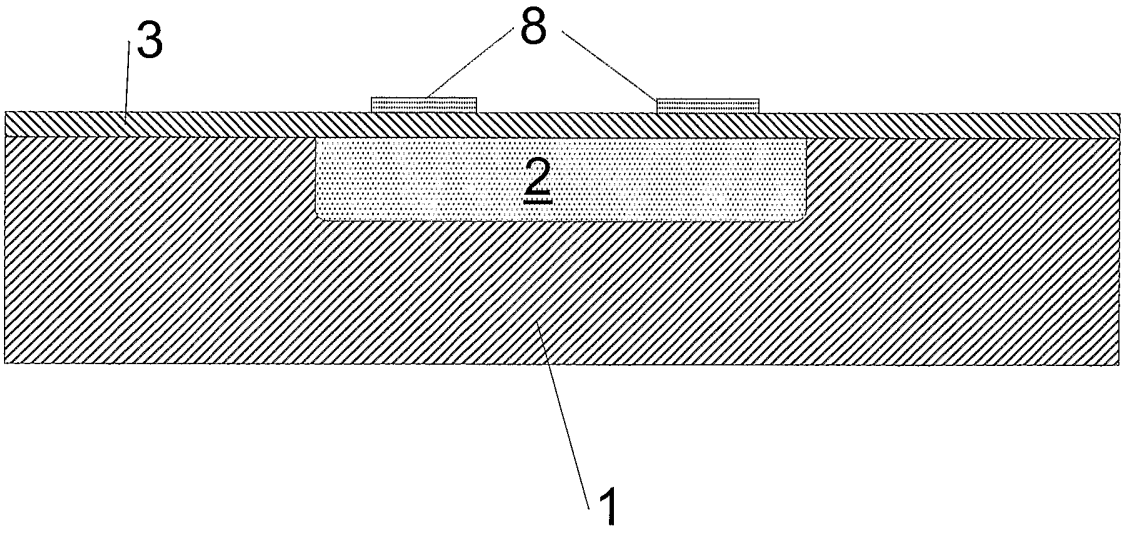


Figure 5A

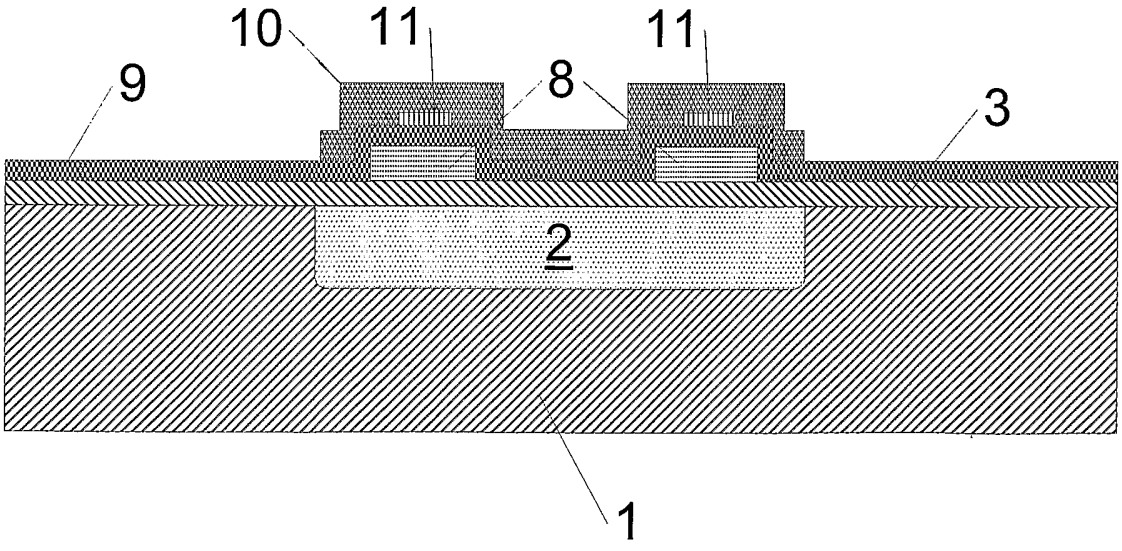


Figure 5B

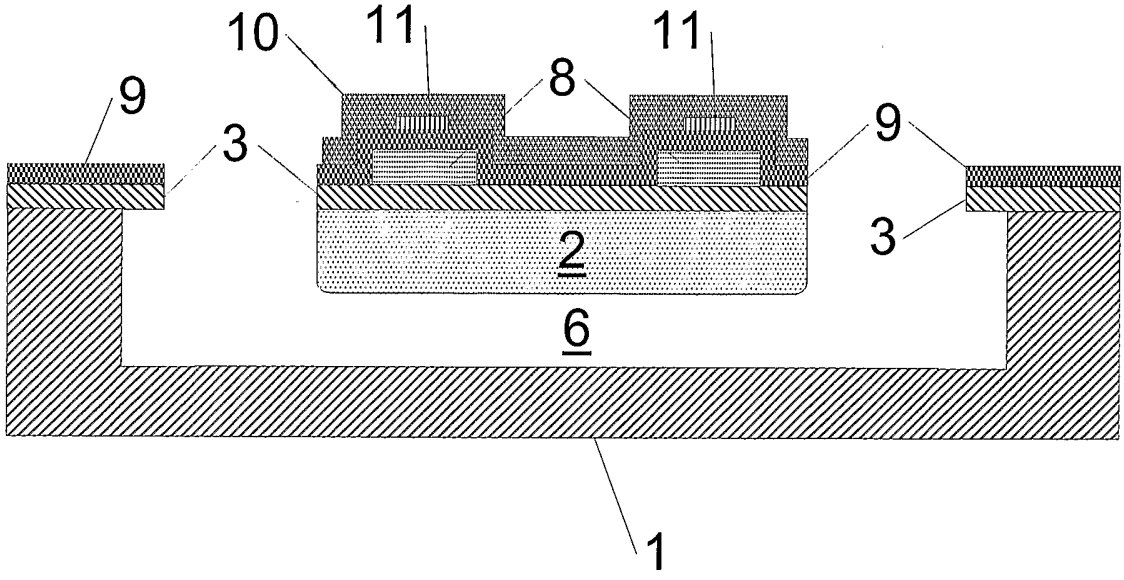


Figure 5C

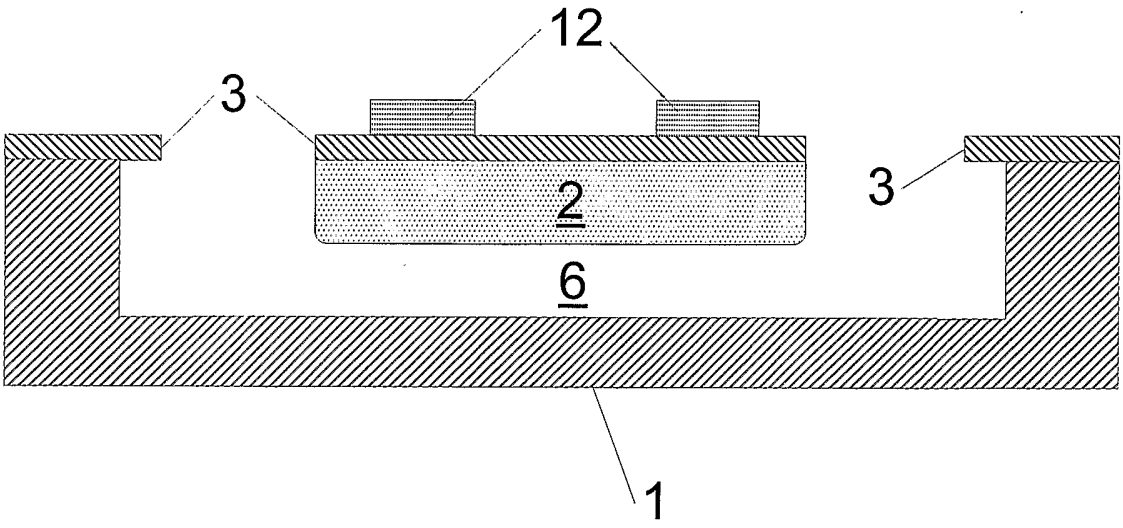


Figure 6

INTERNATIONAL SEARCH REPORT

International Application No
PCT/GR 02/00008

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 B81B3/00 G01F1/684 H05B1/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 B81B G01F H05B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, PAJ, INSPEC, COMPENDEX

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	MACCAGNANI P ET AL: "Thick porous silicon thermo-insulating membranes for gas sensor applications" SENSORS AND MATERIALS, 1999, MYU, JAPAN, vol. 11, no. 3, pages 131-147, XP008001539 ISSN: 0914-4935 cited in the application figure 1 --- -/--	3,4,7,8

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
29 April 2002	07/05/2002

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Polesello, P

INTERNATIONAL SEARCH REPORT

International Application No
PCT/GR 02/00008

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
X	KOLEV S D ET AL: "Thermal modelling of a porous silicon-based pellistor-type catalytic flammable gas sensor with two supporting beams" MICROELECTRONICS JOURNAL, MACKINTOSH PUBLICATIONS LTD. LUTON, GB, vol. 31, no. 5, May 2000 (2000-05), pages 339-342, XP004193977 ISSN: 0026-2692 figure 1 paragraph '0002!	3
A	---	1,2,4,8
X	PARBUKOV A N ET AL: "The production of a novel stain-etched porous silicon, metallization of the porous surface and application in hydrocarbon sensors" INTERNATIONAL CONFERENCE ON ELECTRONIC MATERIALS AND EUROPEAN MATERIALS RESEARCH SOCIETY (EMRS-IUMRS ICEM 2000) SPRING MEETING, SYMPOSIUM E: CURRENT TRENDS IN NANOTECHNOLOGIES, SAN FRANCISCO, CA, USA, APRIL 2000, vol. C15, no. 1-2, pages 121-123, XP002193596 Materials Science & Engineering C, Biomimetic and Supramolecular Systems, 2001, Elsevier, Netherlands ISSN: 0928-4931 figure 1 paragraph '0005!	8
A	---	1-7
A	LAMMEL G ET AL: "Free-standing, mobile 3D porous silicon microstructures" SENSORS AND ACTUATORS A, ELSEVIER SEQUOIA S.A., LAUSANNE, CH, vol. 85, no. 1-3, 25 August 2000 (2000-08-25), pages 356-360, XP004214496 ISSN: 0924-4247 figures 4-6 paragraph '0002!	1,4,7,8

A	EP 0 819 935 A (DAIMLER BENZ AG ;FRAUNHOFER GES FORSCHUNG (DE); SCHLUMBERGER IND S) 21 January 1998 (1998-01-21) figures 1,3,4 column 2, line 31 -column 6, line 6	1-8

	-/--	

INTERNATIONAL SEARCH REPORT

International Application No
PCT/GR 02/00008

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
A	LI Y X ET AL: "SIMPLE - A technique of silicon micromachining using plasma etching" SENSORS AND ACTUATORS A, ELSEVIER SEQUOIA S.A., LAUSANNE, CH, vol. 57, no. 3, 1 December 1996 (1996-12-01), pages 223-232, XP004081084 ISSN: 0924-4247 cited in the application figure 1 paragraph '0002! ---	1
A	WO 98 50763 A (NASSIOPOULOU ANDROULA G ;NCSR DEMOKRITOS (GR); KALTSAS GRIGORIS (G) 12 November 1998 (1998-11-12) cited in the application figures 1-3 page 2, line 9 -page 3, line 4 -----	6

INTERNATIONAL SEARCH REPORT

Information on patent family members

l al Application No
PCT/GR 02/00008

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 0819935 A	21-01-1998	EP 0819935 A1	21-01-1998
		DE 69601930 D1	06-05-1999
		DE 69601930 T2	07-10-1999
WO 9850763 A	12-11-1998	GR 1003010 B	20-11-1998
		WO 9850763 A1	12-11-1998