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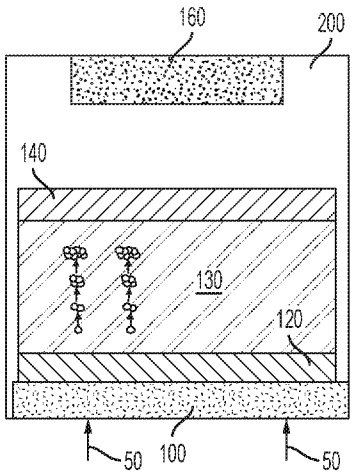

FIG. 1A

(57) Abstract: A sensor including a layer of amorphous selenium (a-Se) and at least one charge blocking layer is formed by depositing the charge blocking layer over a substrate prior to depositing the amorphous selenium, enabling the charge blocking layer to be formed at elevated temperatures. Such a process is not limited by the crystallization temperature of a-Se, resulting in the formation of an efficient charge blocking layer, which enables improved signal amplification of the resulting device. The sensor can be fabricated by forming first and second amorphous selenium layers over separate substrates, and then fusing the a-Se layers at a relatively low temperature.

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FABRICATION METHOD FOR FUSED MULTI-LAYER AMORPHOUS SELENIUM SENSOR

GOVERNMENT LICENSE RIGHTS

[0001] This invention was made with government support under grant number RO1EB2655 awarded by the National Institute of Health. The government has certain rights in the invention.

BACKGROUND

[0002] The present application relates generally to sensors adapted to detect optical or ionizing radiation, and more specifically to multi-layer amorphous selenium (a-Se) sensors and their methods of production.

[0003] Amorphous selenium (a-Se) has been commercialized both as an optical sensor and direct x-ray detector, and a-Se with avalanche gain has also been proposed for use in an indirect x-ray detector. Advantages of a-Se over other photoconductors such as silicon, which may be used in both optical and x-ray sensing applications, and CdTe, which may be used to detect x-rays, include the capability for large area deposition, avalanche multiplication of holes at electric fields (ESe) greater than 70 V/um, and monotonically increasing x-ray conversion gain with ESe.

[0004] As will be appreciated, conventional x-ray detectors, especially x-ray detectors adapted for low photon flux applications, suffer from image degradation due to electronic noise. However, decreasing the electronic noise of readout electronics increases the cost of the imager and has limited effect.

[0005] On the other hand, for a-Se detectors electronic noise can be overcome by increasing ESe to amplify the signal prior to the introduction of electronic noise. For optical

sensors, ESe greater than 70 V/um is required for avalanche gain, while for direct x-ray sensors any increase in ESe will increase conversion gain.

SUMMARY

[0006] Notwithstanding recent developments, there is a need for improved methods for fabricating a-Se-containing structures that can be incorporated into systems for optical and x-ray sensing where signal amplification can be realized prior to the introduction of electronic noise. As described herein, a-Se-containing structures may be made by delaying the formation of temperature-sensitive amorphous selenium layers until after the elevated temperature processing of charge blocking layers within the structures.

[0007] In accordance with various embodiments, a method of fabricating a sensor includes forming a first charge blocking layer over a first substrate, forming a first layer of amorphous selenium over the first charge blocking layer, forming a second charge blocking layer over a second substrate, and forming a second layer of amorphous selenium over the second charge blocking layer.

[0008] The first layer of amorphous selenium is then brought into contact with the second layer of amorphous selenium to form a multi-layer structure, which is heated to fuse the first layer of amorphous selenium to the second layer of amorphous selenium. Fusion may be accomplished by heating to above the glass transition temperature (T_g) of amorphous selenium, but below its crystallization temperature (T_c).

[0009] According to further embodiments, a sensor-forming method includes forming a charge blocking layer over a substrate, forming a layer of amorphous selenium over the charge blocking layer, and heating the layer of amorphous selenium to fuse the layer of amorphous selenium to the charge blocking layer.

Brief Description of Several Views of the Drawings

[0010] The following detailed description of specific embodiments of the present application can be best understood when read in conjunction with the following drawings, where like structure is indicated with like reference numerals and in which:

[0011] Fig. 1A is a schematic diagram of an optical sensor including a layer of amorphous selenium;

[0012] Fig. 1B is a schematic diagram of a direct x-ray sensor that includes an active layer of amorphous selenium;

[0013] Fig. 1C is a schematic diagram of a combination solid state active matrix flat panel imager (AMFPI) and optical imager that include a layer of amorphous selenium;

[0014] Fig. 2A illustrates the sequential formation of a charge blocking layer and a first layer of amorphous selenium over a substrate including an electronic readout;

[0015] Fig. 2B illustrates the formation of a charge blocking layer and a second layer of amorphous selenium over a substrate;

[0016] Fig. 2C shows the formation of a multi-layer structure by the alignment and subsequent fusion of first and second layers of amorphous selenium according to various embodiments;

[0017] Fig. 3A illustrates the sequential formation of a charge blocking layer and a first layer of amorphous selenium having a first thickness over a substrate including an electronic readout;

[0018] Fig. 3B illustrates the formation of a charge blocking layer and a second layer of amorphous selenium having a second thickness different from the first thickness over a substrate;

[0019] Fig. 3C shows the formation of a multi-layer structure by the alignment and subsequent fusion of first and second layers of amorphous selenium according to certain embodiments;

[0020] Fig. 4A shows an example sensor structure formed by the lamination and fusion of separately-formed layers of amorphous selenium;

[0021] Fig. 4B shows a further example sensor structure formed by the lamination and fusion of separately-formed layers of amorphous selenium;

[0022] Fig. 5 depicts an experimental set-up used to evaluate the disclosed multi-layer sensors;

[0023] Fig. 6 is a plot of time of flight versus electric field for an example multi-layer sensor; and

[0024] Fig. 7 is a plot of normalized signal versus time demonstrating minimal ghosting for an exemplary multi-layer sensor.

DETAILED DESCRIPTION

[0025] Reference will now be made in greater detail to various embodiments of the subject matter of the present application, some embodiments of which are illustrated in the accompanying drawings. The same reference numerals will be used throughout the drawings to refer to the same or similar parts.

[0026] Schematic diagrams of an example optical sensor, direct x-ray detector, and indirect x-ray detector are shown in Fig. 1A, Fig. 1B and Fig. 1C, respectively.

[0027] Referring to Fig. 1A, an optical sensor includes a transparent substrate 100 such as an electroded glass substrate. The high voltage electrode (not separately shown) can be formed on the substrate from a suitable transparent, conductive material such as indium tin

oxide (ITO) using conventional deposition and patterning techniques such as physical vapor deposition (e.g., evaporation or sputtering) and photolithography.

[0028] A first charge blocking layer 120 is formed over the substrate 100. First charge blocking layer 120 may be a high temperature, high field hole blocking layer formed from an organic polymer, for example. First charge blocking layer 120 may be formed using a thermal or chemical deposition process.

[0029] Referring still to Fig. 1A, a layer of amorphous selenium (a-Se) 130 is disposed over the first charge blocking layer 120. In the various embodiments disclosed herein, a layer of amorphous selenium may have a thickness of 0.5 to 100 microns, e.g., 0.5, 1, 2, 4, 8, 10, 20, 50 or 100 microns, including ranges between any of the foregoing values. The amorphous selenium may be doped (stabilized) or un-doped. Example dopants include arsenic, tellurium and chlorine, which may be included in amounts of 0.1 to 0.5 atomic percent, e.g., 0.1, 0.2, 0.3, 0.4 or 0.5 at.%, including ranges between any of the foregoing values.

[0030] A second charge blocking layer 140 is formed over the layer of amorphous selenium 130. In a comparative structure, second charge blocking layer 140 may be a low temperature, high field electron blocking layer formed from an organic polymer, for example. Second charge blocking layer 140 may be formed using a thermal or chemical deposition process. As will be appreciated, a low temperature process for forming the second charge blocking layer 140 directly over the layer of amorphous selenium (a-Se) 130 may be used to avoid crystallization of the underlying selenium layer 130. In the present context, "low temperature" means a process temperature less than a crystallization onset temperature for selenium, e.g., less than 80°C or less than 60°C.

[0031] In the illustrated embodiment, a space 200 such as an air gap or vacuum gap separates the multi-layer structure including substrate 100, first charge blocking layer 120, a-Se layer 130, and second charge blocking layer 140 from readout electronics 160. Readout electronics 160 may include an electron beam readout. Insomuch as the optical avalanche structure of Fig. 1A relies on a vacuum tube design, the direct conversion sensor cannot operate above an ESe of about 10 V/um. The optical sensor of Fig. 1A is adapted to receive optical radiation 50 through transparent substrate 100. When the a-Se is capable of avalanche gain, the structure is referred to as High Gain Avalanche Rushing Photoconductor (HARP).

[0032] Referring to Fig. 1B, shown schematically is an exemplary direct x-ray sensor. The direct x-ray sensor includes a layer of amorphous selenium 230 disposed between a first charge blocking layer 240 and a second charge blocking layer 220. First charge blocking layer 240 may be a high temperature, low field electron blocking layer, while in a conventional structure, second charge blocking layer 220 may be a low temperature, low field hole blocking layer. That is, for thermal compatibility with an already-formed layer of amorphous selenium 230, the second charge blocking layer 220 may be formed at a low temperature, i.e., less than a crystallization onset temperature for amorphous selenium.

[0033] Pixel electrodes 250 may be disposed proximate to readout electronics 260. During operation, ionizing radiation such as x-ray radiation 60 may enter the x-ray sensor of Fig. 1B through a transparent, high-voltage (HV) electrode 210. HV electrode 210 may include a patterned layer of ITO, for example.

[0034] Referring to Fig. 1C, shown is a scintillating HARP-AMFPI (left) and optical imager (right). Each sensor includes, from bottom to top, readout electronics 360, one or more pixel electrodes 350, an electron blocking layer (EBL) 340, a layer of amorphous

selenium 330, a hole blocking layer (HBL) 320, and a high voltage electrode 310. During use, optical radiation 50 may enter the optical imager through the HV electrode 310.

[0035] In the illustrated structure, the scintillating HARP-AMFPI sensor additionally includes a scintillator 305 disposed over the HV electrode 310. During use, ionizing radiation 60 may enter the scintillating HARP-AMFPI sensor through the scintillator 305.

[0036] In certain structures, an air gap 300 between the scintillator 305 and the a-Se layer 330 may lead to spatial blurring and image degradation. The scintillating HARP-AMFPI shown in Fig. 1C, when formed with a low temperature (i.e., defect-containing) HBL 320 may exhibit inferior performance, such as breakdown during operation.

[0037] As will be appreciated, a challenge facing developers of optical and x-ray detectors, such as those described with reference to Figs. 1A-1C, and including solid-state active matrix flat panel imagers (AMFPI) utilizing an avalanche a-Se sensor, relates to the potential for a processing incompatibility between the amorphous selenium layer and the dielectric layer(s) (i.e., charge blocking layers) used to isolate the a-Se and inhibit charge injection, i.e., dark current injection, from adjacent electrodes during operation.

[0038] A difficulty lies in creating a multi-layer structure that can withstand the high ESe and limit dark current injection from the electrodes. A typical detector structure, regardless of application geometry or ESe requirements, includes an n-type, hole blocking layer (HBL) and a p-type, electron blocking layer (EBL) to isolate the a-Se from the positive high voltage (HV) and negatively biased electrodes, respectively, to prevent charge injection.

[0039] Desired materials for the charge blocking layers include semiconducting oxides and polymers. Exemplary oxide layers (e.g., silicon dioxide) are typically formed via physical vapor deposition (PVD) or chemical vapor deposition (CVD) at a substrate temperature of at least 200°C. Polymer layers, on the other hand, may be deposited by solution-based

processing, but typically require an annealing step at elevated temperatures (e.g., greater than 60°C) to remove solvent and cross-link the polymer.

[0040] During the fabrication of the comparative detectors shown in Figs. 1A-1C, a charge blocking layer formed over a layer of a-Se must be deposited at substrate temperature less than the crystallization onset temperature for amorphous selenium (i.e., about 60°C) in order to avoid the formation polycrystalline aggregates within the amorphous selenium.

[0041] As will be appreciated, semiconducting oxides and polymers that are formed using sub-optimal conditions (i.e., deposition or curing temperatures of less than about 200°C) result in poor stoichiometry and the incorporation of defects into the charge blocking layer that may negatively impact performance or even cause failure, particularly at high ESe. Thus, the performance of the sensors depicted in Figs. 1A-1C may be limited by the deposition temperature of the top charge blocking layer.

[0042] According to various embodiments, the fabrication of a multi-layer sensor architecture, including a layer of amorphous selenium, includes the formation of a first portion of the amorphous selenium layer over a previously-formed first charge blocking layer, i.e., an electron blocking layer (EBL), and the formation of a second portion of the amorphous selenium layer over a previously-formed second charge blocking layer, i.e., a hole blocking layer (HBL). The disclosed process delays the formation of the first and second portions of the (temperature sensitive) amorphous selenium layer until after formation of the respective charge blocking layers. In certain embodiments, the charge blocking layers are formed on separate substrates. This allows the EBL and HBL deposition processes to be conducted at a relatively high temperature without adversely affecting the layer(s) amorphous selenium. An example process can be understood with reference to Figs. 2A-2C.

[0043] Referring to Figs. 2A, the fabrication process flow for a fused selenium sensor according to various embodiments includes the formation of an electron blocking layer (EBL) 440 over a first substrate 460. The first substrate 460 may include an electronic readout such as a thin film transistor, CMOS transistor or photon counting sensor. A pixel electrode or a pixel electrode array 450 may be disposed over the first substrate 460, e.g., between the first substrate 460 and the EBL 440. A first doped or un-doped layer of amorphous selenium 431 having a first thickness (T1) is deposited over the EBL 440.

[0044] Separately, referring to Fig. 2B, a hole blocking layer (HBL) 420 is formed over a second substrate 405. The second substrate 405 may include any substrate suited for the desired application, including a scintillator, fiber optic faceplate, glass, or glass carrier for a de-bonded clear thin polymer. The second substrate 405 may be an electroded substrate, including a high voltage (HV) electrode 410. The HV electrode may include indium tin oxide, for example. A second doped or un-doped layer of amorphous selenium 432 having a second thickness (T2) is then deposited over the HBL 420.

[0045] In certain embodiments, the first layer of amorphous selenium 431 and the second layer of amorphous selenium 432 may each be doped. In certain embodiments, the first layer of amorphous selenium 431 and the second layer of amorphous selenium 432 may each be un-doped.

[0046] Referring to Fig. 2C, in a further step, the first layer of amorphous selenium 431 is brought into contact with the second layer of amorphous selenium 432 to form a multi-layer structure 400, which is heated at a temperature sufficient to fuse the first layer of amorphous selenium to the second layer of amorphous selenium. Fusion may be accomplished by heating to above the glass transition temperature (T_g) of amorphous selenium, but below its crystallization temperature (T_c). The fusion temperature will be determined by the glass

transition temperature, which is dependent on the extent of doping of the amorphous selenium layer(s). In certain embodiments, fusion of the first and second layers of amorphous selenium may be accompanied by the application of a compressive force. In certain embodiments, the fusion may be performed in air or under vacuum, e.g., if air cavities inhibit uniform fusion.

[0047] Above its glass transition temperature, a-Se becomes a viscos, rubber like adhesive allowing for two layers of selenium to be fused together. The soft and flexible state will planarize and remove surface topology in the a-Se, which may result from deposition imperfections or substrate topology. By fusing the first and second layers of amorphous selenium at a temperature less than the recrystallization temperature of selenium, the resulting composite (multi-layer) structure 431, 432, which has a total thickness T=T1+T2, may be free of any crystalline phase(s).

[0048] In certain embodiments, one or both substrates may be a flexible substrate. Flexible substrates such as thin glass, phosphor screens and Mylar films may induce less stress on the a-Se, resulting in more uniform fusion over a large area compared to inflexible glass substrates, for example.

[0049] Applicant has shown that unequal charge transport of holes and electrons across the fusion interface can be advantageous to device performance. Although T1 is equal to T2 in the illustrated embodiment of Fig. 2C, the respective thicknesses of the first and second layers of amorphous selenium can be varied such that the fusion interface is closer to one of the blocking layers, which can improve by blocking property of that blocking layer.

[0050] For instance, according to various embodiments, time of flight (TOF) measurements for a single pixel sensor measuring about 2 cm x 2 cm demonstrate that holes, which are the primary charge carrier in a-Se, move across the fusion interface. In such case,

if electron transport across the fusion interface is significantly worse than holes, the thicknesses of the respective a-Se layers can be selected such that T2 is greater than T1, whereby poor transport across the fusion interface can contribute to electron blocking. The thickness of T1 may be decreased so long as the substrate topology is planarized and uniform fusion can be achieved.

[0051] Thus, referring to Figs. 3A-3C, according to further embodiments, a first layer of amorphous selenium 431 has a thickness T1, while a second layer of amorphous selenium 432 has a thickness T2, where T1 is less than T2. In an example structure formed by the fusion of two separate layers of amorphous selenium, the thickness (T1) of one layer may be 5 to 200% of the thickness (T2) of the other layer, e.g., 5, 10, 20, 50, 100, 150 or 200%, including ranges between any of the foregoing values. For instance, a first layer of amorphous selenium and a second layer of amorphous selenium may each have a thickness of 5.4 microns. In a further example, a first layer of amorphous selenium may have a thickness of 10 microns and a second layer of amorphous selenium may have a thickness of 5 microns.

[0052] A further method of fabricating a multi-layer sensor includes forming a charge blocking layer over a substrate, forming a layer of amorphous selenium over the previously-deposited charge blocking layer, and heating the layer of amorphous selenium to fuse the layer of amorphous selenium to the charge blocking layer.

[0053] Referring to Fig. 4A and Fig. 4B, shown are exemplary sensor architectures that may be formed by the fusion of separately deposited (i.e., top and bottom) layers of amorphous selenium. The architecture in Fig. 4A includes an electroded (e.g., indium tin oxide coated) glass substrate 660 and an over-formed first layer of amorphous selenium 631 that has been fused to a high voltage ITO coated glass substrate 605 via an indium gallium zinc oxide (IGZO) layer 610, and an over-formed second layer of amorphous selenium 632.

After forming the foregoing structure, one of the substrates 605, 660 may be removed (e.g., delaminate) if desired. An analogous structure, referring to Fig. 4B, includes poly(3,4-ethylenedioxythiophene) (PEDOT) electrodes 650 formed over a surface of the first layer of amorphous selenium 631.

[0054] A measurement system 700 for evaluating a multi-layer sensor is shown schematically in Fig. 5. The measurement system 700 includes a power supply 710, high voltage filter 720, current amplifier 730 and oscilloscope 740. An example current amplifier 730 is a Stanford SR 570 amplifier. A multi-layer sensor 400 may be mounted between the power supply 710 and the oscilloscope 740, and irradiated with a source of optical radiation (e.g., 500 ps, 500 nJ laser pulses).

[0055] Fig. 6 is a plot of hole time-of-flight (TOF) versus electric field for an example multi-layer sensor confirming that charge traverses the fused interface between first and second layers of amorphous selenium. Fig. 7 is a plot of normalized signal versus time for an exemplary multi-layer sensor under continuous 30 Hz excitation at 30V (~5 V/micron) demonstrating negligible ghosting, which is a measure of the drop in x-ray sensitivity of the exposed region of the sensor.

[0056] According to various embodiments, by depositing the charge blocking layer(s) prior to depositing amorphous selenium, the charge blocking layer(s) as well as readout electronics can be fabricated at elevated temperatures. Such processing is not limited by the crystallization temperature of a-Se, resulting in the formation of efficient charge blocking layers, which enables improved signal amplification.

[0057] The disclosed methods can be used to form solid state sensors, which are more reliable than vacuum tube-based sensors. Moreover, such sensors can be fabricated using existing materials and materials deposition technologies. In certain embodiments, unequal

charge transport across the interface between the fused first and second amorphous selenium layers can be advantageous if the interface is located proximate to the blocking layer for the slower charge carrier.

[0058] As used herein, the singular forms “a,” “an” and “the” include plural referents unless the context clearly dictates otherwise. Thus, for example, reference to a “photoconductor layer” includes examples having two or more such “photoconductor layers” unless the context clearly indicates otherwise.

[0059] Unless otherwise expressly stated, it is in no way intended that any method set forth herein be construed as requiring that its steps be performed in a specific order. Accordingly, where a method claim does not actually recite an order to be followed by its steps or it is not otherwise specifically stated in the claims or descriptions that the steps are to be limited to a specific order, it is no way intended that any particular order be inferred. Any recited single or multiple feature or aspect in any one claim can be combined or permuted with any other recited feature or aspect in any other claim or claims.

[0060] It will be understood that when an element such as a layer, region or substrate is referred to as being formed on, deposited on, or disposed "on" or "over" another element, it can be directly on the other element or intervening elements may also be present. In contrast, when an element is referred to as being "directly on" or "directly over" another element, no intervening elements are present.

[0061] While various features, elements or steps of particular embodiments may be disclosed using the transitional phrase “comprising,” it is to be understood that alternative embodiments, including those that may be described using the transitional phrases “consisting” or “consisting essentially of,” are implied. Thus, for example, implied alternative embodiments to a photoconductor layer that comprises amorphous selenium

include embodiments where a photoconductor layer consists essentially of amorphous selenium and embodiments where a photoconductor layer consists of amorphous selenium.

[0062] It will be apparent to those skilled in the art that various modifications and variations can be made to the present invention without departing from the spirit and scope of the invention. Since modifications, combinations, sub-combinations and variations of the disclosed embodiments incorporating the spirit and substance of the invention may occur to persons skilled in the art, the invention should be construed to include everything within the scope of the appended claims and their equivalents.

CLAIMS
What is claimed is:

1. A method of fabricating a sensor, comprising:

forming a first charge blocking layer over a first substrate;

forming a first layer of amorphous selenium over the first charge blocking layer;

forming a second charge blocking layer over a second substrate;

forming a second layer of amorphous selenium over the second charge blocking layer;

contacting the first layer of amorphous selenium with the second layer of amorphous selenium to form a multi-layer structure;

heating the multi-layer structure to fuse the first layer of amorphous selenium to the second layer of amorphous selenium.

2. The method of claim 1, wherein the first charge blocking layer and the second charge blocking layer each comprise an organic polymer.

3. The method of claim 1, wherein the first charge blocking layer and the second charge blocking layer are formed by physical vapor deposition, chemical vapor deposition or solution-based deposition.

4. The method of claim 1, wherein the first substrate comprises an electronic readout.

5. The method of claim 1, wherein the first charge blocking layer is formed over a pixel electrode.

6. The method of claim 1, wherein a thickness of the first layer of amorphous selenium is less than a thickness of the second layer of amorphous selenium.

7. The method of claim 1, wherein at least one of the first layer of amorphous selenium and the second layer of amorphous selenium comprises doped amorphous selenium.

8. The method of claim 1, wherein the second substrate comprises electroded glass or a scintillator.

9. The method of claim 1, wherein at least one of the first substrate and the second substrate is a flexible substrate.

10. The method of claim 1, further comprising forming a high voltage electrode over the second substrate prior to forming the second charge blocking layer.

11. The method of claim 1, wherein the multi-layer structure is heated to a temperature between 35°C and 60°C to fuse the amorphous selenium layers.

12. The method of claim1, further comprising applying a compressive force to the multi-layer structure during the heating.

13. The method of claim 1, wherein heating the multi-layer structure to fuse the first and second layers of amorphous selenium is performed under vacuum.

14. The method of claim 1, wherein the fused layers of amorphous selenium are free of pores.

15. A method of fabricating a sensor, comprising:

forming a charge blocking layer over a substrate;

forming a layer of amorphous selenium over the charge blocking layer; and

heating the layer of amorphous selenium to fuse the layer of amorphous selenium to the charge blocking layer.

16. The method of claim 15, wherein the substrate is a flexible substrate.

17. The method of claim 15, wherein the charge blocking layer is formed by physical vapor deposition or chemical vapor deposition at a temperature of at least 200°C.

18. The method of claim 15, wherein the layer of amorphous selenium is heated to a temperature between 35°C and 60°C to fuse the layer of amorphous selenium to the charge blocking layer.

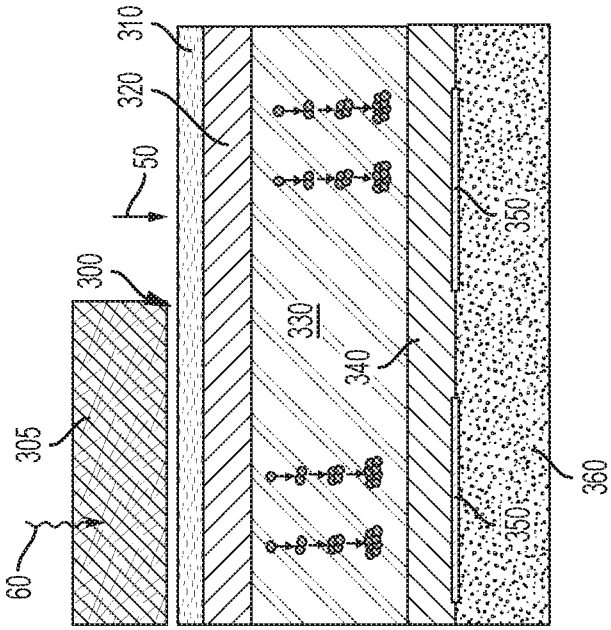

FIG. 1C

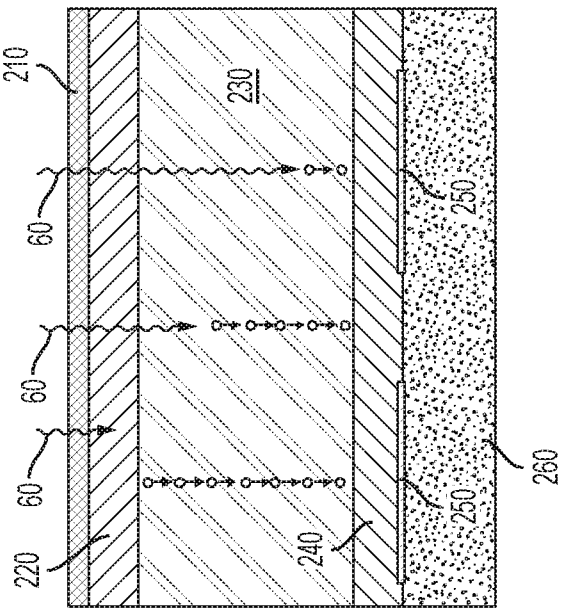

FIG. 1B

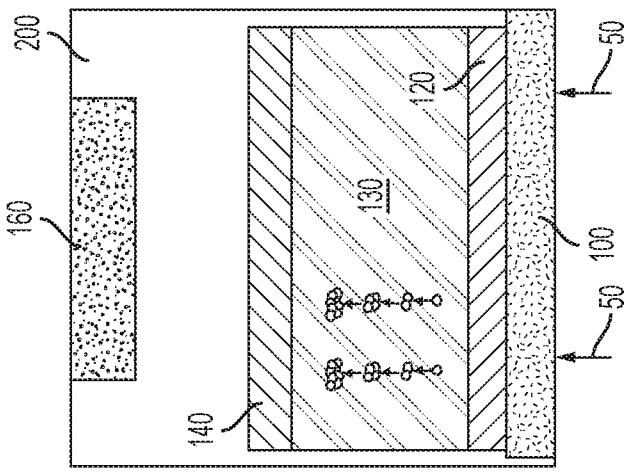

FIG. 1A

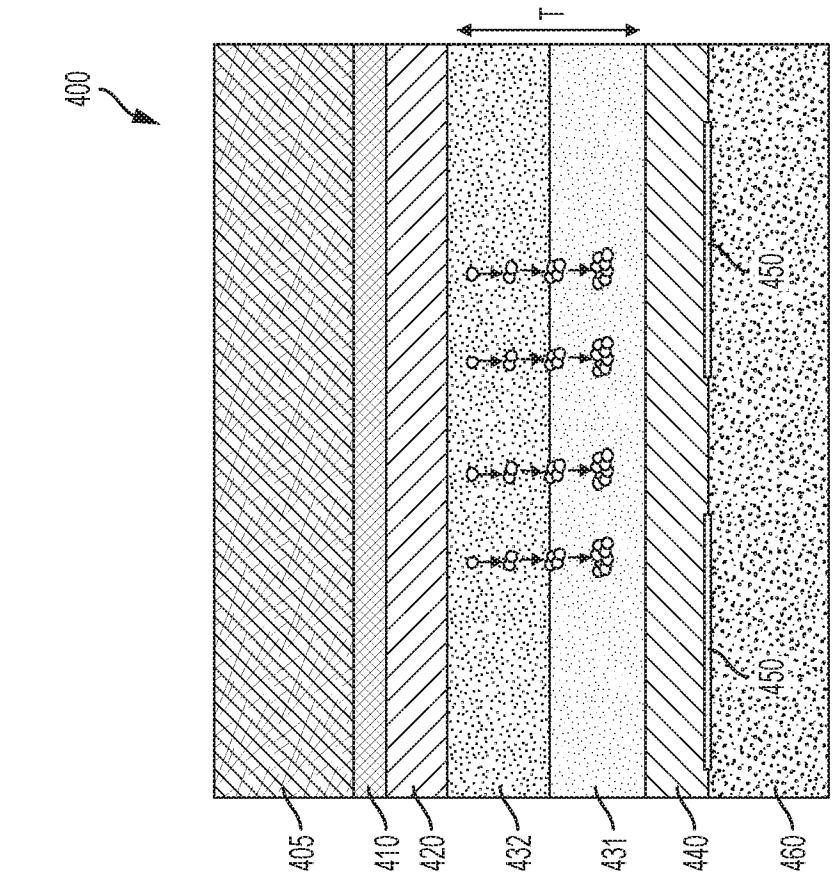

FIG. 2C

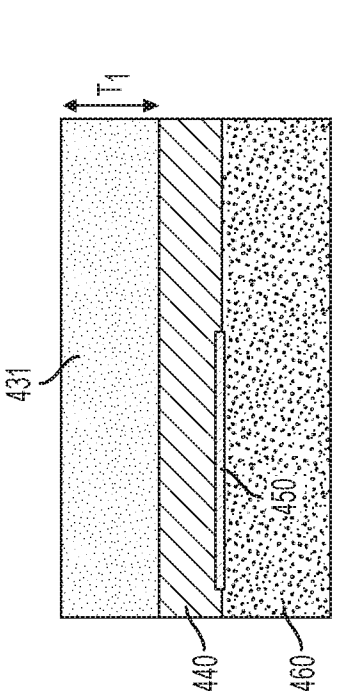

FIG. 2A

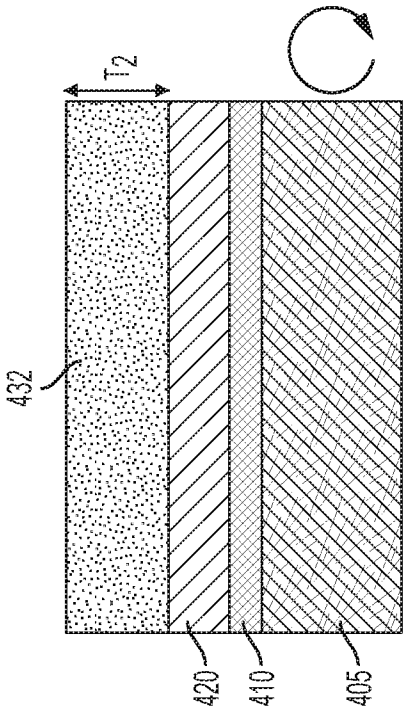

FIG. 2B

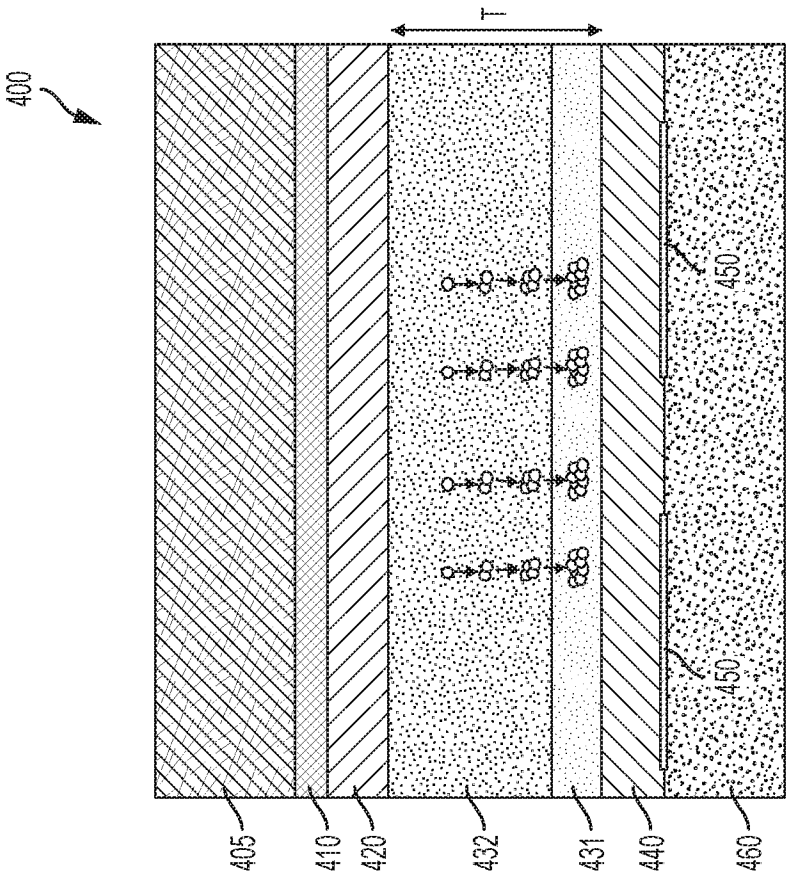

FIG. 3C

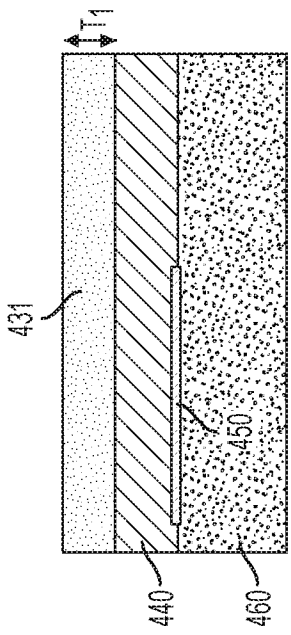

FIG. 3A

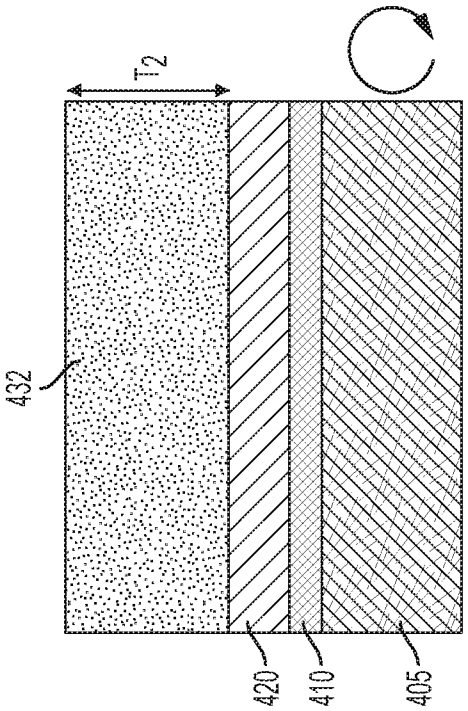

FIG. 3B

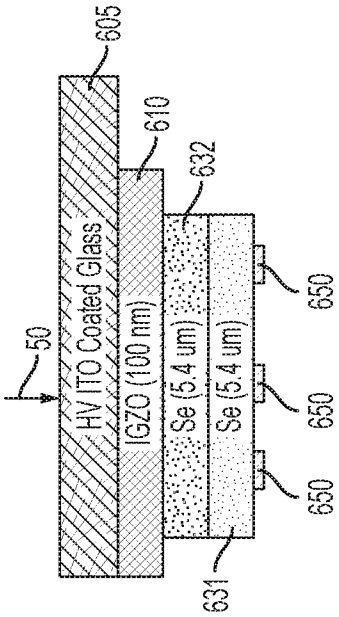
605
610
632
650
650
650
50
HV ITO Coated Glass
IGZO (100 nm)
Se (5.4 um)
Se (5.4 um)
631

FIG. 4B

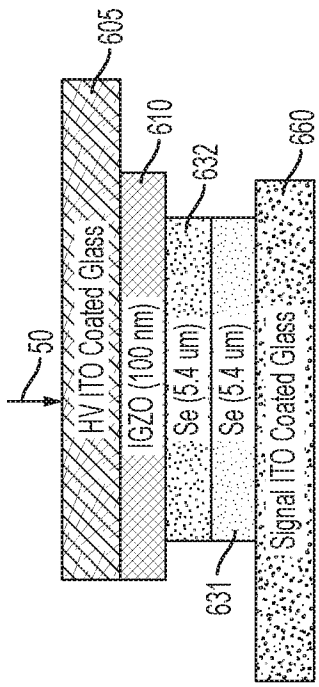
605
610
632
660
50
HV ITO Coated Glass
IGZO (100 nm)
Se (5.4 um)
Se (5.4 um)
Signal ITO Coated Glass
631

FIG. 4A

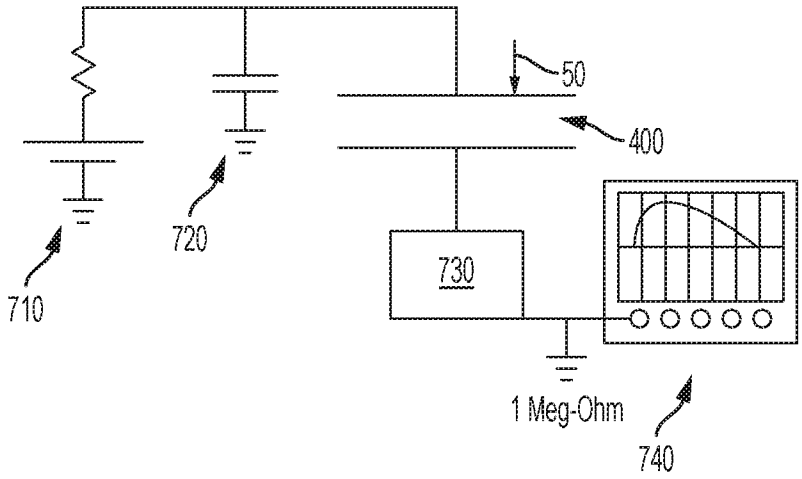

FIG. 5

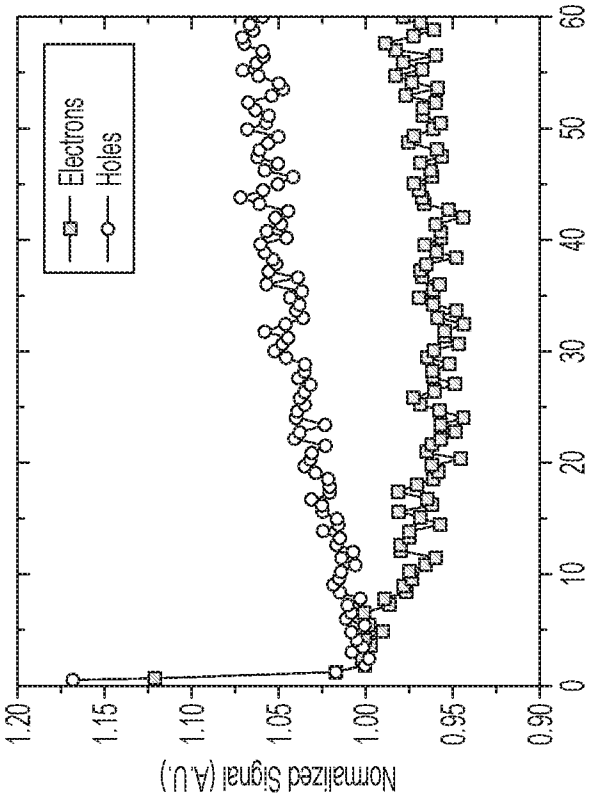
Electrons
Holes
Normalized Signal (A.U.)
Time (min)
1.20
1.15
1.10
1.05
1.00
0.95
0.90
0
10
20
30
40
50
60

FIG. 7

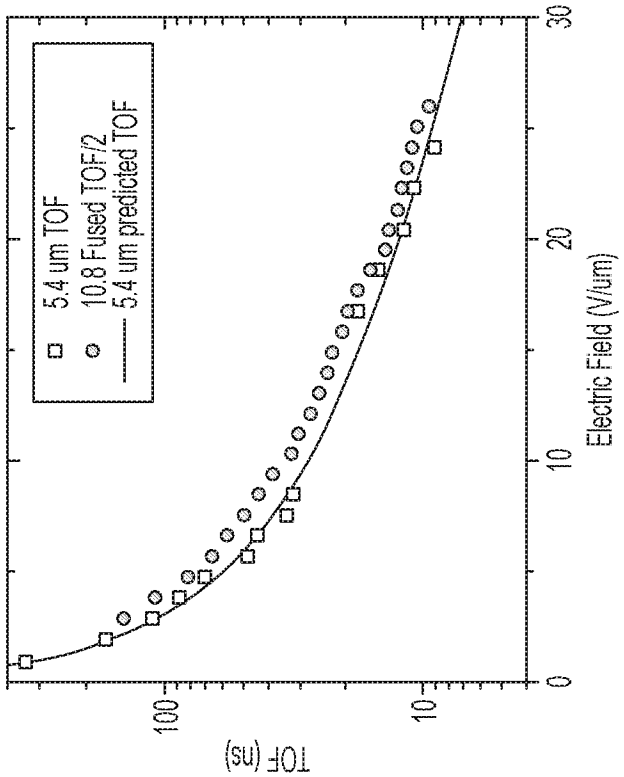
5.4 um TOF
10.8 Fused TOF/2
5.4 um predicted TOF
TOF (ns)
Electric Field (V/um)
100
10
0
10
20
30

FIG. 6

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US17/63857

A. CLASSIFICATION OF SUBJECT MATTER

IPC - H01L 31/0272, 31/0376, 31/115; H01L 27/14, 27/146 (2018.01)

CPC - H01L 31/0272, 31/0376, 31/115; H01L 27/14, 27/146

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

See Search History document

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

See Search History document

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

See Search History document

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X - Y	US 2011/0163305 A1 (OGUSU, K et al.) July 7, 2011; abstract; figures 1-3, 5; paragraphs [0021], [0070], [0083]-[0084], [0088], [0090]	15, 18 - 16-17
Y	(ZHOU, J et al.) Flexible piezotronic strain sensor. Nano Letters. August 16, 2008; abstract; page 3039, right column, fifth paragraph, lines 13-14	16
Y	US 2009/0163014 A1 (LEE, KH et al.) June 25, 2009; figures 3-4; paragraphs [0002], [0017]	17
A	US 2015/0171232 A1 (The Research Foundation for The State University of New York) June 18, 2015; figures 1-3; paragraph [0031]	1-14
A	US 2016/0111473 A1 (General Electric Company) April 21, 2016; *entire document*	1-14
A	US 2014/0217284 A1 (SO, F et al.) August 7, 2014; entire document	1-14

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:

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"E" earlier application or patent but published on or after the international filing date

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
12 January 2018 (12.01.2018)	27 FEB 2018
Name and mailing address of the ISA/ Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-8300	Authorized officer Shane Thomas PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

Form PCT/ISA/210 (second sheet) (January 2015)