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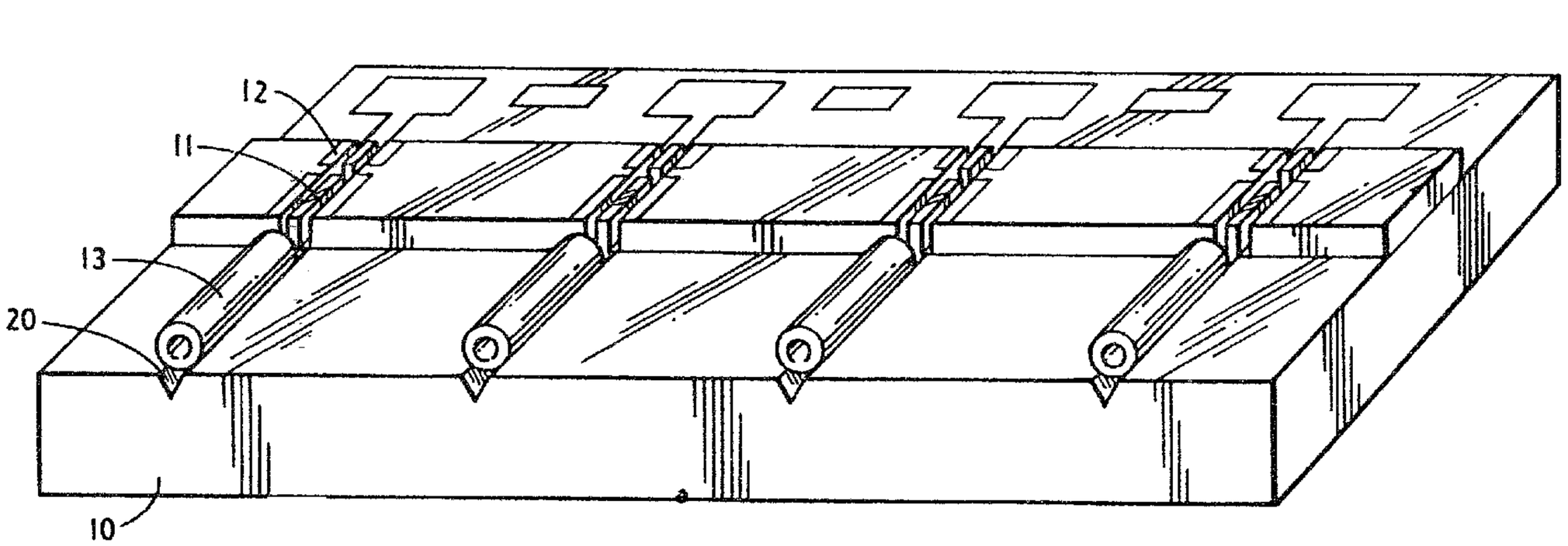
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(54) Title: A MONOLITHICALLY INTEGRATED SEMICONDUCTOR STRUCTURE AND METHOD OF FABRICATING SUCH STRUCTURE



(57) Abrégé/Abstract:
A heterostructure device includes a ridge-waveguide laser (11) monolithically integrated with a ridge-waveguide rear facet monitor [RFM] (12). An integral V-groove etched directly into the device substrate (10) enables passive alignment of an optical fiber (13) to the active region (11-1) of the laser (11). The laser and RFM facets were formed using an in-situ multistep reactive ion etch process.

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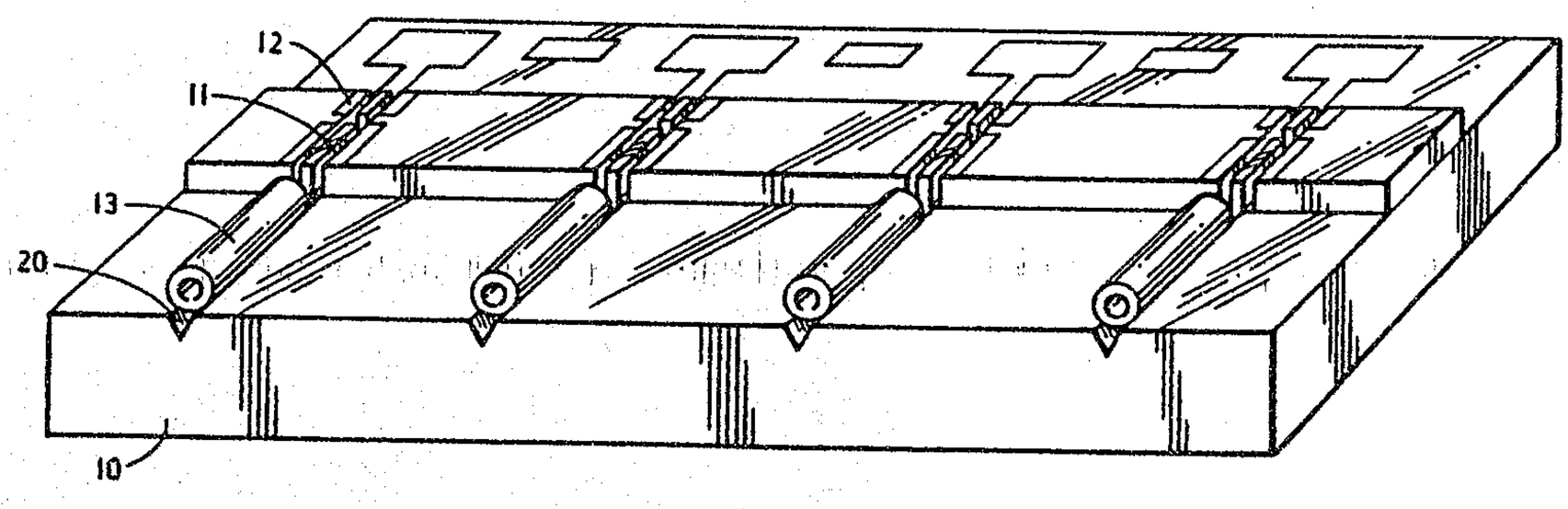
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(54) Title: A MONOLITHICALLY INTEGRATED SEMICONDUCTOR STRUCTURE AND METHOD OF FABRICATING SUCH STRUCTURE



(57) Abstract

A heterostructure device includes a ridge-waveguide laser (11) monolithically integrated with a ridge-waveguide rear facet monitor [RFM] (12). An integral V-groove etched directly into the device substrate (10) enables passive alignment of an optical fiber (13) to the active region (11-1) of the laser (11). The laser and RFM facets were formed using an in-situ multistep reactive ion etch process.

A MONOLITHICALLY INTEGRATED SEMICONDUCTOR STRUCTURE AND METHOD OF FABRICATING SUCH STRUCTURE

Technical Field

The present invention relates to semiconductor structures and, more particularly, to a monolithically integrated laser, detector, and fiber-receiving channel.

Background Art

Development of monolithically integrated photonic circuits will enhance the functionality, reliability, and cost effectiveness of optical subsystems. However, the packaging of both discrete devices and optoelectronic integrated circuits (OEICs) often requires active alignment of optical fiber pigtails that substantially increases the cost of such components. Techniques for cost-effective fiber coupling of lasers, using passive rather than active alignment, have been demonstrated using separate silicon substrates that incorporated V-grooves for fiber placement.

In particular, mechanical features such as fiducials are etched into a silicon substrate platform, and serve as reference pedestals for positioning a chip which abuts against the pedestals.

Examples of prior art alignment techniques may be found in Armiento et al., "Passive Coupling of InGaAsP/InP Laser Array and Single-Mode Fibers using Silicon Waferboard," Electronic Letters, pp. 1109-1110 (1991), Cohen et al., "Passive Laser-Fiber Alignment by Index Method," IEEE Trans. Phot. Tech. Letters, Vol. 3, pp. 985-987 (1991), and U.S. Patent No. 5,077,878.

Disclosure of Invention

In one aspect of the present invention, a semiconductor structure comprises a fiber-receiving channel, an optical detection region, and a lasing region

interposed between and in monolithic serial integration with said fiber-receiving channel and said optical detection region.

In another aspect of the present invention, a method of fabricating a device structure from a starting wafer having a heterostructure material grown on a substrate, comprising the steps of: masking the wafer with a first mask pattern having exposure windows corresponding to device regions of said wafer; controllably etching through the exposed device regions of said wafer, patterned by the first mask pattern, to define a ridge waveguide area and a fiber-receiving area; masking the wafer with a second mask pattern having exposure windows corresponding to areas for forming facet surfaces in said ridge waveguide area; controllably etching through the exposed regions of said wafer, patterned by the second mask pattern, to define a lasing region and a detection region; masking the wafer with a third mask pattern having an exposure window corresponding to said fiber-receiving area; and controllably etching through the exposed regions of said wafer, patterned by the third mask pattern, to define a fiber-receiving channel in said wafer.

Brief Description of Drawings

The details of the invention will be described in connection with the accompanying drawing, in which:

Figure 1 is a cross-sectional view of an integrated device structure in accordance with the present invention;

Figure 2 illustrates an upper perspective view of a monolithic array including a plurality of the device structures in Figure 1;

Figure 3 shows the optical output power from a laser facet and the corresponding detected current level as a function of laser drive current for the Figure 1 device structure;

Figure 4 shows the responsivity of a rear facet monitor in accordance with the present invention;

Figure 5 plots the optical power introduced into a single-mode and multi-mode fiber integrated with the device structure in Figure 1; and

Figures 6-10 present perspective and cross-sectional views illustrating a sequence of process steps for fabricating an integrated device structure in accordance with a preferred embodiment of the present invention.

As noted above, conventional approaches to integrating an optoelectronic component with an optical fiber have involved an active alignment procedure requiring the component to be powered while the fiber is actively manipulated into alignment. Recent work has avoided active alignment processes by using substrate platforms with alignment pedestals and standoffs or fiducials. Advantageously, the present invention detailed below incorporates the laser with an integral V-groove that enables passive fiber alignment without the need for a hybrid substrate such as silicon.

Best Mode for Carrying Out the Invention

The present invention shown illustratively in Figure 1 concerns a device structure and fabrication method for monolithically integrating a laser, detector, and fiber-receiving channel. As indicated in the cross-sectional view, a lasing region 11 with active laser 11-1 is monolithically integrated with an adjacent detecting region 12 with active layer 12-1. Although not shown, a fiber-receiving channel is etchably formed in substrate 10 adjacent lasing region 11 for receiving a fiber 13 having core 14. When sufficient drive current is applied to the lasing region, light is transmitted from a front facet of laser 11 in a forward direction towards fiber 13, and is transmitted from a rear facet of laser 11 in a rearward direction towards detector 12.

Preferably, the detection region 12 is a rear facet monitor (RFM) photodetector serving to monitor the optical output of the lasing region 11 so that the laser drive current from a driver circuit (not shown) can be adjusted to maintain a desired output power in optical signal 15. As will be detailed below, regions 11 and 12 are fabricated from a common initial wafer structure; accordingly, the active layers 11-1 and 12-1 are in strict coaxial alignment. The processing of the fiber-receiving channel is appropriately controlled so that when fiber 13 is positioned in the channel, core 14 is in substantial coaxial alignment with the active layer 11-1.

Figure 2 shows a monolithically integrated array of four device structures each conforming to the device assembly in Figure 1. For purposes of clarity and consistency, similar structures among the drawings are designated with like numerals. Each of the individual device structures includes a respective fiber-receiving channel 20 preferably etched in the shape of a V-groove for receiving a fiber 13.

The performance of the device structure according to the present invention was evaluated by obtaining a variety of measurements. The laser/RFM characteristics were measured on unpackaged devices while operating in a pulsed mode. Measurement of the relative light-current characteristics of the devices was performed in wafer form by probing the integrated photodetector.

Figure 3 shows the optical power from the front laser facet (curve 31) and the corresponding photocurrent detected by the RFM (curve 32) as a function of laser drive (LD) current. A device with the V-groove removed was used to make this measurement. The graph indicates a device with a laser threshold current of 40mA and an RFM responsivity of 0.36 A/W. Measurements obtained over a variety of device structures revealed threshold currents as low as 38 mA and RFM responsivities as high as 0.49

A/W. Figure 4 plots RFM responsivity versus laser optical power. The optical characteristics of an integrated laser/RFM structure passively coupled to optical fibers in accordance with the present invention is shown in Figure 5. In particular, measurements of such optical characteristics were obtained by placing a single-mode fiber (SMF) or multi-mode fiber (MMF) in the V-groove. The measurements indicated coupling efficiencies as high as 8% and 18% for single-mode and multi-mode fibers, respectively.

Figures 6-10 represent successive intermediate views of a device structure undergoing processing to fabricate the monolithically integrated device structure of the present invention. Although the following discussion of the fabrication steps is directed to a specific material system and geometry in accordance with a preferred embodiment, this should not serve as a limitation of the present invention as it should be obvious to those skilled in the art that other material systems and dimensions are possible within the scope of the present invention.

Figure 6 shows a structure illustrating the first step of the fabrication sequence (discussed below). Prior to commencement of the fabrication process, however, a starting wafer structure was provided including substrate 10 and layers 61-65. In particular, a double heterostructure layer material was grown by metallorganic vapor phase epitaxy (MOVPE). The layers included a p-InGaAs ohmic contact layer 65 (Zn-doped $2x10^{19}cm^{-3}$), a p-InP upper cladding layer 64 (Zn-doped $1x10^{18}cm^{-3}$, an undoped InGaAsP etch stop layer 63 (λ=.0 μm), an undoped InGaAsP active layer 62 (λ=1.3μm) and a 4.0 μm n-InP lower cladding layer 61 grown on a (100) n^{+}-InP substrate 10.

In general, many of the fabrication steps for the monolithically integrated laser/RFM/V-groove device utilize a reactive ion etching (RIE) process. The RIE

process is performed in a computer-controlled reactive ion etch system equipped with four separate etch chambers, each with a different etch chemistry. The RIE system has a load lock chamber and a central transfer chamber with a robotic arm for wafer transfer between the four etch chambers. An illustrative discussion of an RIE system may be found in Rothman et al., "Multichamber RIE Processing for InGaAsP Ridge Waveguide Laser Arrays," Mat. Res. Soc. Symp. Proc., Vol. 242, pp. 341-348 (1992).

The fabrication sequence for the integrated device structure commences with the deposition of a layer of SiN_x on the as-grown starting wafer using a Plasma Tech. PECVD machine. The process 1 step 3 timer of the PECVD machine is set to 16 minutes for depositing an SiN layer of 200 nm thickness. A buffered HF etch lasting 15 seconds precedes the SiN_x deposition.

A first lithographic pattern is then developed having mask openings defining the ridge-waveguide and the area for the fiber-receiving channel. In particular, the ridge waveguide region corresponds to the laser and RFM structures, and the channel area refers to the V-groove region. The use of one mask level for the ridge and V-groove structures ensures precise alignment and spacing of the laser ridge and the V-groove. The pattern is developed with the following steps:

a) spin HMDS at 5 krpm for 60s;
b) spin Shipley 2400 at 5 krpm for 60s;
c) bake at 90°C for 20 minutes;
d) align the proper orientation of the wafer to the mask via the cleaved edge;
e) expose mask with ST mode on Karl Suss 300 mask aligner for 13s; and
f) develop mask in solution (1 part of Az 2401 to 4 parts of water) for 75s.

The photoresist pattern is then transferred to the SiN_x layer using an SF_6-based RIE process. In particular, the patterned SiN_x layer is etched in an SF_6 plasma for 2 minutes, followed by an oxygen plasma etch for 10 minutes. The wafer structure after the patterned etch step is shown in the perspective view of Figure 6, with SiN_x layer 66 being etched in accordance with the photoresist pattern to expose selected regions of contact layer 65.

A reactive ion etching (RIE) step is then used to etch through the exposed regions of the contact layer 65 and the underlying cladding layer 64. Specifically, a dry etch using a $CH_4/H_2/Ar$ plasma is executed for 30 minutes, the depth of the etch is measured, and the dry etching is continued until the etch depth is within 0.25 μm of the etch stop layer 63. Prior to the wet etch, the wafer is cleaned by being boiled sequentially in acetone and isopropyl alcohol (10 minutes each), and blown dry in N_2. The wet chemical etch uses an 8:1 H_3PO_4/HCl mixture, and lasts for 5 minutes. A perspective view of the wafer structure following the dry etch and wet chemical etch is shown in Figure 7A.

Figure 7B shows a front cross-sectional view of the Figure 7A structure after the remainder of the original SiN_x layer 66 is removed in buffered HF. The wafer is then rinsed in DI water and blown dry in N_2.

A second SiN_x layer is then deposited on the wafer of Figure 7B to protect the wafer during a subsequent processing step (detailed below) which patterns p-ohmic metal (AuZn) and final metal (TiAu) on the ridge. For the SiN_x deposition step, shown illustratively in the front cross-sectional view of Figure 8, the Plasma Tech. PECVD Process 2 step 5 timer is set to 32 minutes and an SiN_x layer 81 of 400 nm thickness is deposited. The metal patterning on the ridge structure of the RFM and laser regions is performed by the steps described below.

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A second lithography pattern is formed to define exposure areas corresponding to the ridge structure of the wafer. The pattern is formed with the following steps:

(a) spin HMDS at 5 krpm for 60s;

(b) spin AZ 1450 at 5 krpm for 5s and at 1 krpm for 25s;

(c) bake mask at 90°C for 20 minutes;

(d) align and expose mask with ST mode on Karl Suss 300 mask aligner for 25s; and

(e) develop mask in solution (1 part of AZ 351 to 5 parts of water) for 75s.

The mask pattern is then transferred to the wafer and the exposed SiN_x on the ridge structure is removed by etching the SiN_x in an SF_6 plasma for 4 minutes. The exposed underlying contact layer is cleaned by etching in an 80:1:1 mixture of $H_2O/H_2O_2/H_2SO_4$ for 20s, rinsed in DI water, and then blown dry in N_2. A 200 nm-thick layer 65 of Au:Zn is then deposited on the entire wafer, and lifted off in acetone by boiling and spraying, which leaves Au-Zn on the ridge structure only. The Au:Zn layer is alloyed by placing the wafer face-up in a Heat Pulse 210 assembly, manually raising the temperature to 400°C by using 30% power level, and remaining at this temperature for 10s before terminating power. The wafer is then cooled to 100°C before being removed from the assembly.

Figure 9A is a perspective view of the structure resulting from the processing steps (detailed below) for depositing the final metal on the wafer, and for forming the vertical facet surfaces in the ridge waveguide area to define the individual RFM and laser structures. The facet surfaces, in particular, are produced by a reactive ion etching step.

For depositing the final metal on the wafer, a third lithographic pattern is formed to define exposure areas corresponding to surfaces 92-95 in Figure 9A. The third lithographic pattern is formed with the following steps:

(a) spin HMDS at 5 krpm for 60s;

(b) spin AZ 2400 at 5 krpm for 60s;

(c) bake at 90°C for 20 minutes;

(d) align and expose mask with ST mode on Karl Suss 300 mask aligner for 30s; and

(e) develop mask in 4:1 solution of H_2O/AZ 2401 for 30s.

The Ti/Au is then deposited on the patterned wafer in accordance with the following steps:

(a) etch SiN in SF_6 plasma for 25s;

(b) etch in oxygen plasma for 60 minutes;

(c) deposit 50 nm of Ti and 500 nm of Au on the top surface, and preferably tilting around the ridge line 45° either way alternately to improve step coverage;

(d) lift off in acetone by boiling and spraying; and

(e) etch in SF_6 plasma for 4 minutes.

The fabrication process proceeds next with formation of the vertical facet surfaces.

As preparation for defining the individual RFM and laser device structures in the ridge waveguide region, a third SiN_x layer is deposited on the wafer. In particular, the Plasma Tech. PECVD machine process 2 step 5 timer is set to 32 minutes, and a 400 nm-thick layer of SiN_x is deposited. A fourth lithographic pattern is then formed to define exposure areas corresponding to regions of facet formation in the wafer. The pattern is formed with the following steps:

(a) spin HMDS at 5 krpm for 60s;

(b) spin AZ4400 at 5 krpm for 60s;

(c) bake mask at 90°C for 60 minutes;

(d) expose mask on Karl Suss mask aligner for 15s; and

(e) develop mask in 3:1 solution of H_2O/AZ 400K for 90s.

The SiN_x layer is then patterned using the above mask, and then etched in an SF_6 plasma for 3 minutes to expose

regions of the wafer corresponding to desired areas of facet formation. A dry RIE etching step followed by a wet chemical etch step are used to etch through the active layer to a depth of 4 μm and yield smooth vertical facet surfaces. The dry etch involves etching in oxygen plasma for 5 minutes, and reactive ion etching in a $CH_4/H_2/Ar$ plasma at 300Å/min. until a depth of 4 μm is reached. The wet etch uses an 8:1 mixture of H_3PO_4/HCl for 30s to straighten the face walls.

As shown in the perspective view of Figure 9A, the facet formation during the RIE etching stop provides channels separating the laser and RFM, and separating the laser and V-groove area. The RIE etching step also removes a portion of the wafer above the substrate that is adjacent to and bordering the ridge-waveguide and V-groove areas. The final processing step involves the formation of a fiber-receiving channel in the wafer. In particular, a V-groove geometry is etched into the region of the wafer which is forward the lasing region.

As preparation for forming the V-groove in the wafer, a fourth layer 91 of SiN_x is deposited on the wafer. The Plasma Tech. PECVD machine process 2 step 5 timer is set to 32 minutes, and a 400 nm-thick layer of SiN is deposited. A fifth lithographic pattern is then formed to define an exposure area corresponding to the desired V-groove area. In particular, the mask pattern protects the laser/RFM structure while exposing the V-groove area during a subsequent deep etching step (detailed below). The pattern is formed with the following steps:

(a) spinning HMDS at 5 krpm for 60s;

(b) spinning AZ4400 at 5 krpm for 60s;

(c) baking at 90°C for 60 minutes;

(d) exposing mask on Karl Suss 400 mask aligner for 15s; and

(e) developing mask in 3:1 solution of H_2O/AZ 400k for 90s.

The wafer is then patterned with the mask, and the SiN_x layer 91 is etched in an SF_6 plasma for 4 minutes to expose the underlying etch stop layer 63 in the V-groove area. A portion 96 of the contact layer 65 is also exposed. Figure 9B shows a front cross-sectional view of the V-groove area following the patterned etching of SiN_x layer 91.

The V-groove geometry is defined by a dry reactive ion etching (RIE) step followed by a wet chemical etch. In particular, the dry etch involves etching in oxygen plasma for 5 minutes, and etching in a $CH_4/Ar/H_2$ plasma for 30 minutes. The wet etch uses a 1:1 mixture of HCl/CH_3COOH for 15 minutes, and is followed by etching of the remaining SiN layer in SF_6 plasma for 4 minutes. The etching steps reveal the (112)A crystal plane at an angle of 35° with respect to the (100) wafer surface. A perspective and front cross-sectional view of the final structure are shown in Figures 10A and 10B, respectively. As shown, a step-like border is produced on the edges of the V-groove by etching down to the etch stop layer.

The V-groove has a depth of 44.7 µm. The end of the groove is the vertical (110) plane, which serves as a mechanical stop to ensure accurate and reproducible spacing between the laser facet and the end of the fiber. The vertical plane of the groove also protects the laser facet from mechanical damage during the fiber insertion process.

The fabricated structure includes a 3 µm-wide ridge waveguide for both the laser and RFM structures, which are separated by a 5 µm-wide channel. The laser cavity length was 300 µm, and the length of the RFM section was 150 µm. The width and depth of the V-groove was controllably etched so that the core of an optical fiber inserted in the V-groove was aligned to the active region of the laser.

Preferably, the fabrication process includes formation of an SnAu n-ohmic contact metallization on the substrate. This back metallization is accomplished by depositing 10 nm of Sn, 30 nm of Au, 50 nm of Ti, and 200 nm of Au on the back of the wafer, and then alloying the metal deposits.

Although the processing steps detailed above and shown in the Figures concern the formation of a single RFM/laser/V-groove structure, it should be obvious to those skilled in the art that a plurality of such structures may be fabricated on a single wafer using the appropriate lithographic mask patterns. A wafer with a plurality of fabricated RFM/laser/V-groove device structures may then be sawed into individual bars each having an array of such device structures, as shown in Figure 2 for example.

While there has been shown and described what are at present considered the preferred embodiments of the invention, it will be obvious to those skilled in the art that various changes and modifications can be made therein without departing from the scope of the invention as defined by the appended Claims.

CLAIMS

1. A monolithically integrated semiconductor structure, comprising:
a fiber-receiving channel;
an optical detection region; and
a lasing region interposed between and in serial alignment with said fiber-receiving channel and said optical detection region.

2. The monolithically integrated semiconductor structure as recited in claim 1 further comprising:
a V-groove within said fiber-receiving channel;
an optical fiber positionable within said V-groove; and
a rear facet monitor structure within said detection region.

3. The semiconductor structure as recited in claim 1 wherein:
said optical detection region and said lasing region each include a ridge waveguide structure.

4. The semiconductor structure as recited in claim 1 further comprises:
an InP substrate;
a first InP cladding layer;
an InGaAsP active layer;
an InGaAsP etch stop layer;
a second InP cladding layer; and
an InGaAs ohmic contact layer.

5. A method of fabricating a device structure from a starting wafer having a heterostructure material grown on a substrate, comprising the steps of:

masking the wafer with a first mask pattern having exposure windows corresponding to device regions of said wafer;

controllably etching through the exposed device regions of said wafer, patterned by the first mask pattern, to define a ridge waveguide area and a fiber-receiving area;

masking the wafer with a second mask pattern having exposure windows corresponding to areas for forming facet surfaces in said ridge waveguide area;

controllably etching through the exposed regions of said wafer, patterned by the second mask pattern, to define a lasing region and a detection region;

masking the wafer with a third mask pattern having an exposure window corresponding to said fiber-receiving area; and

controllably etching through the exposed regions of said wafer, patterned by the third mask pattern, to define a fiber-receiving channel in said wafer.

6. The method as recited in claim 5 wherein the step of controllably etching through the exposed device regions of said wafer to define a ridge waveguide area and a fiber-receiving area includes the step of:

reactively ion etching the exposed device regions until reaching the etch stop layer.

7. The method as recited in claim 5 further includes the steps of:

prior to masking the wafer with a second mask pattern, patterning ohmic metal and final metal on said ridge waveguide area.

8. The method as recited in claim 5 wherein the step of

controllably etching through the exposed regions of said wafer to define a lasing region and a detection region includes the step of:

reactively ion etching the exposed regions to a depth below the active layer.

9. The method as recited in claim 5 wherein the step of controllably etching through the exposed regions of said wafer to define a fiber-receiving channel in said wafer includes the step of:

reactively ion etching the exposed regions of said wafer to form said fiber-receiving channel.

10. The method as recited in claim 9 wherein said fiber-receiving channel includes a V-groove geometry.

11. A monolithically integrated wafer assembly, comprising:

a plurality of fiber-receiving channels;

a plurality of optical detection regions each associated with a respective fiber-receiving channel; and

a plurality of lasing regions each interposed between and in serial alignment with a respective fiber-receiving channel and its associated optical detection region.

12. The monolithically integrated wafer assembly as recited in claim 11 further comprising:

a V-groove within each of said fiber-receiving channels; and

a rear facet monitor structure within each of said detection regions.

13. The monolithically integrated wafer assembly as recited in claim 11 wherein each of said optical detection regions and lasing regions comprises:
a ridge waveguide structure.

14. A monolithically integrated optical assembly, comprising:
a plurality of light detection means;
a plurality of channels each associated with a respective light detection means; and
a plurality of light generating means each interposed between and optically accessible to a respective light detection means and a respective light-guiding means positionable within the channel associated with said light detection means.

15. The monolithically integrated optical assembly as recited in claim 14 wherein:
each of said light detection means includes a rear facet monitor photodetector;
each of said channels includes a V-groove; and
each of said light generating means includes a laser.

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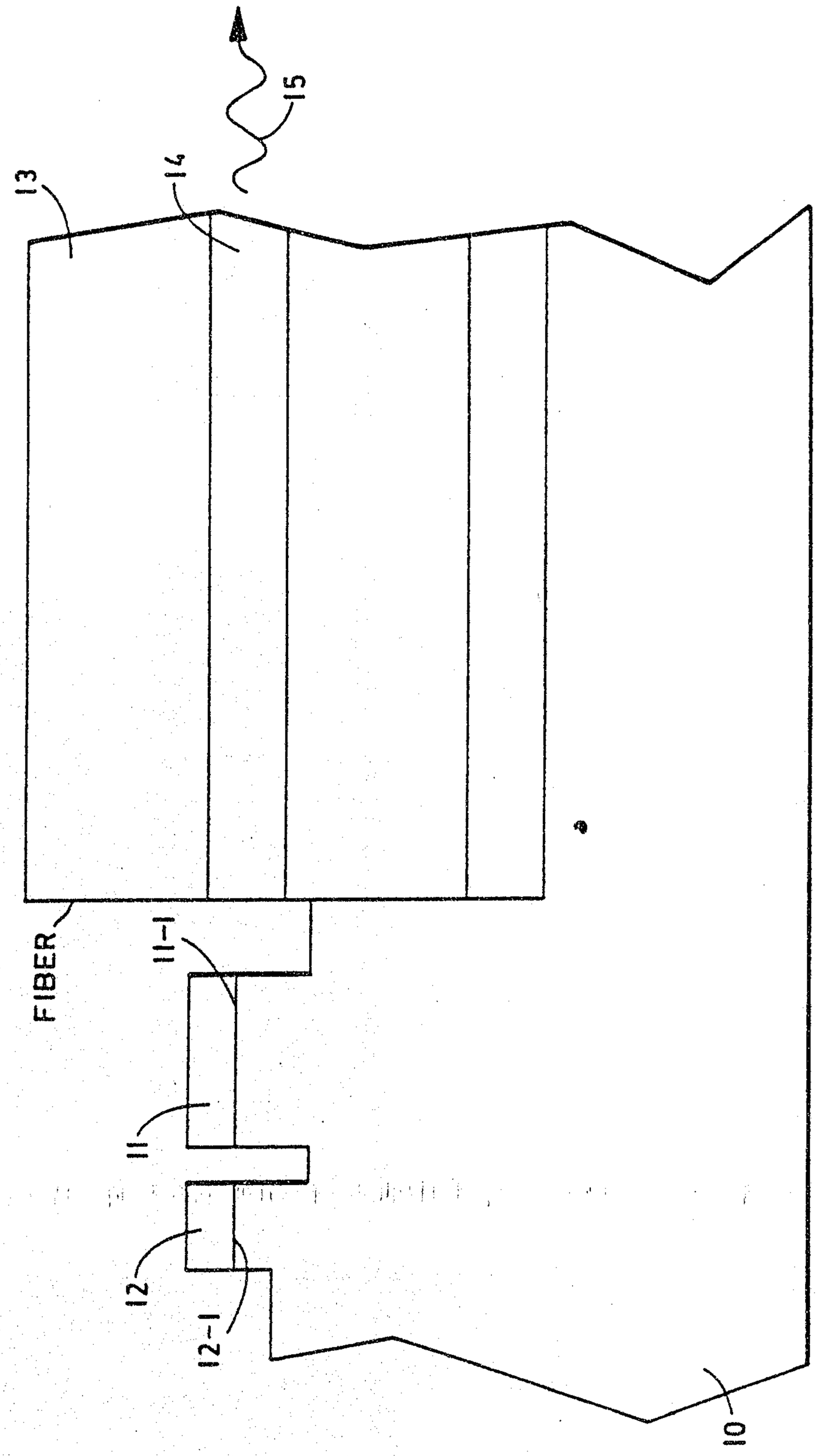


FIG. 1

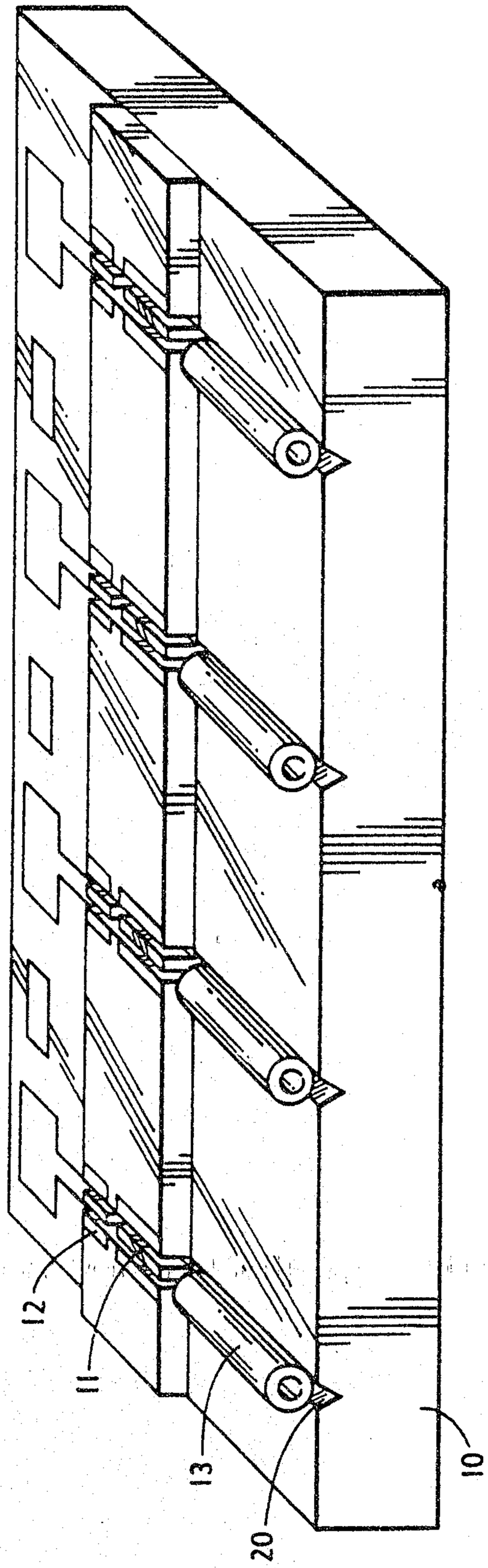


FIG. 2

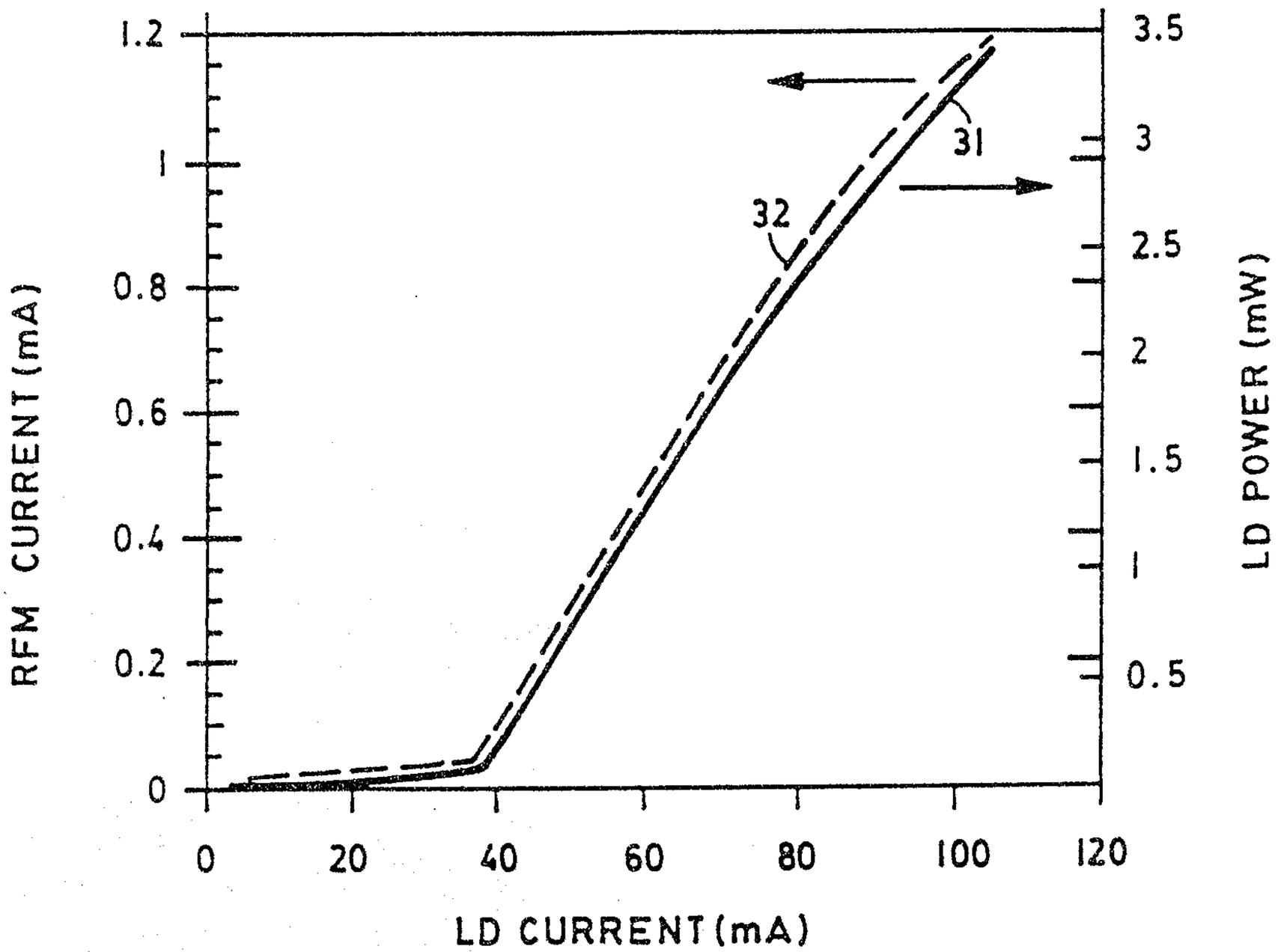

1.2
1
0.8
0.6
0.4
0.2
0
RFM CURRENT (mA)
3.5
3
2.5
2
1.5
1
0.5
LD POWER (mW)
31
32
0
20
40
60
80
100
120
LD CURRENT (mA)

FIG. 3

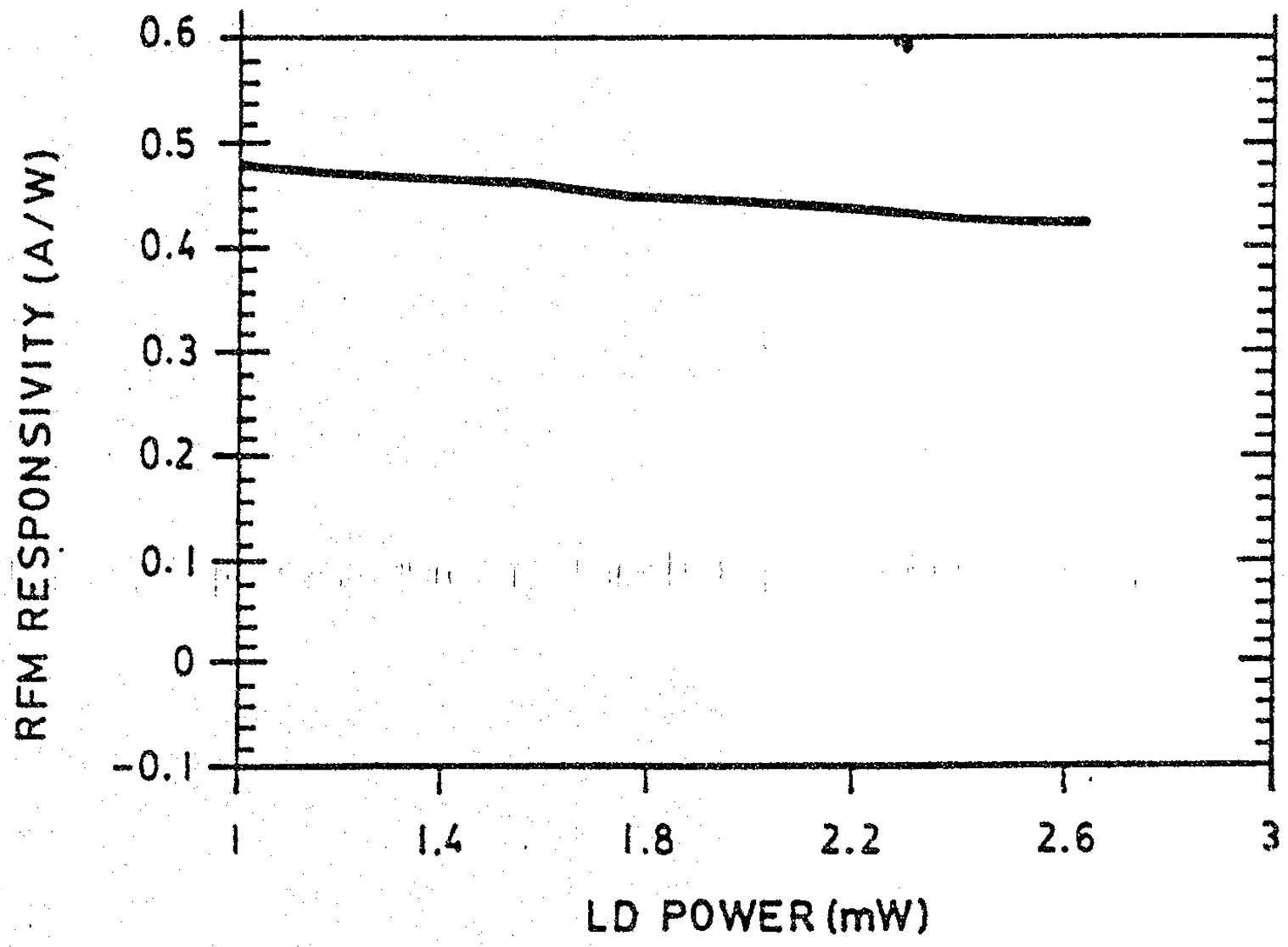

0.6
0.5
0.4
0.3
0.2
0.1
0
-0.1
RFM RESPONSIVITY (A/W)
1
1.4
1.8
2.2
2.6
3
LD POWER (mW)

FIG. 4

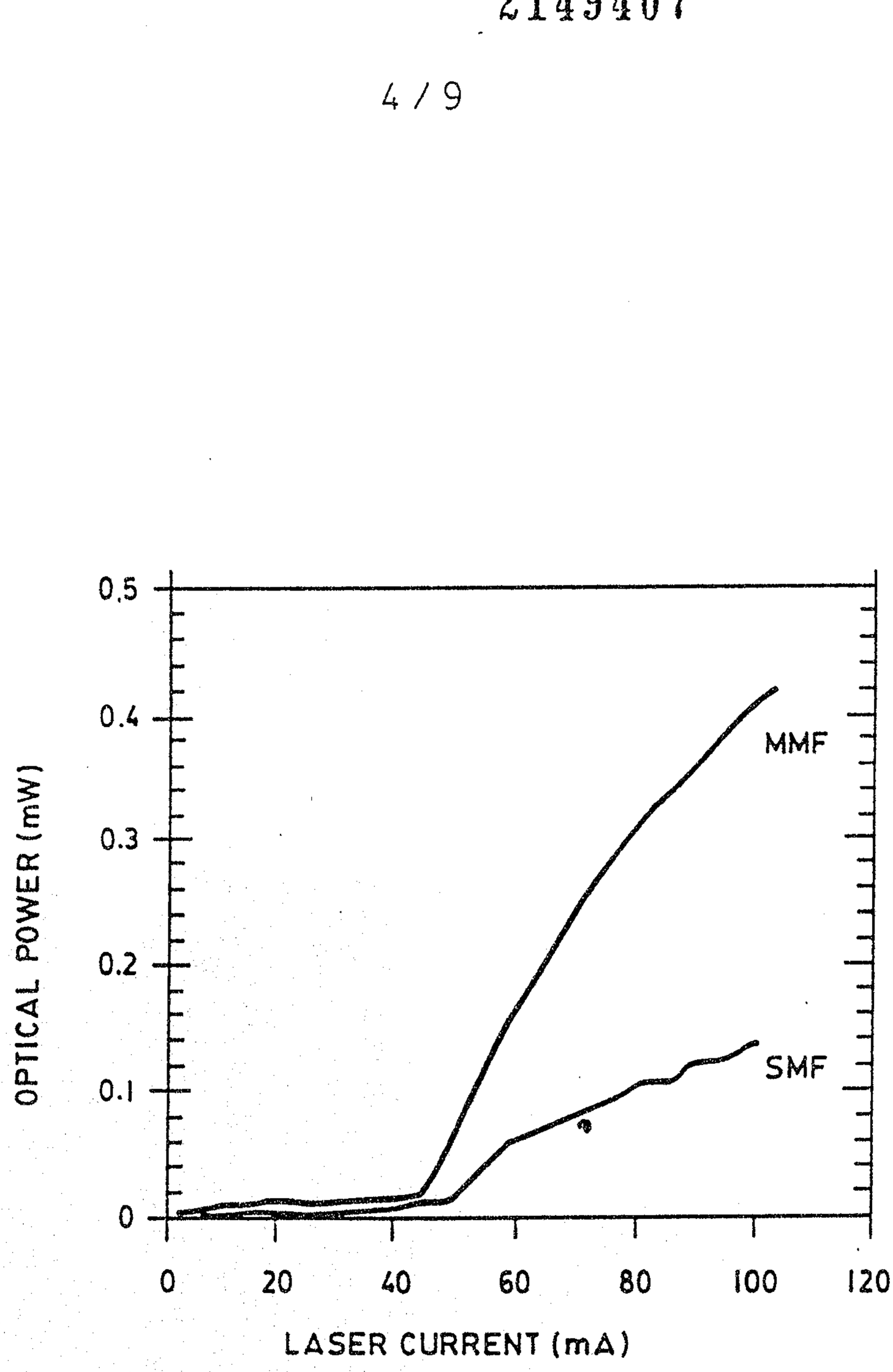

0.5
0.4
0.3
0.2
0.1
0
OPTICAL POWER (mW)
MMF
SMF
0
20
40
60
80
100
120
LASER CURRENT (mA)

FIG. 5

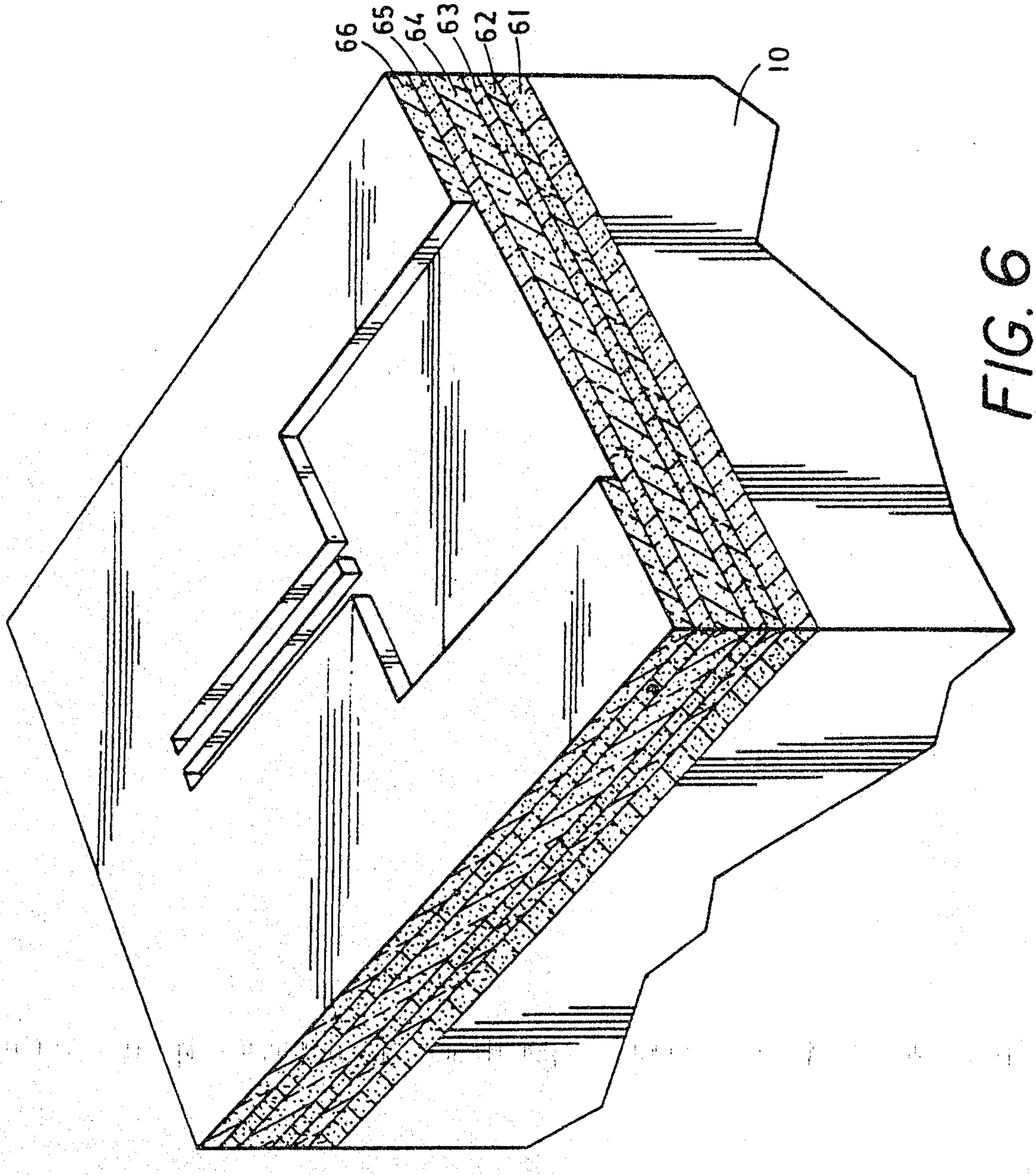


FIG. 6

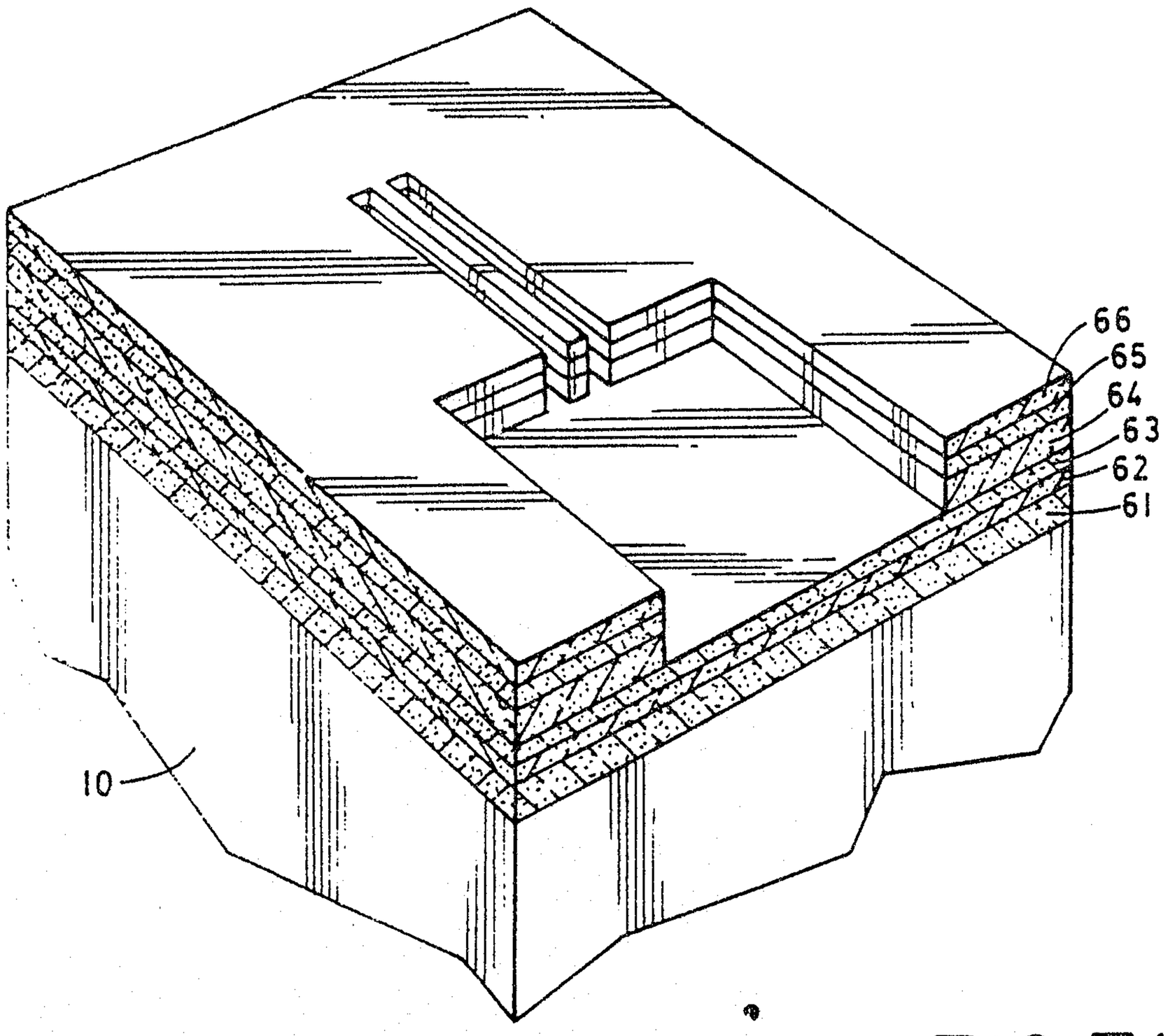


FIG. 7A

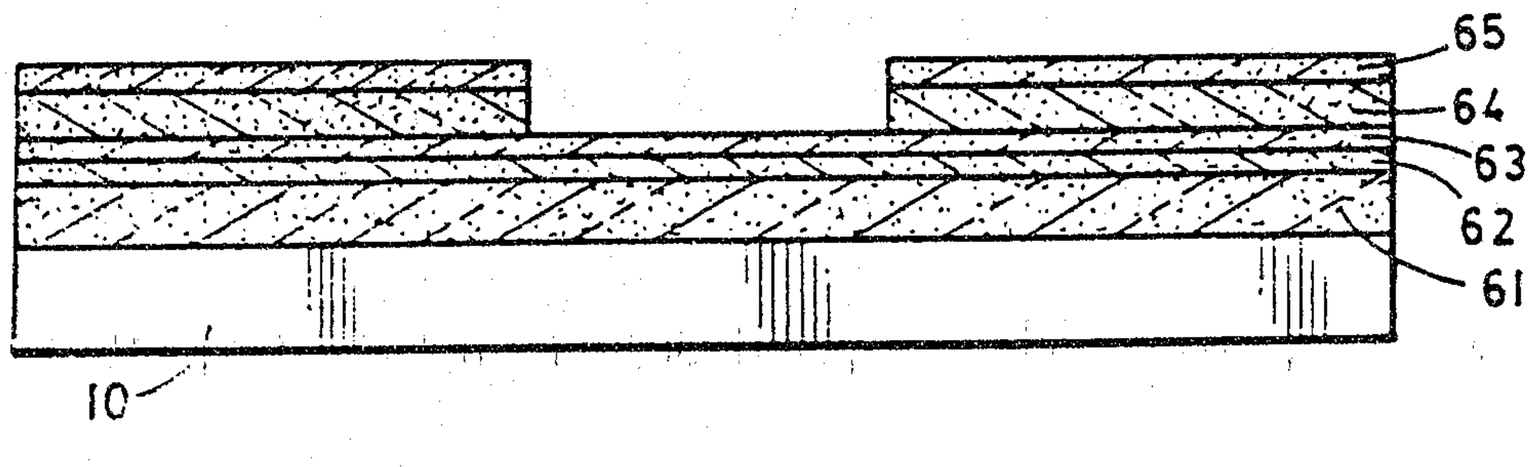


FIG. 7B

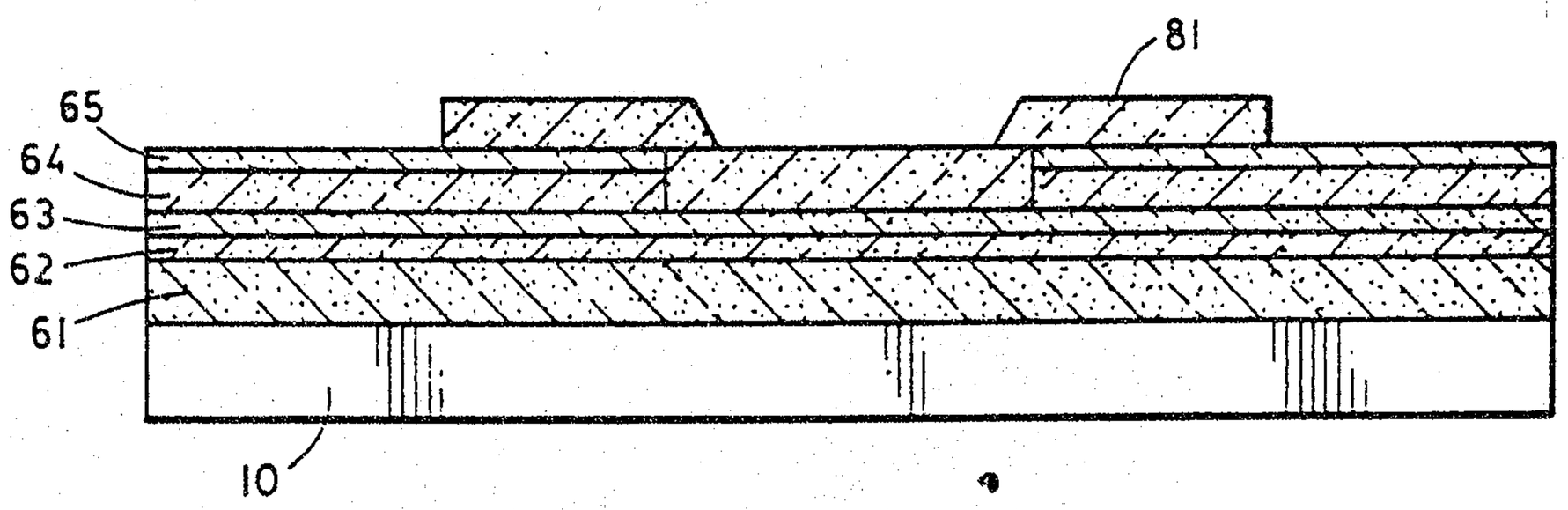


FIG. 8

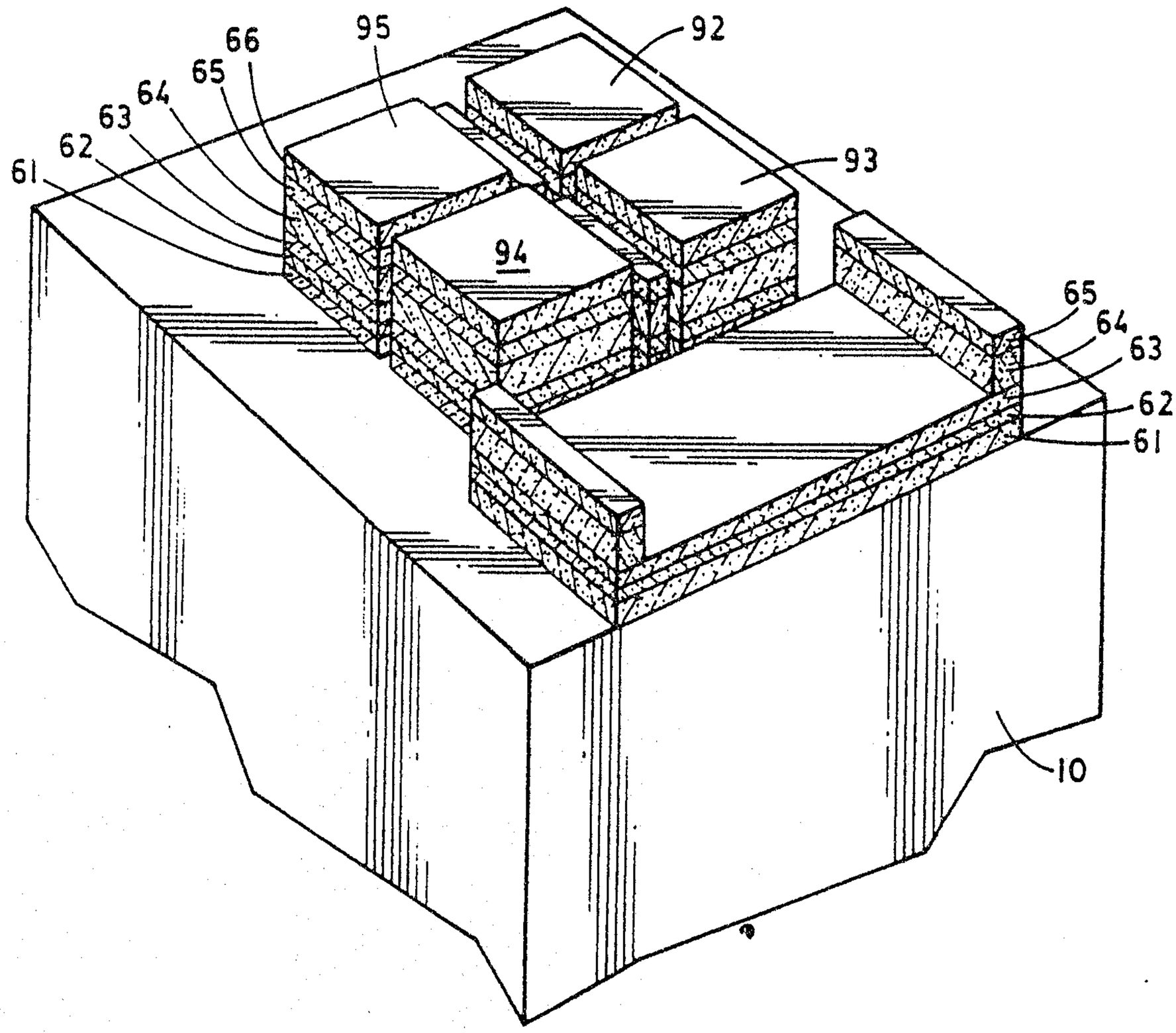


FIG. 9A

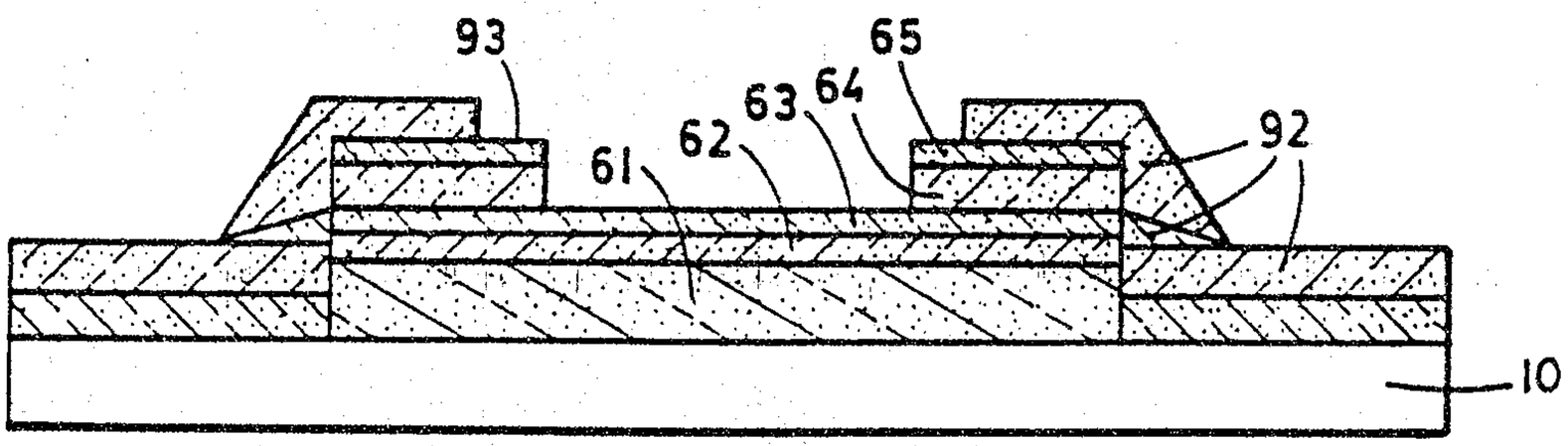


FIG. 9B

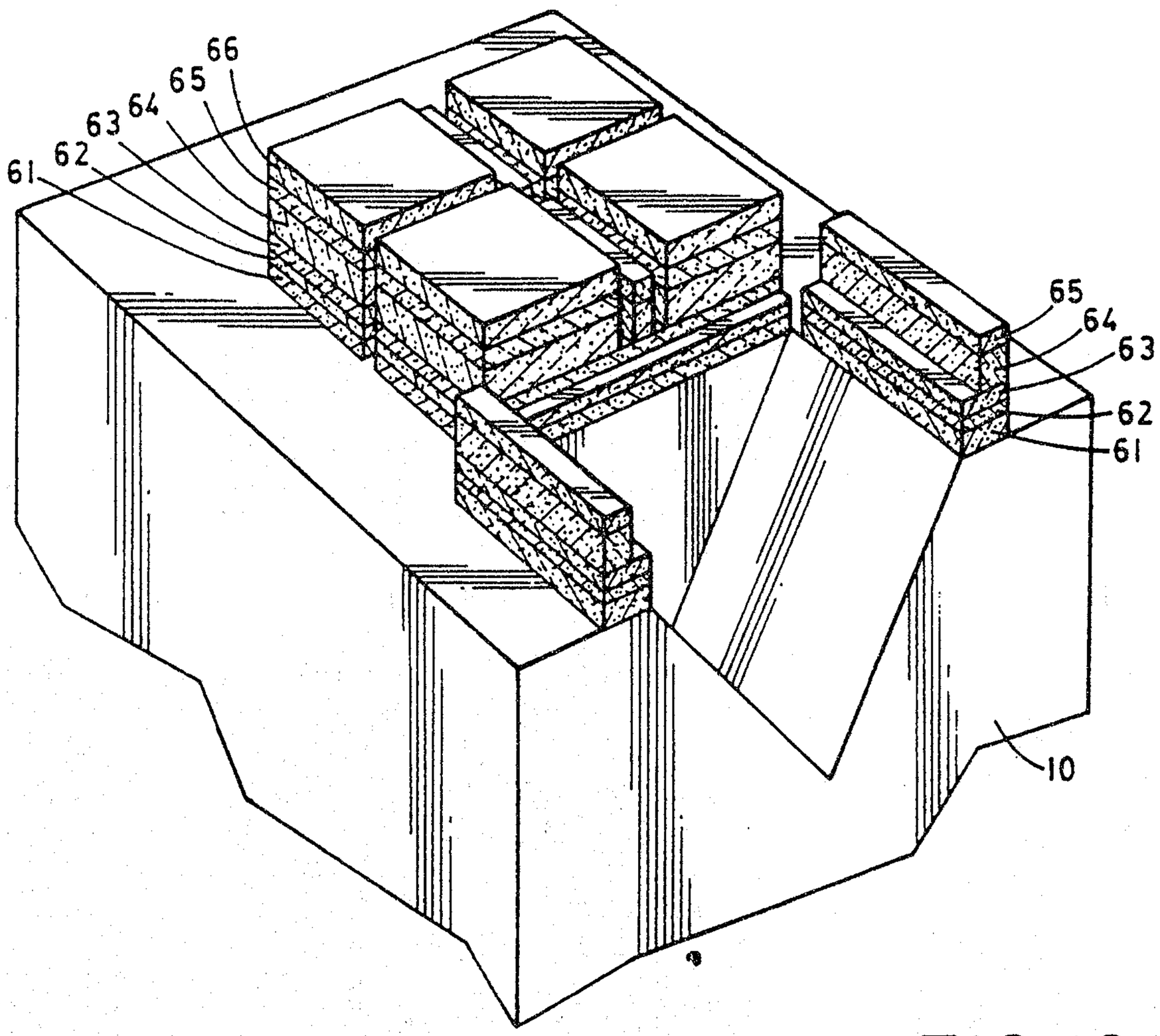


FIG. 10A

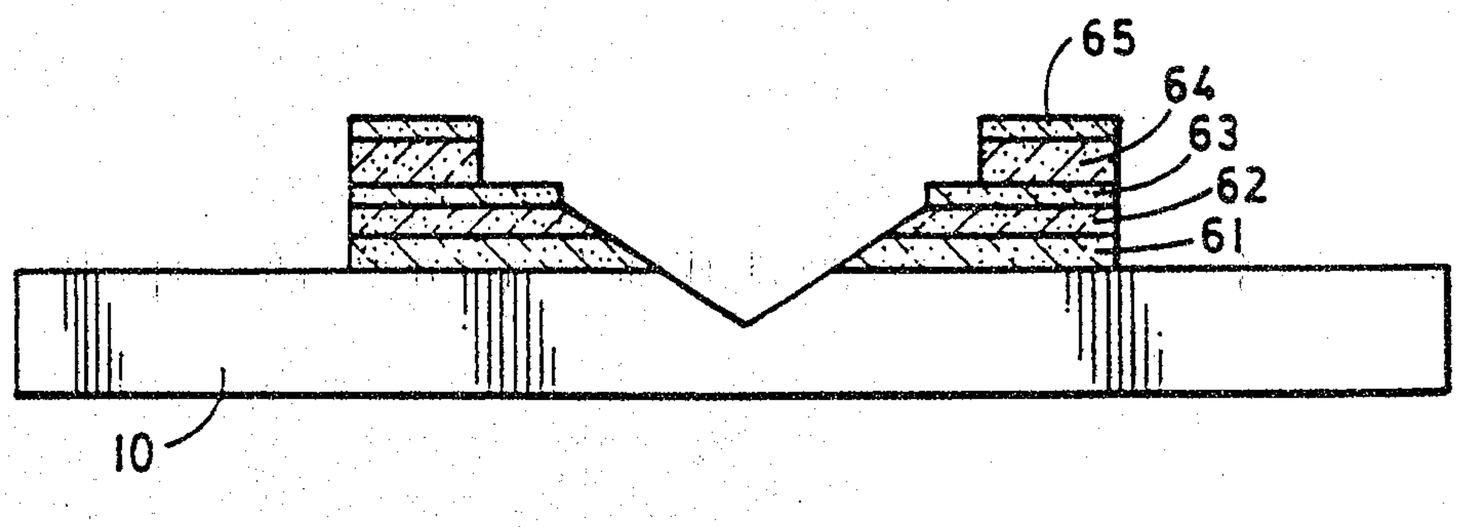
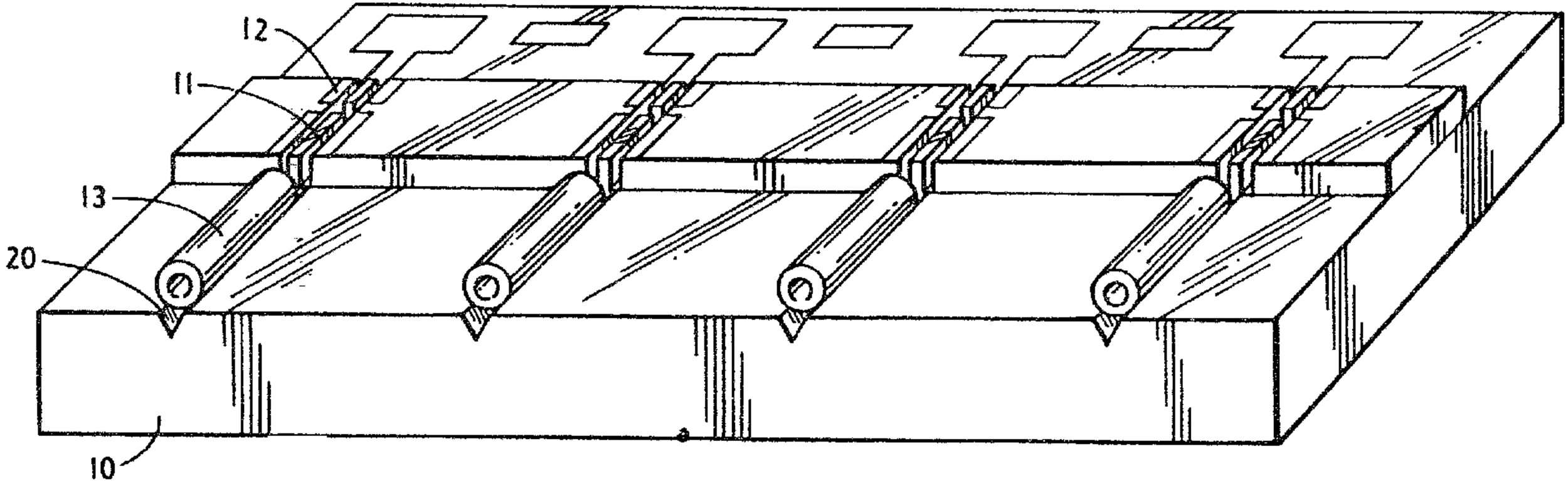


FIG. 10B


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