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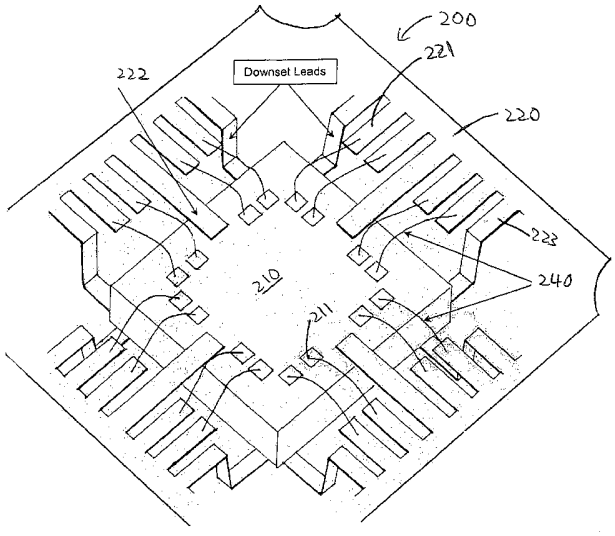
(54) Title: PACKAGING OF INTEGRATED CIRCUITS TO LEAD FRAMES



(57) Abstract: A lead frame (200) for housing an integrated circuit is disclosed comprising a main member (220) and an engagement portion (230) for receiving an integrated circuit (210). The integrated circuit (210) is located at the engagement portion (230) and engaged with the lead frame through resilient engagement with the first and second engagement members (222, 223). The first and second engagement members (222, 223) which depend from the main member, secure the integrated to the lead frame by engaging in resilient contact respective opposed surfaces of the integrated circuit. The integrated circuit is engaged to the lead frame by clipping into it into position between the engagement members. There is no need for a gluing process unlike conventional lead frame designs which where the integrated circuit is attached to a lead frame by gluing it onto the die paddle.

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Packaging of integrated circuits to lead frames

Field of the Invention

The present invention relates to methods of packaging an integrated circuit to a lead frame, to lead frames suitable for use in the methods and to the combinations of integrated circuits and lead frames produced using the methods.

Background of the Invention

Lead frames are commonly used as a substrate for the packaging of integrated circuits. Figure 1 illustrates a conventional lead frame 100 comprising a central die paddle 101 adapted for receiving an integrated circuit 110 and a plurality of leads 102 encircling the die paddle 101. The leads 102 which serve as electrical contacts are spaced away from the die paddle. In well known methods, an integrated circuit 110 is attached onto the die paddle 101 by dispensing a layer of epoxy glue 120 onto the die paddle 101 and attaching the lower surface of the integrated circuit to it. The epoxy glue is then cured to hold the integrated circuit securely in place. Following this, wire bonds are formed to electrically connect the electrical contacts located on the upper surface of the integrated circuit (not shown) with respective leads 102 of the lead frame. The integrated circuit 110, die paddle 101 and wire bonds are subsequently encapsulated in an electrically insulating resin and the leads 102 cut leaving portions of the leads extending out of the resin body so that they may be connected to further circuitry.

Unfortunately, the above described conventional lead frame design 100 and packaging method deployed suffers from a number of problems. First of all, the dispensing of epoxy glue and placement of the integrated circuit 110 has to be carefully controlled in order to avoid problems such as excessive glue bleed, glue void and die tilt. For example, if the amount of epoxy glue

dispensed is too great, the epoxy glue may leak from beneath the integrated circuit 110 and cover some of the electrical contacts of the integrated circuit or inner ends of the leads 102 where the connecting wires are bonded. In this case, it may be impossible to form reliable wire bonds between the electrical contacts of the integrated circuit and the leads of the lead frame. In addition to this, the epoxy glue cure process also introduces additional problems such as out-gassing of parts used in the glue cure process, glue cure oven contamination and the need to control complex glue curing profiles. Aside from the above packaging problems, there are also concerns from the reliability point of view as the conventional integrated circuit packages formed are found to be susceptible to delamination effects during subsequent use. This is because delamination between the resin body and die paddle are often observed after the package has been subjected to accelerated reliability testing such as temperature cycling and pressure cooker test. The glue region 120a in particular is especially prone to delamination.

As a result of these problems associated with the conventional lead frame design and packaging methods, the packaging yield and reliability of the resulting integrated circuit packages formed are severely compromised. It is an object of the invention to provide a lead frame design and packaging method which alleviates these problems and/or provides the general public with a useful choice.

Summary of the Invention

In accordance with a first aspect of the present invention, there is provided a lead frame comprising a main member, an engagement portion within the main member for receiving an integrated circuit and engagement means depending from the main member. The integrated circuit being located at the engagement portion through resilient engagement with the engagement means.

Preferably the engagement means comprise a plurality of first and second engagement members adapted to resiliently engage respective opposed surfaces of the integrated circuit. The first and second engagement members are arranged such that an engaged integrated circuit has an interference fit with the engagement members.

In one embodiment, the total available contact area of the second engagement members exceeds the total available contact area of the first engagement members. Preferably, the arrangement of the lead frame being such that an individual contact area of each second engagement member is greater than an individual contact area of each first engagement member.

In accordance with a second aspect of the present invention, an integrated circuit is packaged to a lead frame by providing a lead frame comprising a main member, an engagement portion within the main member for receiving an integrated circuit and engagement means depending from the main member, locating an integrated circuit at the engagement portion and engaging the integrated circuit to the lead frame through resilient engagement with the engagement means.

The lead frame of the present invention and the method of packaging an integrated circuit to it departs from conventional lead frame designs. Conventional lead frame designs comprise a die paddle and epoxy glue is used to attach the integrated circuit to the die paddle. Accordingly, since the present invention removes the need for a die paddle and gluing process, the problems associated with integrated circuit attachment and glue cure are also eliminated. Furthermore, the removal of the die paddle also improves the reliability of the resulting integrated circuit package tremendously as the delamination effects between the resin body and die paddle/glue region are also eradicated.

Brief Description of the Drawings

An embodiment of the invention will now be described, by way of example, with reference to the accompanying drawings in which:

Figure 1 shows the cross-sectional view of an integrated circuit attached to a lead frame having a known design;

Figure 2 shows the cross-sectional view of an integrated circuit clipped onto a lead frame which is a first embodiment of the invention;

Figure 3 shows the top view of an integrated circuit clipped onto the lead frame of Figure 2 with wire bonds being formed between the electrical contacts of the integrated circuit and the corresponding contact members of the lead frame; and

Figure 4, which is composed of Figures 4(a) to 4(d), shows the process of attaching an integrated circuit to the lead frame of Figures 2 and 3;

Detailed Description of the Preferred Embodiment of the Invention

The present invention addresses the problems with the conventional lead frame design by eliminating both the die paddle and the gluing process. Figures 2 and 3 illustrate a lead frame 200 in accordance with one embodiment of the invention. Figure 2 shows a cross-sectional view of the lead frame 200 with an integrated circuit 210 mounted on it while Figure 3 shows the top view. The lead frame 200 includes a central aperture 230 for receiving an integrated circuit 210 and a main member 220 surrounding the central aperture 230. The main member 220 has a set of electrical contact members 221 extending from the main member in a direction towards the central aperture 230. During the packaging process, wire bonds 240 are formed to electrically connect the contact members 221 with corresponding electrical contacts 211 located on the upper surface of the integrated circuit

210. In addition to this, the main member 220 also has a set of first engagement members 222 and a set of second engagement members 223 extending radially inwards from the main member 220 towards the central aperture 230. The first and second engagement members 222, 223 are used to fasten the integrated circuit 210 to the lead frame 220 and have a longer span length wise as compared to the contact members 221. As shown in Figures 2 and 3, the ends of the first engagement members 222 remote from the main member engage the upper surface of the integrated circuit 210. Meanwhile, a portion of the second engagement members 223 is downset so that the ends of the second engagement members 223 remote from the main member 220 engage the lower surface of the integrated circuit 210. By contrast, the contact members 221 which have a shorter span than the engagement members are arranged to be spaced apart from the integrated circuit 210. Since the engagement members engage a surface of the integrated circuit, they also serve as a heat sink which dissipates heat away from the integrated circuit.

The vertical distance d between the lower surface of the first engagement members 222 and the upper surface of the second engagement members 223 is arranged to be slightly smaller than thickness of the integrated circuit to be fastened. This causes the engagement members to exert a slight pressure on the respective upper and lower surfaces of the integrated circuit 210 thereby ensuring that the engaged integrated circuit 210 is securely fastened by having an interference fit with the engagement members. In a preferred embodiment, the second engagement members 223 engage a portion of the surface near the corners of the integrated circuit with a first engagement member 223 interposed between them.

Preferably, each second engagement member 223 is arranged to engage a larger surface of the integrated circuit than a corresponding first engagement member 222. For example, in a preferred embodiment shown in Figure 2, the

second engagement members 223 have a longer lateral span and extend further inward from the edge of the integrated circuit 210 to engage a larger surface area of the integrated circuit 210 than the first engagement members 222. Since the second engagement members 223 engage the lower inactive surface of the integrated circuit 210, this arrangement results in better support for the integrated circuit 210 without affecting the amount of surface area available for electronic circuitry.

The process of fastening an integrated circuit to the lead frame of Figures 2 and 3 is illustrated in Figure 4. First of all in Figure 4(a), a bonding arm in the form of a die collet (not shown) connected to a vacuum source holds the integrated circuit to be fastened by suction and positions the integrated circuit such that it is in register with the central aperture of a lead frame 200. The die collet then lowers the integrated circuit downwards. As shown in Figure 4(b), the lower surface of the integrated circuit first touches the upper surface of the first engagement members 222, pushing the first engagement members 222 downwards as the integrated circuit 210 is lowered. The lowering of the integrated circuit 210 continues with the first engagement members 222 being deflected downwards until the integrated circuit 210 has travelled past the first engagement members 222 as shown in Figure 4(c). When this happens, the first engagement members 222 which are made of a resilient material spring back to their original position by cantilever action. In one embodiment, the lead frame is made from a copper alloy (such as C19400, C70250, C19210) or alloy 42. Alternatively, other lead frame materials which are resilient in terms of being able to exhibit cantilever effect may also be used. Since existing lead frames materials generally exhibit these properties, the described embodiment can be implemented without having to develop new lead frame materials.

At this point, the lower surface of the integrated circuit 210 is in contact with the upper surface of the second engagement members 222 and as evident

from Figure 4(c), the second engagement members 223 are also deflected downwards when the integrated circuit 210 is lowered past the first engagement members 222. In Figure 4(d), the die collet subsequently releases the integrated circuit 210 from suction and the second engagement members 223 return to their original position by cantilever action. The integrated circuit 210 is accordingly secured to the lead frame 200 with the first and second engagement members 222, 223 engaging the upper and lower surfaces of the integrated 210 respectively. Preferably, the downward deflection of the second engagement members 223 should be slight so that the integrated circuit 210 does not shift sideways when the second engagement members 223 return to their original position.

After the integrated circuit 210 has been secured to the lead frame 200, wire bonds 240 are formed to electrically connect the electrical contacts 211 located on the upper surface of the integrated circuit with the respective contact members 221. The top view of the resulting arrangement is shown in Figure 3. An encapsulation process is then carried out to encase the integrated circuit 210 and wire bonds 240 in an electrically insulating material.

Although the lead frame 200 illustrated in Figure 3 shows a first engagement member 222 and two second engagement members 223 located on each side of the integrated circuit 210, other configurations of the lead frame are also possible. For example, the number of engagement members may be varied or the engagement members may be located on the corners instead of at the sides of the integrated circuit.

While the invention has been particularly shown and described with reference to various embodiments, it will be recognised by those skilled in the art that modifications and changes may be made to the present invention without departing from the scope thereof. The scope of the invention should therefore

be determined not with reference to the above description but with reference to the appended claims.

Claims

1. A lead frame for packaging an integrated circuit comprising:

a main member;

an engagement portion within the main member for receiving an integrated circuit; and

engagement means depending from the main member;

wherein the integrated circuit is located at the engagement portion through resilient engagement with the engagement means.

2. A lead frame according to claim 1 wherein the engagement portion comprises an aperture.

3. A lead frame according to claim 1 wherein the engagement portion is a recess.

4. A lead frame according to claim 1 wherein the engagement portion is coplanar with a plane defined by the lead frame.

5. A lead frame according to any of the preceding claims wherein the engagement means comprises a plurality of resilient engagement members.

6. A lead frame according to claim 5 wherein the engagement members comprise a plurality of first and second engagement members adapted to resiliently engage respective opposed surfaces of the integrated circuit.

7. A lead frame according to claim 6 wherein the first and second engagement members are arranged such that an engaged integrated circuit has an interference fit with said engagement members.

8. A lead frame according to claims 6 or 7 wherein the number of second engagement members exceeds the number of first engagement members.

9. A lead frame according to claim 8 wherein for each side of the engaged integrated circuit there is located two second engagement members and a first engagement member, said first engagement member disposed midway between the second engagement members, with said second engagement members disposed adjacent ends of each side.

10. A lead frame according to any of claims 6 to 9 wherein a total available contact area of the second engagement members exceeds a total available contact area of the first engagement members.

11. A lead frame according to claim 10, wherein an individual contact area of each second engagement member is greater than an individual contact area of each first engagement member.

12. A lead frame according to any of the preceding claims further comprising a plurality of contact members depending from the main member, the contact members adapted for connecting to respective electrical contacts on the surface of the integrated circuit.

13. An assembly comprising an integrated circuit in resilient engagement with a lead frame according to any of claims 1 to 12.

14. A method of packaging an integrated circuit on a lead frame, the method comprising:

providing a lead frame comprising a main member, an engagement portion within the main member for receiving an integrated circuit and engagement means depending from the main member;

locating an integrated circuit at the engagement portion; and

engaging the integrated circuit to the lead frame through resilient engagement with the engagement means.

15. A method according to claim 14 wherein the engagement portion comprises an aperture.

16. A method according to claim 14 wherein engagement portion is a recess.

17. A method according to claim 14 wherein the engagement portion is coplanar with a plane defined by the lead frame.

18. A method according to any of claims 13 to 17 wherein the engagement means comprises a plurality of resilient engagement members.

19. A method according to any of claim 18 wherein the engagement members comprise a plurality of first and second engagement members adapted to resiliently engage respective opposed surfaces of the integrated circuit.

20. A method according to claim 19, wherein the first and second engagement members are arranged such that an engaged integrated circuit has an interference fit with said engagement members.

21. A method according to claim 19 or 20 wherein the number of second engagement members exceeds the number of first engagement members.

22. A method according to claim 21 wherein for each side of the engaged integrated circuit there is located two second engagement members and a first engagement member, said first engagement member disposed midway between the second engagement members, with said second engagement members disposed adjacent ends of each side.

23. A method according to any of claims 19 to 22 wherein a total available contact area of the second engagement members exceeds a total available contact area of the first engagement members.

24. A method according to claim 23, wherein an individual contact area of each second engagement member is greater than an individual contact area of each first engagement member.

25. A method according to claim 15 further comprising the steps of:

positioning the integrated circuit in register with the engagement portion;

biasing the integrated circuit past first engagement members until said first engagement members resiliently recover;

contacting with second engagement members;

releasing the integrated circuit and engaging the integrated circuit in an interference fit with the first engagement members engaging an upper surface of the integrated circuit and the second engagement members engaging a lower surface of the integrated circuit.

26. A method according to any of the claims 14 to 24, further comprising the steps of:

connecting electrical contacts on the surface of the engaged integrated circuit with respective contact members of the lead frame;

encapsulating the engaged integrated circuit in an electrically insulating material.

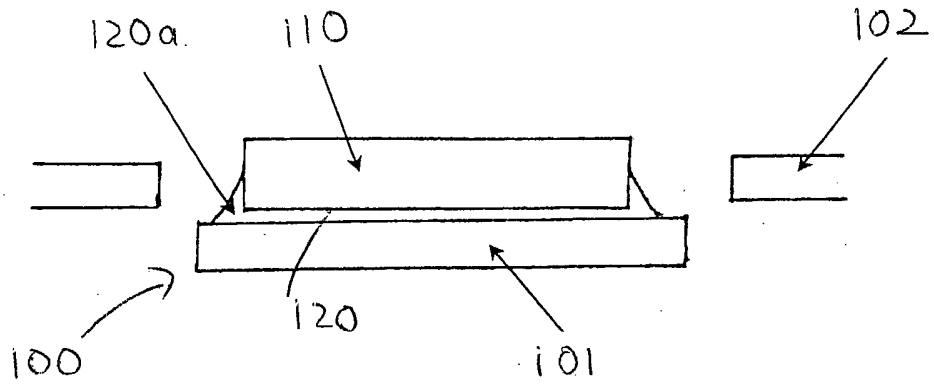

Figure 1
Prior Art

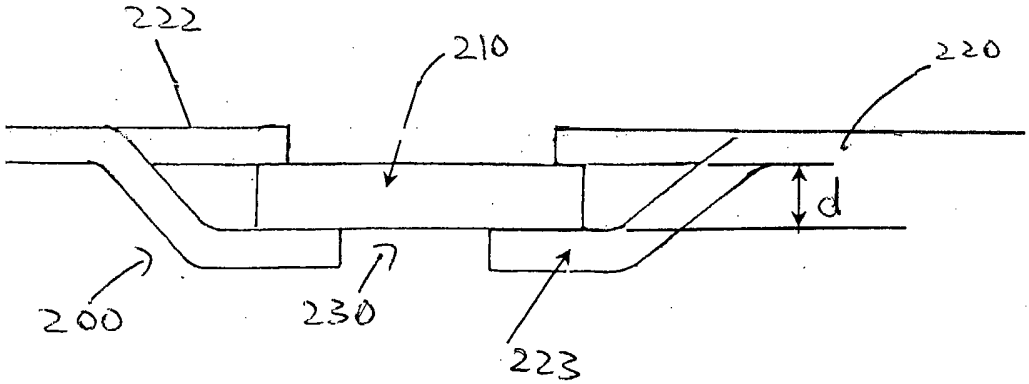

Figure 2

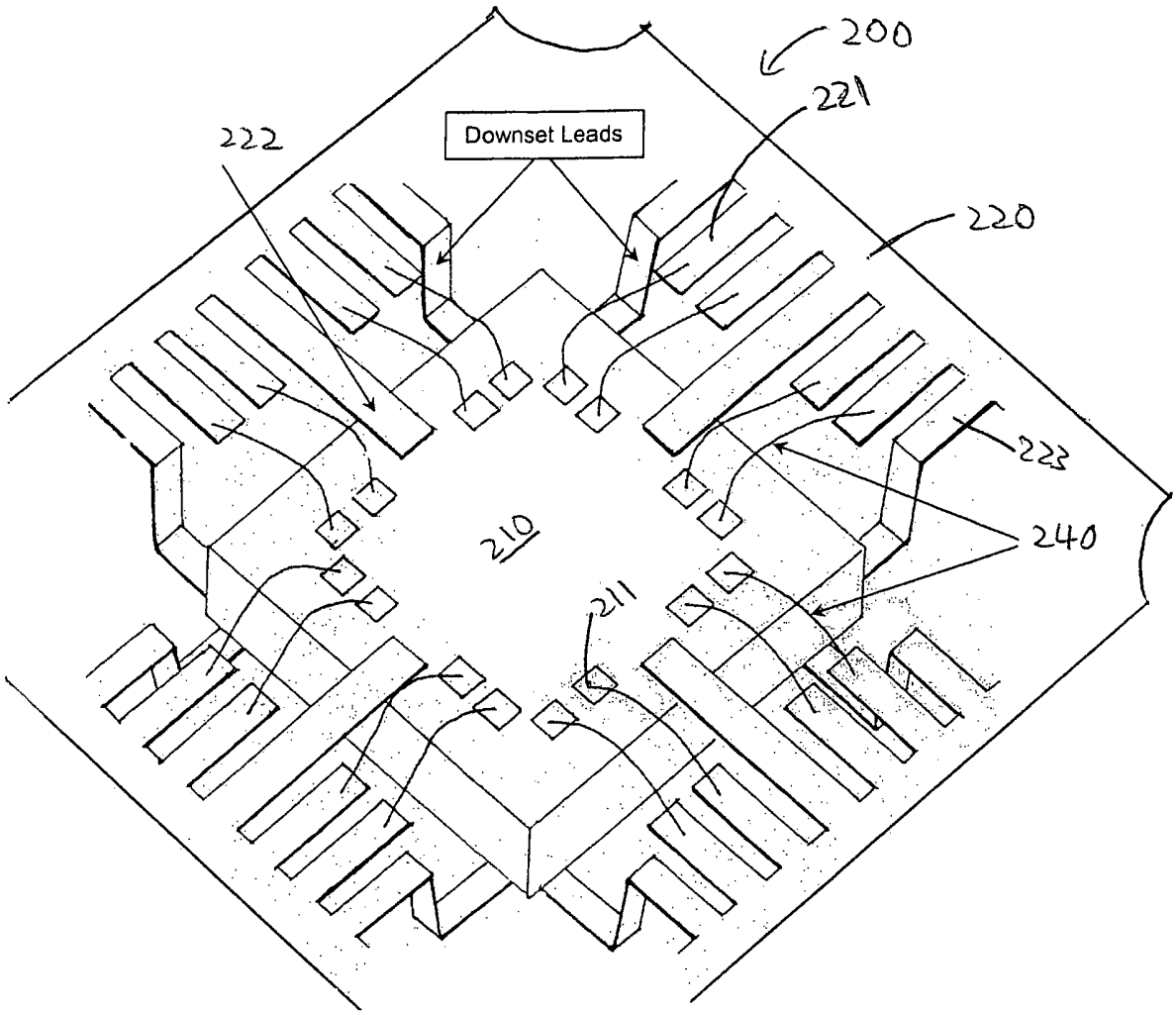

Figure 3

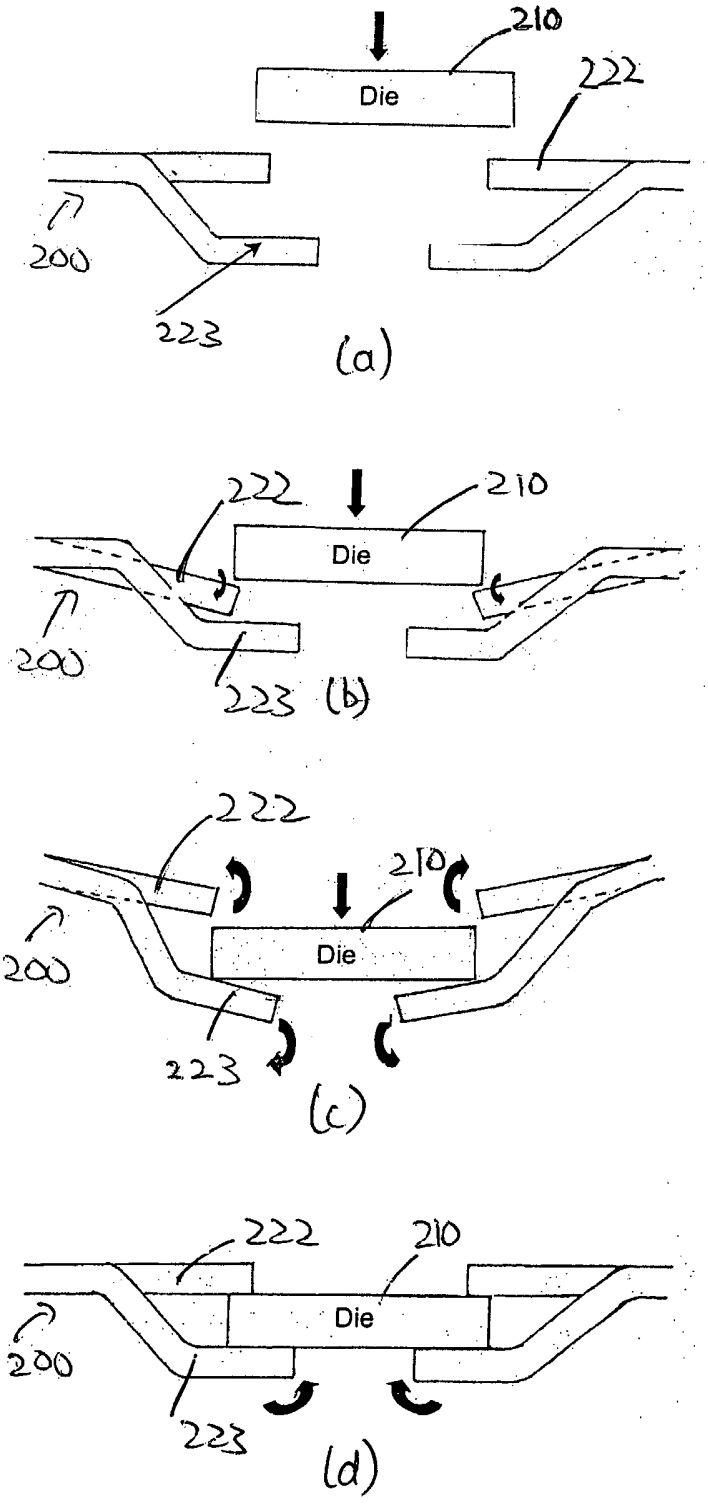
210
Die
222
200
223
(a)
222
210
Die
200
223
(b)
222
210
Die
200
223
(c)
222
210
Die
200
223
(d)

Figure 4

INTERNATIONAL SEARCH REPORT

International Application No
PCT/SG2004/000259

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L23/495 H01L21/48

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

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X	US 5 307 929 A (SEIDLER ET AL) 3 May 1994 (1994-05-03) column 3, line 30 - column 4, line 68; figures 4,5,7 -----	1-8, 10-21, 23-26
X	US 5 998 866 A (OCHI ET AL) 7 December 1999 (1999-12-07) column 8, line 49 - column 12, line 22; figures 1,2 ----- -/--	1,5-7, 12-14, 18-20,26

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
2 June 2005	10/06/2005

Name and mailing address of the ISA	Authorized officer
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INTERNATIONAL SEARCH REPORT

International Application No
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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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