



- (51) International Patent Classification:  
G06F 9/48 (2006.01)
- (21) International Application Number:  
PCT/US2018/016206
- (22) International Filing Date:  
31 January 2018 (31.01.2018)
- (25) Filing Language: English
- (26) Publication Language: English
- (30) Priority Data:  
15/420,267 31 January 2017 (31.01.2017) US
- (63) Related by continuation (CON) or continuation-in-part (CIP) to earlier application:  
US 15/420,267 (CON)  
Filed on 31 January 2017 (31.01.2017)
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- (81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME,

(54) Title: INTERRUPT HANDLING METHOD AND APPARATUS FOR SLOW PERIPHERALS

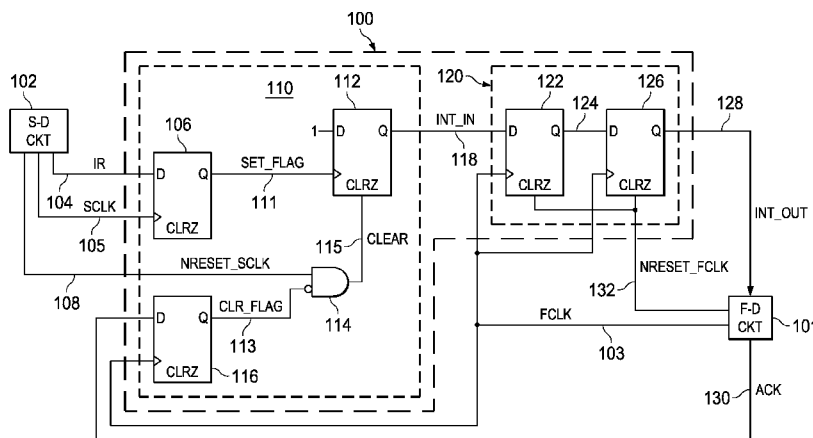


FIG. 1

(57) Abstract: Described examples include interrupt handling circuitry (100) and methods for managing interrupts of a fast clock domain circuit (101) operated according to a first clock signal (FCLK) by a slow clock domain circuit (102) operated according to a second clock signal (SCLK) in which an interrupt generator circuit (110) generates an interrupt input signal (INT\_IN) synchronized to the second clock signal (SCLK), and an interrupt clear circuit (114, 116) selectively resets the interrupt generator circuit (110) in response to an acknowledgment signal (ACK) from the first circuit (101) asynchronously with respect to the second clock signal (SCLK).



MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ,  
OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA,  
SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN,  
TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

- (84) Designated States** (*unless otherwise indicated, for every kind of regional protection available*): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

**Declarations under Rule 4.17:**

- *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*
- *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

**Published:**

- *with international search report (Art. 21(3))*

## INTERRUPT HANDLING METHOD AND APPARATUS FOR SLOW PERIPHERALS

## BACKGROUND

[0001] Electronic circuits and systems often include multiple circuit segments or clock domains that operate at different clock speeds. For example, processor circuits often operate at high clock speeds and interact with one or more peripheral circuits that run at much lower clock speeds. A slow clock domain circuit often generates interrupt service requests for servicing by the fast clock domain circuit. Servicing and clearing an interrupt from a slow clock domain circuit may take many fast clock cycles and can lead to inability of the fast clock domain circuit to service other interrupts. In one example, interrupts from peripheral circuits operating at very slow frequencies (e.g., 10-100 KHz) are serviced by a CPU operating at high clock frequencies of 1-100 MHz or even higher. Application software executed by a fast clock domain processor circuit or CPU may need to update or write a new counter value in a register of a low clock speed pulse width modulation (PWM) control circuit in response to an interrupt triggered by the counter value reaching a predetermined value. Previous interrupt handling techniques and circuits synchronize a clear request from the servicing CPU to the slow clock signal and/or use a handshaking approach to clear the interrupt request. This results in a delay of two or more slow clock cycles before the peripheral circuit receives the clear request and removes the interrupt request signal. This interrupt clearance delay can be significant, particularly for large differences in the fast and slow clock speeds. For a peripheral operating at 10 KHz functional clock, the delay would be at least 200 microseconds, which is significant for a CPU operating at 100 MHz. During this time, the fast clock domain CPU must wait to avoid re-entry into the same service routing. Moreover, if another interrupt event occurs in the peripheral circuit before the initial interrupt is cleared, the new interrupt event from the same peripheral will be lost. Also, conventional interrupt handling circuits and techniques generate interrupt requests with some latency. For example, the slow clock domain interrupt generation conditions may be based on rising slow clock edges and the interrupt request signal is generated according to a rising slow clock edge or vice versa, where synchronization to the slow clock signal introduces further delays in servicing an interrupt event.

## SUMMARY

**[0002]** Described examples include interrupt handling circuitry and methods for managing interrupts of a fast clock domain first circuit by a slow clock domain second circuit, where the first circuit operates according to a first clock signal and the second circuit operates according to a second clock signal slower than the first clock signal. A described interrupt handling circuit includes an interrupt generator circuit that generates an interrupt input signal, and an interrupt clear circuit that resets the interrupt generator circuit in response to an acknowledgment signal from the first circuit asynchronously with respect to the second clock signal.

**[0003]** In certain examples, the interrupt generator circuit includes a first input to receive an interrupt request signal, a second input to receive an interrupt clear signal, and an output to provide an interrupt input signal synchronized to the interrupt request signal to selectively interrupt the first circuit. The interrupt clear circuit in one example includes an output synchronized to the first clock signal to provide the interrupt clear signal to reset the interrupt generator circuit in response to an acknowledgment signal from the first circuit.

**[0004]** Methods are described to manage interrupts of a first circuit operated according to a first clock signal by a second circuit operated according to a slower second clock signal. The methods include generating an interrupt input signal synchronized to the second clock signal, providing an interrupt output signal to the first circuit in response to the interrupt input signal, and clearing the interrupt input and output signals asynchronously with respect to the second clock signal in response to an acknowledgment signal from the first circuit.

## BRIEF DESCRIPTION OF THE DRAWINGS

**[0005]** FIG. 1 is a schematic diagram showing an interrupt handling circuit configured to manage interrupts of a fast clock domain first circuit by a slow clock domain second circuit.

**[0006]** FIG. 2 is a signal diagram showing operating signals in the circuit of FIG. 1 for an arbitrary ratio of fast and slow clock speeds.

**[0007]** FIG. 3 is a signal diagram showing operating signals in the circuit of FIG. 1 for one example ratio of fast and slow clock speeds.

**[0008]** FIG. 4 is a signal diagram showing a handshaking acknowledgment interrupt handling technique with a missed interrupt event.

**[0009]** FIG. 5 is a signal diagram showing interrupt generation with synchronization delays.

**[0010]** FIG. 6 is a flow diagram illustrating a process or method for managing interrupts of a

fast domain circuit by a slow domain circuit.

#### DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

**[0011]** In the drawings, like reference numerals refer to like elements throughout, and the various features are not necessarily drawn to scale. In this description, the terms “couple”, “coupled” or “couples” include indirect or direct electrical or mechanical connection or combinations thereof. For example, if a first device couples to or is coupled with a second device, that connection may be through a direct electrical connection, or through an indirect electrical connection via one or more intervening devices and connections.

**[0012]** Described examples include integrated circuits, and interrupt handling circuitry and processes for managing interrupts of a first circuit operated according to a first clock signal by a second circuit operated according to a slower second clock signal. The described technique can be employed in a variety of different applications in which first and second clock domains or circuits are operated according to different clock speeds, which can be asynchronous or synchronous with respect to one another. Also, the described examples provide interrupt handling circuitry and methods which can be employed in association with first and second clock domain circuits of a single integrated circuit, or with respect to fast and slow clock domain circuits on separate ICs or combinations thereof.

**[0013]** FIG. 1 shows a system including an interrupt handling circuit 100, a first circuit 101 (a “fast domain circuit” labelled F-D CKT in the drawing) and a second circuit 102 (a “slow domain circuit” labeled S-D CKT in FIG. 1). The first and second circuits 101 and 102 respectively operate according to different first and second clock signals FCLK and SCLK. The circuits 101 and 102 can be formed in separate integrated circuits (ICs), or can be circuits on a single IC. The circuits 101 and 102 are part of two separate clock domains through operation according to corresponding clock signals FCLK and SCLK. The clock signals FCLK and SCLK can operate independently of one another with respect to clock phasing and/or clock frequency, although not a strict requirement of all embodiments. The first clock signal FCLK is provided by a clock source (not shown) of the first circuit 101 on a circuit node 103, and the clock signal SCLK is provided by a clock source (not shown) of the second circuit 102 on a node 105. The second clock signal SCLK is slower than the first clock signal FCLK in this example.

**[0014]** The interrupt handling circuit 100 includes an interrupt generator circuit 110, a synchronizer circuit 120 and an interrupt clear circuit 114, 116 to manage signaling and

clearance of interrupt events associated with the second circuit 102 serviced by the first circuit 101. In this example, the interrupt generator circuit 110 includes inputs 104 and 105 as well as an output 118 and selectively interrupts the first circuit 101 synchronously with respect to the first clock signal FCLK. The interrupt clear circuit 114, 116 includes a flip-flop 116, and AND gate 114, and an output 115 synchronized to the first clock signal FCLK to selectively provide an interrupt clear signal CLEAR to reset the interrupt generator circuit 110 in response to an acknowledgment signal ACK from the first circuit 101. Moreover, the interrupt clear circuit 114, 116 clears or resets the interrupt generator circuit 110 asynchronously with respect to the second clock signal SCLK. In this manner, the interrupt handling circuit 100 mitigates or avoids synchronization delays associated with conventional interrupt clearance circuits, and facilitates response by the interrupt generator circuit 110 to further interrupts from the second circuit 102.

**[0015]** In operation, the second circuit 102 provides an interrupt request signal IR on a node 104 as an input to the interrupt generator circuit 110. The second circuit 102 also includes an output node 108 to provide a reset signal NRESET\_SCLK to reset the interrupt generator circuit. The interrupt generator circuit 110 provides an interrupt input signal INT\_IN at a node 118 as an input to the synchronizer circuit 120. The synchronizer circuit 120 provides an interrupt output signal INT\_OUT at a node 128 connected to the first circuit 101. The first circuit 101, in turn, services the interrupt, and generates an acknowledgment signal ACK on a circuit node 130, provided as an input to the interrupt clear circuit 114, 116. The interrupt clear circuit 114, 116 generates an interrupt clear signal CLEAR at a node 115 to clear the interrupt input signal INT\_IN.

**[0016]** Conventional fast/slow clock domain interrupt handling circuits and techniques typically introduce latency or delay into the interrupt request signaling, and suffer from significant delays due to slow clock domain clear signal synchronization, which can lead to delays in servicing and clearing interrupts and potentially lost or missed interrupt events.

**[0017]** In order to address the first problem, the present disclosure provides solutions that can generate an interrupt without significant latency. In this example, the interrupt generator circuit 110 includes an interrupt flag or interrupt generator flip-flop 112, in this case a data or “D” flip-flop that generates the interrupt input signal INT\_IN according to a synchronized interrupt request signal SET\_FLAG on a circuit node 111 received from a flip-flop 106. The flip-flop 106 receives the interrupt request signal IR from the node 104 as a data input, and includes a clock

input connected to the slow clock node 105. In operation, the second circuit 102 activates the interrupt request signal IR in an active high state, and the flip-flop 106 generates the signal SET\_FLAG on the node 111 in a high state at the next rising edge of the slow clock signal SCLK. The data (D) input of the interrupt generator flip-flop 112 is connected to a logic high signal (“1” IN FIG. 1), and the clock input of the flip-flop 112 is connected to receive the synchronized interrupt request signal SET\_FLAG from the node 111. The AND gate 114 provides the CLEAR signal to the clear input CLRZ of the flip-flop 112 to selectively reset the interrupt generator circuit 110 in response to the acknowledgment signal ACK from the first circuit 101.

**[0018]** The interrupt generator output 118 provides the interrupt input signal INT\_IN in a low first state in response to the second interrupt generator input 115 receiving the interrupt clear signal CLEAR in the low first state. The output 118 provides the interrupt input signal INT\_IN in a high second state in response to a low-high transition and the synchronized interrupt request signal SET\_FLAG when the interrupt clear signal CLEAR is in the high second state. When the CLEAR signal is high, the flip-flop 112 generates the interrupt input signal INT\_IN in an active high state at or shortly following the rising edge of slow clock signal SCLK when the interrupt request signal IR is asserted in the high state. In this manner, the interrupt request signal SET\_FLAG is synchronized to the second clock signal SCLK by the flip-flop 106 in order to avoid or mitigate metastability issues. The interrupt generation circuitry 110 provides significant advantages compared to other interrupt generation circuitry, which often suffer from half cycle or full cycle synchronization delays as described hereinbelow in connection with FIG. 5. The circuit 110 advantageously asserts the interrupt input signal INT\_IN in a timely fashion relative to the rising edge of the interrupt request signal IR received from the second circuit 102.

**[0019]** The interrupt clear circuit 114, 116 provides the interrupt clear signal CLEAR in the low first state to reset the interrupt generator circuit 110 to set the interrupt input signal INT\_IN to the low first state in response to the acknowledgment signal ACK from the first circuit 101. The flip-flop 116 in this example is a D flip-flop, with a data input “D” connected to the node 130 to receive the acknowledgment signal ACK, and a clock input connected to the node 103 to receive the first clock signal FCLK. The output “Q” of the flip-flop 116 is connected to provide a clear flag signal CLR\_FLAG on a node 113 as shown in FIG. 1. The AND gate 114 receives the CLR\_FLAG signal via an inverted input, and receives the reset signal NRESET\_SCLK from

the second circuit 102 via the node 108. This second input to the AND gate 114 allows the second circuit 102 to reset the AND gate 114. In other possible implementations, the AND gate 114 can be omitted, and the CLR\_FLAG signal can be provided directly to the CLRZ input of the interrupt generator flip-flop 112. In operation, the clear circuitry 114, 116 quickly clears the flip-flop 112 in response to the ACK signal going high without synchronizing delays associated with the second clock signal SCLK, causing the interrupt input signal INT\_IN and the interrupt output signal INT\_OUT to go low asynchronously relative to the slow clock signal SCLK. In this manner, the pending interrupt signal INT\_OUT is quickly cleared once the first circuit 101 has serviced the pending interrupt, thus allowing the first circuit 101 to receive and properly service further subsequent interrupts from the second circuit 102.

**[0020]** In this example, the interrupt handling circuit 100 also includes the synchronizer circuit 120. In operation, the circuit 120 quickly synchronizes the interrupt input signal INT\_IN with respect to the fast first clock signal FCLK in order to avoid any metastability issues with the INT\_IN signal generated by the interrupt generator circuit 110. The synchronizer circuit 120 includes an input coupled with the interrupt generator output 118 to receive the interrupt input signal INT\_IN, and an output 128 synchronized to the first clock signal FCLK to provide an interrupt output signal INT\_OUT to the first circuit 101. The circuit 120 in this example includes a first flip-flop 122 with a data input D connected to the interrupt generator output 118, a clock input connected to receive the first clock signal FCLK. The output 124 (Q) of the first synchronizer flip-flop 122 is connected to a data input D of a second synchronizer flip-flop 126 that also has a clock input connected to the first clock signal FCLK at the node 103. The output Q of the second synchronizer flip-flop 126 is connected to the first circuit 101 to provide the interrupt output signal INT\_OUT synchronized to the first clock signal FCLK. The synchronizer flip-flops 122 and 126 each include an active low clear input CLRZ connected to receive a reset signal NRESET\_FCLK provided on a circuit node 132 by the first circuit 101.

**[0021]** FIG. 2 shows a signal diagram 200 illustrating operating signals in the interrupt handling circuit 100 of FIG. 1 for an arbitrary ratio of fast and slow clock speeds. In this example, two example cycles of the second clock signal SCLK are shown as curve 202, and a FCLK curve 204 can have any number of fast clock signal transitions, where the first and second clock signals FCLK and SCLK can be completely asynchronous with respect to one another regarding clock speed and phase relationship. As seen in the example of FIG. 2, the flip-flop 106

of the interrupt generator circuit 110 asserts the SET\_FLAG signal (curve 206) active high in response to a rising edge of the interrupt request signal IR from the second circuit 102 at a rising edge of the second clock signal SCLK (curve 202). The interrupt generator circuit 110 generates the interrupt input signal INT\_IN, and the synchronizer circuit 120 synchronizes this signal, and generates a rising edge in the interrupt output signal INT\_OUT (curve 210) within two FCLK cycles asynchronously with respect to the second clock signal SCLK. When the fast domain first circuit 101 completes an associated interrupt service routine, the first circuit 101 asserts the acknowledgment signal ACK at the node 130, which provides an active high data input to the interrupt clearance flip-flop 116. At the next rising edge of the first clock signal FCLK, the flip-flop 116 asserts the clear flag signal CLR\_FLAG (active high, curve 208 in FIG. 2). This signal transition clears the signal generator flip-flop 112, causing the interrupt input signal INT\_IN to go low. The synchronizer circuit 120 synchronizes this falling edge transition within two fast clock cycles, causing a falling edge in the interrupt output signal INT\_OUT. In this manner, the interrupt handling circuitry 100 effectively clears the interrupt signal INT\_OUT provided to the first clock 101 within two FCLK cycles of the acknowledgment signal ACK.

**[0022]** FIG. 3 shows operating signals in the circuit of FIG. 1 for one example ratio (e.g., approximately 8) of fast and slow clock speeds. In this example, the slow domain (second) circuit 102 is a PWM timer peripheral service by the fast domain CPU or processor first circuit 101. In this example, fast domain CPU provides a counter value to a PWM control peripheral second circuit 102 in a closed loop control application to control a pulse width of a power converter signal (not shown). The peripheral second circuit 102 decrements the count value, and issues an interrupt request signal IR when the count value reaches a predetermined value (e.g., “1” in this implementation). Curve 302 in FIG. 3 illustrates the slow clock signal SCLK, and curve 304 schematically illustrates the PWM timer/counter data value, in this case initially decrementing through values 3, 2, 1 and then 0, before being reprogrammed by the fast clock domain CPU to another value 2. The peripheral PWM timer second circuit 102 then decrements from this value 2 to 1 and then again to 0. In this example, the curve 306 illustrates the SET\_FLAG signal output from the flip-flop 106, a curve 308 shows the fast domain clock signal FCLK, a curve 310 illustrates the interrupt output signal INT\_OUT from the synchronizer circuit 120, and a curve 312 illustrates the CLEAR\_FLAG signal from the flip-flop 116. The second circuit 102 in this example asserts the interrupt request signal IR in response to the counter value

reaching “1”. As seen in FIG. 3, the interrupt output signal INT\_OUT undergoes a rising edge transition within two fast clock cycles of a rising edge in the SET\_FLAG signal. In response to the interrupt output signal, the first circuit 101 begins an interrupt service routine or process. Once the first circuit 101 completes the interrupt service processing, the first circuit 101 asserts the acknowledgment signal ACK, and the flip-flop 116 generates a rising edge in the CLEAR\_FLAG signal shown as curve 312. The CLEAR\_FLAG signal transition clears the interrupt generator flip-flop 112, and the synchronizer circuit 120 causes the resulting falling edge in the interrupt output signal INT\_OUT (curve 310) within two fast clock cycles.

**[0023]** The examples of FIGs. 2 and 3 illustrate the advantageous operation of the interrupt handling circuit 100 with respect to quick notification of the first circuit 101 of the occurrence of an interrupt event associated with the second circuit 102 (e.g., within two fast clock cycles). Also, the circuit 100 provides fast asynchronous clearing of the interrupt signal (e.g., within two fast clock cycles) in response to assertion of the acknowledgment signal ACK by the first circuit 101. These quick response advantages of the described interrupt handling circuitry 101 provide significant benefits as shown in FIGs. 2 and 3. Moreover, these advantages are more pronounced when the ratio between the fast and slow clock speeds is increased. Thus, the benefits of the described circuits and techniques find particular utility in association with high-speed CPUs or other fast clock domain circuitry interacting with relatively slow clock speed second circuits 102.

**[0024]** FIG. 4 provides a signal diagram 400 showing a handshaking acknowledgment interrupt handling technique with a missed interrupt event. A curve 402 in FIG. 4 illustrates an example slow clock signal (labeled LOW CLOCK in FIG. 4), curve 404 illustrates another example of counter or timer values (PWM DATA) in a PWM timer peripheral, curve 406 shows an interrupt signal (INTERRUPT) from the PWM timer peripheral to a fast clock domain processor circuit, and curve 408 shows an example fast clock signal (FAST CLOCK). A curve 410 in FIG. 4 shows the interrupt signal synchronized to the fast clock signal, and a curve 412 shows an example interrupt clear event from the fast clock domain circuit. A further curve 414 illustrates the interrupt clear event signal synchronized to the slow clock signal, and a curve 416 illustrates the interrupt clear event acknowledge handshaking signal from the peripheral circuit to the fast clock domain circuit. The signals in FIG. 4 illustrate the adverse consequences of conventional handshaking/acknowledgment-based interrupt handling between fast and slow clock domain circuitry. As seen in the curves 404 and 406, for instance, the slow domain circuit

102 generates the interrupt signal IR in response to the counter value reaching “1”, and the subsequent fast domain circuit interrupt service routine reprograms the slow domain PWM counter value to “2”. However, the synchronization of the interrupt clearance event to the slow second clock signal (shown in curves 412, 414 and 416) introduces significant synchronization delays in providing a signal (falling edge of curve 414) to actually terminate the interrupt signaling (falling edge in the curve 406). In the interim delay, in this example, the PWM counter value has again transitioned to 1, but the fast clock domain circuit is unable to respond and properly service this second interrupt event. As described hereinabove in connection with FIGS. 1-3, the described interrupt handling circuitry 100 advantageously provides quick asynchronous clearance of the interrupt request signaling, thereby facilitating proper interrupt service processing by the fast clock domain circuit 101 to avoid or mitigate the shortcomings illustrated in FIG. 4.

**[0025]** FIG. 5 provides a signal diagram 500 illustrating advantages of the interrupt handling circuitry 100 with respect to fast interrupt request signal generation. FIG. 5 includes a curve 502 illustrating a slow clock signal SCLK, a curve 504 illustrating the PWM timer peripheral counter value, and curves 506, 508 and 510 illustrating generated interrupt signals with different latencies. In particular, curve 506 illustrates an interrupt signal (e.g., INTHL provided to a fast clock domain servicing circuit) with a half cycle latency corresponding to half a slow clock signal cycle, and curve 508 illustrates an interrupt signal INTFL with a full slow clock cycle latency. The curve 510, in contrast, shows the fast interrupt generation provided by the interrupt generator 110 and synchronizer 120 in FIG. 1 (INT\_OUT) described hereinabove. As previously mentioned, previous solutions use synchronization circuitry (not shown) to synchronize signaling associated with an interrupt event in the slow clock circuitry, which introduces a half cycle delay (e.g., curve 506) or a full slow clock cycle delay (curve 508). The above-described circuit 100, in contrast, does not use slow clock domain synchronizers, and delivers the interrupt request signal SET\_FLAG as the interrupt request line after it is synchronized to the fast clock domain as signal INT\_OUT so that asynchronous logic is fully contained. In this regard, the SET\_FLAG signal on node 111 is used as the clock to the flip-flop 112 that generates the interrupt input signal INT\_IN, and the circuitry 110, 120 generates the interrupt output signal INT\_OUT without any penalty in the slow clock domain.

**[0026]** FIG. 6 shows a method 600 to manage interrupts of a first circuit (e.g., circuit 101

described hereinabove) operated according to a first clock signal by a second circuit (e.g., circuit 102) operated according to a second clock signal slower than the first clock signal. The method 600 can be implemented using any suitable interrupt handling circuitry, such as the circuit 100 described hereinabove, or in other circuitry (not shown). At 602, an interrupt signal is generated, synchronized to the second clock signal. In one example, the slow clock domain circuit 102 described hereinabove provides the SET\_FLAG signal to the interrupt generator flip-flop 112, synchronized to the SCLK signal via the flip-flop 106. This generates the interrupt input signal INT\_IN at 602 with no slow clock domain latency (e.g., avoids the delays shown in curves 506 and 508 of FIG. 5 described hereinabove).

**[0027]** At 604 and 606, an interrupt output signal is provided to the first circuit 101 in response to the interrupt input signal. In the example described hereinabove, the interrupt generator flip-flop 112 provides the interrupt input signal INT\_IN to the synchronizer circuit 120 at 604 in FIG. 6, and the synchronizer circuit 120 provides the interrupt output signal INT\_OUT to the first circuit 101 at 606, synchronized to the fast clock signal FCLK. At 608, the first circuit provides an acknowledgement signal (e.g., ACK described hereinabove), synchronized to the fast clock signal FCLK. The method 600 further includes clearing the interrupt input and output signals at 610. In certain examples, the INT\_IN and INT\_OUT signals are cleared asynchronously with respect to the second clock signal SCLK by the clear circuitry 114, 116 in response to the acknowledgment signal ACK. In the circuit 100, the interrupt input and output signals INT\_IN and INT\_OUT are quickly cleared within two cycles of the first clock signal FCLK after the clear flip-flop 116 receives the acknowledgment signal ACK.

**[0028]** The described examples provide significant response time advantages over other solution that use slow clock domain synchronization of clear event signals generated in the fast clock domain. As shown in FIG. 4, such alternate solutions consume two additional slow clock cycles for synchronization before actually clearing the interrupt signal provided to the fast clock domain circuitry. In contrast, the described circuitry 100 and methods 600 avoid such additional interrupt clearing latency or delay by clearing the interrupt generated in the slow clock domain asynchronously to the slow clock signal SCLK. For example, in the circuit 100, the clear event signal ACK from the fast clock domain circuit 101 is used asynchronously to clear the same flip-flop 112 that generates the interrupt input signal INT\_IN to reliably clear the interrupt output signal INT\_OUT without any penalty in the slow clock domain. For interrupt generation, the

described circuits and methods deliver the interrupt output signal INT\_OUT synchronously with respect to the fast clock signal FCLK using the synchronizer circuit 120 to ensure clean signaling to avoid any asynchronous paths (e.g., metastability). This synchronization in practice is a small delay, particularly where the first clock speed is significantly higher than the slow clock speed. In the described circuit 100, moreover, implements a fast asynchronous clear path while still maintaining the final interrupt line to be fully synchronous to the fast clock domain.

**[0029]** Modifications are possible in the described embodiments, and other embodiments are possible, within the scope of the claims.

## CLAIMS

What is claimed is:

1. An interrupt handling circuit to manage interrupts of a first circuit operated according to a first clock signal by a second circuit operated according to a second clock signal slower than the first clock signal, the interrupt handling circuit comprising:

an interrupt generator circuit, including a first interrupt generator input to receive an interrupt request signal, a second interrupt generator input to receive an interrupt clear signal, and an interrupt generator output to provide an interrupt input signal synchronized to the interrupt request signal to selectively interrupt the first circuit; and

an interrupt clear circuit, including an output synchronized to the first clock signal to selectively provide the interrupt clear signal to reset the interrupt generator circuit in response to an acknowledgment signal from the first circuit.

2. The interrupt handling circuit of claim 1, wherein:

the interrupt request signal has a first state indicating no interrupt is requested by the second circuit, and a different second state indicating an interrupt is requested by the second circuit;

the interrupt clear signal has a first state, and a different second state;

the interrupt generator output is configured to provide the interrupt input signal in a first state in response to the second interrupt generator input receiving the interrupt clear signal in the first state, and to provide the interrupt input signal in a different second state in response to the interrupt request signal transitioning from the first state to the second state when the interrupt clear signal is in the second state; and

the interrupt clear circuit is configured to selectively provide the interrupt clear signal in the first state to reset the interrupt generator circuit to set the interrupt input signal to the first state in response to the acknowledgment signal from the first circuit.

3. The interrupt handling circuit of claim 2, further comprising a synchronizer circuit, including an input coupled with the interrupt generator output to receive the interrupt input signal, and an output synchronized to the first clock signal to provide an interrupt output signal to the first circuit.

4. The interrupt handling circuit of claim 3, wherein the synchronizer circuit comprises:  
a first flip-flop, including a data input connected to the interrupt generator output, a clock input connected to the first circuit to receive the first clock signal, and an output; and  
a second flip-flop, including a data input connected to the output of the first flip-flop, a clock input connected to the first circuit to receive the first clock signal, and an output connected to the first circuit to provide the interrupt output signal synchronized to the first clock signal.
5. The interrupt handling circuit of claim 4, wherein the interrupt generator circuit comprises a third flip-flop, including a data input connected to a reference voltage, a clock input connected to receive the interrupt request signal, a clear input connected to the output of the interrupt clear circuit to receive the interrupt clear signal, and an output connected to the interrupt generator output to provide the interrupt input signal to the data input of the first flip-flop.
6. The interrupt handling circuit of claim 3, wherein the interrupt generator circuit comprises a flip-flop, including a data input connected to a reference voltage, a clock input connected to receive the interrupt request signal, a clear input connected to the output of the interrupt clear circuit to receive the interrupt clear signal, and an output connected to the interrupt generator output to provide the interrupt input signal to the input of the synchronizer circuit.
7. The interrupt handling circuit of claim 2, wherein the interrupt generator circuit comprises a flip-flop, including a data input connected to a reference voltage, a clock input connected to receive the interrupt request signal, a clear input connected to the output of the interrupt clear circuit to receive the interrupt clear signal, and an output connected to the interrupt generator output to provide the interrupt input signal.
8. The interrupt handling circuit of claim 7, further comprising a second flip-flop, including a data input connected to the second circuit to receive the interrupt request signal, a clock input connected to receive the second clock signal, and an output to provide a synchronized interrupt request signal synchronized to the second clock signal.
9. The interrupt handling circuit of claim 1, wherein the first circuit, the second circuit, the interrupt generator circuit and the interrupt clear circuit are formed in a single integrated circuit.

10. An interrupt handling circuit to manage interrupts of a first circuit operated according to a first clock signal by a second circuit operated according to a second clock signal slower than the first clock signal, the interrupt handling circuit comprising:

an interrupt generator circuit to selectively interrupt the first circuit synchronously with respect to the first clock signal; and

an interrupt clear circuit, including an output to selectively reset the interrupt generator circuit in response to an acknowledgment signal from the first circuit asynchronously with respect to the second clock signal.

11. The interrupt handling circuit of claim 10, further comprising a synchronizer circuit, including an input coupled with an output of the interrupt generator circuit, and an output synchronized to the first clock signal to provide an interrupt output signal to the first circuit.

12. The interrupt handling circuit of claim 11, wherein the synchronizer circuit comprises:

a first flip-flop, including a data input connected to an output of the interrupt generator circuit, a clock input connected to the first circuit to receive the first clock signal, and an output; and

a second flip-flop, including a data input connected to the output of the first flip-flop, a clock input connected to the first circuit to receive the first clock signal, and an output connected to the first circuit to provide the interrupt output signal synchronized to the first clock signal.

13. The interrupt handling circuit of claim 12, wherein the interrupt generator circuit comprises a third flip-flop, including a data input connected to a reference voltage, a clock input connected to the first circuit to receive an interrupt request signal, a clear input connected to receive an interrupt clear signal from the interrupt clear circuit, and an output to selectively provide an interrupt input signal to reset the interrupt generator circuit.

14. The interrupt handling circuit of claim 10, further comprising a flip-flop, including a data input to receive an interrupt request signal from the second circuit, a clock input connected to receive the second clock signal, and an output to provide a synchronized interrupt request signal synchronized to the second clock signal to the interrupt generator circuit to selectively interrupt the first circuit.

15. The interrupt handling circuit of claim 10, wherein the first circuit, the second circuit, the interrupt generator circuit and the interrupt clear circuit are formed in a single integrated circuit.

16. A method to manage interrupts of a first circuit operated according to a first clock signal by a second circuit operated according to a second clock signal slower than the first clock signal, the method comprising:

generating an interrupt input signal synchronized to the second clock signal;

providing an interrupt output signal to the first circuit in response to the interrupt input signal; and

clearing the interrupt input and output signals asynchronously with respect to the second clock signal in response to an acknowledgment signal from the first circuit.

17. The method of claim 16, further comprising:

synchronizing the interrupt output signal to the first clock signal.

18. The method of claim 17, further comprising:

clearing the interrupt input and output signals within two cycles of the first clock signal of the acknowledgment signal.

19. The method of claim 16, further comprising:

clearing the interrupt input and output signals within two cycles of the first clock signal of the acknowledgment signal.

20. The method of claim 16, further comprising:

receiving an interrupt request signal from the second circuit;

generating the interrupt input signal in response to the interrupt request signal; and

providing the interrupt output signal to the first circuit in response to the interrupt input signal asynchronously with respect to the second clock signal.

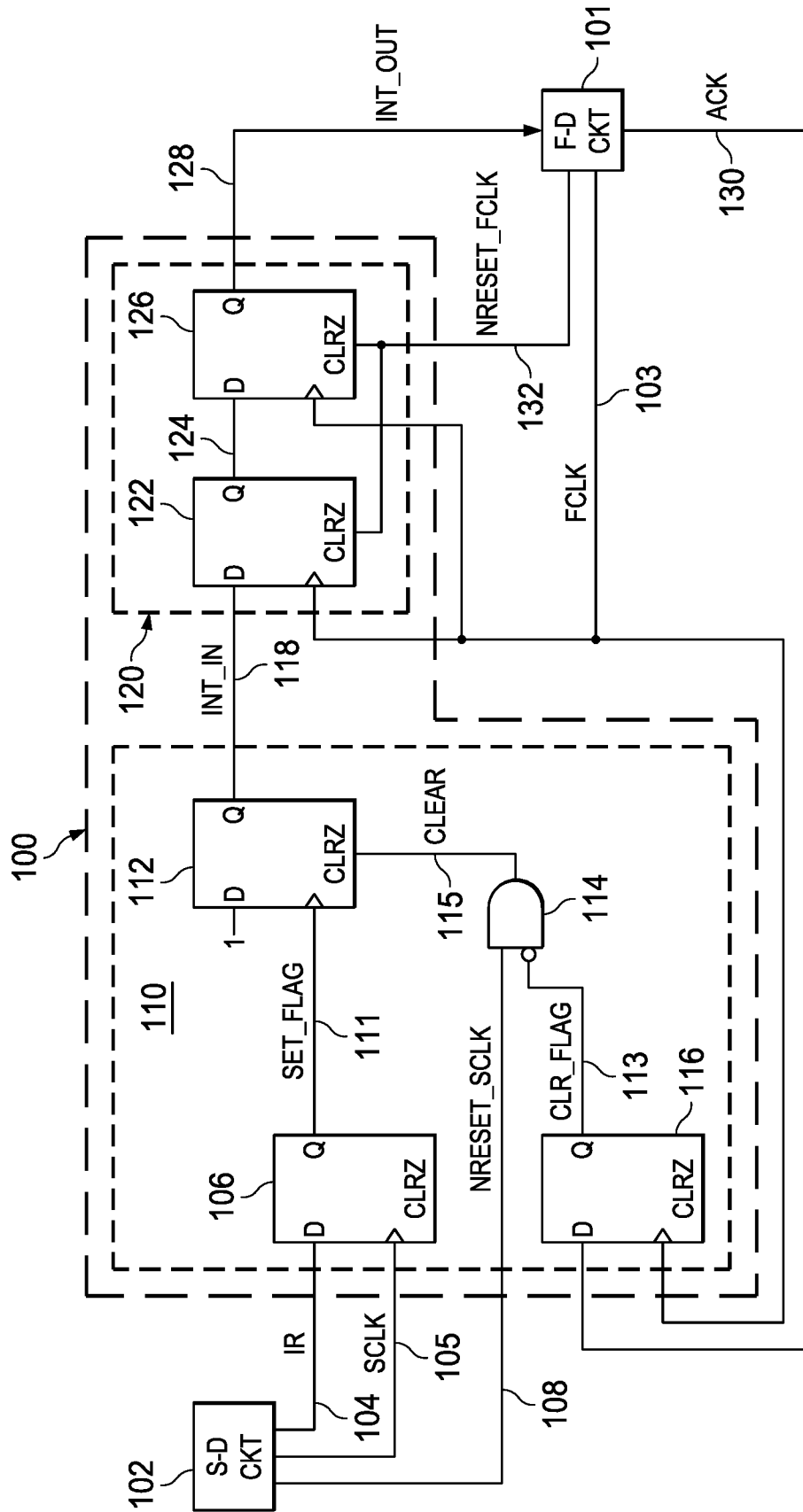


FIG. 1

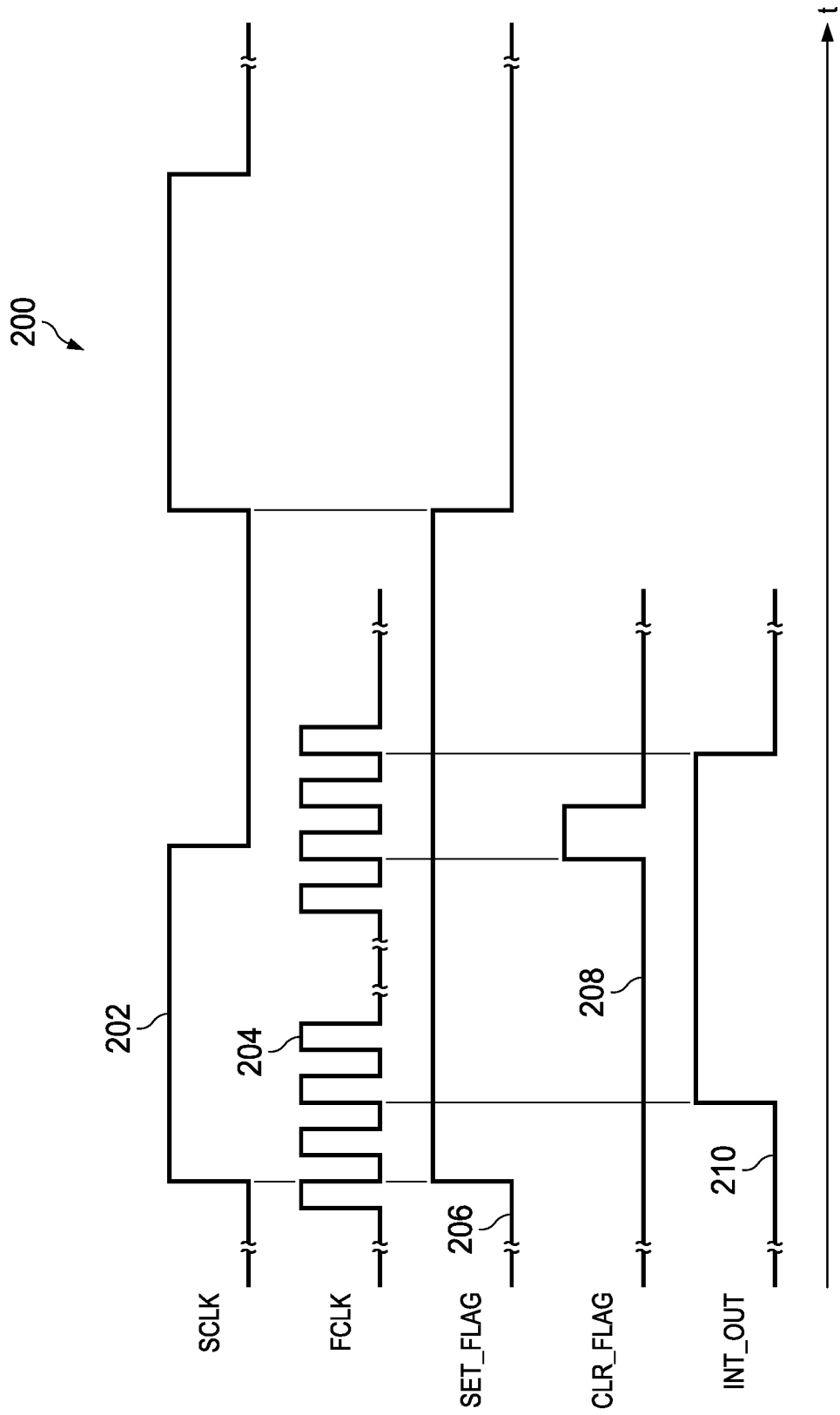


FIG. 2

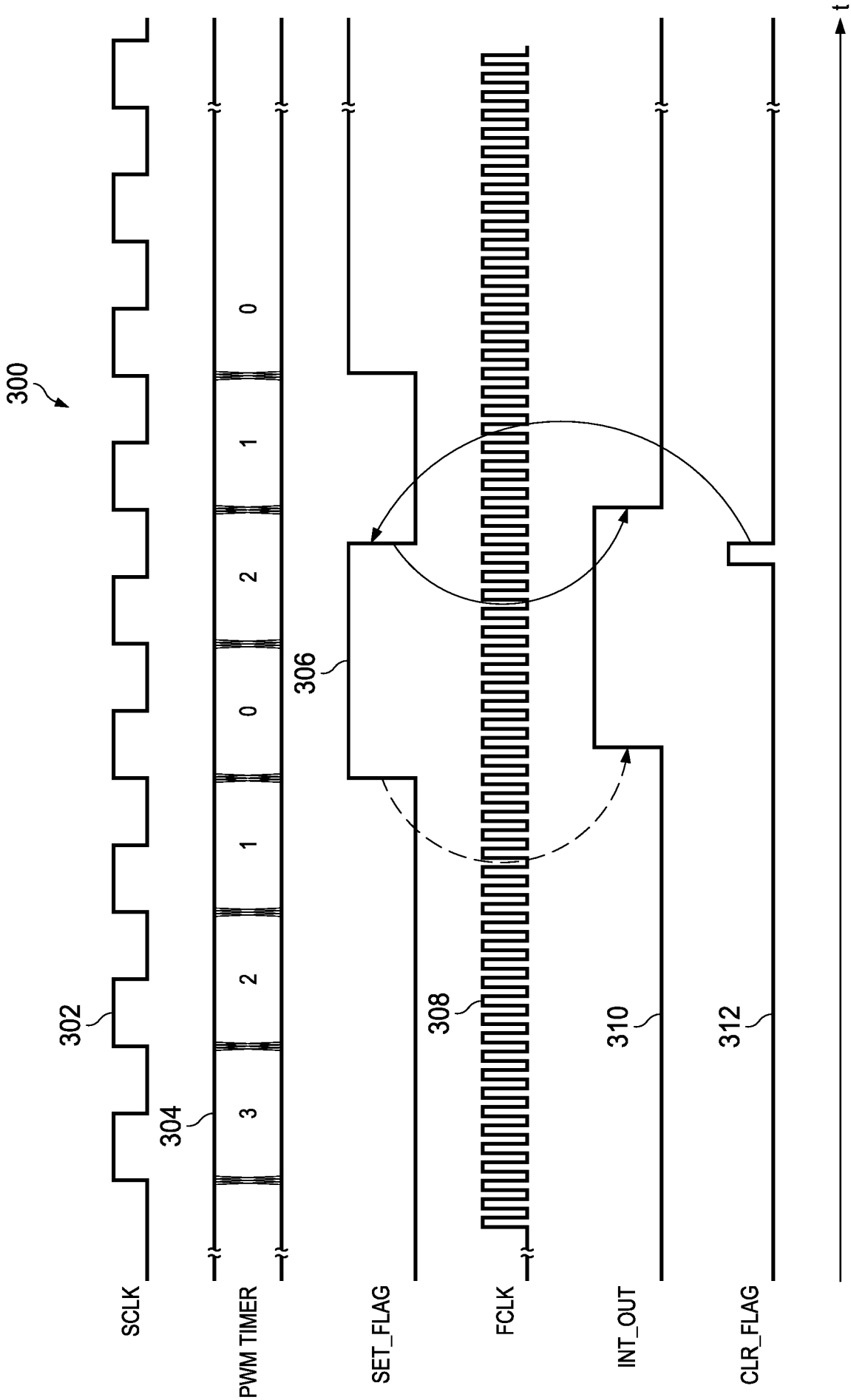


FIG. 3

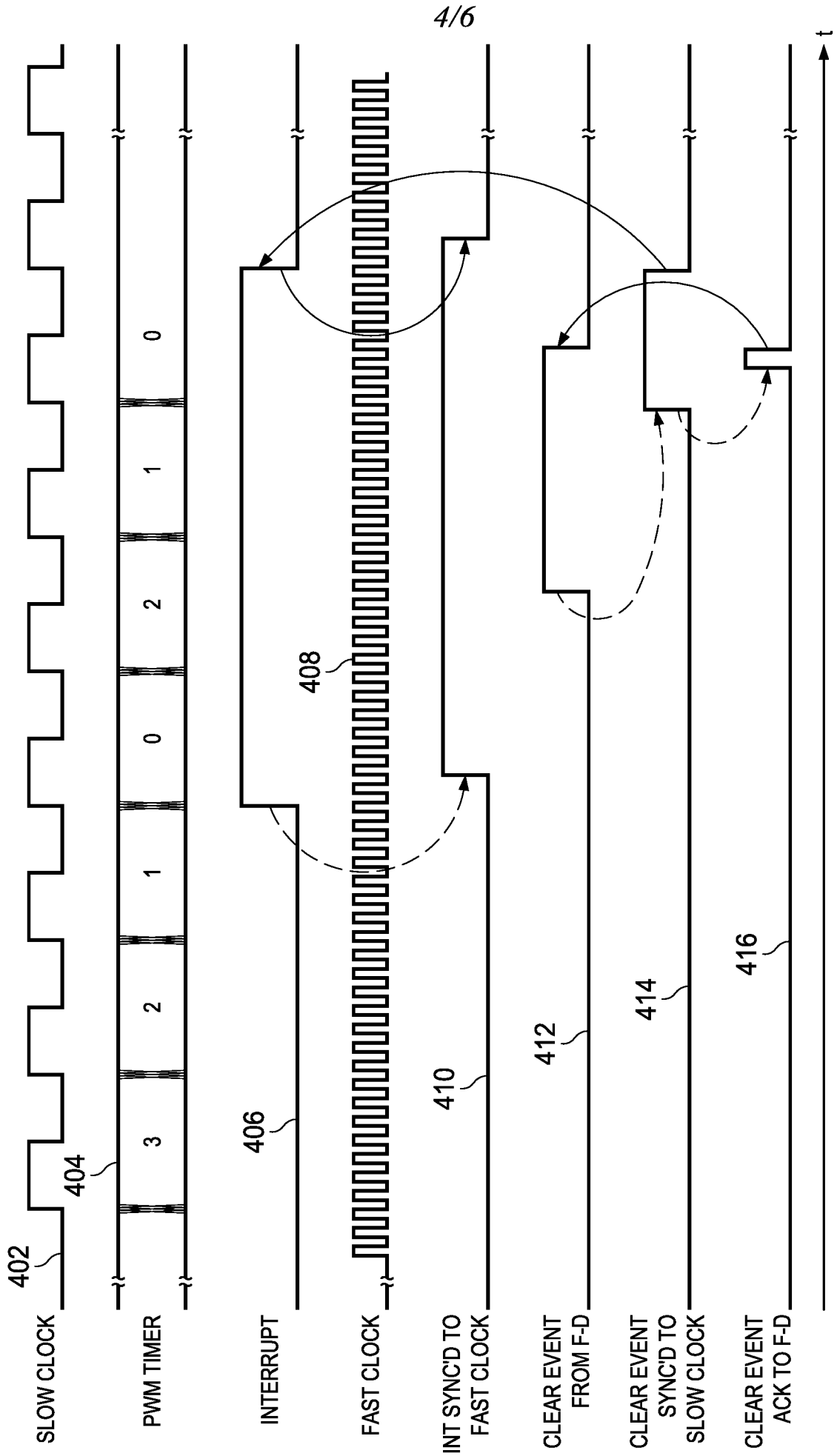


FIG. 4

400

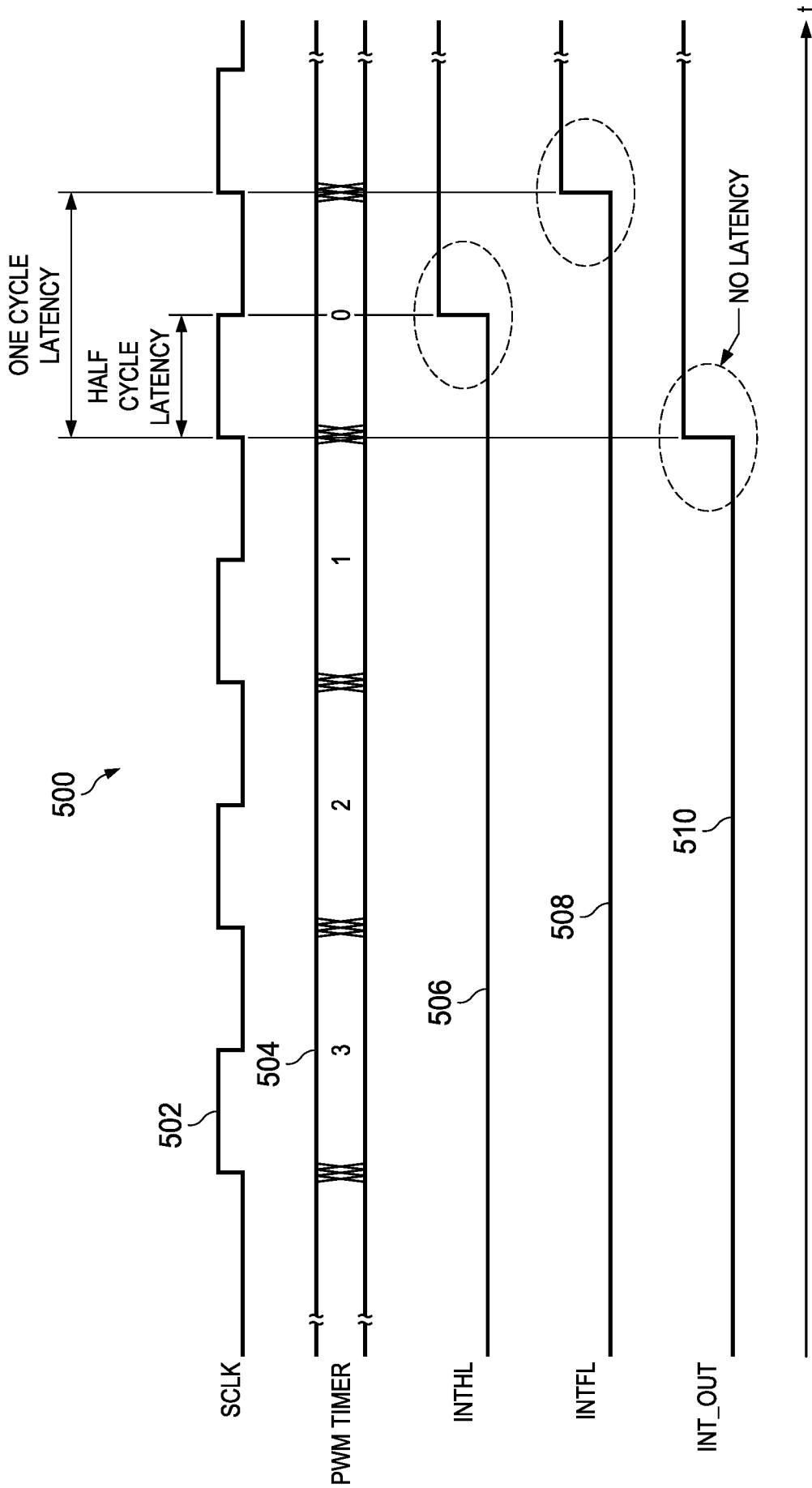


FIG. 5

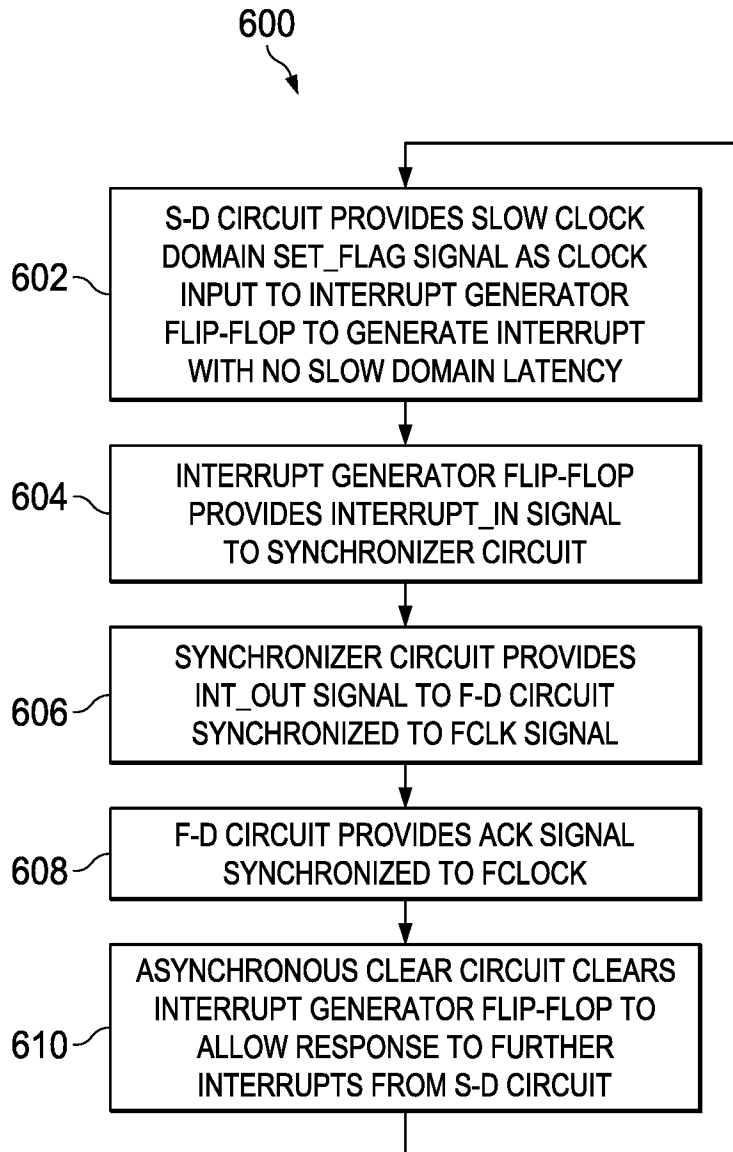


FIG. 6

**INTERNATIONAL SEARCH REPORT**

International application No.

PCT/US 2018/016206

A. CLASSIFICATION OF SUBJECT MATTER		
<i>G06F 9/48 (2006.01)</i>		
According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED		
Minimum documentation searched (classification system followed by classification symbols)		
G06F 9/00, 9/06, 9/46, 9/48		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched		
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)		
PatSearch (RUPTO internal), USPTO, PAJ, Esp@cenet, Information Retrieval System of FIPS		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	EP 0469543 A2 (GOLD STAR CO. LTD) 05.02.1992, abstract	1-20
A	US 2002/0019898 A1 (HITACHI, LTD) 14.02.2002, claim 10	1-20
A	US 2006/0064529 A1 (IBM CORP.) 23.03.2006, paragraphs [0024] - [0031]	1-20
<input type="checkbox"/> Further documents are listed in the continuation of Box C. <input type="checkbox"/> See patent family annex.		
* Special categories of cited documents:  "A" document defining the general state of the art which is not considered to be of particular relevance "E" earlier document but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed	"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art "&" document member of the same patent family	
Date of the actual completion of the international search		Date of mailing of the international search report
17 April 2018 (17.04.2018)		04 May 2018 (04.05.2018)
Name and mailing address of the ISA/RU: Federal Institute of Industrial Property, Berezhkovskaya nab., 30-1, Moscow, G-59, GSP-3, Russia, 125993 Facsimile No: (8-495) 531-63-18, (8-499) 243-33-37		Authorized officer  V. Alexandrov  Telephone No. (495) 531-64-81