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EUROPEAN PATENT APPLICATION

21 Application number: 78300236.3

51 Int. Cl.2: **A 61 N 1/36**

22 Date of filing: 03.08.78

30 Priority: 19.08.77 GB 34916/77
19.06.78 US 917140

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43 Date of publication of application: 07.03.79
Bulletin 79/5

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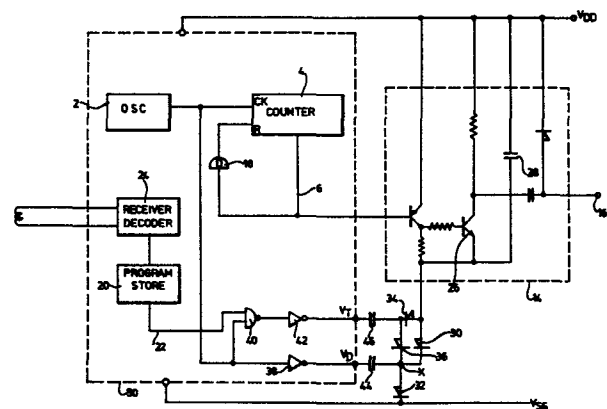
84 Designated Contracting States: **DE FR GB NL SE**

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64 Programmably variable voltage multiplier for implanted stimulator.

57 A free running oscillator (2) clocks a counter (4), which produces stimulation control signals at a predetermined count.

An output stage includes transistors, energized by the counter, to issue stimulating pulses having a voltage equal to that across a capacitor (28) in parallel with the output stage. The output capacitor is charged, between output pulses, by successive charge sharing cycles with at least one other capacitor (46), which is enabled by a stored program word, at a rate determined by the oscillator output cycles.



EP 0 000 983 A1

Programmably Variable Voltage Multiplier
For Implanted Stimulator

Technical Field

This invention relates to implantable body function control apparatus and particularly, but not exclusively, to body tissue stimulating devices such as cardiac pacemakers.

Background Art

Pacemakers for generating artificial stimulating pulses for the heart, and which may be implanted in the body, are well known. Originally the electrical circuitry for such pacemakers was of analog design, but in recent years digital circuitry has been also employed. A digital approach to pacemakers has led to the evolution of programmable pacemakers - pacemakers having parameters such as pulse rates which are adjustable (programmable) once the pacemaker has been implanted. Programmable pacemakers are described in, for instance, British Specifications 1,385,954 and 1,398,875. Such pacemakers have circuitry to detect and decode signals transmitted outside the body and alter the program accordingly. In British Specification 1,385,954 (claiming priority based on U.S.S.N. 141,694, in turn a parent of U.S.P.N. 3,805,796 to Tenz), the programming is accomplished by means of a magnetic field which is sensed by a magnetic reed switch; the opening and closing of the switch providing programming pulses to a program store. In British Specification 1,398,875 (based on U.S.P.N. 3,833,005 to Wingrove) the programming is by means of radio frequency transmission and reception.

It is desirable to miniaturize pacemaker components as far as possible, especially where implanted pacemakers are concerned, and although integrated circuit techniques can

help enormously to achieve this aim, the battery size is still a major problem. The most recently-available miniature batteries having sufficient power and life for pacemaker usage are lithium batteries (both of the "solid" and "viscous" types), and such batteries are now employed in pacemakers. Unfortunately, lithium batteries only generate about 3 volts and although this voltage is sufficient to provide the supply voltage for, say, an integrated circuit pacemaker, it is insufficient, in itself, for the pacemaker output stage which needs to generate artificial stimulating pulses of at least 5 volts. Under certain circumstances, it is even desirable to generate pacing pulses of greater magnitude (e.g. about 7.5 volts). Although two or more lithium batteries can be employed for such purposes (and, indeed, have in the past been so employed), this militates against the desire for maximum miniaturization.

Disclosure of Invention

We have now designed an implantable body function control apparatus which employs a single relatively low voltage source, but which generates, by means of voltage multiplication, the higher voltages for the pacing pulses issued.

According to the invention, there is provided a body function control apparatus comprising an oscillator, means responsive to the oscillator for generating tissue stimulating pulse control signals, an output stage responsive to signals from the control signal generating means for providing tissue stimulating pulses to the body, a voltage source for said apparatus, voltage multiplication means responsive to said oscillator and said voltage source for generating one or more voltages of magnitude higher than that supplied by said voltage source and for supplying said higher voltage(s) to said output stage whereby tissue stimulating pulses of voltage magnitude higher than that supplied by said voltage source are provided.

Although this invention is of especial use for cardiac pacemakers, it is not restricted to such use and could be employed for controlling other body functions.

Brief Description of the Drawing

Preferred features of the invention are illustrated

with reference to the accompanying drawing, which schematically illustrates an electrical circuit diagram of a programmable fixed-rate implanted cardiac pacemaker according to the invention.

Best Mode of Carrying Out the Invention

5 Referring to the drawing, the pacemaker comprises an oscillator 2 which drives a ripple counter 4. An output of the ripple counter (which may actually be the combination of several stages of the counter) supplies an output line 6. The oscillator frequency and the ripple counter output
10 selected provided signals on line 6 at an appropriate body stimulation pulse frequency. Line 6 is connected to an output amplifier (within the block formed by the dashed line 14), from whence amplified stimulating pulses are passed to a connection 16 which itself is connected to the active stimulating
15 electrode (not shown) disposed in or on the heart. Line 6 is also connected to a delay unit 18 which, after an appropriate time, resets the counter 4, to enable the next appropriately timed pulse to be transmitted.

The output amplifier 14 includes an output transistor
20 26, across which is connected a capacitor 28. One end of the latter is connected to the rail V_{DD} of the supply voltage. The other end of capacitor 28 and the emitter of transistor 26 are connected to a chain of Schottky diodes 30, 32, 34, and
25 36 (Schottky diodes are chosen for their low voltage drop when forward-biased). The cathode of diode 32 is connected to the rail V_{SS} of the supply voltage. For the purposes of illustration, the supply voltage $V_{SS}-V_{DD}$ is about 3 volts. The output of oscillator 2 is supplied to an inverter 38 and via a NAND
30 gate 40 to a second inverter 42. The inverters feed, respectively, capacitors 44 and 46 which lead into the diode chain as illustrated. NAND gate 40 is supplied with a further input, which is from a control line 22 from a pacemaker program store 20.

The pacemaker program store 20 holds a binary bit of
35 information which is transmitted on line 22 for voltage multiplication purposes as to be described. A receiver/decoder 24 is arranged to receive and decode data signals transmitted from outside the patient's body to the implanted pacemaker,

and to employ the decoded signals for changing the pacemaker program held in program store 20. For the purposes of illustration, the receiver/decoder 24 and store 20 have been depicted very simply and as providing an output for selecting only the stimulating pulse amplitude. In practice it would be desirable to make these features much more sophisticated so that the program store is employed to provide a varying control for several different pacemaker parameters (e.g. not only pulse amplitude, but also pulse rate, pulse width, hysteresis). The data signals may be transmitted to the receiver/decoder 24 by any suitable means, but preferably we employ data signals transmitted by tone burst modulation (a carrier frequency being pulse width modulated). A receiver/decoder and program store for such data signals is described in copending Application No. filed on even date (ref. DLD-10).

Many of the pacemaker components described are constructed as a MOS integrated circuit, and this has been indicated by the block formed by the dashed line 50. The integrated circuit is supplied as is customary, with V_{DD} and V_{SS} , but it will be observed that the output transistor 26 of amplifier 14 is connected across V_{DD} and V_{SS} in series with the diode chain and with capacitor 28 in parallel.

The pacemaker operates as follows. Each pulse on output line 6 at the selected rate is passed to output amplifier 14 where it is amplified and conducted to the heart; it is also conducted to delay unit 18. After an appropriate delay corresponding to the pacing pulse width desired, delay unit 18 resets counter 4 and the count then commences in counter 4 for the next appropriately timed pulse to be issued.

In normal operation V_{DD} is essentially the circuit ground by reason of being connected to the pacemaker indifferent electrode and V_{SS} is supplied at about 3 volts. This 3 volt supply is sufficient for the integrated circuit 50, but insufficient for the output amplifier 14, which in conventional practice needs to generate stimulating pulses of at least about 5 volts for satisfactory pacing. It will be assumed that normally about 5 volts is desired for each pacing pulse but that, under certain circumstances, larger pacing pulses (of

about 7.5 volts) are required. The manner in which the approximately 5 volt pulses are generated will first be described, and then the manner in which the 7.5 volt pulses are generated.

For 5 volt stimulating pulses, a "0" is held in
5 program store 20 and is supplied on line 22 to NAND gate 40. The output of NAND gate 40 will be high and point V_T (between inverter 42 and capacitor 46) will always be low. V_T will therefore not manifest the oscillator square wave output. On the other hand, point V_D (between inverter 38 and capacitor
10 44) will manifest the square wave output of oscillator 2. Point "X", at the junction of diodes 30, 32, 36 will, in the absence of the oscillator square wave pulse train and ignoring the voltage drop across diode 32, normally be held at V_{SS} (-3 volts). Capacitor 28 charges to -30 volts via diodes 30 and
15 32. When V_D goes to its most positive due to the square wave pulse train supplied by oscillator 2, a 3 volt drop will exist across capacitor 44 and the latter will charge via diode 32. When V_D goes negative due to the oscillator pulse train, point X goes further negative. At this time diode 30 is forward-
20 biased and it conducts, causing capacitor 28 to acquire an amount of charge due to the sharing of charge between capacitors 44 and 28. Taking into account diode voltage drops and assuming that no current is being drawn from the output amplifier circuit (no pacing pulse being issued), capacitor 28
25 will charge to about 5 volts over several cycles of the oscillator pulse train and it will hold its charge until a pacing pulse is transmitted to the output amplifier 14 from the integrated circuit 50. With no current being drawn from the output transistor 26, and hence no potential drop across
30 its collector resistor, the 5 volt potential held by capacitor 28 appears directly across output transistor 26 and hence the amplitude of the pacing pulse transmitted to the active electrode at connection 16, when this transistor is switched on, is at about 5 volts rather than the 3 volts supplied by
35 V_{DD}/V_{SS} . It will be appreciated that capacitor 28 will charge to 5 volts gradually over several cycles of the oscillator frequency, but provided that the latter frequency is much higher than the stimulating pulse frequency, capacitor 28 will

always be charged to 5 volts ready for discharge on the next pacing pulse.

5 When pacing pulses of about 7 volts magnitude are desired, a "1" is held in program store 20 and is supplied on line 22 to NAND gate 40. The output downstream of inverter 42 (at V_T) is the oscillator square wave pulse train but in anti-phase to the similar pulse train at V_D .

10 Under such circumstances, when V_D goes negative, point X goes further negative, as previously explained, and V_T will be positive charging capacitor 46 (about about -5 volts). When V_D goes positive, V_T will go negative and capacitor 46 will share its charge with capacitor 28. The effect is for capacitor 28 to charge to a higher voltage than it would have done if charged only from capacitor 44. Taking into account
15 diode drops, and assuming that no current is drawn from output transistor 26, capacitor 28 will charge, over several cycles of the oscillator pulse train, to a potential difference of about 7.5 volts. When a pacing pulse is transmitted to the output amplifier 14, this 7.5 volts is employed to provide
20 a pacing pulse to connection 16 of corresponding magnitude.

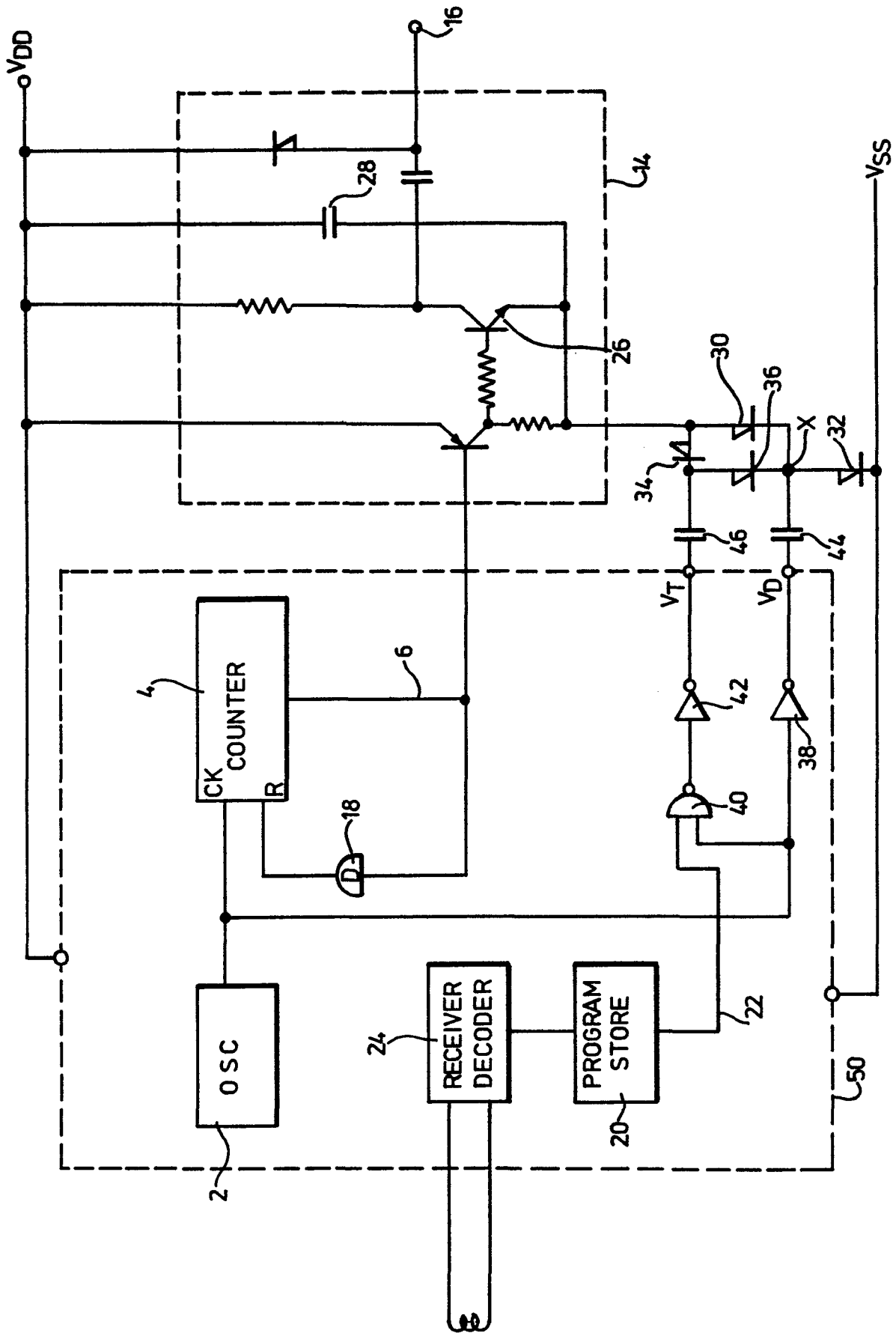
It will thus be appreciated that the presence of a "0" or "1" on line 22 controls the magnitude of the pacing pulses.

25 Although the above embodiment relates to a fixed-rate cardiac pacemaker, it will be appreciated that this is only given for the purposes of example, and the invention is equally-applicable to demand cardiac pacemakers, or to body function control apparatus employed to provide stimulating pulses of varying amplitude to other parts of the body.

What is claimed is:

- 1 1. In a programmable pacer system having a remote
2 source of program control signals, an implantable pacer
3 comprising:
 - 4 a) a voltage supply;
 - 5 b) oscillator means for producing a pulse signal
6 having a fixed frequency;
 - 7 c) counter means for generating a pacer output
8 control signal upon each occurrence of a pre-determined
9 number of oscillator pulses;
 - 10 d) memory means for receiving from said source and
11 for storing a program control signal representative
12 of a desired multiplication factor of said supply
13 voltage for pacer stimulation signals;
 - 14 e) output means, responsive to said output control
15 signal, for generating pacer stimulation signals,
16 said output means including:
 - 17 (i) a first capacitor coupled on one side to
18 said supply, and
 - 19 (ii) transistor means, connected in parallel
20 with said capacitor and enabled by said output
21 control signal, for generating stimulation signals
22 having an amplitude of the voltage on said capacitor
23 at the time occurrence of said control signal;
 - 24 f) capacitor means, enabled by said stored program
25 control signal, and charged by successive excursions
26 of said oscillator pulse signal, for supplying charge
27 increments to the other side of said first capacitor
28 during successive opposite excursions of said oscillator
29 pulse signal.
- 1 2. A pacer as described in claim 1 wherein said
2 capacitor means includes a plurality of capacitors, in parallel
3 with one another, and switching means, controlled by said
4 memory means, for selectively coupling said plurality of
5 capacitors to said oscillator, thereby correspondingly altering
6 said supplying of charge to said first capacitor, and in turn
7 altering the amplitude of said stimulator signals.
- 1 3. A pacer as described in claim 2 wherein said
2 capacitor means further includes a plurality of diodes connected

3 with said other side of said first capacitor, and closing a
4 circuit with said supply, said plurality of capacitors being
5 respectively coupled to respective nodes intermediate said
6 diodes.





DOCUMENTS CONSIDERED TO BE RELEVANT			CLASSIFICATION OF THE APPLICATION (Int. Cl.?)
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	
	<p><u>US - A - 4 031 899</u> (VITETRON) * Column 7, lines 14-20, 37,38; column 8, lines 10-23, 55-66; column 9, lines 11-17 *</p> <p>---</p> <p><u>US - A - 3 707 974</u> (RADDI) * Column 5, line 50 to column 6, line 41 *</p> <p>---</p> <p><u>US - A - 3 726 285</u> (GEC) * Column 5, line 43 to column 6, line 14 *</p> <p>---</p> <p>D <u>US - A - 3 833 005</u> (MEDTRONIC) * Column 1, lines 25-35; column 12, lines 43-48 *</p> <p>---</p> <p><u>US - A - 3 656 487</u> (MEDTRONIC) * Column 2, lines 21-26 *</p> <p>---</p> <p><u>DE - A - 2 639 554</u> (PLESSEY) * Page 6 *</p> <p>-----</p>	<p>1</p> <p>1,2</p> <p>1,2</p> <p>1</p> <p>1</p> <p>2,3</p>	<p>A 61 N 1/36</p> <p>TECHNICAL FIELDS SEARCHED (Int.Cl.?)</p> <p>A 61 N 1/36 H 02 M 3/00 H 03 K 3/57</p> <p>CATEGORY OF CITED DOCUMENTS</p> <p>X: particularly relevant A: technological background O: non-written disclosure P: intermediate document T: theory or principle underlying the invention E: conflicting application D: document cited in the application L: citation for other reasons</p> <p>&: member of the same patent family, corresponding document</p>
<input checked="" type="checkbox"/>	The present search report has been drawn up for all claims		
Place of search	Date of completion of the search	Examiner	
The Hague	27-11-1978	SIMON	