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(71) Applicant *(for all designated States except US)*: **MOSAID TECHNOLOGIES INCORPORATED** [CA/CA]; 11 Hines Road, Suite 203, Ottawa, Ontario K2K 2X1 (CA).

(72) Inventor; and
(75) Inventor/Applicant *(for US only)*: **KIM, Jin-Ki** [CA/CA]; 46 Ironside Court, Kanata, Ontario K2K 3H6 (CA).

(74) Agent: **HAMMOND, Daniel, A.**; Mosaid Technologies Incorporated, 11 Hines Road, Suite 203, Ottawa, Ontario K2K 2X1 (CA).

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(54) **Title**: STACKED SEMICONDUCTOR DEVICES INCLUDING A MASTER DEVICE

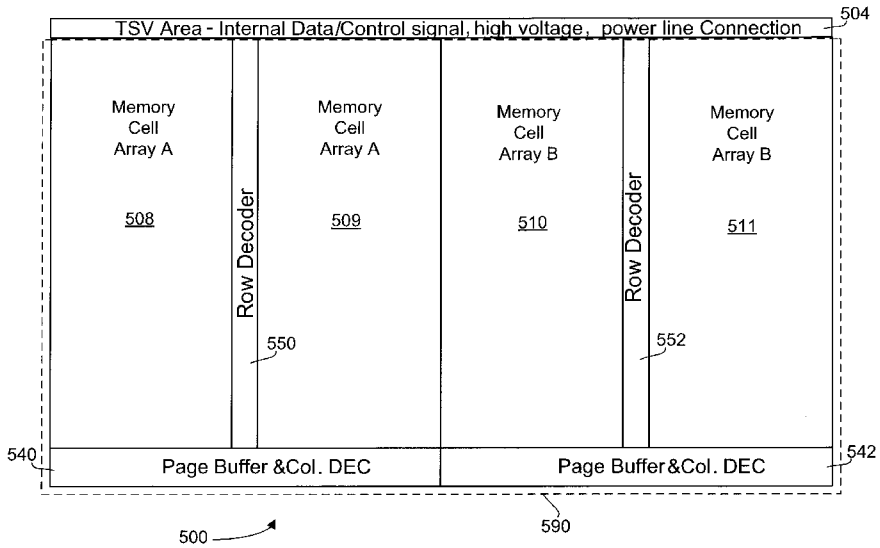


FIG. 5

(57) **Abstract**: The present invention discloses a system comprising a stack which includes a first non-volatile memory chip, and a second non-volatile memory chip, the second non- volatile memory chip lacking in at least some non-core circuitries, and a plurality of electrical paths extending between the first non-volatile memory chip and the second non-volatile memory chip, the electrical paths facilitating the first non-volatile memory chip in providing the second non-volatile memory chip with signals and voltages needed for device operations.

WO 2010/096901 A1

# STACKED SEMICONDUCTOR DEVICES INCLUDING A MASTER DEVICE

## CROSS REFERENCE TO RELATED APPLICATIONS

**[0001]** This application claims the benefit of priority of U.S. Provisional Patent Application Serial No. 61/154,910 filed February 24, 2009 and U.S. Patent Application Serial No. 12/429,310 filed April 24, 2009, which are incorporated herein by reference in their entireties.

## BACKGROUND OF THE DISCLOSURE

**[0002]** Today, many electronic devices include memory systems to store information. Some memory systems store, for example, digitized audio or video information for playback by a respective media player. Other memory systems store, for example, software and related information to carry out different types of processing functions. Also, some types of memory systems such as, for example, Dynamic Random Access Memory (DRAM) systems and Static Random Access Memory (SRAM) systems are volatile memory systems in that stored data is not preserved when the power is off, whereas other types of memory systems such as, for example, NAND flash memory systems and NOR flash memory systems are nonvolatile memory systems in that stored data is preserved when the power is off.

**[0003]** As time progresses, consumers have an expectation that memory systems will have increasingly larger capacities provided by chips of increasing smaller size. Historically an important factor in the ability to do this has been the scaling down of process technology; however it is quite possible that in the near future the costs and limits of this approach could become increasingly more ominous. For example, as process technology is scaled down below 50nm, it becomes extremely challenging to develop memory devices in smaller geometry, especially flash memories due to worsening transistor characteristics and reliability such as retention and endurance. Also, the scaling down of process technology is a huge investment. Thus, in view of the above costs and limits of the scaling down of process technology, there is a need to research and develop new ways to realize memory systems of increasingly larger capacities.

SUMMARY

**[0004]** It is an object of the invention to provide improved semiconductor devices that are adapted to be stacked.

**[0005]** According to one aspect of the invention, there is provided a system that includes a stack. The stack includes a first non-volatile memory chip and a second non-volatile memory chip. The second non-volatile memory chip is lacking in at least some non-core circuitries so that chip size reduction is facilitated. A plurality of electrical paths extend between the first non-volatile memory chip and the second non-volatile memory chip. The electrical paths facilitate the first non-volatile memory chip in providing the second non-volatile memory chip with signals and voltages needed for device operations.

**[0006]** According to another aspect of the invention, there is provided a method that includes manufacturing first and second non-volatile memory chips that are compatible with each other. The first and second non-volatile memory chips are manufactured having substantially similar core chip areas, but with only the first non-volatile memory chip having additional chip areas within which are located circuitries providing functionality for the shared of benefit of both the first and second non-volatile memory chips. The circuitries of the additional chip areas are configured to generate signals and voltages needed for device operations in relation to both the first and second non-volatile memory chips.

**[0007]** According to yet another aspect of the invention, there is provided a method that includes stacking at least two semiconductor chips. One of the semiconductor chips is a master memory device and another of the semiconductor chips is a slave memory device. The method also includes wiring the stacked semiconductor chips together by Through-Silicon Vias, and connecting the stacked semiconductor chips to a package printed circuit board by flip chip and bumping.

**[0008]** According to yet another aspect of the invention, there is provided a non-volatile memory chip that includes core chip areas that take up most (for example, greater than eighty percent, or even greater than ninety percent) of an entire chip area of the non-volatile memory chip. Within an additional chip area of the non-volatile

memory chip there are located circuitries configured to receive signals and voltages from another non-volatile memory chip. The core chip areas having a more miniaturized process technology as compared to the additional chip area.

**[0009]** Thus, an improved system that includes one or more memory devices has been provided.

BRIEF DESCRIPTION OF THE DRAWINGS

**[0010]** Reference will now be made, by way of example, to the accompanying drawings:

**[0011]** FIG. 1 is a block diagram of an example NAND flash chip floor plan;

**[0012]** FIG. 2 is a block diagram of another example NAND flash chip floor plan;

**[0013]** FIG. 3 is a block diagram of yet another example NAND flash chip floor plan;

**[0014]** FIG. 4 is a block diagram of a NAND flash chip floor plan for a master memory device in accordance with an example embodiment;

**[0015]** FIG. 5 is a block diagram of a NAND flash chip floor plan for a slave memory device in accordance with an example embodiment;

**[0016]** FIG. 6 is a block diagram showing a master memory device and three slave memory devices in accordance with an example embodiment;

**[0017]** FIG 7 shows, in diagrammatic form, a top view of one example of a stack consistent with the flash memory example embodiment shown in FIG. 6;

**[0018]** FIG 8 shows, in diagrammatic form, a cross sectional view of the example stack shown in FIG. 7;

**[0019]** FIG. 9 shows, in diagrammatic form, a cross sectional view similar to a the cross sectional view of the example of FIG. 8, but additionally illustrating details of how an apparatus comprising the stacked devices may further include a package in which flip chip and bumping technology is employed;

**[0020]** FIG. 10 shows, in diagrammatic form, a cross sectional view similar to a the cross sectional view of the example of FIG. 8, but additionally illustrating details of

how an apparatus comprising the stack (i.e. stacked devices) may further include a conventional Ball Grid Array (BGA) package adapted for wire bonding technology;

**[0021]** FIG. 11 is a block diagram of a NAND flash chip floor plan for a master memory device in accordance with an alternative example embodiment;

**[0022]** FIG. 12 is a block diagram of a NAND flash chip floor plan for a slave memory device in accordance with an alternative example embodiment; and

**[0023]** FIG. 13 is a block diagram of a NAND flash chip floor plan for a slave memory device in accordance with another alternative example embodiment.

**[0024]** Similar or the same reference numerals may have been used in different figures to denote similar example features illustrated in the drawings. Also, various example embodiments have not been shown to scale in the drawings. For example, the dimensions of certain illustrated elements or components may have been exaggerated for convenience of illustration.

## DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

**[0025]** Although the term "area" may in other contexts be understood to mean a two-dimensionally defined space, it will be understood that a three-dimensionally defined space (zone) is consistent with the term "area" as is it used herein.

**[0026]** FIG. 1 is a block diagram of an example NAND flash chip floor plan 100 illustrating one possible dividing of the placement of major components within the chip area of a flash memory device. In the floor plan 100, two row decoder areas 110 and 112 extend between adjacent memory cell array areas 114 and 116, and 118 and 120 respectively. With respect to row decoder areas 110 and 112, it is within these areas that the row decoders of the flash memory device can be found. As will be understood by those skilled in the art, a row decoder is a component of a memory device that selects a page for either a read or program operation. By contrast, for a conventional erase operation, a block rather than a page is selected by the row decoder. With respect to memory cell array areas 114, 116, 118 and 120, it is within these areas that the memory cell arrays of the flash memory device can be found. As will be understood by those skilled in the art, the memory cell array of a flash memory device comprises many

(for example, millions) of flash memory cells, each within which one or more bits (logic '1's or '0's) may be stored.

**[0027]** Extending along width-wise edges of the floor plan 100 are input/output pad areas 124 and 126, and extending along length-wise edges of the floor plan 100 are high voltage generator areas 130 and 132, and peripheral circuit area 134. With respect to input/output pad areas 124 and 126, it is within these areas that the input/output pads of the flash memory device can be found. As will be well understood by those skilled in the art, various signals travel through these pads, into or out from the memory chip. Also, in accordance with at least one alternative example, it is contemplated that an input/output pad area similar to the illustrated areas may extend along the length-wise edge (of a floor plan) nearest the peripheral circuit area.

**[0028]** With respect to high voltage generator areas 130 and 132, it is within these areas that one finds the high voltage generators of the flash memory device such as, for example, charge pumps. In some examples, a "high voltage" means a voltage higher than an operating voltage (for instance, a voltage higher than Vcc). Also the high voltage generators, in some examples, collectively generate a range of higher voltages.

**[0029]** With respect to peripheral circuit area 134, it is within this area that other circuitry important for device operation such as, for example, the following:

**[0030]** • Input and output buffers for address and data

**[0031]** • Input buffers for control and command signals

**[0032]** • State machine including command decoder

**[0033]** • Address counter

**[0034]** • Row and column pre-decoder

**[0035]** • Status register

**[0036]** Also, adjacent the peripheral circuit area 134 is additional circuit areas 140 and 142. It is within these areas that the page buffers and column decoders of the flash memory device can be found. Page buffers and column decoders are components of a flash memory device having functions well known to those skilled in the art. For

example, input data is sequentially loaded into a page buffer via a column decoder during flash memory programming.

**[0037]** Those skilled in the art will appreciate that chip floor plans for non-volatile memories will vary, within working constraints and specifications, depending on the choice of the designer. For instance, FIG. 2 is a block diagram of another example NAND flash chip floor plan 200 different from the one shown in FIG. 1. In the floor plan 200, there is a row decoder area 202 extending between two relatively adjacent edges of the areas of planes 214 and 220. Comparing the floor plan 200 to the floor plan 100, one finds the following differences (non-exhaustive list): the row decoder area 202 extends down the center of the floor plan 200 rather than having two spaced-apart row decoder areas, there is only a single high voltage generator area 230, input/output pad areas 232 and 234 extend along a floor plan edge that is adjacent peripheral circuit area 237. As contrasted to some of the other areas, it is noted that additional circuit areas 240 and 242 for page buffers and column decoders are similarly located to the areas 140 and 142 shown in FIG. 1.

**[0038]** FIG. 3 is a block diagram of yet another example NAND flash chip floor plan 300 different from the others shown and described previously. In the floor plan 300, a first circuit area 310 for page buffers and column decoders is located midway between areas of a first plane (Plane 0). A second circuit area 312 also for page buffers and column decoders is located midway between areas of a second plane (Plane 1). Somewhat similar to the floor plan 200 shown in FIG. 2, there is provided an input/output pad area 320 that extends along a floor plan edge that is adjacent the peripheral circuit area, and also there is only a single high voltage generator area 340.

**[0039]** Further details regarding the floor plan 300 are provided in Zeng et al., "A 172mm2 32Gb MLC NAND Flash Memory in 34nm CMOS", ISSCC 2009 Digest of Technical Papers, pp. 236-237.

**[0040]** In accordance with at least some example embodiments, flash memory devices are categorized as one of two possible types: a master flash chip and a slave flash chip. The floor plan of a master device may in many respects be similar to one of a conventional NAND flash memory, but with the inclusion of a TSV area. In this

regard, FIG. 4 is a block diagram of a NAND flash chip floor plan 400 in accordance with an example embodiment.

**[0041]** In the illustrated floor plan 400, a Through-Silicon Vias (TSV) area 404 is located along a length-wise edge adjacent cell array area 408-411 (illustrated top of the chip, opposite side from input and output pads area 420). Also, areas 430, 432, 434, 440, 442, 450 and 452 are similar in layout to the areas 130, 132, 134, 140, 142, 110, 112 respectively that were described previously (floor plan 100 shown in FIG. 1). In accordance with at least some examples, the illustrated floor plan 400 corresponds to the floor plan of a master memory device of a system, as contrasted to a slave device.

**[0042]** In accordance with some example embodiments, a master device includes an address decoder, a pre-row decoder and a pre-column decoder for addressing slave devices. Differences between master and slave devices will become more clear from details subsequently provided in the present disclosure.

**[0043]** Reference will now be made to FIG. 5. FIG. 5 is a block diagram of a NAND flash chip floor plan 500 for a slave memory device in accordance with an example embodiment. The device architecture of the illustrated example slave device includes a TSV area 504. Signal interface circuitries are located in the TSV area 504 and also the TSV area 404 (FIG. 4). Signal interface circuitries are, for example, circuitries that facilitate the transmitting and receiving of internal data and control signals, high voltage signals for read, program and erase operations, and Vcc and Vss power supply signals. Also, it will be apparent that TSV areas are so named because they are adapted to have TSVs extend through them, in order to provide electrical paths between chips in a stack.

**[0044]** Still with reference to FIG. 5, the other illustrated areas are NAND memory cell array areas 508-511, page buffer and column decoder areas 540 and 542, and row decoder areas 550 and 552. These areas comprise core areas 590 for the NAND memory core. In some examples, the core areas 590 are characterized by smaller sized features as compared to features within the TSV area 504 (for example, the process technology is more miniaturized).

**[0045]** FIG. 6 is a block diagram showing a four device, 64Gb flash memory 600 in accordance with an example embodiment, and the 64Gb flash memory 600 having one 16Gb master device 602 and three 16Gb slave devices 605-607. From the block diagram, it will be seen that the master device 602 includes a block 610 representative of areas for the input and output pads, peripheral circuitries and the high voltage generators; however similar areas are lacking within the slave devices 605-607 translating into very significant chip size reduction.

**[0046]** With respect to the above-described quad die stacked example embodiment, there is one 16Gb master device and three 16Gb slave devices (i.e. total 64Gb memory capacity for all four devices). The master device 602 addresses 64Gb memory space total, 16Gb in the master device 602 and 48Gb in the slave devices 605-607. Of course it will be understood that in some alternative example embodiments more than four dies will be stacked, and in other alternative example embodiments fewer than four devices may be stacked. Furthermore, example embodiments are in no way limited by memory capacities of the devices, and all suitable memory capacities are contemplated.

**[0047]** FIG. 7 and FIG. 8 diagrammatically depict the top view and cross sectional view respectively of the 64Gb flash memory 600 described in connection with FIG. 6. The master device and three slave devices are connected with TSVs. The number of TSVs could be any number (for example, several tens, hundred or thousands) that one skilled in the art would understand to be suitable for the given stack of master and slave chips. In the illustrated example of FIG. 8, four flash devices are stacked, but stacking of any two or more non-volatile memory devices is contemplated.

**[0048]** FIG. 9 diagrammatically depicts a cross sectional view similar to FIG. 8, but additionally illustrating details of how the flash memory 600 may be in a package in which flip chip and bumping technology is employed. In the illustrated example, bumping balls 920 are located between the master flash chip and a package Printed Circuit Board (PCB) 930. Beneath and in connection with the package PCB 930 are package balls 940. Although for simplicity and convenience of illustration only two paths that each extend from the master flash chip, through a bumping ball, through the

package PCB and through a package ball are shown, it will understood that many such paths will normally be present. Flip chip and bumping technology is well known to those skilled in the art, and background details regarding this technology may be obtained from a web page entitled "Flip-Chip Assembly" (currently publicly accessible at URL http://www.siliconfareast.com/flipchipassy.htm).

**[0049]** Reference will now be made to FIG. 10 which illustrates an alternative example in which wire bonding is employed between a package PCB 1030 and the master flash device. Although not shown in FIG. 10, electrical paths formed by wires 1040 extending between the master flash chip and the package PCB 1030 also extend through the package PCB 1030 and package balls 1050. Furthermore, as BGA package technology is a very well known technology which has been the subject of many extensive writings, it will be understood that further specific implementation details need not be herein provided, as they should be readily apparent to one skilled in the art.

**[0050]** FIG. 11 is a block diagram of a NAND flash chip floor plan 1100 in accordance with an alternative example embodiment. In the illustrated floor plan 1100, a TSV area 1104 is located between memory core areas 1105 and a peripheral circuit area 1134. Also, it will be understood that areas 1108-1111, 1120, 1130, 1132, 1134, 1140, 1142, 1150 and 1152 shown in FIG. 11 are similar to the areas 408-411, 420, 430, 432, 434, 440, 442, 450 and 452 respectively that were shown in the previously described floor plan 400 of FIG. 4. Thus, the primary difference between the floor plan 1100 and floor plan 400 of FIG. 4 is the placement of the TSV area within the chip floor plan. In accordance with at least some examples, the illustrated floor plan 1100 corresponds to the floor plan of a master memory device of a system, as contrasted to a slave device. Additionally, the core areas 1105 are, in some examples, characterized by smaller sized features as compared to features within the remaining (non-core) areas. In this regard, the process technology may, for instance, be more miniaturized.

**[0051]** Reference will now be made to FIG. 12. FIG. 12 is a block diagram of a NAND flash chip floor plan 1200 for a slave memory device in accordance with an alternative example embodiment. The device architecture of the illustrated example slave device includes a TSV area 1204 along a length-wise edge of the floor plan 1200

and adjacent page buffer and column decoder areas 1240 and 1242. Also, it will be understood that areas 1208-1211, 1240, 1242, 1250 and 1252 shown in FIG. 12 are similar to the areas 508-511, 540, 542, 550 and 552 respectively that were shown in the previously described floor plan 500 of FIG. 5. Thus, the primary difference between the floor plan 1200 and floor plan 500 of FIG. 5 is the placement of the TSV area within the chip floor plan.

**[0052]** Thus from a comparison of FIGS. 11 and 12 with FIGS. 4 and 5, it will be seen that the placement of the TSV area within a chip floor plan will vary (any suitable location is contemplated). For instance, in another alternative example embodiment the TSV area extends along a width-wise edge (instead of length-wise edge) of the chip floor plan. Also, it will be understood that the TSV area may extend along only a portion of (as opposed to entirely along) the length or width of the chip floor plan. In yet another alternative example embodiment, the TSV area is not proximate any of the chip floor plan edges, and could be, for example, centrally positioned between two opposing edges of the chip floor plan. In yet another alternative example embodiment, the TSV area is at least substantially interposed between two core areas of the chip floor plan. Also, in some example embodiments there may be a plurality of TSV areas within one chip floor plan. Thus, it is contemplated that the TSV area or areas may be positioned anywhere within the chip floor plan that one skilled in the art would understand to be suitable.

**[0053]** It will be understood that master and slave devices in accordance with various alternative example embodiments (including those example embodiments illustrated in FIGS. 11 and 12) may be stacked and packaged in a manner similar to the examples of FIGS. 7-10 previously shown and described.

**[0054]** In some example embodiments, the slave memory device may optionally include slave device test logic for facilitating the enhancement of the assembly yield. In this regard, reference is made to FIG. 13. The illustrated block diagram is similar to the block diagram of FIG. 5, but floor plan 1300 includes an additional area 1310 for slave device test logic that is configured to be driven by the master device during testing. The illustrated area 1310 is adjacent the TSV area 504; however placement of the area for

slave device test logic in a variety of suitable alternative locations within any given chip floor plan is contemplated.

**[0055]** Having described master and slave chips, it will be apparent that the master and slave chips should be suitably compatible with each other so that non-core circuitries in the master chip are able to provide functionality for shared benefit of both the master and slave chips.

**[0056]** It will be understood that some example embodiments can be applied to any suitable non-volatile memory integrated circuit system, including those that might be characterized as, for example, NAND Flash, EEPROM, NOR Flash, EEPROM, AND Flash EEPROM, DiNOR Flash EEPROM, Serial Flash EEPROM, ROM, EPROM, FRAM, MRAM and PCRAM.

**[0057]** It will be understood that when an element is herein referred to as being "connected" or "coupled" to another element, it can be directly connected or coupled to the other element or intervening elements may be present. In contrast, when an element is herein referred to as being "directly connected" or "directly coupled" to another element, there are no intervening elements present. Other words used to describe the relationship between elements should be interpreted in a like fashion (i.e., "between" versus "directly between", "adjacent" versus "directly adjacent", "extend through" versus "extend entirely through", etc.).

**[0058]** Certain adaptations and modifications of the described embodiments can be made. Therefore, the above discussed embodiments are considered to be illustrative and not restrictive.

# CLAIMS

What is claimed is:

1. A system comprising:

a stack including:

a first non-volatile memory chip; and

a second non-volatile memory chip, the second non-volatile memory chip lacking in at least some non-core circuitries to facilitate chip size reduction; and

a plurality of electrical paths extending between the first non-volatile memory chip and the second non-volatile memory chip, the electrical paths facilitating the first non-volatile memory chip in providing the second non-volatile memory chip with signals and voltages needed for device operations.

2. The system as claimed in claim 1 further comprising at least one additional non-volatile memory chip, the first non-volatile memory chip being a master device, and the second and additional memory chips being slave devices.

3. The system as claimed in claim 1 or 2 wherein the electrical paths comprise Through-Silicon Vias.

4. The system as claimed in claim 3 further comprising a package printed circuit board, the stack connected to the package printed circuit board by flip chip and bumping.

5. The system as claimed in claim 1 wherein only the first non-volatile memory chip includes a high voltage generator.

6. The system as claimed in claim 1 or 5 wherein the voltages include high voltages for program and erase operations.

7. The system as claimed in any one of claims 1, 2 and 5 wherein the second non-volatile memory chip includes slave device test logic that is configured to be driven by the first non-volatile memory chip during testing.

8. The system as claimed in any one of claims 1, 2 and 5 wherein the first non-volatile memory chip and the second non-volatile memory chip are NAND flash memory chips.

9. A method comprising manufacturing first and second non-volatile memory chips that are compatible with each other, the first and second non-volatile memory chips having substantially similar core chip areas, but only the first non-volatile memory chip having a number of additional chip areas within which are located circuitries providing functionality for shared of benefit of both the first and second non-volatile memory chips, and the circuitries of the additional chip areas configured to generate signals and voltages needed for device operations in relation to both the first and second non-volatile memory chips.

10. The method as claimed in claim 9 wherein the core chip areas have a more miniaturized process technology as compared to the additional chip areas.

11. The method as claimed in claim 10 wherein the additional chip areas include a peripheral circuit area, an input and output pads area, and at least one high voltage generator area.

12. The method as claimed in any one of claims 9, 10 and 11 wherein the first and second non-volatile memory chips are NAND flash memory chips.

13. The method as claimed in any one of claims 9, 10 and 11 wherein the manufacturing includes the manufacture of at least one additional non-volatile memory

chip, the first non-volatile memory chip being a master device, and the second and additional memory chips being slave devices.

14. The method as claimed in any one of claims 9, 10 and 11 wherein the second non-volatile memory chip includes slave device test logic that is configured to be driven by the first non-volatile memory chip during testing.

15. The method as claimed in any one of claims 9, 10 and 11 wherein only the first non-volatile memory chip includes a high voltage generator.

16. A method comprising:

stacking at least two semiconductor chips, one of the semiconductor chips being a master memory device and another of the semiconductor chips being a slave memory device;

wiring the stacked semiconductor chips together by Through-Silicon Vias; and

connecting the stacked semiconductor chips to a package printed circuit board by flip chip and bumping.

17. The method as claimed in claim 16 wherein the master and slave memory devices are flash memory devices.

18. The method as claimed in claim 16 or 17 wherein the master memory device is substantially larger dimensioned than the slave memory device, and during the connecting the master memory device is positioned substantially adjacent the package printed circuit board.

19. A non-volatile memory chip comprising:

core chip areas that take up more than eighty percent of an entire chip area of the non-volatile memory chip; and

an additional chip area within which are located circuitries configured to receive signals and voltages from another non-volatile memory chip, the core chip areas having a more miniaturized process technology as compared to the additional chip area.

20. The non-volatile memory chip as claimed in claim 19 wherein the additional chip area is a Through-Silicon Vias area.

21. The non-volatile memory chip as claimed in claim 19 wherein the non-volatile memory chip lacks a high voltage generator.

22. The non-volatile memory chip as claimed in any one of claims 19 to 21 further comprising another additional chip area within which is located slave device test logic that is configured to be driven by a separate device during testing.

23. The non-volatile memory chip as claimed in claim 22 wherein the another additional chip area is located directly adjacent the additional chip area.

24. The non-volatile memory chip as claimed in any one of claims 19 to 21 wherein NAND flash memory cells are located within some of the core chip areas.

25. The non-volatile memory chip as claimed in any one of claims 19 to 21 wherein the core chip areas take up more than ninety percent of the entire chip area of the non-volatile memory chip.

26. A system comprising:

a stack including:

a first chip, a first chip area of the first chip having more miniaturized process technology as compared to a second chip area of the first chip; and

a second chip, a first chip area of the second chip having more miniaturized process technology as compared to a second chip area of the second chip,

and the second chip area of the second chip as a percentage of total chip area of the second chip is much smaller than the second chip area of the first chip as a percentage of total chip area of the first chip.

27. The system as claimed in claim 26 wherein the first and second chips are memory chips and at least the second chip is a non-volatile memory chip.

28. The system as claimed in claim 26 or 27 further comprising a plurality of electrical paths extending between the first chip and the second chip, the electrical paths facilitating the first chip in providing the second chip with signals and voltages needed for device operations.

29. The system as claimed in claim 28 wherein the electrical paths comprise Through-Silicon Vias.

30. The system as claimed in claim 26 or 27 wherein only the first chip includes a high voltage generator.

31. The system as claimed in claim 26 or 27 further comprising a package printed circuit board, the stack connected to the package printed circuit board by flip chip and bumping.

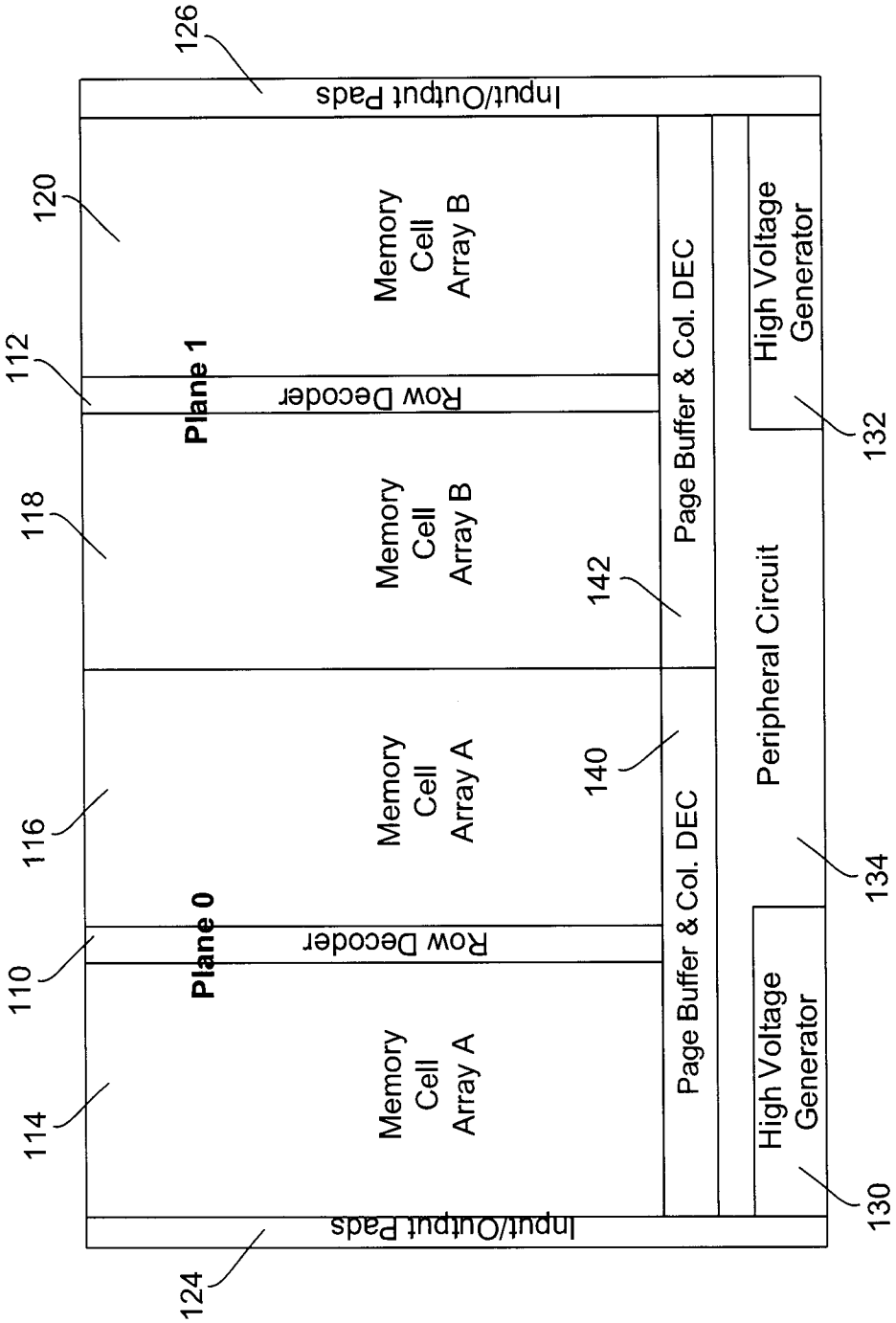
126
Input/Output Pads
120
Memory Cell Array B
112
Plane 1
Row Decoder
118
Memory Cell Array B
142
Page Buffer & Col. DEC
High Voltage Generator
132
116
Memory Cell Array A
140
Page Buffer & Col. DEC
Peripheral Circuit
134
110
Plane 0
Row Decoder
114
Memory Cell Array A
High Voltage Generator
130
Input/Output Pads
124
100

FIG. 1

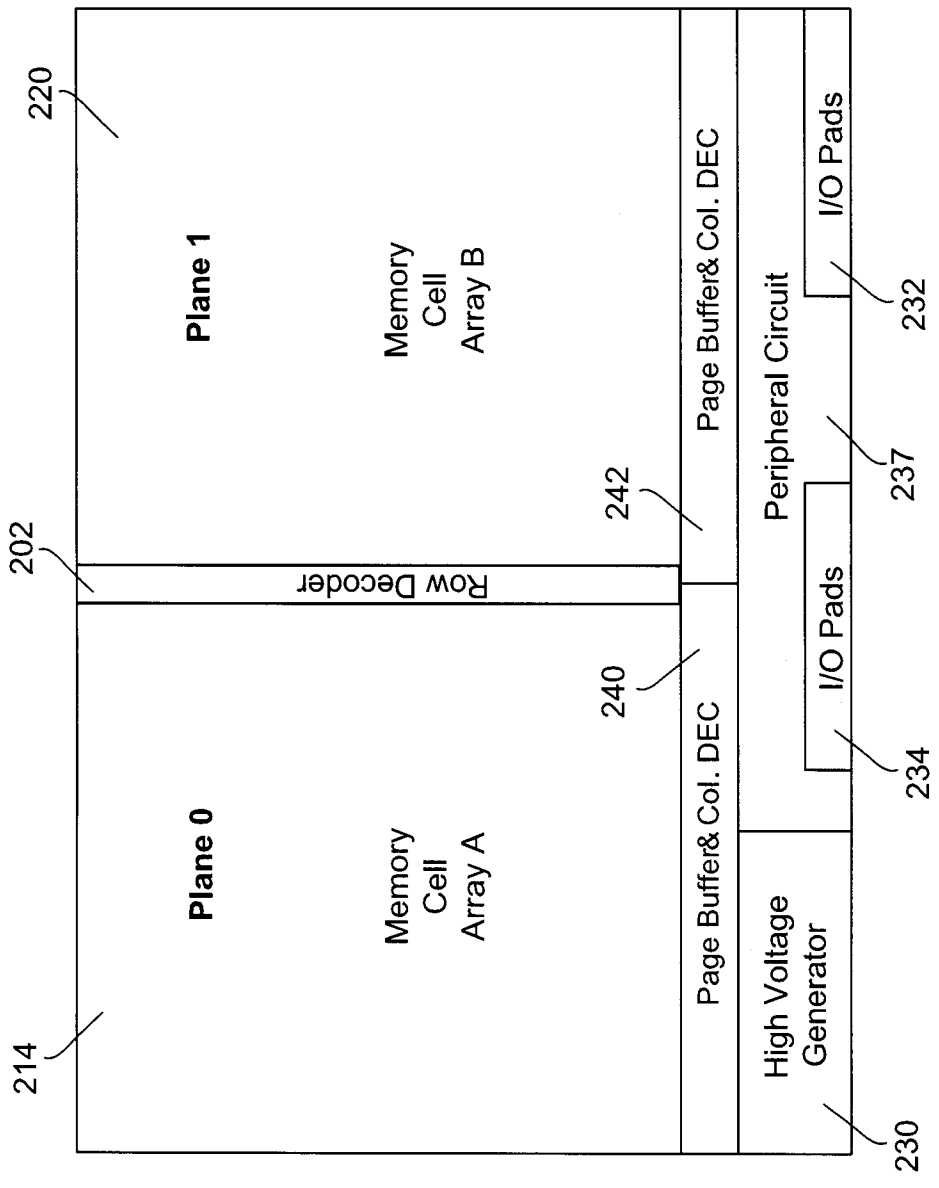
220
Plane 1
Memory Cell Array B
Page Buffer& Col. DEC
I/O Pads
232
242
237
202
Row Decoder
Peripheral Circuit
240
I/O Pads
234
Plane 0
Memory Cell Array A
Page Buffer& Col. DEC
High Voltage Generator
214
230
200

FIG. 2

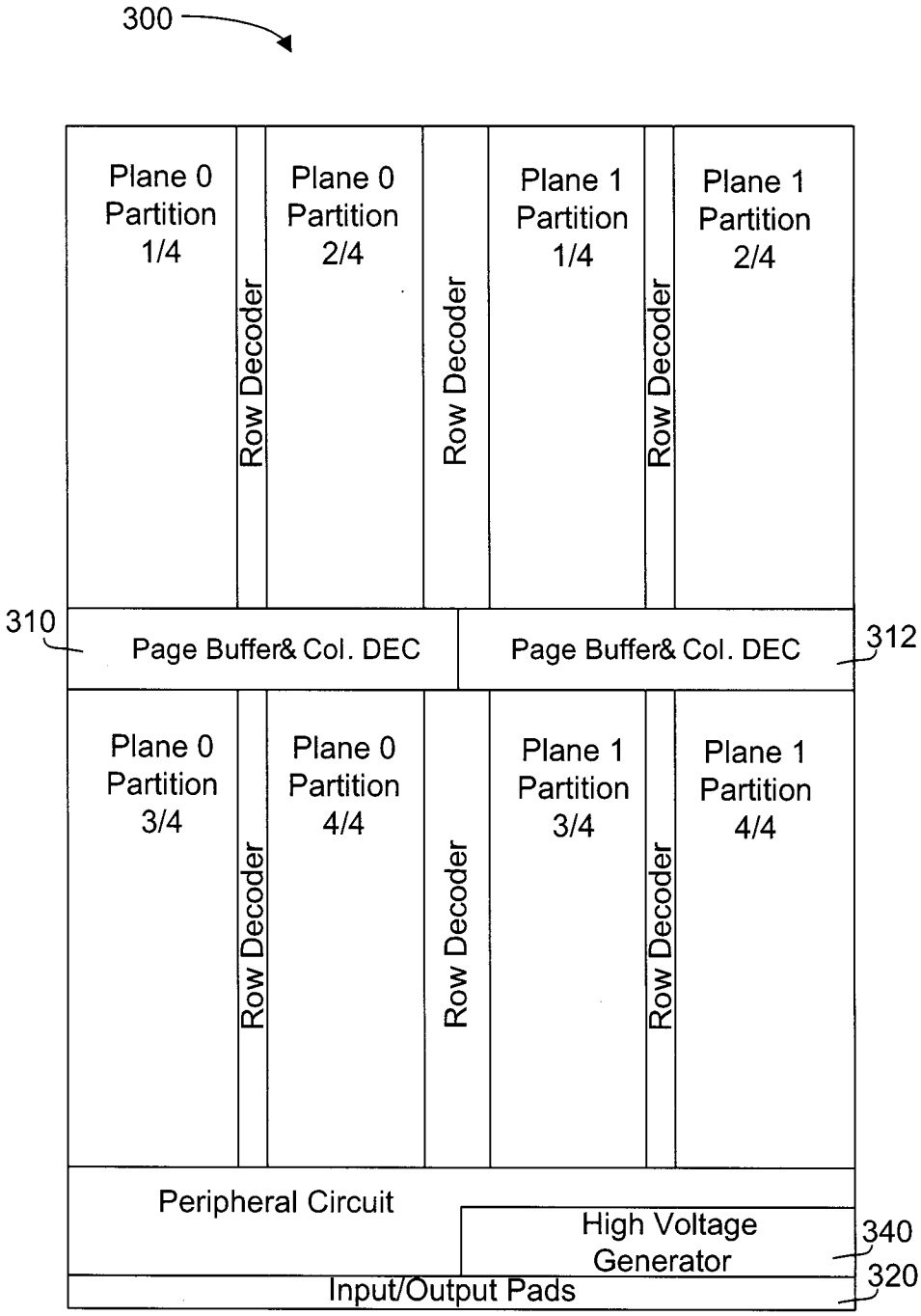
300
Plane 0 Partition 1/4
Row Decoder
Plane 0 Partition 2/4
Row Decoder
Plane 1 Partition 1/4
Row Decoder
Plane 1 Partition 2/4
310
Page Buffer& Col. DEC
Page Buffer& Col. DEC
312
Plane 0 Partition 3/4
Row Decoder
Plane 0 Partition 4/4
Row Decoder
Plane 1 Partition 3/4
Row Decoder
Plane 1 Partition 4/4
Peripheral Circuit
High Voltage Generator
340
Input/Output Pads
320

FIG. 3

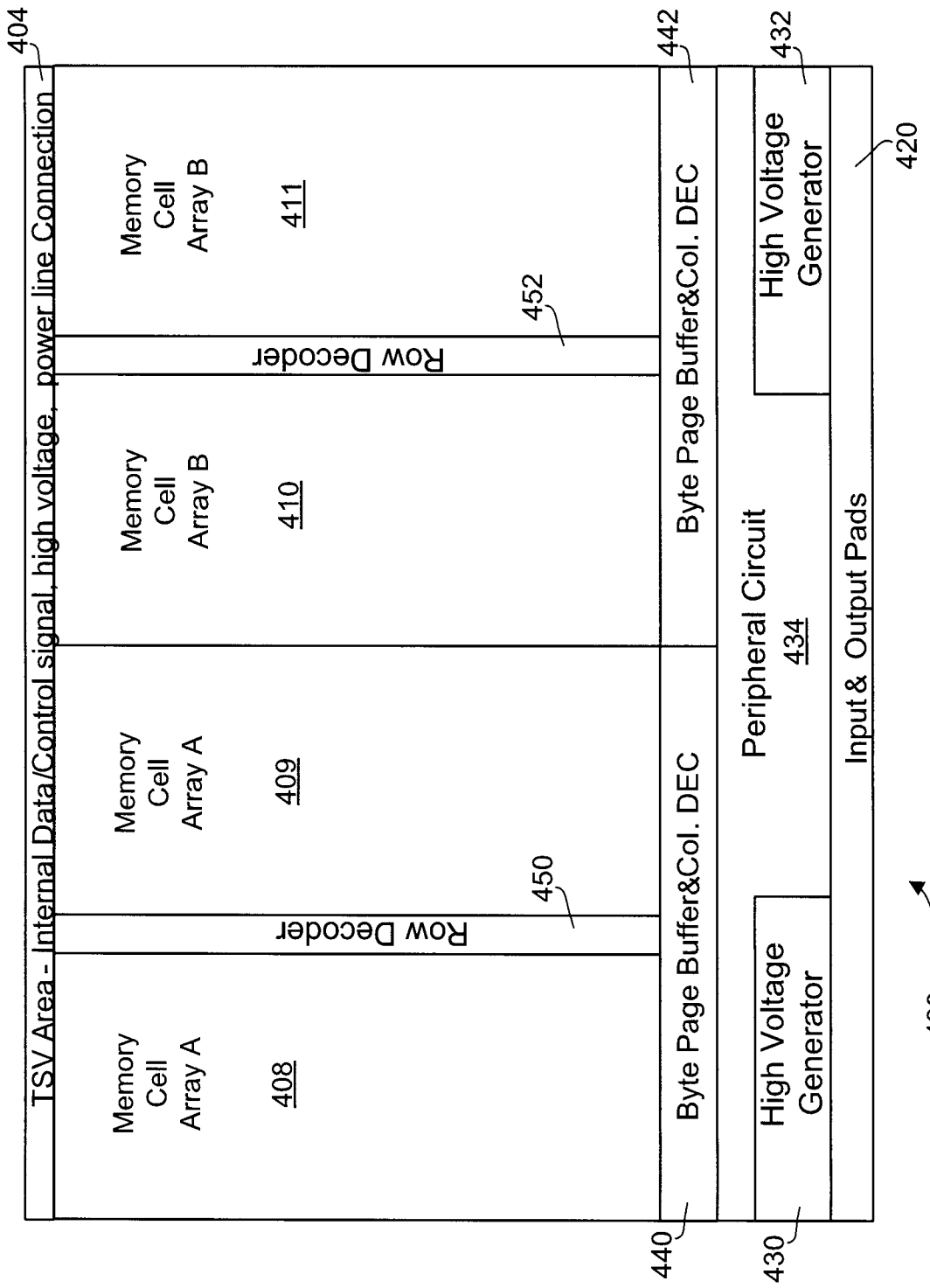
404
TSV Area - Internal Data/Control signal, high voltage, power line Connection
Memory Cell Array A
408
Row Decoder
450
Memory Cell Array A
409
Memory Cell Array B
410
Row Decoder
452
Memory Cell Array B
411
442
Byte Page Buffer&Col. DEC
Byte Page Buffer&Col. DEC
440
Peripheral Circuit
434
High Voltage Generator
High Voltage Generator
430
432
Input & Output Pads
420
400

FIG. 4

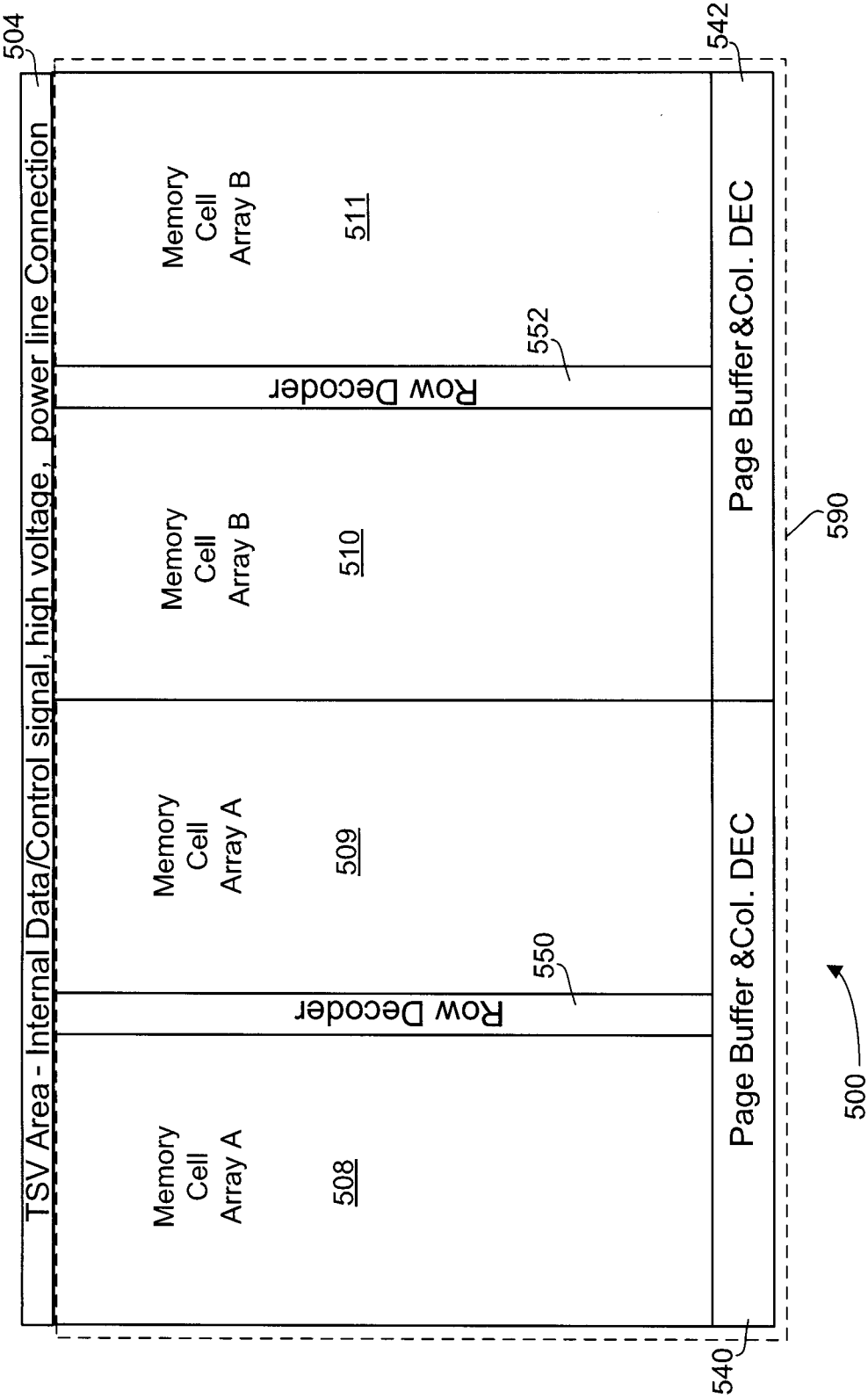
504
542
TSV Area - Internal Data/Control signal, high voltage, power line Connection
Memory Cell Array B
511
552
Row Decoder
Memory Cell Array B
510
Page Buffer&Col. DEC
590
Memory Cell Array A
509
550
Row Decoder
Memory Cell Array A
508
Page Buffer &Col. DEC
500
540

FIG. 5

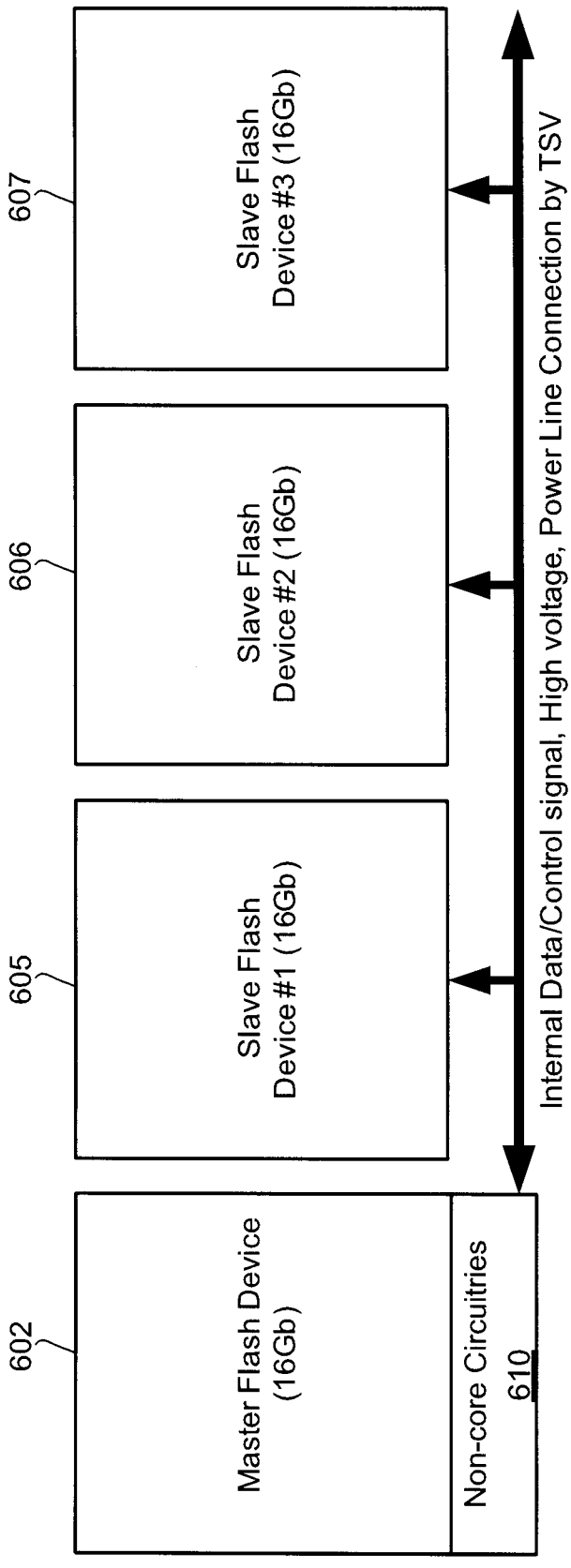
607
Slave Flash
Device #3 (16Gb)
606
Slave Flash
Device #2 (16Gb)
605
Slave Flash
Device #1 (16Gb)
602
Master Flash Device
(16Gb)
Non-core Circuitries
610
Internal Data/Control signal, High voltage, Power Line Connection by TSV
600

FIG. 6

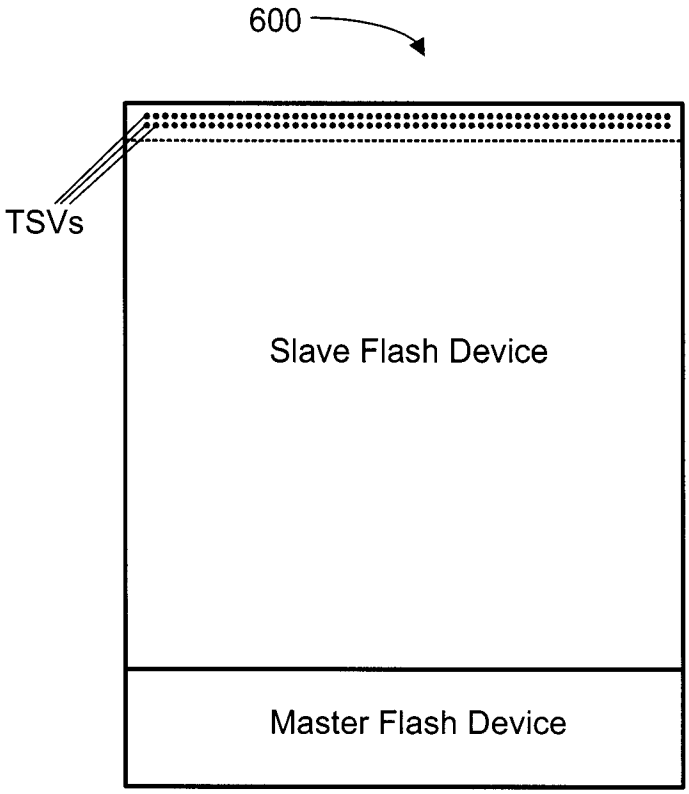
600
TSVs
Slave Flash Device
Master Flash Device

FIG. 7

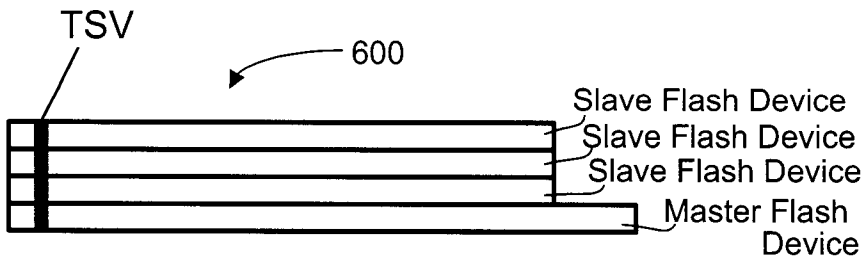
TSV
600
Slave Flash Device
Slave Flash Device
Slave Flash Device
Master Flash Device

FIG. 8

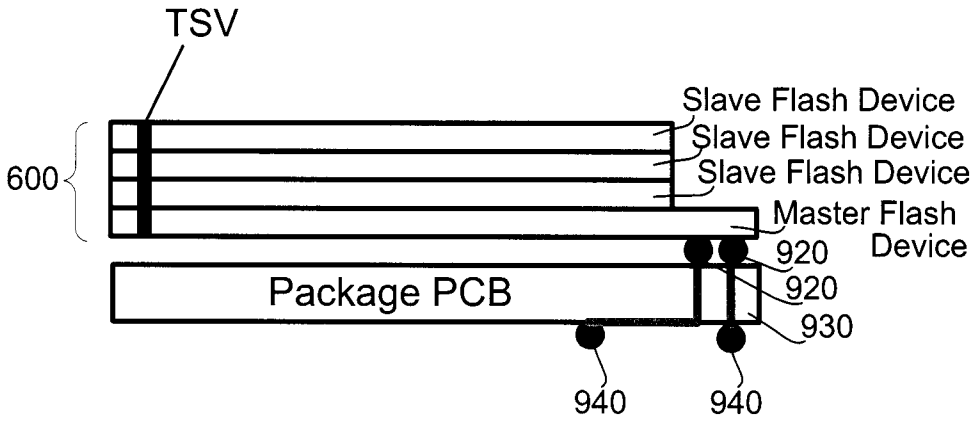
TSV
Slave Flash Device
Slave Flash Device
Slave Flash Device
Master Flash Device
600
920
920
930
Package PCB
940
940

FIG. 9

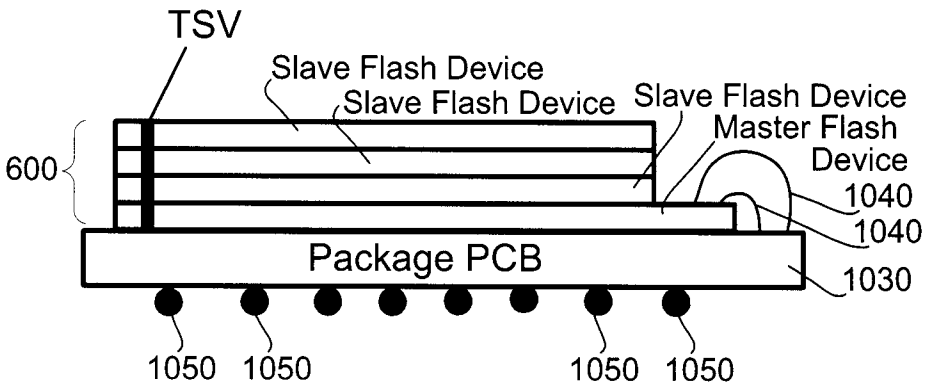
TSV
Slave Flash Device
Slave Flash Device
Slave Flash Device
Master Flash Device
600
1040
1040
Package PCB
1030
1050
1050
1050
1050

FIG. 10

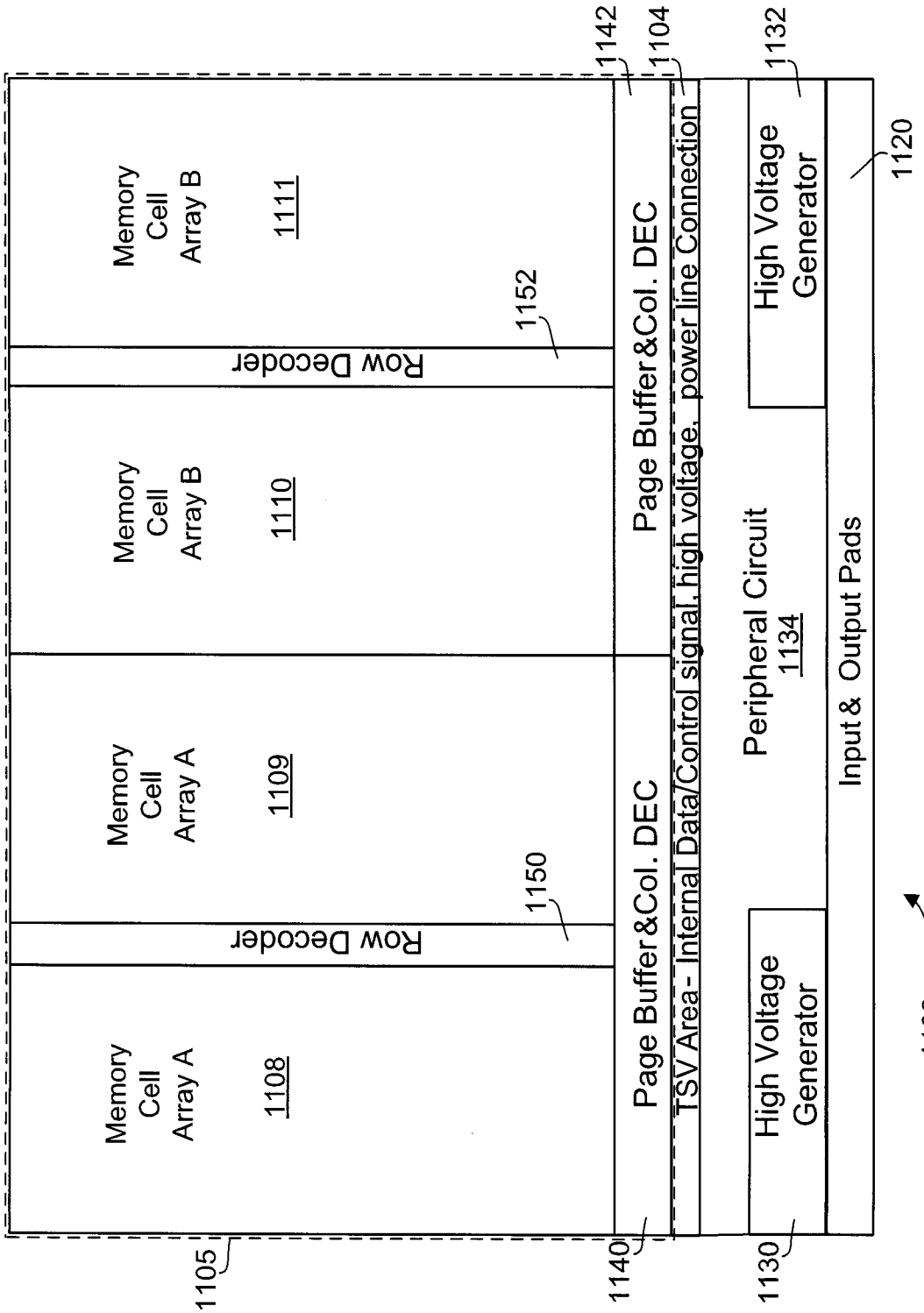
Memory Cell Array A
1108
Memory Cell Array A
1109
Memory Cell Array B
1110
Memory Cell Array B
1111
Row Decoder
Row Decoder
1150
1152
Page Buffer &Col. DEC
Page Buffer &Col. DEC
1140
1142
TSV Area - Internal Data/Control signal, high voltage, power line Connection
1104
Peripheral Circuit
1134
High Voltage Generator
High Voltage Generator
1130
1132
Input & Output Pads
1120
1105
1100

FIG. 11

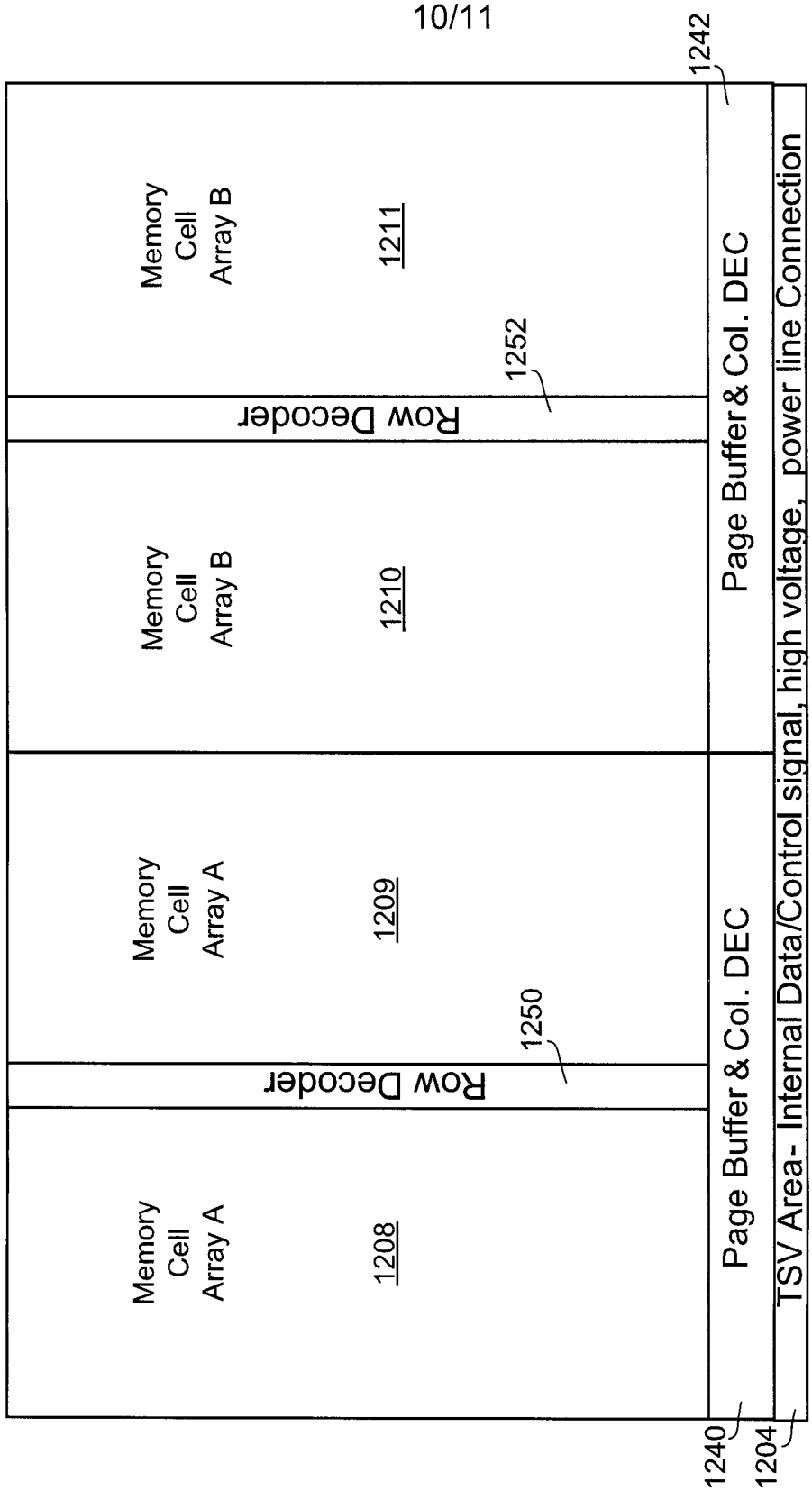
Memory Cell Array A
1208
Row Decoder
1250
Memory Cell Array A
1209
Memory Cell Array B
1210
Row Decoder
1252
Memory Cell Array B
1211
1242
Page Buffer & Col. DEC
Page Buffer & Col. DEC
1240
TSV Area- Internal Data/Control signal, high voltage, power line Connection
1204
1200

FIG. 12

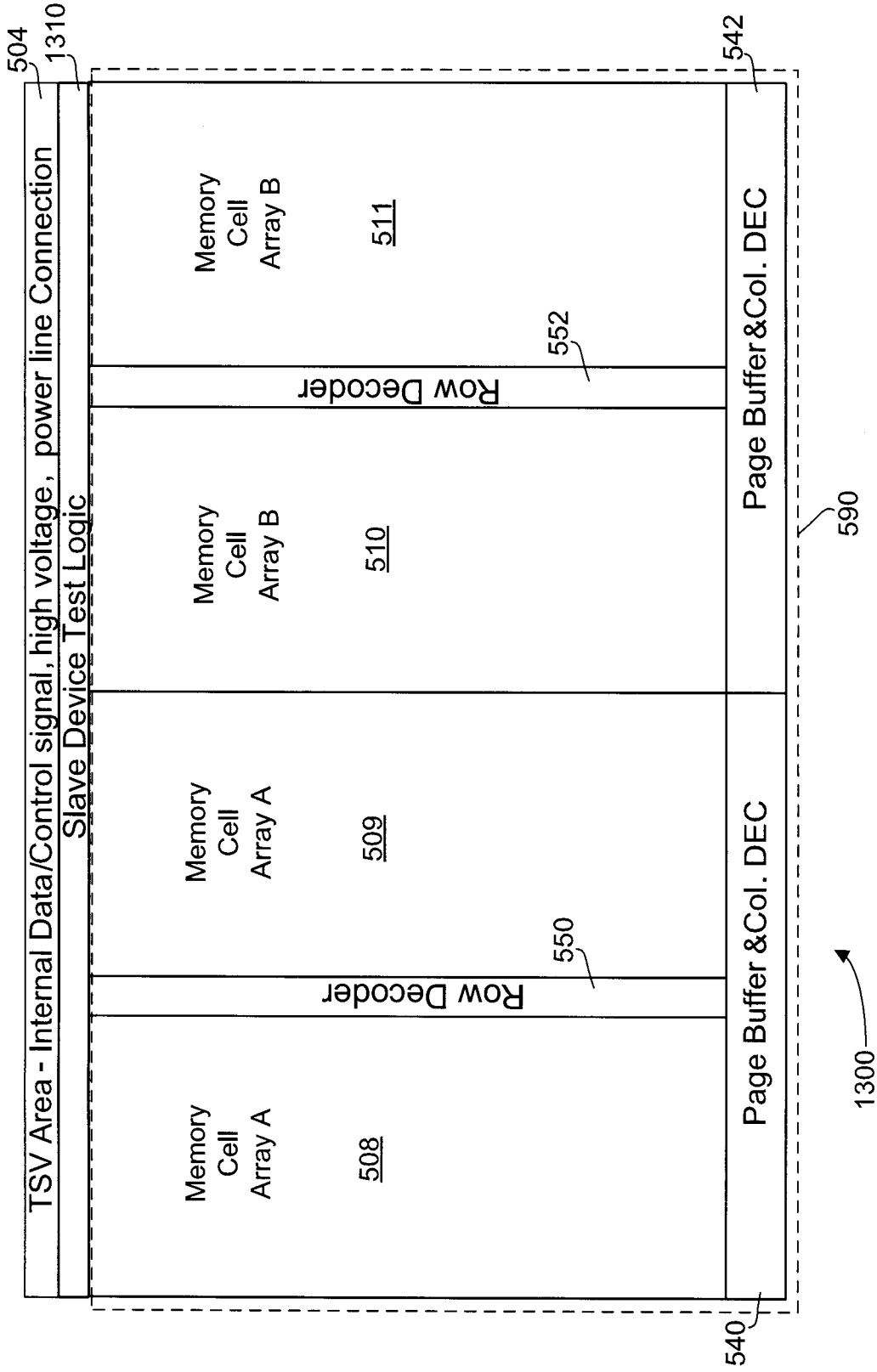
504
1310
542
TSV Area - Internal Data/Control signal, high voltage, power line Connection
Slave Device Test Logic
Memory Cell Array B
511
552
Row Decoder
Memory Cell Array B
510
Page Buffer &Col. DEC
590
Memory Cell Array A
509
550
Row Decoder
Memory Cell Array A
508
Page Buffer &Col. DEC
1300
540

FIG. 13

**INTERNATIONAL SEARCH REPORT**

International application No.
PCT/CA2010/000195

A. CLASSIFICATION OF SUBJECT MATTER
IPC: ***G11C 16/02*** (2006.01) , ***G11C 16/06*** (2006.01) , ***G11C 5/06*** (2006.01)
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC: G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic database(s) consulted during the international search (name of database(s) and, where practicable, search terms used)
Databases: Canadian patent database, EPOQUE, WEST, IEEE Xplore
Search terms used: memory, flash, non-volatile, stack, master, slave, Through-silicon via, size, reduce

C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category* | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| X | US 2009/0040861 A1 (Ruckerbauer)<br>12 February 2009 (12-02-2009)<br>*see figure 6 and paragraphs [0057]-[0060]* | 1-31 |
| X, P | WO 2009/102821 A2 (Karamcheti et al.)<br>20 August 2009 (20-08-2009)<br>*see entire document* | 1-31 |
| A | US 5, 818, 107 (Pierson et al.)<br>6 October 1998 (06-10-1998)<br>*see entire document* | 1-31 |
| A | US 2008/0080261 A1 (Shaeffer et al.)<br>3 April 2008 (03-04-2008)<br>*see entire document* | 1-31 |

[ ] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

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| Date of the actual completion of the international search | Date of mailing of the international search report |
|---|---|
| 16 April 2010 (16-04-2010) | 27 April 2010 (27-04-2010) |

| Name and mailing address of the ISA/CA | Authorized officer |
|---|---|
| Canadian Intellectual Property Office<br>Place du Portage I, C114 - 1st Floor, Box PCT<br>50 Victoria Street<br>Gatineau, Quebec K1A 0C9<br>Facsimile No.: 001-819-953-2476 | Kazem Ziaie (819) 934-2667 |

**INTERNATIONAL SEARCH REPORT**
Information on patent family members

International application No.
PCT/CA2010/000195

| Patent Document Cited in Search Report | Publication Date | Patent Family Member(s) | Publication Date |
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| | | WO2007038225A2 | 05-04-2007 |
| | | WO2007038225A3 | 14-06-2007 |
| | | WO2008124503A1 | 16-10-2008 |