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Chen et al.(10) **Pub. No.: US 2019/0214366 A1**(43) **Pub. Date: Jul. 11, 2019**(54) **STACKED PACKAGE INCLUDING
EXTERIOR CONDUCTIVE ELEMENT AND A
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H01L 21/768	(2006.01)
H01L 21/78	(2006.01)

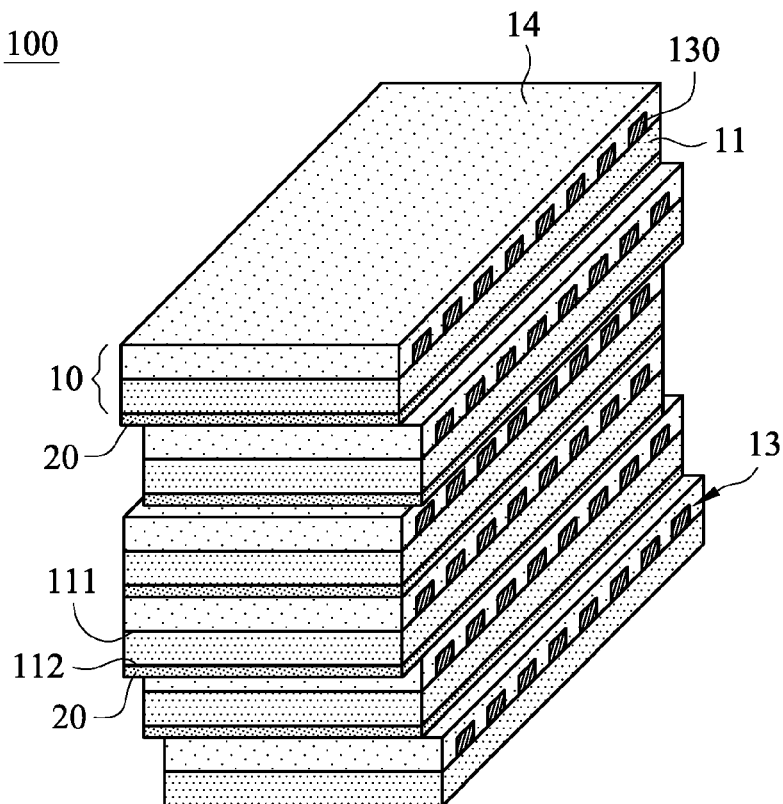
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(57)

ABSTRACT

A stacked package has plurality of chip packages stacked on active surfaces of each other, a dielectric layer, a redistribution layer and a plurality of external terminals. Each chip package has an exterior conductive element formed on the active surface. Each exterior conductive element has a cut edge exposed on at least one of the lateral side of the chip package. The dielectric layer, the redistribution layer and the external terminals are formed in sequence on the lateral side with the exposed cut edges to form the electrical connection between the cut edges, the redistribution layer and the external terminals. Therefore, the process for forming the electrical connections is simplified to enhance the reliability and the UPH for manufacturing the stacked package.



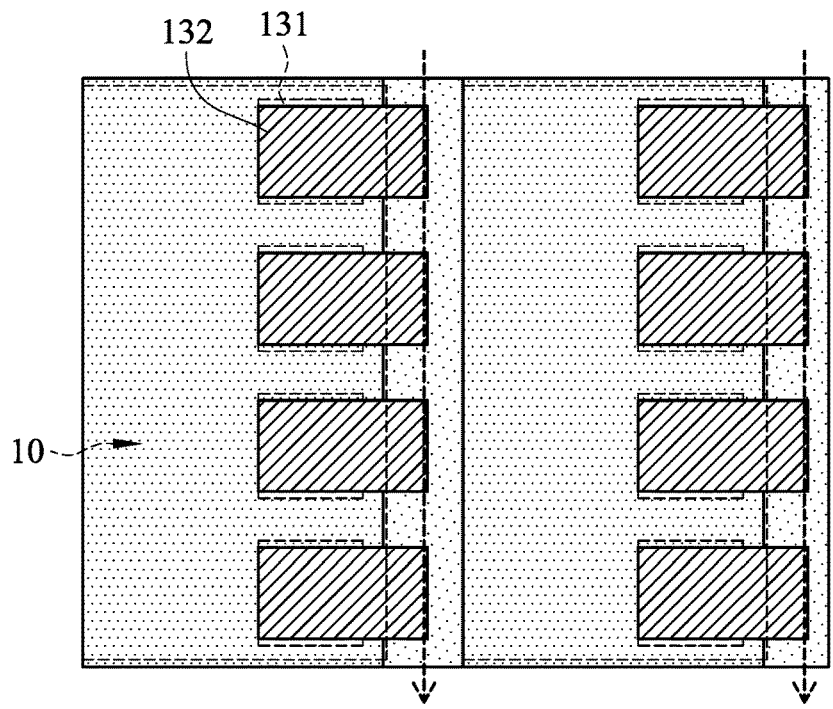


FIG. 1A

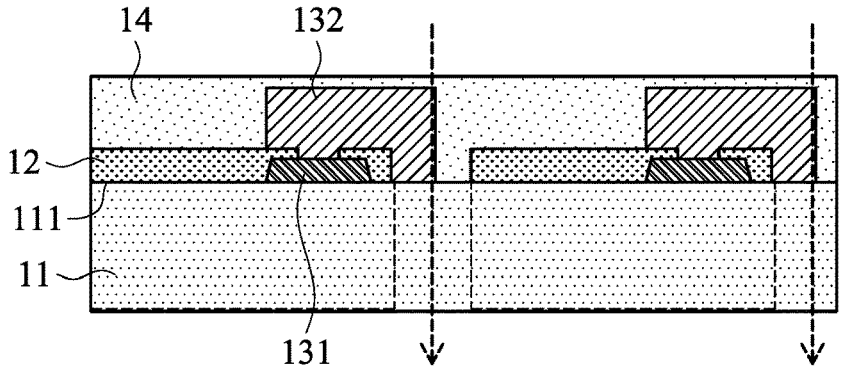


FIG. 1B

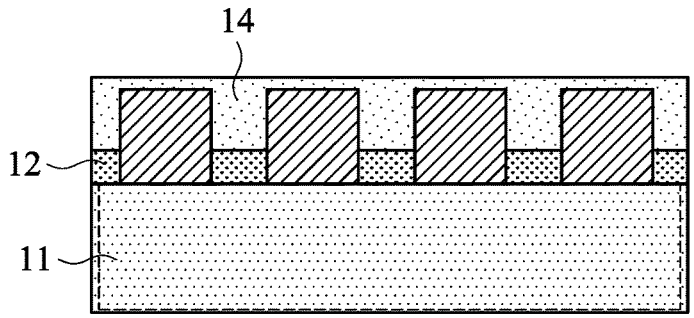


FIG. 1C

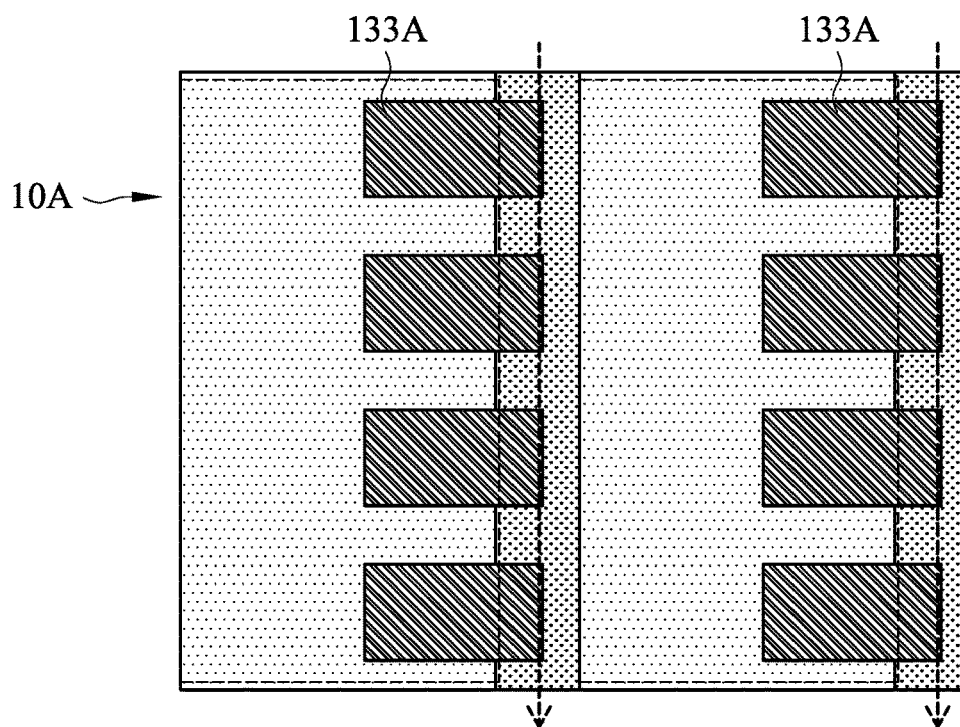


FIG. 2A

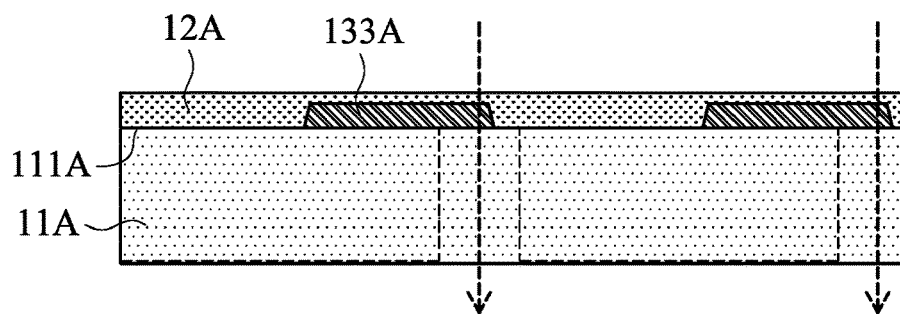


FIG. 2B

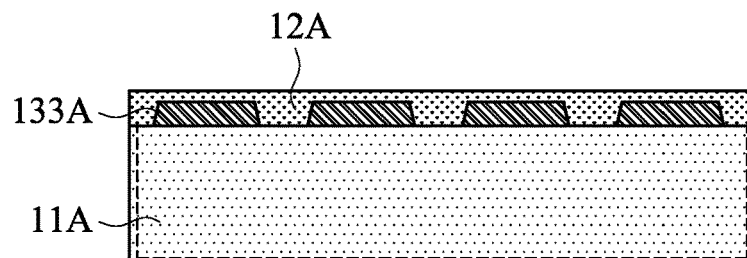


FIG. 2C

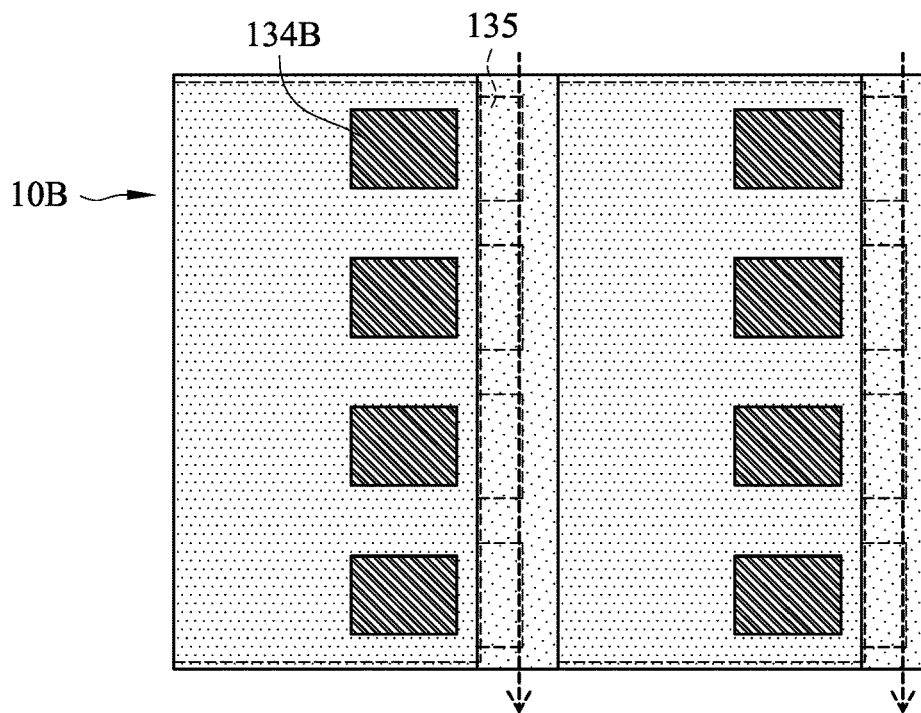


FIG. 3A

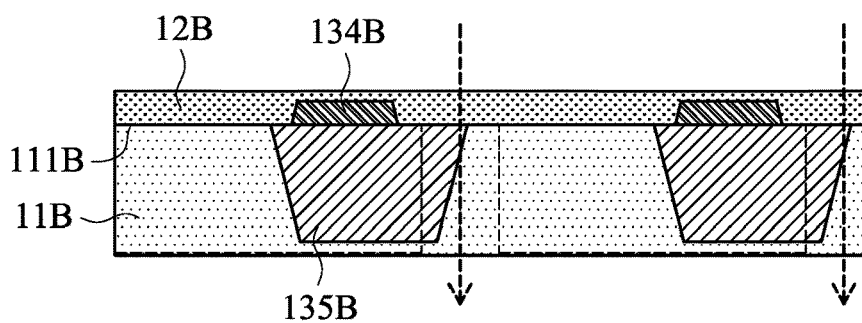


FIG. 3B

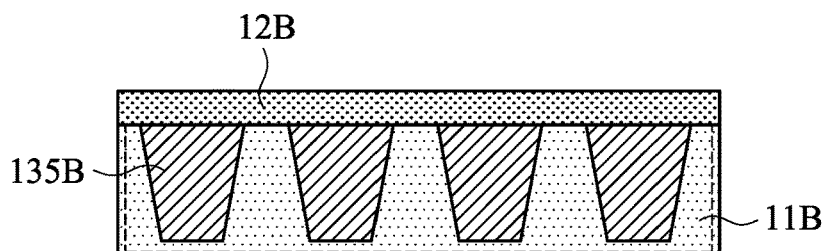


FIG. 3C

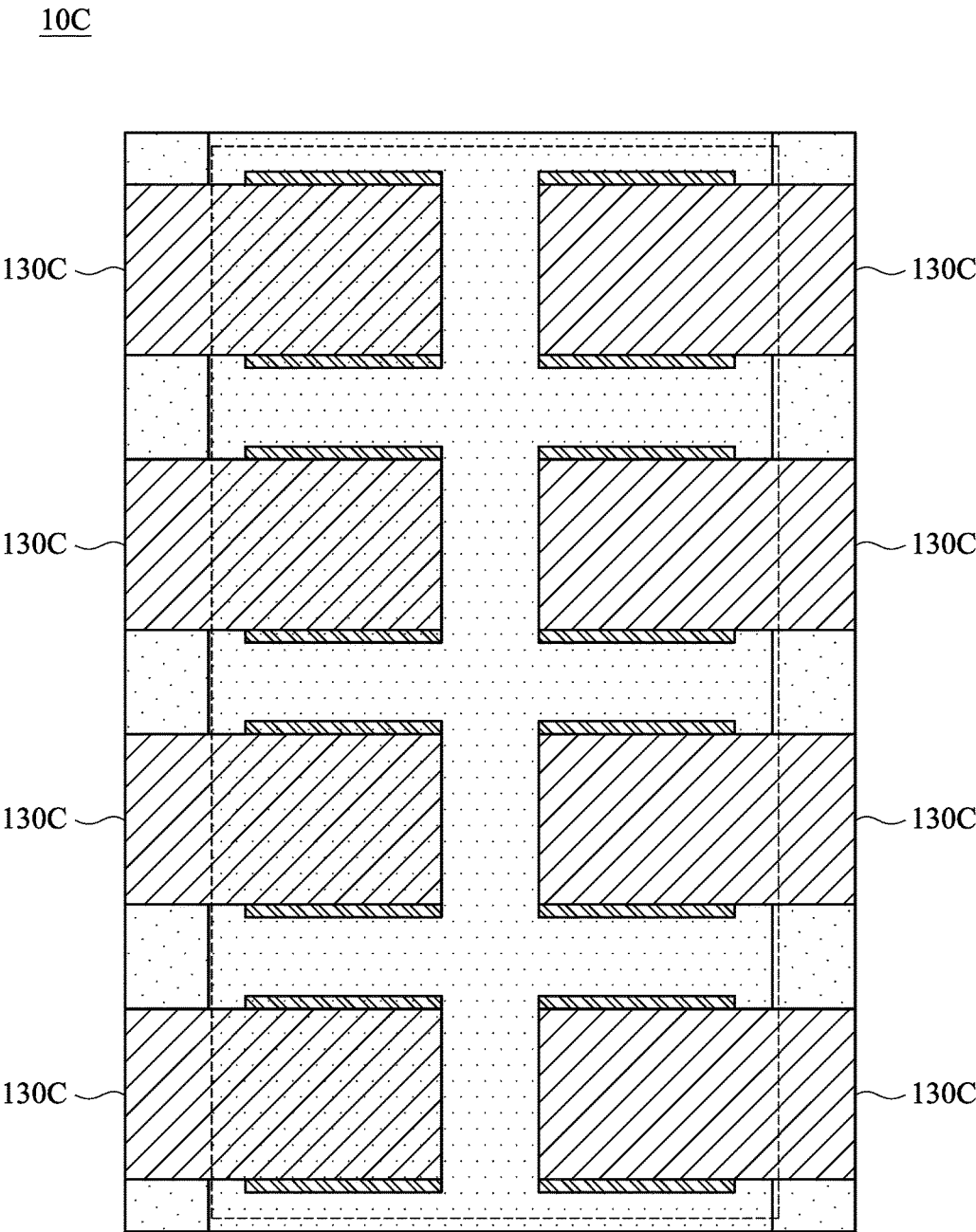


FIG. 4

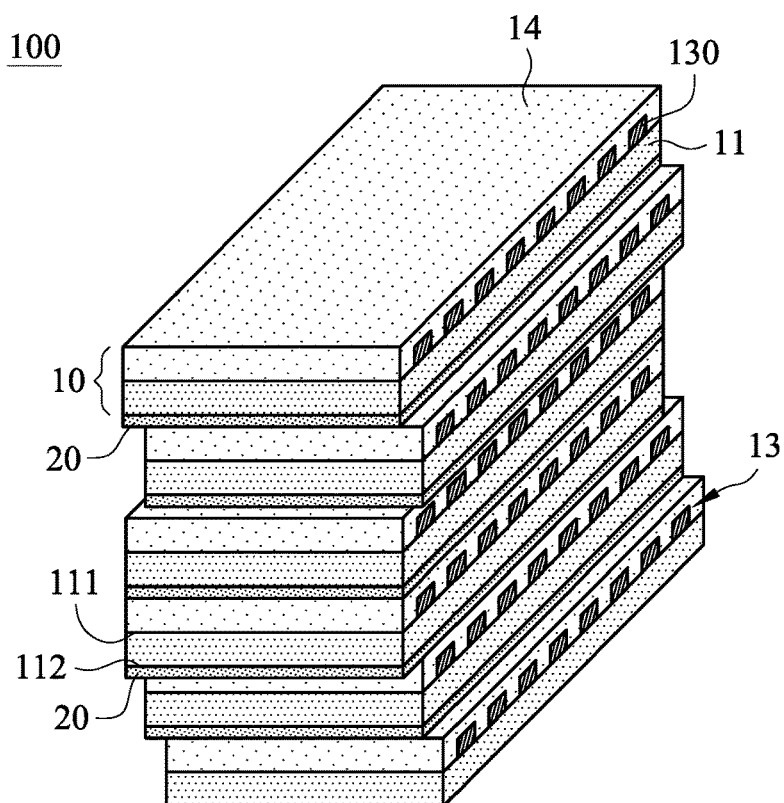


FIG. 5A

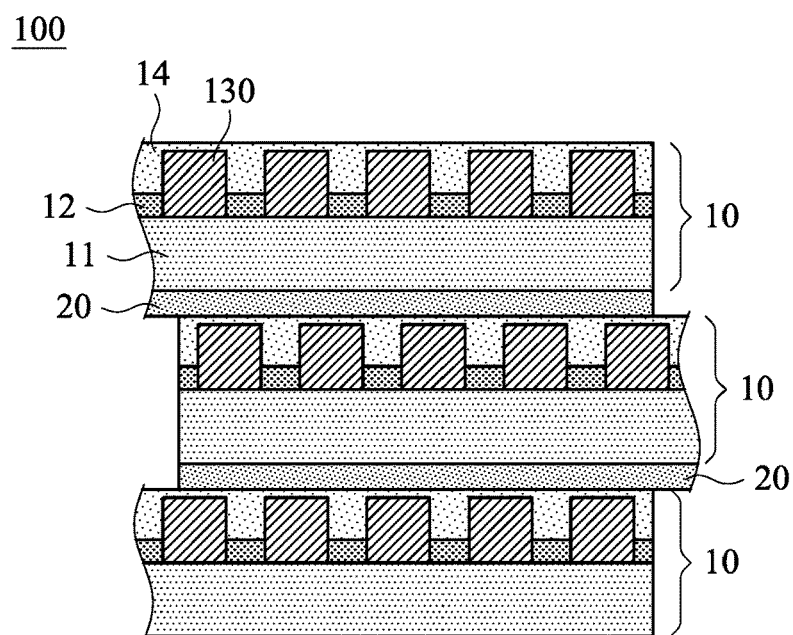


FIG. 5B

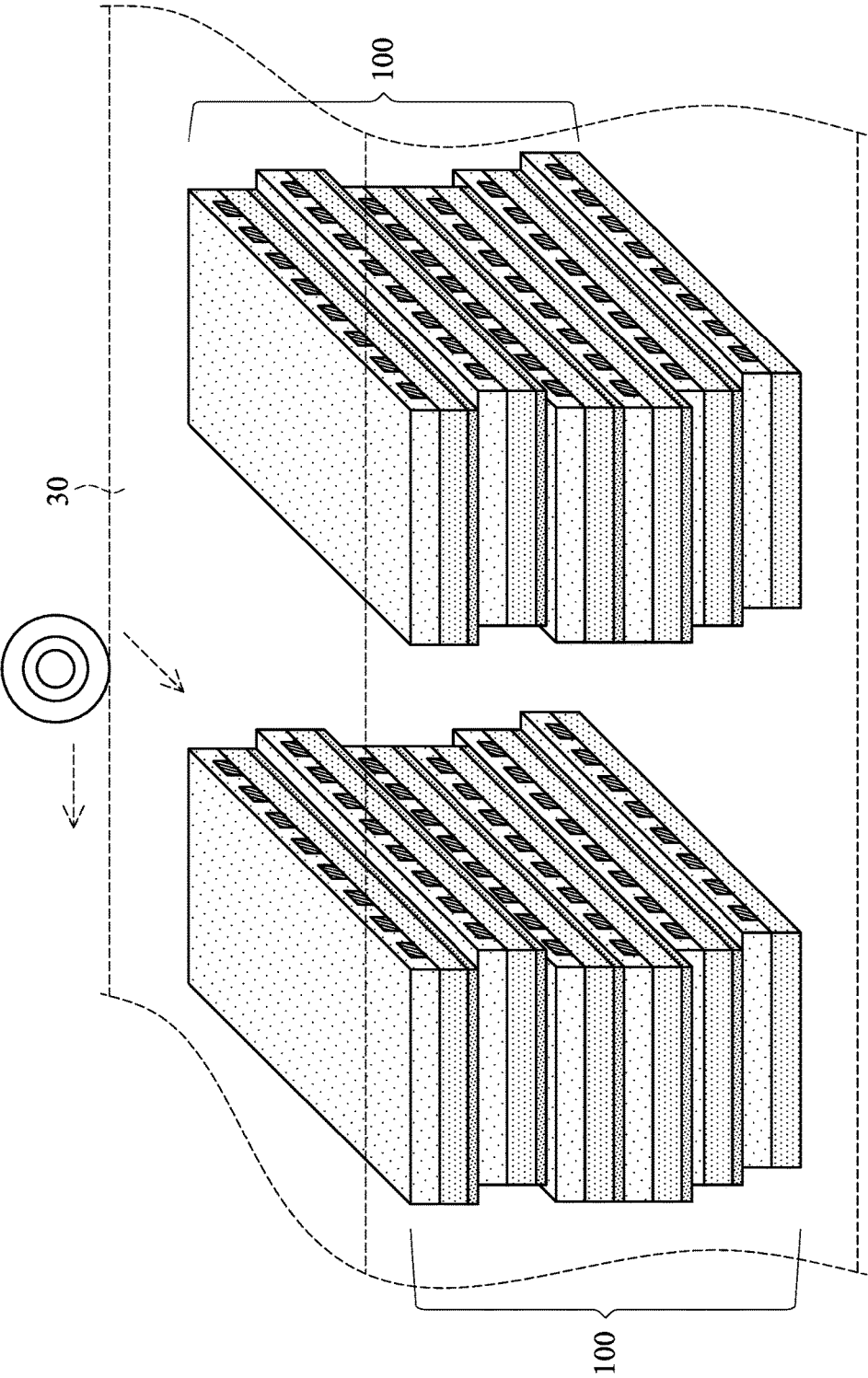


FIG. 6

40

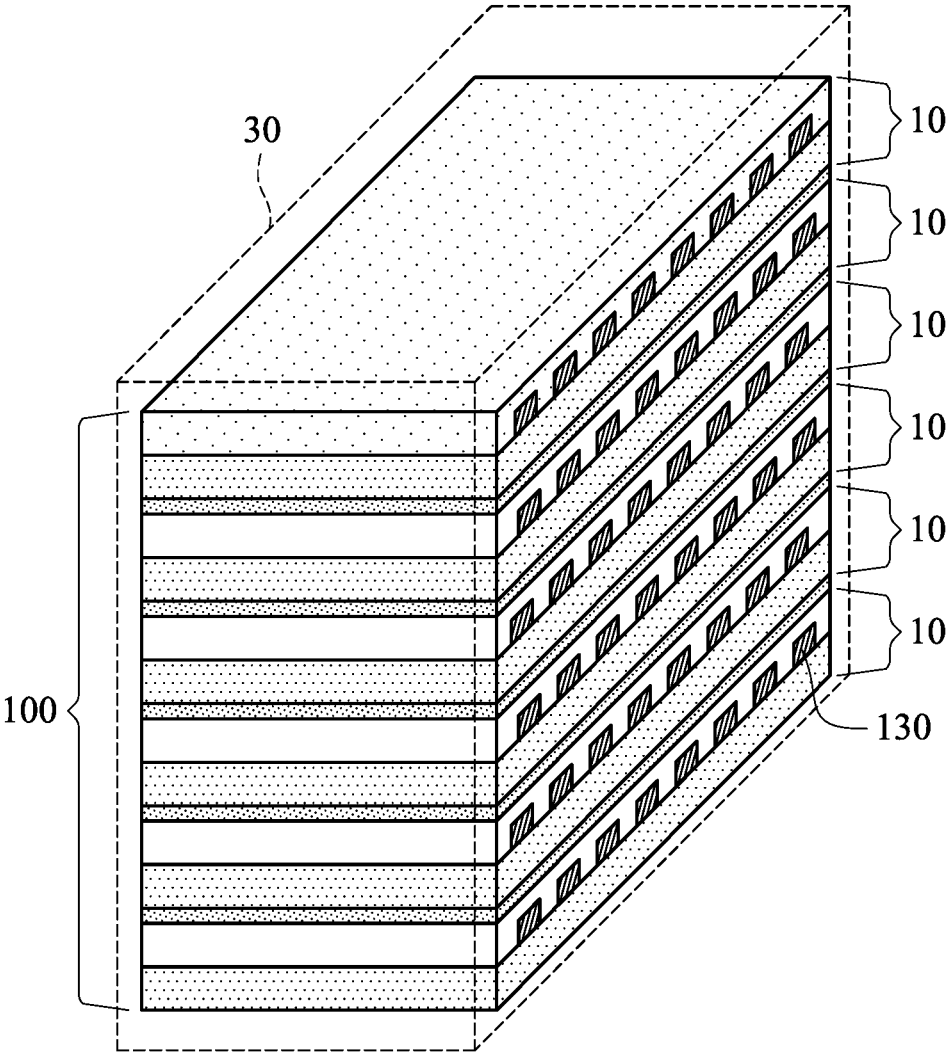


FIG. 7

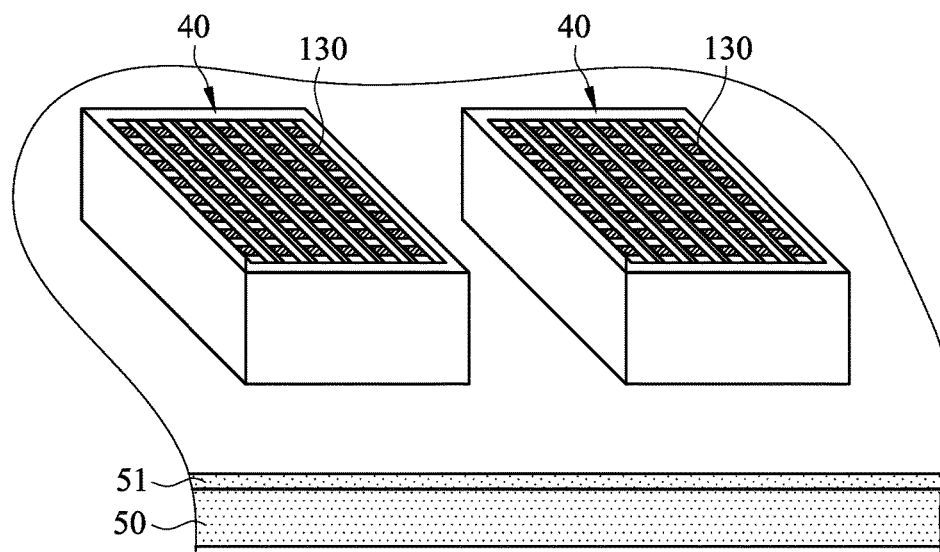


FIG. 8A

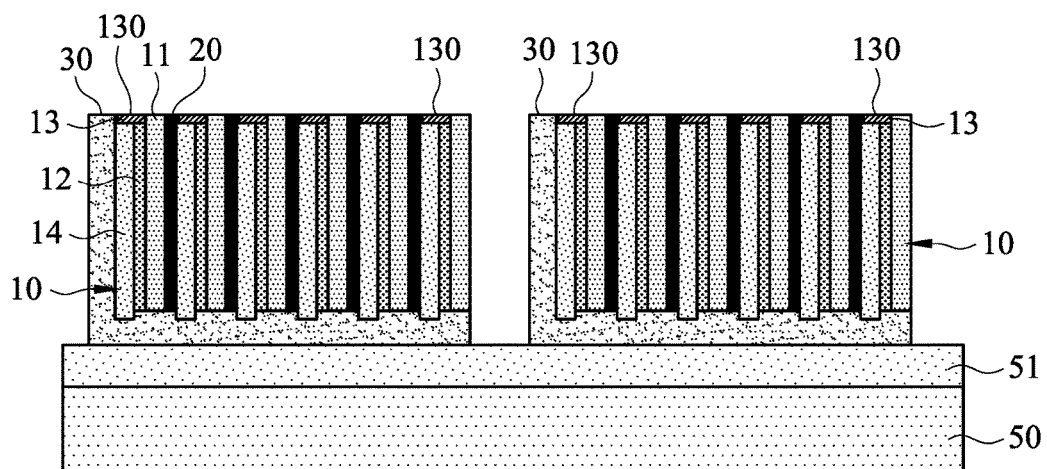


FIG. 8B

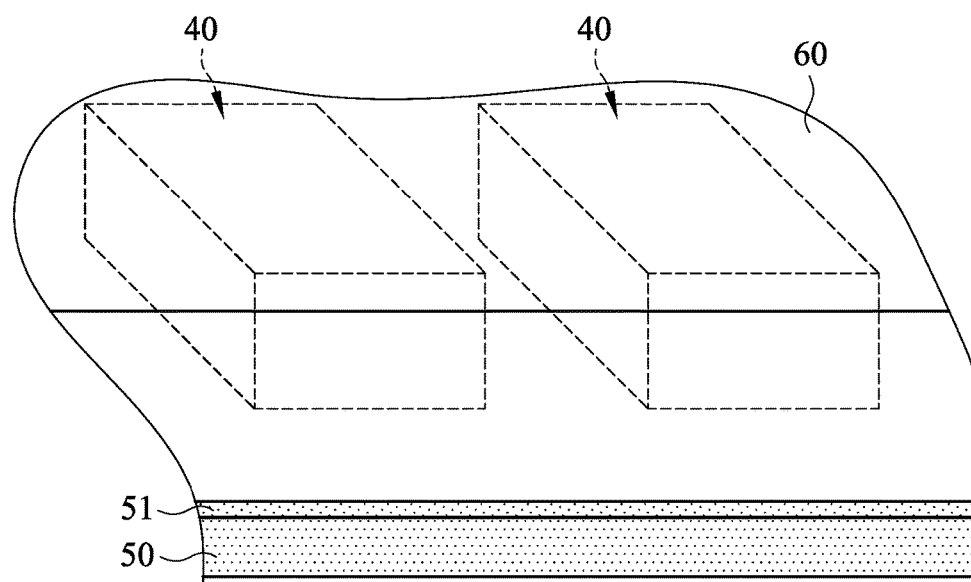


FIG. 9A

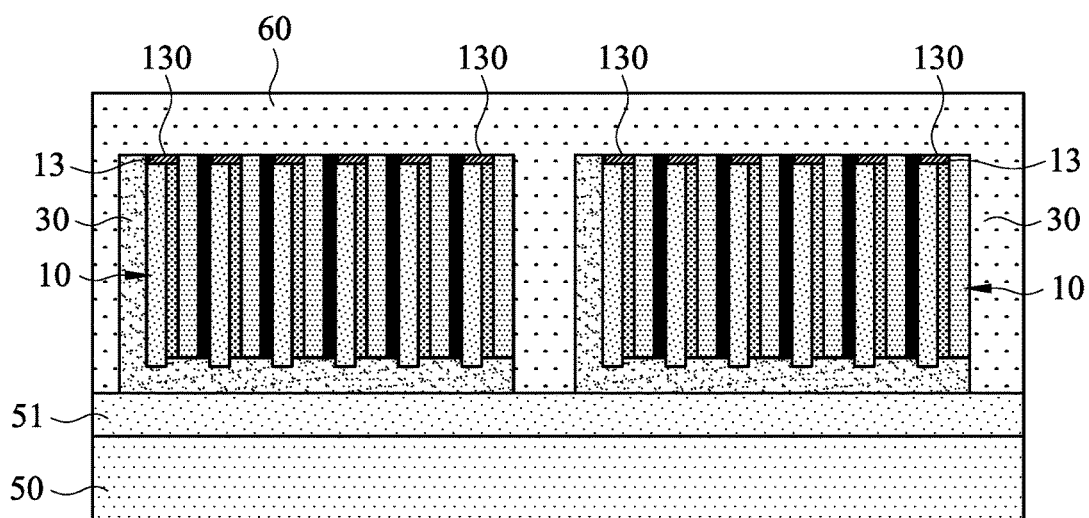


FIG. 9B

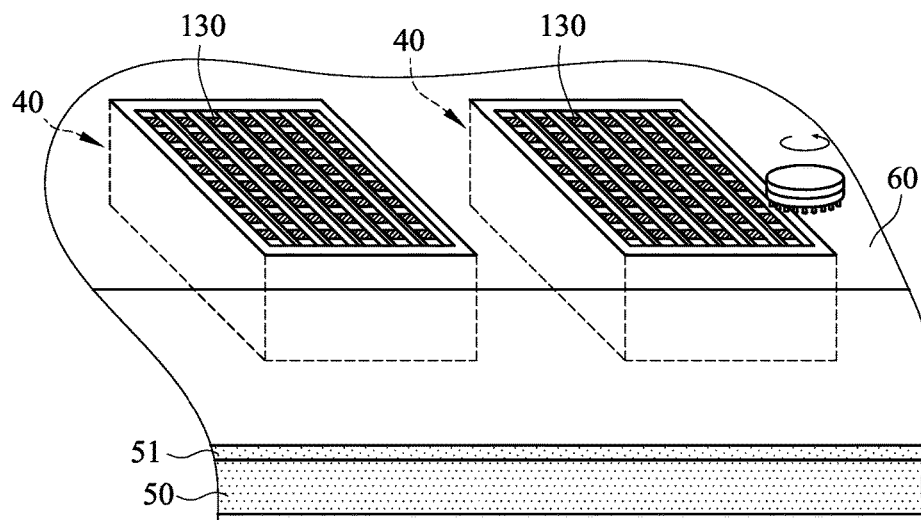


FIG. 10A

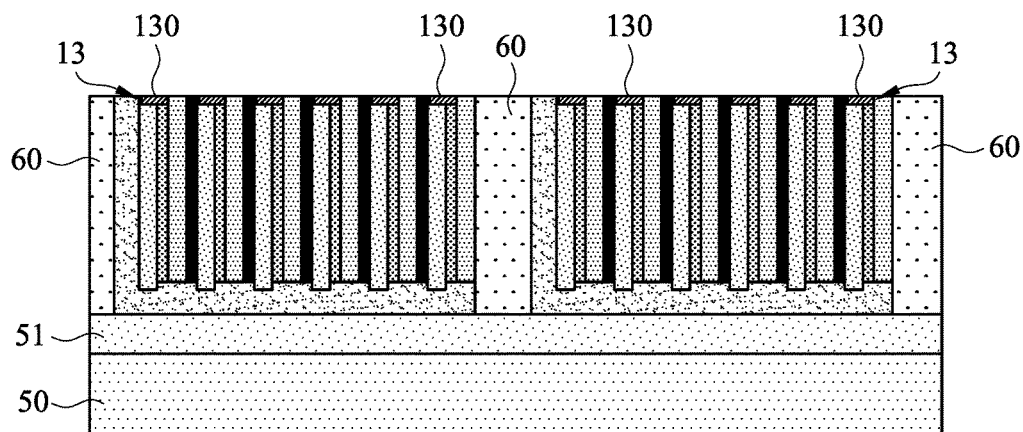


FIG. 10B

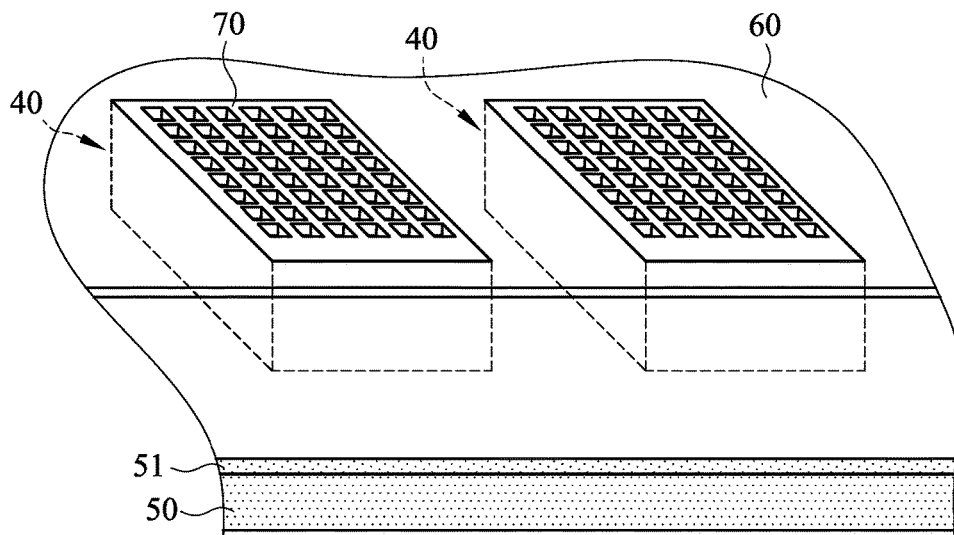


FIG. 11A

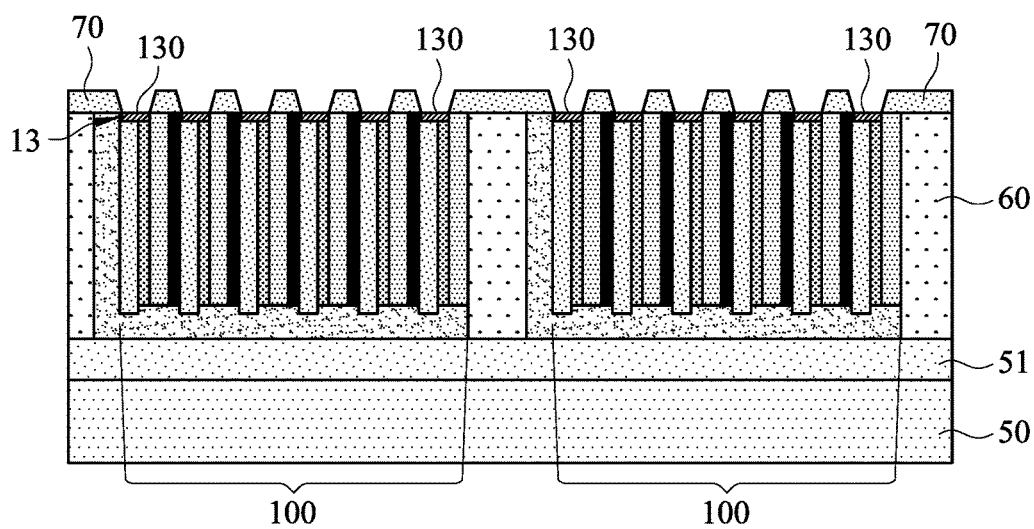


FIG. 11B

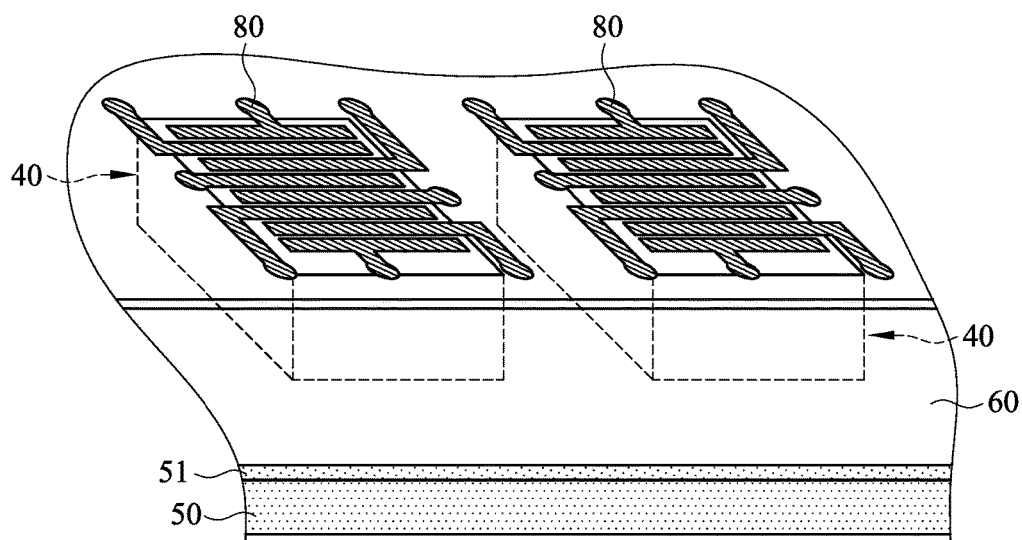


FIG. 12A

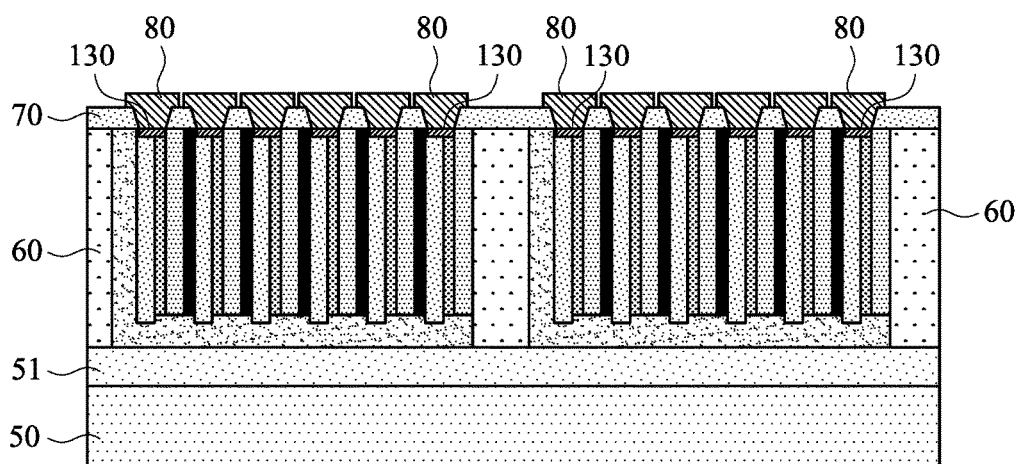


FIG. 12B

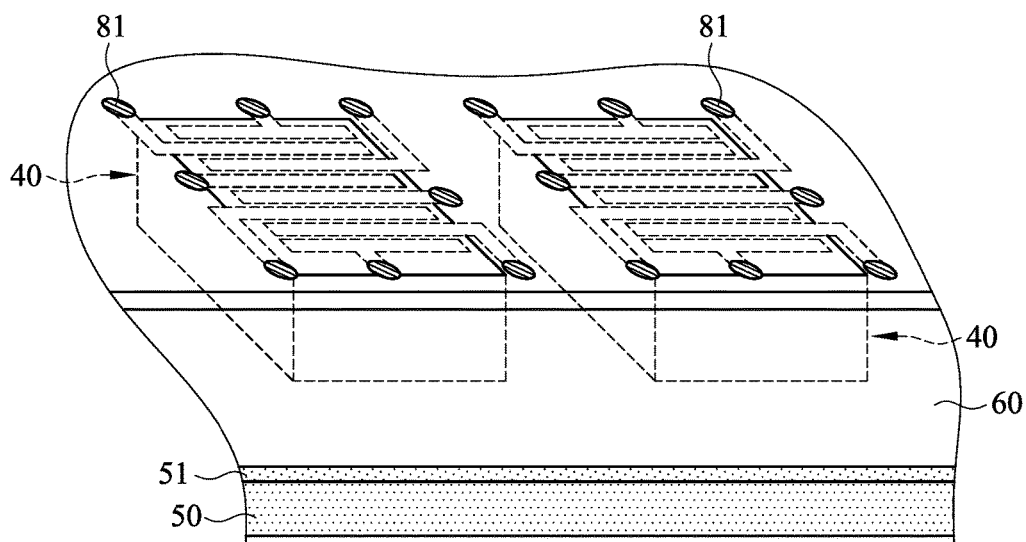


FIG. 13A

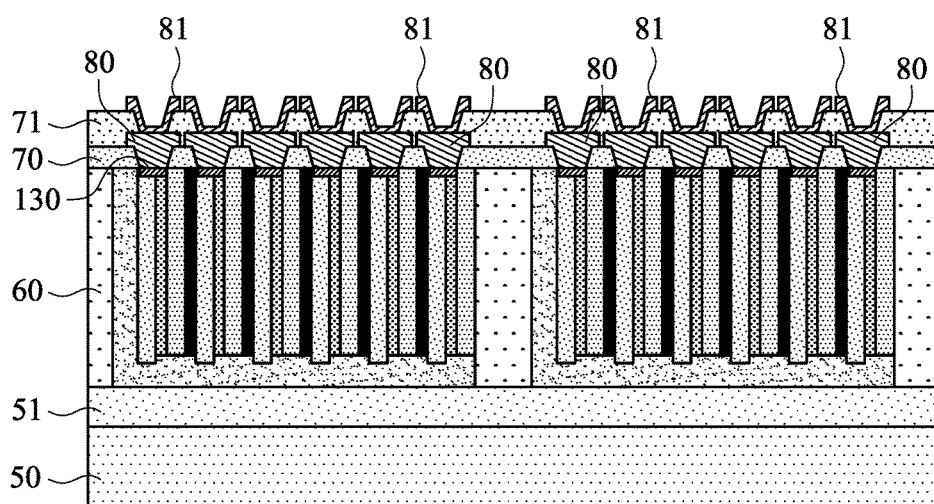


FIG. 13B

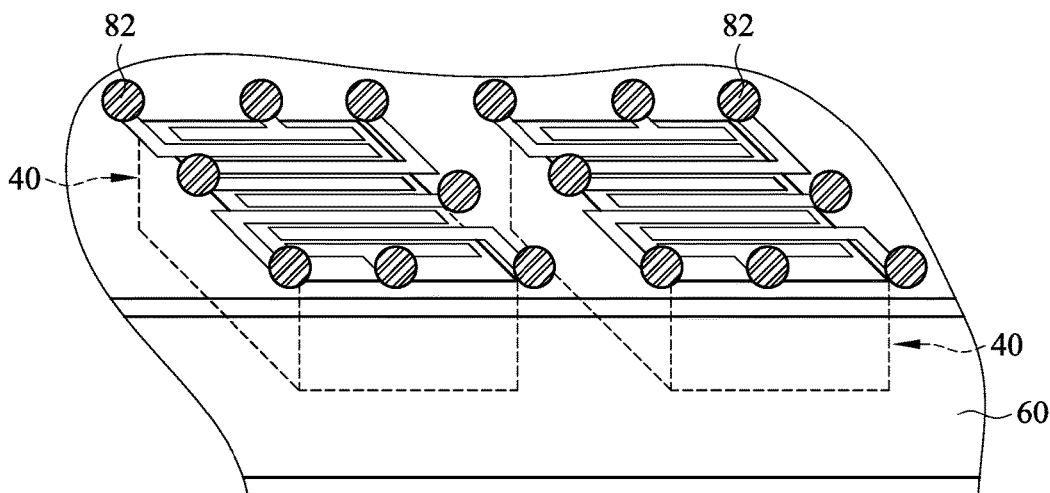


FIG. 14A

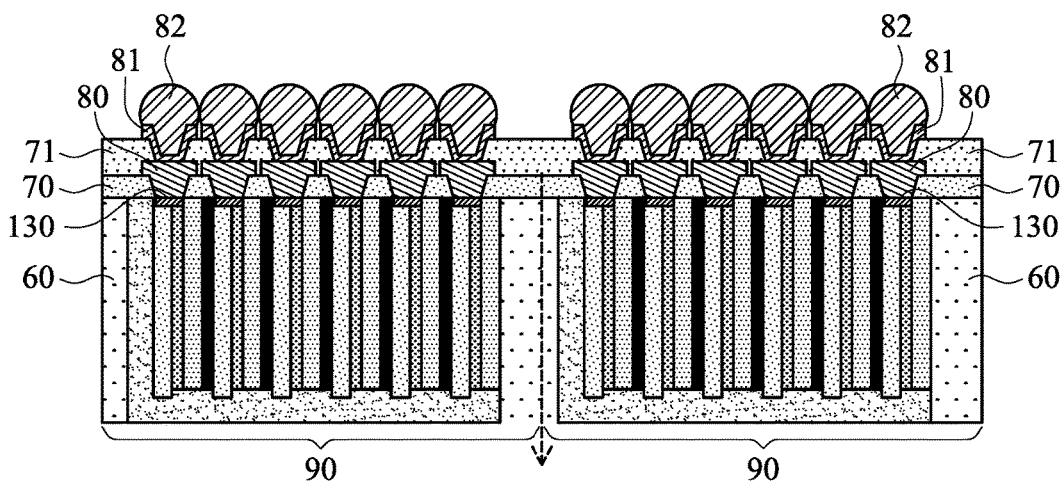


FIG. 14B

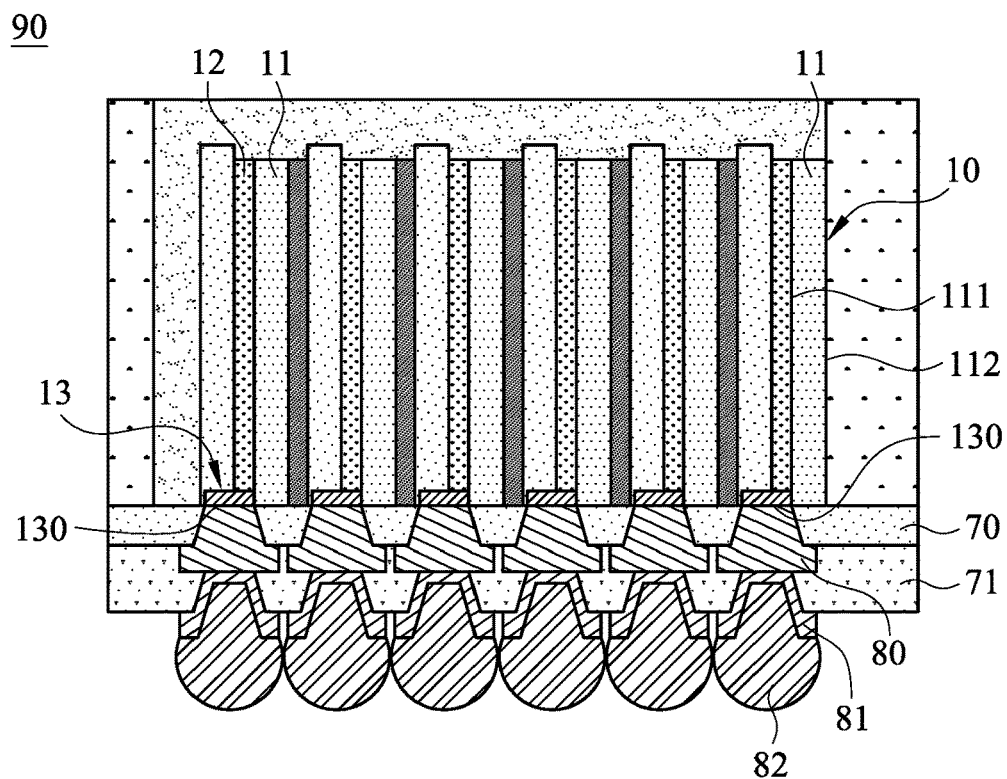


FIG. 15A

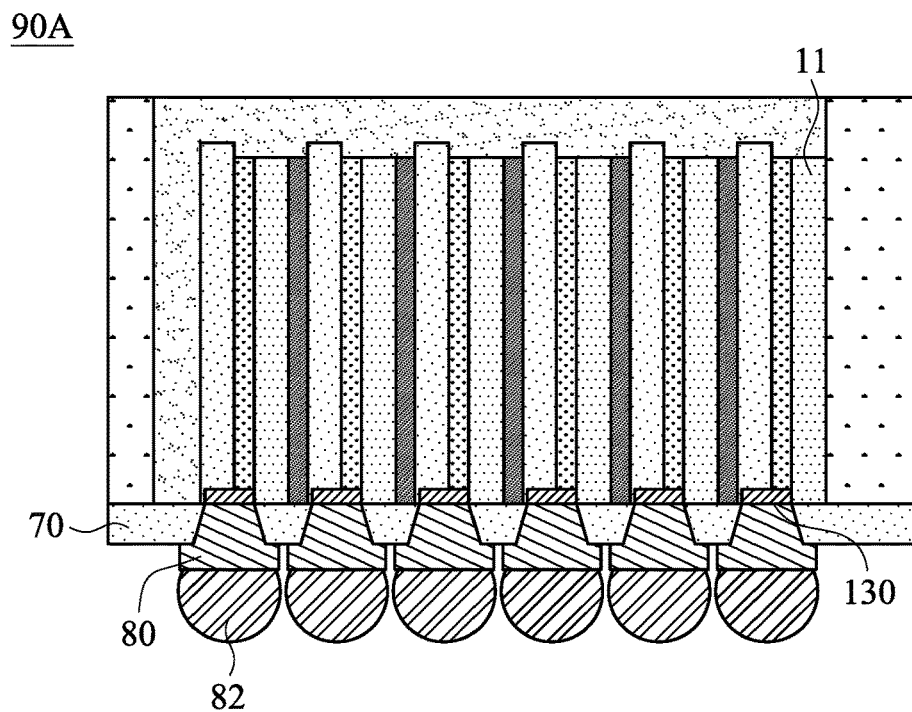


FIG. 15B

90B

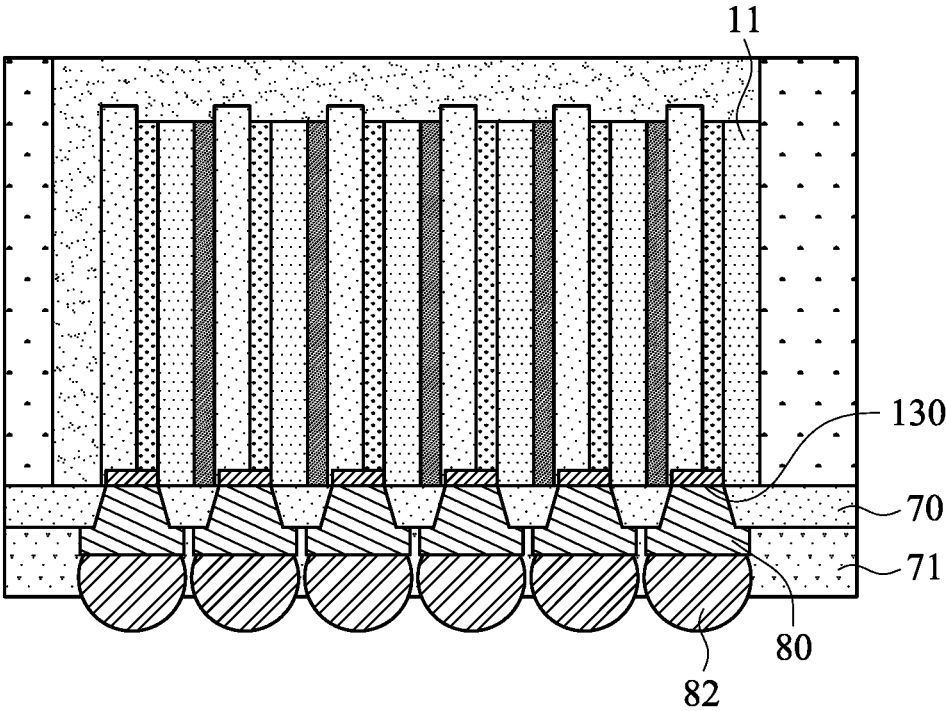


FIG. 15C

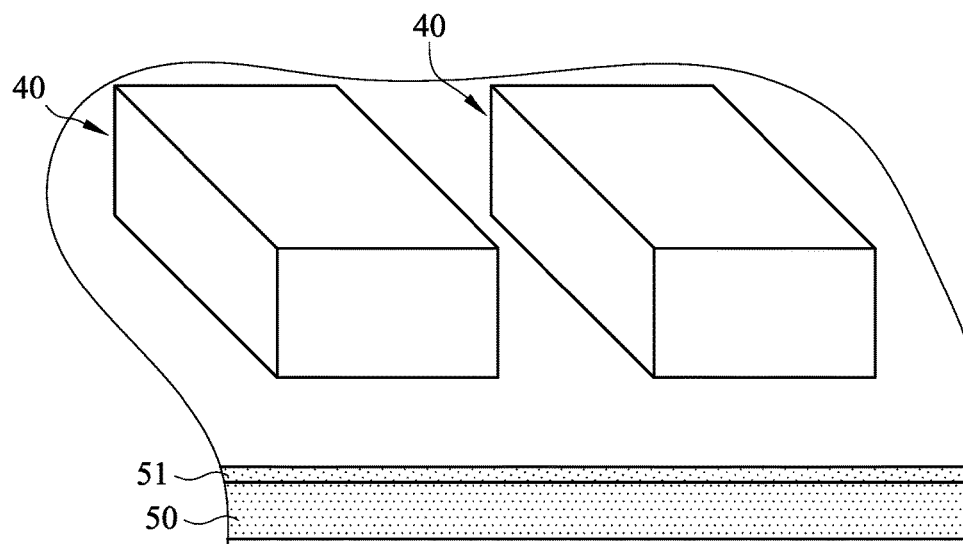


FIG. 16A

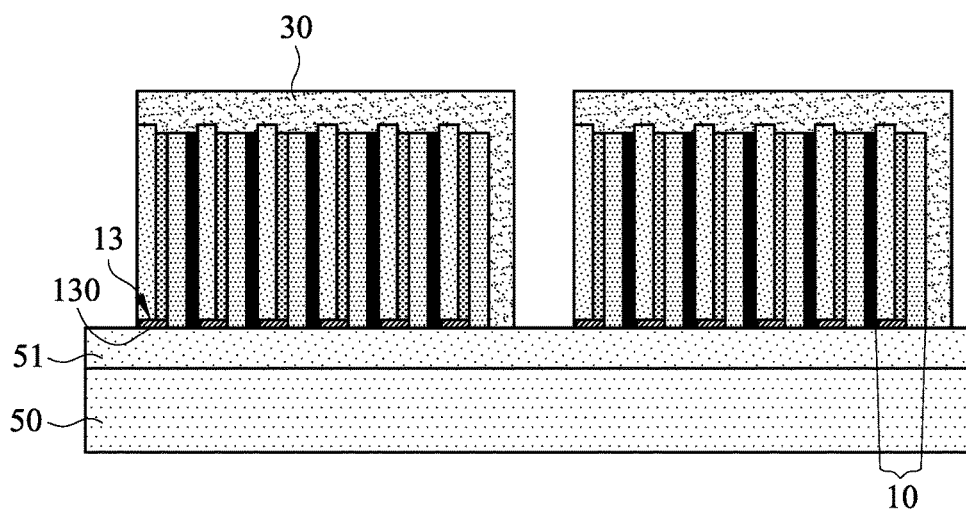


FIG. 16B

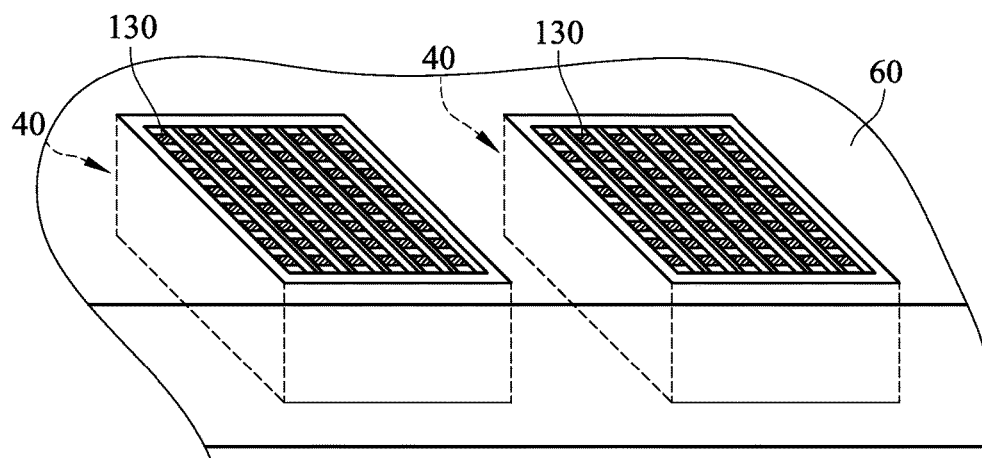


FIG. 17A

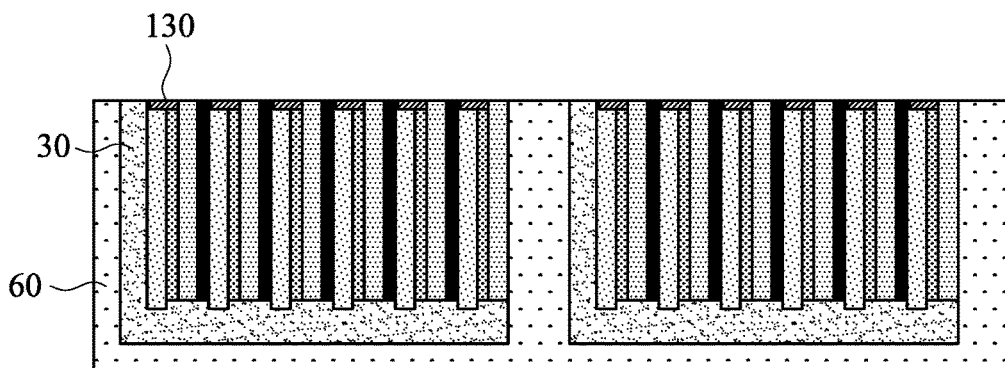


FIG. 17B

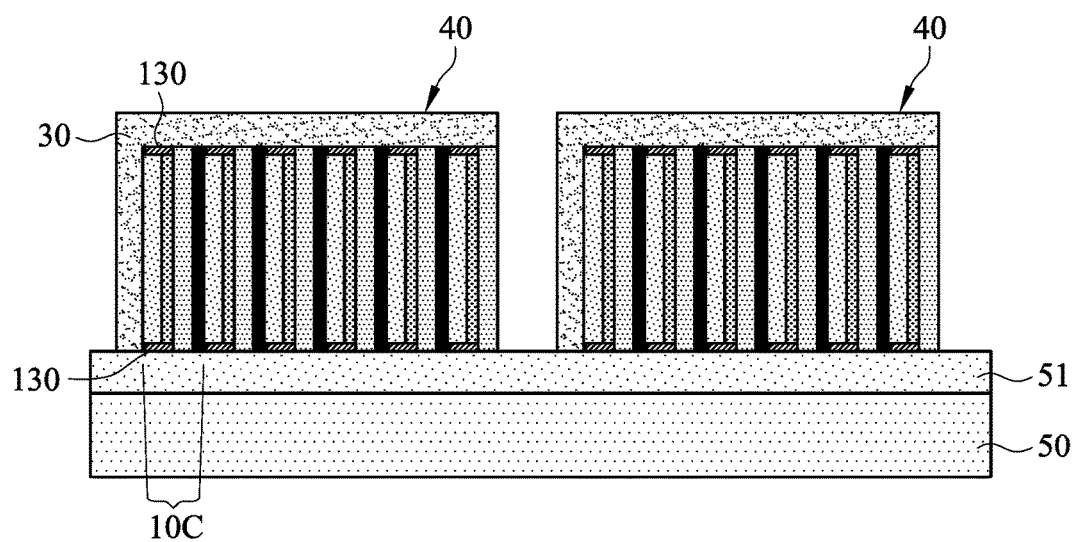


FIG. 18

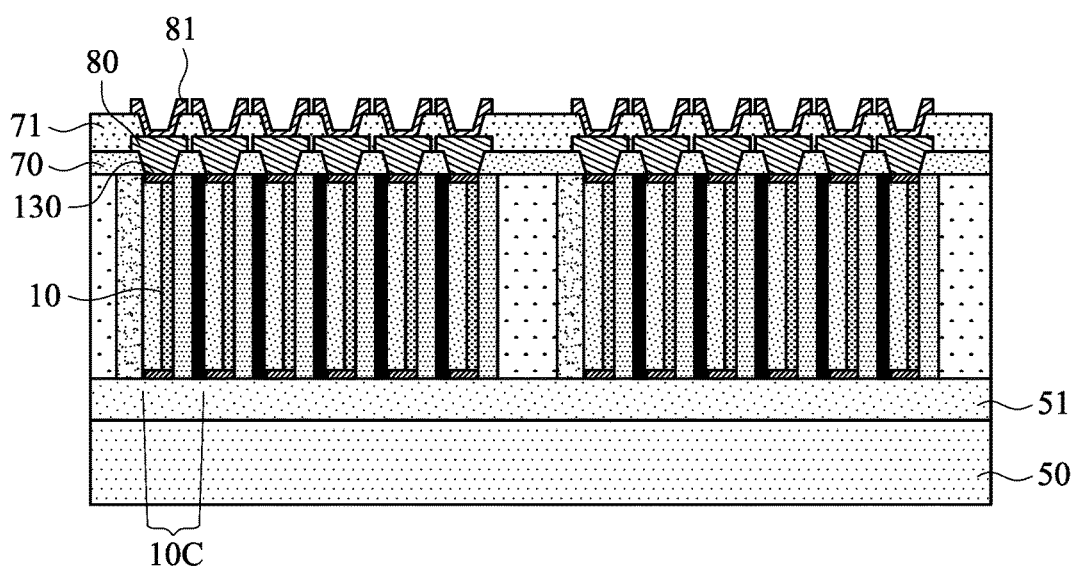


FIG. 19

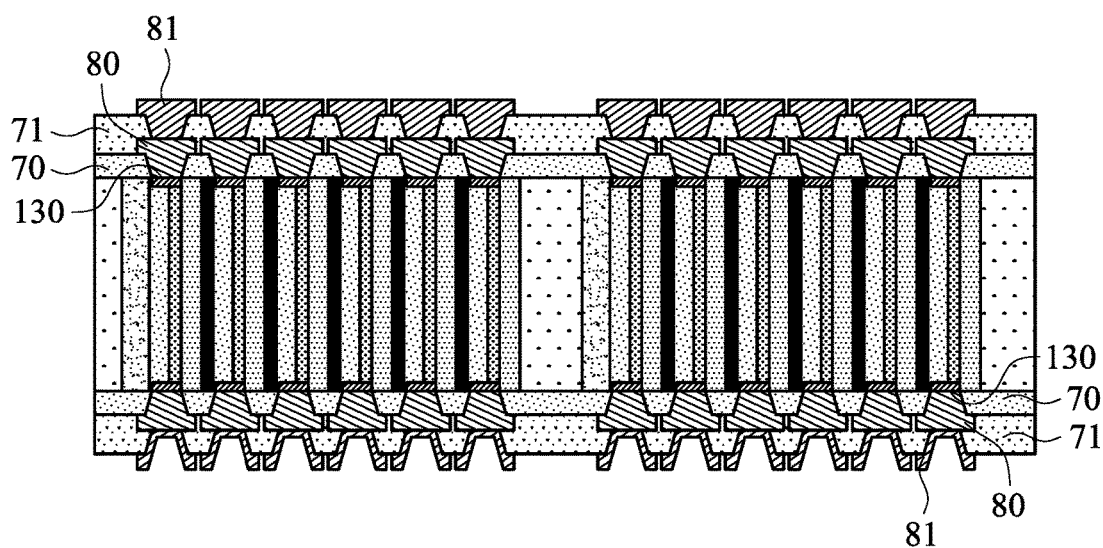


FIG. 20

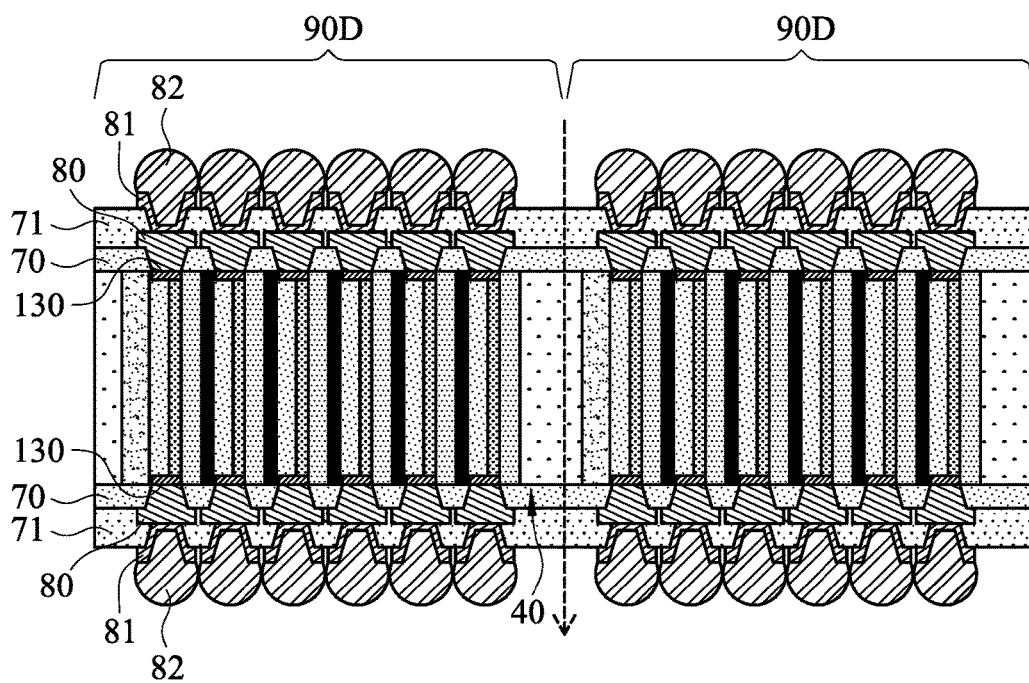


FIG. 21

STACKED PACKAGE INCLUDING EXTERIOR CONDUCTIVE ELEMENT AND A MANUFACTURING METHOD OF THE SAME

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] The present invention relates to a semiconductor package, and in particular to a stacked package and a manufacturing method of the same.

2. Description of the Prior Arts

[0002] Stacking a plurality of chips has been implemented in various semiconductor packages to achieve miniaturization of component integration. The wire bonding method and the through silicon via (TSV) with micro bump are conventional ways to provide electrical interconnection between the stacked chips and the external terminals. However, the conventional ways have following disadvantages.

[0003] When the chips are connected to the external terminals by wire bonding, the intervals between the bonding wires need to be preserved to avoid contacts between the adjacent bonding wires. The intervals inevitably increase the size of the conventional stacked package. Thus, the conventional stacked package with bonding wires does not easily achieve miniaturization. In addition, the wire bonding process takes a lot of time since all of the wires for one conventional stacked package cannot be bonded simultaneously. Therefore, the unit per hour (UPH) of the conventional stacked package manufactured by the wire bonding process is relatively low.

[0004] When the chips are connected to each other by the TSV and the micro bumps, the TSV increases stacked heights and processing complexity leading to larger package thickness and lower manufacturing yield. In addition, the requirements for the precision of alignment and locating among the micro bumps are very high. When the dimension of the conventional stacked packages become larger and larger, the position shift of the micro bumps becomes greater and greater leading to poor packaging yield.

[0005] To overcome the shortcomings, the present invention provides a stacked package and a manufacturing method of the same to mitigate or to obviate the aforementioned problems.

SUMMARY OF THE INVENTION

[0006] The main objective of the present invention is to provide a stacked package and a manufacturing method of the same that has higher UPH and better reliability. The stacked package has plurality of chip packages stacked on active surfaces of each other, a dielectric layer, a redistribution layer and a plurality of external terminals. Each chip package has an exterior conductive element formed on the active surface. Each exterior conductive element has a cut edge exposed on at least one of the lateral side of the chip package. The dielectric layer, the redistribution layer and the external terminals are formed in sequence on the lateral side with the exposed cut edges to form the electrical connection between the cut edges, the redistribution layer and the external terminals. Therefore, the process for forming the electrical connections is simplified to enhance the reliability and the UPH for manufacturing the stacked package.

[0007] Other objectives, advantages and novel features of the invention will become more apparent from the following detailed description when taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] FIG. 1A is a top view in partial section of a first embodiment of a chip package of a stacked package in accordance with the present invention;

[0009] FIG. 1B is a front view in partial section of the chip package in FIG. 1A;

[0010] FIG. 1C is a side view in partial section of the chip package in FIG. 1A;

[0011] FIG. 2A is a top view in partial section of a second embodiment of a chip package of a stacked package in accordance with the present invention;

[0012] FIG. 2B is a front view in partial section of the chip package in FIG. 2A;

[0013] FIG. 2C is a side view in partial section of the chip package in FIG. 2A;

[0014] FIG. 3A is a top view in partial section of a third embodiment of a chip package of a stacked package in accordance with the present invention;

[0015] FIG. 3B is a front view in partial section of the chip package in FIG. 3A;

[0016] FIG. 3C is a side view in partial section of the chip package in FIG. 3A;

[0017] FIG. 4 is a top view in partial section of a fourth embodiment of a chip package of a stacked package in accordance with the present invention;

[0018] FIGS. 5A, 6, 7, 8A, 9A, 10A, 11A, 12A, 13A and 14A are perspective views of a structure of a stacked package during a first embodiment of a manufacturing process in accordance with the present invention;

[0019] FIGS. 5B, 8B, 9B, 10B, 11B, 12B, 13B and 14B are front views in partial section of a stacked package during the first embodiment of the manufacturing process in accordance with the present invention;

[0020] FIG. 15A is a front view in partial section of a first embodiment of a stacked package in accordance with the present invention;

[0021] FIG. 15B is a front view in partial section of a second embodiment of a stacked package in accordance with the present invention;

[0022] FIG. 15C is a front view in partial section of a third embodiment of a stacked package in accordance with the present invention;

[0023] FIGS. 16A and 17A are perspective views of a structure of a stacked package during a second embodiment of a manufacturing process in accordance with the present invention;

[0024] FIGS. 16B and 17B are front views in partial section of a stacked package during the second embodiment of the manufacturing process in accordance with the present invention; and

[0025] FIGS. 18 to 21 are front views in partial section of a stacked package during a third embodiment of the manufacturing process in accordance with the present invention.

DETAILED DESCRIPTION OF THE EMBODIMENTS

[0026] With reference to the attached drawings, the present invention is described by means of the embodiment(s)

below where the attached drawings are simplified for illustration purposes only to illustrate the structures or methods of the present invention by describing the relationships between the components and assembly in the present invention. Therefore, the components shown in the figures are not expressed with the actual numbers, actual shapes, actual dimensions, nor with the actual ratio. Some of the dimensions or dimension ratios have been enlarged or simplified to provide a better illustration. The actual numbers, actual shapes, or actual dimension ratios can be selectively designed and disposed and the detail component layouts may be more complicated.

[0027] With reference to FIG. 15A, a stacked package 90 in accordance with the present invention comprises a plurality of chip packages 10. The chip package 10 has at least two lateral sides, a chip 11, a passivation layer 12 and a plurality of exterior conductive elements 13. The chip 11 has an active surface 111 and a back surface 112. The back surface 112 is opposite to the active surface 111. The passivation layer 12 is formed on the active surface 111. The exterior conductive elements 13 are formed on the active surface 111 of the chip 11, and each exterior conductive element 13 has a cut edge 130 exposed on at least one of the lateral sides of the chip package 10. The chip package 10 may include, but is not limited to, following structures.

[0028] In one embodiment as shown in FIGS. 1A to 1C, the chip package 10 includes a plurality of bond pads 131, a plurality of exterior traces 132, and a chip-dielectric layer 14. Each bond pad 131 is formed on the active surface 111 and is encapsulated by the passivation layer 12. Each exterior trace 132 is formed on a corresponding bond pad 131, extends out of the passivation layer 12, and has an end exposed on one of the lateral sides. The chip-dielectric layer 14 is formed on the passivation layer 12 and the exterior traces 132. The chip-dielectric layer 14 may be a polyimide layer.

[0029] In one embodiment as shown in FIGS. 2A to 2C, the chip package 10A includes a plurality of conductive pad 133A. Each conductive pad 133A is formed on the active surface 111A of the chip 11A, is encapsulated by the passivation layer 12A, and has an end exposed on one of the lateral sides of the chip package 10A.

[0030] In one embodiment as shown in FIGS. 3A to 3C, the chip package 10B includes a plurality of bond pads 134B and a plurality of through silicon vias (TSVs) 135B. Each bond pad 134B is formed on the active surface 111B of the chip 11B and is encapsulated by the passivation layer 12B. Each TSV 135B is formed in the chip 11B, is coupled to a corresponding bond pad 134B, and has an end exposed on one of the lateral sides.

[0031] In summary, the cut edge 130 of each exterior conductive element 13 may be the exterior trace 132 as shown in FIGS. 1A to 1B, may be the conductive pad 133A as shown in FIGS. 2A to 2C, or may be the TSV 135B as shown in FIGS. 3A to 3C.

[0032] An exemplary embodiment shown in FIG. 4 has the cut edges 130C of the exterior conductive elements correspondingly exposed on two lateral sides of the chip package 10C.

[0033] A manufacturing method of a stacked package in accordance with the present invention are illustrated from FIGS. 5A to 14B and comprises following steps:

[0034] With reference to FIGS. 5A and 5B, a chip stack 100 is formed by stacking a plurality of chip packages 10 on

top of each other. The plurality of chip packages 10 are adhered to each other by using a plurality of adhesives 20 correspondingly disposed between adjacent chip packages 10. The adhesives 20 are attached to the back surfaces 112 of the chips 11. The adhesives 20 may be die attach films (DAF), epoxies, insulation pastes, or the like. The chip packages 10 may align with each other through a precise alignment process or may have misalignment when alignment process is not implemented.

[0035] With reference to FIG. 6, a plurality of chip stacks 100 are encapsulated by a first encapsulant 30. The first encapsulant 30 may provide packaging protection to the chip stacks 100 to avoid electrical short and contamination.

[0036] With reference to FIGS. 6 and 7, the chip stacks 100 are diced to form a plurality of chip encapsulations 40. In one embodiment, the chip packages 10 are diced to align with each other when the chip packages 10 may misalign with each other after forming the chip stacks 100. In one embodiment, after the chip packages 10 are diced, the at least one lateral side of the chip packages 10 having the cut edges 130 exposed may align with each other.

[0037] With reference to FIGS. 8A and 8B, the chip encapsulations 40 are arranged on a carrier 50. The chip encapsulations 40 can be attached on the carrier 50 through an adhesive film 51 disposed between the chip encapsulations 40 and the carrier 50. One of the lateral sides of each chip package 10 faces the carrier 50, and the cut edges 130 of the exterior conductive elements 13 face away from the carrier 50. In one embodiment, the chip encapsulations 40 are arranged in an array on the carrier 50. In one embodiment, the carrier 50 may be a glass carrier or a semiconductor carrier in wafer type or in panel type.

[0038] With reference to FIGS. 9A and 9B, the chip encapsulations 40 are encapsulated by a second encapsulant 60. The second encapsulant 60 may provide packaging protection to the chip encapsulations 40 to avoid electrical short and contamination.

[0039] With reference to FIGS. 10A and 10B, the second encapsulant 60 is removed partially to reveal the cut edges 130 of the exterior conductive elements 13. In one embodiment, the second encapsulant 60 is removed through an etching, a polishing or a grinding process. The etching, polishing or grinding process is also used to ensure a planar surface when the cut edges 13 are revealed. In some embodiment, the cut edges 130 may not be exposed during the prior dicing process. The cut edges 130 may only be exposed through the first encapsulant 30 and the second encapsulant 60 after performing the process disclosed in FIGS. 10A and 10B.

[0040] With reference to FIGS. 11A and 11B, a first dielectric layer 70 is formed on the lateral side of the chip packages 10 that have the exposed cut edges 130 and is etched to reveal the cut edges 130. In one embodiment, the first dielectric layer 70 is etched by a lithography process to reveal the cut edges 130. The first dielectric layer 70 may be a polyimide layer.

[0041] With reference to FIGS. 12A and 12B, a redistribution layer 80 is formed on the first dielectric layer 70 and is electrically connected to the cut edges 130. The redistribution layer 80 may be a circuitry formed by conductive metals. In one embodiment, the redistribution layer 80 may be a multi-layer metal stack such as Titanium (Ti)/Copper (Cu)/Copper (Cu) or Titanium (Ti)/Copper (Cu)/Copper (Cu)/Nickel (Ni)/gold (Au).

[0042] With reference to FIGS. 13A and 13B, a second dielectric layer 71 is formed on the redistribution layer 80. Then an under bump metallurgy (UBM) layer 81 is formed on the second dielectric layer 71 and is electrically connected to redistribution layer 80. In one embodiment, the second dielectric layer 71 is etched by a lithography process to reveal the redistribution layer 80. The second dielectric layer 71 may be a polyimide layer. In one embodiment, the UBM layer 81 is formed by sputtering. The number of the conductive layers such as redistribution layer 80 and the number of the dielectric layers 70, 71 are not limited to the embodiment as described and can be selectively designed.

[0043] With reference to FIGS. 14A and 14B, a plurality of external terminals 82 are disposed on the second dielectric layer 71 and are electrically connected to the UBM layer 81. Then the carrier 50 and the adhesive film 51 are detached. The chip encapsulations 40 are singulated to form a plurality of stacked packages 90. The external terminals 82 may be a plurality of solder balls, solder pastes, contact pads, or contact pins.

[0044] With the cut edges 130 exposed on the at least one of the lateral side of the chip package 10, the electrical connections between the chips 11 and the electrical connection between the chips 10 and the external terminals 82 are achieved by the redistribution layer 80 formed on the cut edges 130 on the at least one of the lateral sides. Thus, the process for forming the electrical connections of the manufacturing method as described is simplified to enhance the reliability and the UPH for manufacturing the stacked package as described. Moreover, the requirement of the precision for stacking the chip packages 10 is relatively low since the chip packages 10 are aligned after dicing process as shown in FIG. 7 and the cut edges 130 are coplanar after the etching, polishing or grinding process as shown in FIGS. 10A and 10B. Therefore, the manufacturing method as described is further simplified to enhance the UPH for manufacturing the stacked package as described.

[0045] According to an embodiment of the present invention, the stacked package 90 may have, but not limited to, following structures, and the manufacturing method of the stacked package may have accordingly steps.

[0046] In one embodiment as shown in FIG. 15A, the stacked package 90 includes the first dielectric layer 70, the redistribution layer 80, the second dielectric layer 71, the UBM layer 81 and the external terminals 82. The chips 11 may be able to electrically connect to an external printed circuit board through the electrical connections between the cut edges 130, the redistribution layer 80, the UBM layer 81 and the external terminals 82.

[0047] In one embodiment as shown in FIG. 15B, the stacked package 90A comprises the first dielectric layer 70, the redistribution layer 80 and the external terminals 82. The chips 11 may electrically connect to an external printed circuit board through the connections between the cut edges 130, the redistribution layer 80 and the external terminals 82.

[0048] In one embodiment as shown in FIG. 15C, the stacked package 90B comprises the first dielectric layer 70, the redistribution layer 80, the second dielectric layer 71 and the external terminals 82. The chips 11 may be able to electrically connect to an external printed circuit board through the electrical connections between the cut edges 130, the redistribution layer 80 and the external terminals 82.

[0049] Another embodiment of a manufacturing method of a stacked package in accordance with the present invention includes, but not limited to, following steps:

[0050] After the steps are performed as shown in FIGS. 5A to 7, the cut edges 130 of the exterior conductive elements 13 on one of the lateral sides of the chip packages 10 are disposed to face the carrier 50 when the chip encapsulations 40 are arranged on the carrier 50 as shown in FIGS. 16A and 16B.

[0051] With further reference to FIGS. 17A and 17B, the carrier 50 and the adhesive film 51 are detached after forming the second encapsulant 60 to expose the cut edges 130 on one of the lateral sides of the chip packages 10. The steps to form the redistribution layer, the UBM layer and the solder balls are similar to the steps shown in FIGS. 11A to 14B.

[0052] Yet another embodiment of a manufacturing method of a stacked package in accordance with the present invention includes, but not limited to, following steps:

[0053] The chip packages 10C have cut edges 130C exposed on two lateral sides as shown in FIG. 4. After the steps are performed as shown in FIGS. 5A to 7, the cut edges 130 of the exterior conductive elements 13 on the first lateral side of the chip packages 10C are disposed to face the carrier 50 when the chip encapsulations 40 are arranged on the carrier 50 as shown in FIG. 18.

[0054] With reference to FIG. 19, the first dielectric layer 70, the redistribution layer 80, the second dielectric layer 71 and the UBM layer 81 are formed on the first lateral side.

[0055] The electrical connection between the chips 10, the cut edges 130 on the second lateral side, the redistribution layer 80 and the UBM layer 81 is formed after the carrier 50 and the adhesive film 51 are detached. With further reference to FIG. 20, the first dielectric layer 70, the redistribution layer 80, the second dielectric layer 71 and the UBM layer 81 are formed on the second lateral side.

[0056] In some embodiment, with reference to FIG. 21, a plurality of external terminals 82 are disposed on the second dielectric layer 71 on the first and second lateral sides and are electrically connected to the UBM layer 81 on the first and second lateral sides. Then the chip encapsulations 40 are singulated to form a plurality of stacked packages 90D.

[0057] With the stacked package 90D has the external terminals 82 on dual sides, stacking with other semiconductor structures, passive components and so on are more easily.

[0058] Even though numerous characteristics and advantages of the present invention have been set forth in the foregoing description, together with details of the structure and features of the invention, the disclosure is illustrative only. Changes may be made in the details, especially in matters of shape, size, and arrangement of parts within the principles of the invention to the full extent indicated by the broad general meaning of the terms in which the appended claims are expressed.

1. A stacked package comprising:

- a plurality of chip packages stacked on each other, and each chip package of the plurality of chip packages having
 - two lateral sides;
 - a chip having an active surface and a back surface opposite to the active surface, wherein the back surface of each chip package faces the active surface of an adjacent chip package;

a passivation layer formed on the active surface of the chip; and

an exterior conductive element formed on the active surface of the chip and having a cut edge exposed on at least one of the two lateral sides, each of the two lateral sides comprising a lateral side of the chip, a lateral side of the passivation layer, and the cut edge;

an encapsulant encapsulating the chip packages and having an opening expose the at least one of the two lateral sides;

at least one dielectric layer formed on the at least one of the two lateral sides and having patterned recess areas expose the cut edges on the at least one of the two lateral sides; and

at least one redistribution layer formed on the at least one dielectric layer, filled with the patterned recess areas of the at least one dielectric layer and electrically connecting to the cut edges on the at least one of the two lateral sides.

2. The stacked package as claimed in claim 1, wherein each chip package has two cut edges exposed respectively on both of the two lateral sides;

an amount of the at least one dielectric layer is two and the two dielectric layers are formed respectively on the cut edges on both of the two lateral sides; and

an amount of the at least one redistribution layer is two and the two redistribution layers are formed respectively on the two dielectric layers and connect respectively to the cut edges on both of the two lateral sides.

3. The stacked package as claimed in claim 2 further comprising

two additional dielectric layers formed respectively on the two redistribution layers and having a plurality of gaps to reveal the cut edges on the two lateral sides;

two under bump metallurgy layers formed respectively on the two additional dielectric layers and respectively connect to the two redistribution layers; and

a plurality of external terminals formed on and connecting to the two bump metallurgy layers.

4. The stacked package as claimed in claim 1, wherein the exterior conductive element has

a bond pad formed on the active surface and encapsulated by the passivation layer; and

an exterior trace formed on the bond pad and extending out the passivation layer;

the cut edge of the exterior conductive element is disposed on an end of the exterior trace; and

the chip package further comprises a dielectric layer formed on the passivation layer and the exterior trace.

5. The stacked package as claimed in claim 1, wherein the exterior conductive element has a conductive pad formed on the active surface and encapsulated by the passivation layer; and

the cut edge of the exterior conductive element is disposed on an end of the conductive pad.

6. The stacked package as claimed in claim 1, wherein the exterior conductive element has

a bond pad formed on the active surface and encapsulated by the passivation layer; and

a through silicon via formed in the chip and connecting to the bond pad; and

the cut edge of the exterior conductive element is disposed on an end of the through silicon via.

7. The stacked package as claimed in claim 1, wherein the at least one dielectric layer comprises a first dielectric layer and a second dielectric layer, and the first dielectric layer is formed on the cut edges on the at least one of the two lateral sides, and the second dielectric layer is formed between the at least one redistribution layer and the external terminals.

8. The stacked package as claimed in claim 1 further comprising at least one under bump metallurgy layer, wherein

the at least one dielectric layer comprises a first dielectric layer and a second dielectric layer;

the first dielectric layer is formed on the cut edges on the at least one of the two lateral sides;

the at least one redistribution layer is formed on the first dielectric layer;

the second dielectric layer is formed on the at least one redistribution layer;

the at least one under bump metallurgy layer is formed on the second dielectric layer and connects to the at least one redistribution layer; and

external terminals are formed respectively on and connecting to the at least one under bump metallurgy layer.

9. The stacked package as claimed in claim 1, wherein the plurality of chip packages stacked on each other by using a plurality of adhesives attached respectively between adjacent chip packages.

10. A manufacturing method of a stacked package comprising steps of:

stacking a plurality of chip packages on a carrier, wherein each chip package has a two lateral sides, a chip having an active surface and a back surface opposite to the active surface and an exterior conductive element formed on the active surface of the chip and having a cut edge exposed on at least one of the lateral sides, wherein the back surface of one chip package faces the active surface of the adjacent chip package and one of the lateral sides facing the carrier;

encapsulating the chip packages on the carrier by an encapsulant;

revealing the cut edges on the at least one of the lateral sides;

forming at least one dielectric layer on the at least one of the lateral sides and revealing the cut edges on the at least one of the lateral sides;

forming at least one redistribution layer on the at least one dielectric layer, wherein the at least one redistribution layer electrically connects to the cut edges on the at least one of the lateral sides; and

performing singulation to form a plurality of the stacked packages.

11. The manufacturing method as claimed in claim 10 further comprising a step of detaching the carrier, wherein the lateral sides of the chip package include a first lateral side and a second lateral side;

the cut edges of each chip package are exposed on the first lateral side;

in the step of stacking a plurality of chip packages on a carrier, the second lateral sides of the chip packages face the carrier;

in the step of revealing the cut edges, the encapsulant is partially removed to reveal the cut edges on the first lateral side; and

the step of detaching the carrier is performed before the step of performing singulation.

12. The manufacturing method as claimed in claim **10**, wherein

the lateral sides of the chip package include a first lateral side and a second lateral side;

the cut edges of each chip package are exposed on the first lateral side;

in the step of stacking a plurality of chip packages on a carrier, the first lateral sides of the chip packages face the carrier; and

in the step of revealing the cut edges, the carrier is detached to reveal the cut edges on the first lateral side.

13. The manufacturing method as claimed in claim **10**, wherein

the lateral sides of the chip package include a first lateral side and a second lateral side;

the cut edges of each chip package are exposed both on the first and second lateral sides;

in the step of stacking a plurality of chip packages on a carrier, the second lateral sides of the chip packages face the carrier;

in the step of revealing the cut edges, the encapsulant is partially removed to reveal the cut edges on the first lateral side;

in the step of forming at least one dielectric layer, the at least one dielectric layer is formed on the cut edges on the first lateral side;

in the step of forming at least one redistribution layer, the at least one redistribution layer electrically connects to the cut edges on the first lateral side; and

the manufacturing method further comprising steps of after forming at least one redistribution layer, detaching the carrier;

forming at least one additional dielectric layer on the second lateral sides and revealing the cut edges on the second lateral sides;

forming at least one additional redistribution layer on the at least one additional dielectric layer, wherein the at least one additional redistribution layer electrically connect to the cut edges on the second lateral sides; and

forming a plurality of external terminals on the at least one redistribution layer, wherein the external terminals are formed and connect respectively to the at least one redistribution layer and the at least one additional redistribution layer.

14. The manufacturing method as claimed in claim **10**, wherein in the step of stacking a plurality of chip packages on a carrier comprises steps of:

forming a plurality of chip stacks by stacking a plurality of chip packages;

encapsulating the chip stacks;

forming a plurality of chip encapsulations by dicing the chip stacks; and

arranging the chip encapsulations on the carrier.

15. The manufacturing method as claimed in claim **14**, wherein in the step of forming a plurality of chip stacks, a plurality of adhesives are used to attach respectively between adjacent chip packages.

16. The manufacturing method as claimed in claim **10** further comprising steps of:

forming at least one supplemental dielectric layer on the at least one redistribution layer; and

forming a plurality of external terminals on the at least one supplemental dielectric layer.

17. The manufacturing method as claimed in claim **10** further comprising steps of:

forming at least one supplemental dielectric layer on the at least one redistribution layer after the step of forming at least one redistribution layer;

forming at least one under bump metallurgy layer on the at least one redistribution layer; and

forming a plurality of external terminals on the at least one of the under bump metallurgy layer, wherein the external terminals are formed on and electrically connect to the at least one of the under bump metallurgy layer.

18. The manufacturing method as claimed in claim **10**, wherein in the step of stacking a plurality of chip packages on a carrier, the chip packages are stacked on the carrier through an adhesive film.

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