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(54) Title: SOLID STATE LIGHT EMITTING DEVICES BASED ON CRYSTALLOGRAPHICALLY RELAXED STRUCTURES

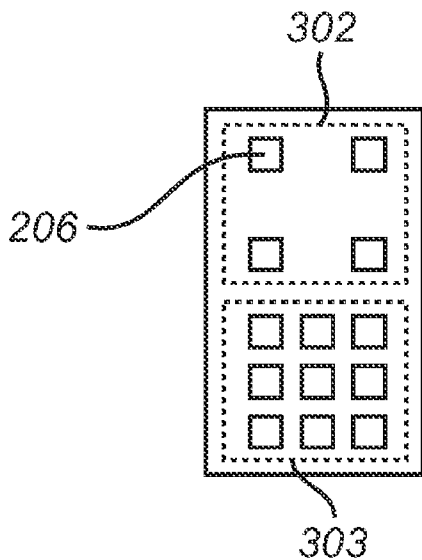


Fig. 3c

(57) Abstract: The present invention discloses a method for manufacturing a solid state light emitting device having a plurality of light-sources, the method comprising the steps of: providing a substrate having a growth surface; providing a mask layer on the growth surface, the mask layer having a plurality of openings through which the growth surface is exposed, wherein a largest lateral dimension of each of said openings is less than 0.3 μm and wherein the mask layer may comprise a first mask layer portion and a second mask layer portion, having the same surface area and comprising a plurality of openings wherein the first mask layer portion exhibits a first ratio between an exposed area of the growth surface and an unexposed area of the growth surface, and wherein the second mask layer portion exhibits a second ratio between an exposed area of the growth surface and an unexposed area of said growth surface, the second ratio being different from the first ratio; growing a base structure on the growth surface in each of the openings of the mask layer; and growing at least one light-generating quantum well layer on the surface of each of the base structures.



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Solid state light emitting devices based on crystallographically relaxed structures

FIELD OF THE INVENTION

The present invention relates to solid state light emitting devices and to a method for manufacturing such solid state light emitting devices.

5 BACKGROUND OF THE INVENTION

Solid state light emitting devices such as light emitting diodes (LEDs) and solid state lasers are used in a wide range of applications from conventional lighting systems to optical communication systems. In particular, nitride based LEDs enable the use of LEDs for general lighting purposes. However, emission efficiency for such devices drops
10 considerably for wavelengths above 480nm. A way to compensate this is to use blue emitting LEDs in such a way that part of the emitted blue light is converted to green-yellow light by interaction with a phosphorescent material. However, phosphorescent conversion suffers from several conversion loss mechanisms during the transition from a higher energy radiation to lower energy radiation resulting in limited conversion efficiency while also the emission
15 peak shape is broadened. Therefore, LEDs emitting directly in the green to red parts of the visible spectrum would provide considerable benefits such as eliminated conversion losses and improved color tunability.

For example, gallium nitride (GaN) based light sources can be adapted to shift the emission wavelength towards the red end of the visible spectrum. WO2008/078297
20 discloses a method for manufacturing a GaN-based semiconductor light emitting device configured to emit multiple wavelengths of light. This is achieved by forming a plurality of posts from a mask layer having a plurality of openings, where each post comprises a light emitting layer disposed between an n-type and a p-type region. The emitted wavelength is controlled by the diameter of the post.

25

SUMMARY OF THE INVENTION

In view of the aforementioned prior art, it is an object of the present invention to provide an improved method for fabrication of solid state light emitting devices, and in

particular an improved method for fabricating solid state light emitting devices enabling fabrication of devices emitting wavelengths in the green to red part of the visible spectrum.

According to a first aspect of the present invention, it is therefore provided a method for manufacturing a solid state light emitting device having a plurality of light-
5 sources, the method comprising the steps of: providing a substrate having a growth surface; providing a mask layer on the growth surface, the mask layer having a plurality of openings through which the growth surface is exposed, wherein a largest lateral dimension of each of said openings is less than 0.3 μm and wherein the mask layer comprises a first mask layer portion and a second mask layer portion, having the same surface area and comprising a
10 plurality of openings wherein the first mask layer portion exhibits a first ratio between an exposed area of the growth surface and an unexposed area of the growth surface, and wherein the second mask layer portion exhibits a second ratio between an exposed area of the growth surface and an unexposed area of said growth surface, the second ratio being different from the first ratio; growing a base structure on the growth surface in each of the openings of the
15 mask layer; and growing at least one light-generating quantum well layer on the surface of each of the base structures.

The term “solid state light emitting devices” should in the present context be understood as semiconductor-based light emitting devices such as photoluminescent devices, LEDs, laser diodes or vertical cavity surface emitting lasers (VCSELs). A light source should
20 in the present context be understood as each individual structure which emits light either in an electrically driven device through direct emission or in a passive device through a photoluminescent reaction following photoexcitation.

The light-generating quantum well (QW) layer is a thin layer of a material having a lower energy band gap than the surrounding materials, thereby forming a potential
25 well. Light is generated when charge carriers recombine over the bandgap and the size of the bandgap determines the wavelength of the emitted light. Charge carriers can be provided either through electrical injection in an electrically driven device or through photoexcitation in a passive device. By growing the light-generating quantum well layer on an at least partially relaxed base structure it is possible to achieve material compositions, and thereby
30 band gap energies, in the quantum well layer not possible to achieve on a non-relaxed surface. Thus, providing at least partially relaxed base structures promotes growth of a quantum well layer with desirable light-emitting properties not achievable on a non-relaxed surface. In particular, it is possible to grow quantum wells having emission peaks in the red part of the visible spectrum. It is equally possible to grow multiple quantum wells stacked on

the base structure in order to manufacture light emitting devices such as LEDs, laser diodes and VCSELs. Furthermore, limiting the size of the openings to achieve the growth of relaxed structures also enables the use of non-lattice matched substrates which would otherwise give rise to stress related problems commonly occurring when growing larger structures or
5 continuous films.

The present invention is based on the realization that the properties of light-sources based on crystallographically relaxed structures, epitaxially grown on a growth surface in openings of a certain size, can be controlled by controlling the relative size and separation distance of the openings, and in particular by controlling the ratio between the
10 exposed growth surface area and the mask layer area.

As base structures which are at least partially relaxed allow subsequent growth of a light-generating quantum well layer with properties different from what is possible to grow on strained material, it is desirable to achieve such crystallographically relaxed base structures. Provided that a largest lateral dimension of each of the openings is less than 0.3
15 μm , local surface relaxation will reduce or eliminate the stress that otherwise would result from a lattice mismatch between the lattice constant of the growth surface and lattice constant of the base structure. The largest lateral dimension of f.i. a polygon is the largest diagonal, i.e. the largest line segment connecting two different non- sequential corners of the polygon. The largest allowable size of each of the openings to achieve relaxed base structures is for a
20 selected material combination determined by material parameters such as Young's modulus and lattice constant.

The wavelength of the light emitted from a quantum well is related to the quantum well thickness which in turn is a result of the growth conditions used when growing the quantum well layer. As a precursor is provided, commonly in gas or vapor form, the
25 precursor can be assumed to uniformly reach the entire surface of the wafer in a common rotating wafer configuration during deposition. Since growth only takes place on the base structures and not on the mask layer surface, precursor material deposited on the mask layer surface migrates towards the openings containing the base structures, there contributing to quantum well growth. Thus, the ratio between exposed and unexposed growth surface area
30 determines the amount of precursor material available to grow the quantum well layer. As a result, a portion of the wafer where a larger fraction of the growth surface is exposed results in thinner quantum wells than on a portion of the wafer where a smaller fraction of the growth surface is exposed.

Hence, the size of the opening in combination with the separation will then determine the relative growth rate and thereby the thickness of QWs grown on a particular base structure. The combination of opening size and separation distance is thus a strong means to tune QW thickness and thereby emission color from a specific light source.

5 A substrate acting as a carrier may be provided. The substrate may advantageously be a wafer in a conducting material enabling contacting of the backside of the substrate. More specifically, the substrate may comprise a material selected from the group consisting of GaN, sapphire, silicon, SiC, ZnO, ScN, TiN, HfN, AlN, ZrB₂, HfB₂, NbB₂, BP, GaAs, GaP, LiGaO₂, NdGaO₃, LiAlO₂, ScMgAlO₄, garnet and spinel.

10 A growth surface may be provided on an upper surface of the substrate where the growth surface promotes growth of the desired relaxed base structure. In the present context a growth surface may advantageously be a surface suitable for epitaxial growth of a group III-V semiconductor-based material, more specifically the growth surface may be suitable for epitaxial growth of GaN based materials. For electrically driven devices, a GaN
15 based n-doped growth layer may be used.

A mask layer may be arranged on top of the growth surface and openings may be created in the mask layer exposing the growth surface. The mask layer may advantageously be insulating as is the case for a SiO₂ based material. The mask layer may also be selected from a wide range of insulating materials such as SiN_x, TiO₂, ZrO₂ or similar
20 oxides, nitrides or carbides.

Epitaxial growth of the base structures starts at the exposed growth surface, meaning that no growth takes place on the surface of the mask layer. Consequently the openings in the mask layer define where base structures are grown. The main purpose of the base structure is to function as a base for subsequent growth of a light-generating quantum
25 well layer which may be grown as a continuous film on the surface of the base structure. For electrically driven solid state lighting devices, the base-structure is preferably n-doped.

It should also be noted that for a photoluminescent device, quantum wells are not strictly required. In a photoluminescent device, the base structures may be the light emitting structures, although also in such devices quantum wells may be used for additional
30 control of the light emitting properties.

According to one embodiment of the present invention, the plurality of openings are of substantially the same size and the distance between adjacent openings is greater in the second mask layer portion than in the first mask layer portion. Hereby, it is possible on a single wafer to tailor the quantum well properties to be different in different

portions of the device while using substantially the same opening size in the first and second portions. Needless to say, there may be more than two mask layer portions having mutually different distances between openings.

5 This provides for a highly flexible way of simultaneously producing on the same surface a combination of light sources emitting different wavelengths, while being able to use an optimal opening size so that relaxed base structures can be grown in all openings if desired.

10 Put in slightly different words, the density of openings of substantially the same size may be different in the first and second mask layer portions. For example, the openings may be arranged substantially regularly, and the pitch may vary between the two portions.

15 The distance between openings may, for example, be at least 10% greater in the second mask layer portion than in the first mask layer portion, whereby a substantial color difference can be achieved while still growing the light-generating quantum well layers on relaxed base structures. By locally varying separation distance of the openings and/or opening size, the emitted wavelength can be tuned locally. By doing this over relatively large areas of a device (large enough to be contacted separately) the device becomes segmented and thereby color tunable. On the other hand, by randomly or quasi-randomly varying either or both of opening size and separation, thus varying QW thickness, a highly uniform mixture of light-sources with different wavelengths may be obtained, which can be an advantage in applications that are highly demanding from a uniformity point of view. Furthermore, the possibility to tailor emission in combination with the possibility to emit wavelengths covering the visible spectrum, as a result of using relaxed base structures, makes it possible to produce LED devices emitting white light.

25 According to another embodiment of the present invention, each opening in the plurality of openings has a polygon shape, wherein at least one side of the opening is aligned substantially parallel to a crystallographic orientation of the growth surface;

30 The shape of the opening will have an effect on the lattice structure of the crystal planes that constrain the polyhedron grown from the polygon shaped opening. Different crystal planes in the base structure may possess different growth properties, thereby resulting in a different material composition or layer thickness of the grown light-generating quantum well layer. A different material composition or thickness of the quantum well may lead to a shift in emission wavelength. The differences in quantum well properties corresponding to different crystal planes of the base structure may be relatively small and

will in that case mainly lead to an apparent broadening of the total emission peak. A broader emission peak results in a more continuous emission spectrum, thus leading to a better color perception of the emitted light. The effect of different crystal planes with different properties will as an example be evident for polyhedrons shaped as truncated pyramids, where a
5 quantum well grown on the top surface is likely to exhibit not only a different material composition, but also a notably different growth rate compared to a quantum well grown on the side walls of the pyramid. Additionally, for pyramids, the total growth area of the structure (initially the opening in the mask) grows once the pyramid shape starts forming and more so when the pyramid is overgrowing the mask, implying that the relative growth rate
10 perpendicular to the surface starts decreasing. This can be exploited as this effect will occur earlier and to a larger extent with small sized holes at a relatively small separation distance.

A different growth rate of the QWs at different planes is one way in which the color of emitted light can be tuned more strongly as this will result in QWs of different thickness. The thickness of a quantum well directly determines the extent of quantum
15 confinement, which in turn (in combination with material composition and strain induced by lattice mismatch) determines the wavelength of the emitted light.

Furthermore, the alignment of the openings may advantageously be selected so that all sides of the base structures are equivalent with respect to the growth surface which results in a higher degree of uniformity over the device area.

20 Additionally, a controlled shape and alignment of the opening may advantageously lead to a base structure with fewer crystallographic defects, thereby reducing the risk of non-radiative recombination centers which reduce the efficiency of the device.

In the case of strong misalignment between the sides of the openings and the underlying crystallographic structure, the grown structure will partly align to various
25 crystallographic directions. For example, a misaligned quadratic opening may result in a grown structure which is faceted, meaning that a polyhedron with 6 or 8 sides may be grown. However, some misalignment may be allowed as the grown structures inherently align to the preferred growth directions.

In one embodiment of the present invention, the shape of the opening may
30 advantageously be hexagonal. By aligning the sides of the grown base structures to a desired underlying crystallographic orientation, making all sides of the structure equivalent, it is possible to achieve a higher uniformity and thereby a better defined emission wavelength, which may be favorable when monochromatic emission is desired. The shape of the opening

may equally well be triangular, rectangular or any other polygon depending on the crystallographic structure of the growth surface.

According to one embodiment of the present invention, the method for fabricating a solid state light emitting device may further comprise the step of providing a first contacting structure on the light-generating quantum well layer of each of the base structures and a second contacting structure electrically contacting the base structure.

According to one embodiment of the present invention the first contacting structure may advantageously comprise a charge carrier confinement layer arranged on the surface of the light-generating quantum well layer followed by a conducting layer on the surface of the confinement layer. The charge carrier confinement layer is part of a heterostructure forming the quantum well, where the function of the confinement layer is to define one of the boundaries of the quantum well, providing an energy barrier between the quantum well and the neighboring material. The opposite quantum well boundary is formed by the base structure. As an example, the charge carrier confinement layer may be an electron-blocking layer and the conducting layer may comprise a p-doped hole conduction layer with contacts arranged on the conducting layer. The device can be contacted as planar grown LEDs, i.e. by applying proper contacting layers to both the n-doped growth layer and the p-doped top layer.

The contacts may be formed on opposite sides of the device or they may both be on the same side of the device. When both contacts are arranged on the same side, the device may be formed either with transparent contacts and mounted such that light is extracted on the same side as the contacts. Alternatively, the contacts may be reflective and mounted as a flip chip in which case light is extracted from the opposite side of where the contacts are arranged.

In one embodiment of the present invention, the step of providing the mask layer may comprise the steps of depositing a mask layer material on the growth surface and selectively removing mask layer material according to a predefined pattern to form the aforementioned openings.

According to one embodiment of the present invention, patterning of the mask layer may advantageously be done by nano-imprinting. By using a patterning method such as surface conformal nano-imprinting, patterning can be done on wafer scale in a single process step. Additionally, problems with wafer bending associated with other lithography methods can be reduced or even avoided. A pattern may advantageously be imprinted in deformable silica provided in the form of sol-gel derived SiO_2 , there forming a plurality of depressions

corresponding to a predefined imprinting template. After nano-imprinting, a thin residual layer of silica may remain at the bottom of the depressions. The residual layer may preferably be removed by selectively etching the mask layer material with respect to the underlying growth layer where the removal, for example, can be done using reactive ion etching (RIE).

5 Other patterning methods are also available such as stepper lithography, e-beam lithography and holographic interference lithography. Suitable mask removal methods would be used for the respective lithography methods.

According to a second aspect of the present invention, it is provided a solid state light emitting device comprising: a substrate having a growth surface; a mask layer on
10 the growth surface, the mask layer having a plurality of openings, wherein a largest lateral dimension of each of said openings is less than $0.3\ \mu\text{m}$ and wherein the mask layer comprises a first mask layer portion and a second mask layer portion, having the same surface area and comprising a plurality of openings wherein the first mask layer portion exhibits a first ratio between the opening area and the mask layer area, and wherein the second mask layer portion
15 exhibits a second ratio between the opening area and the mask layer area, the second ratio being different from the first ratio; an at least partially crystallographically relaxed base structure grown on the growth surface in each of the openings of the mask layer; and a light-generating quantum well layer grown on the surface of each of the base structures.

Effects and features of this second aspect of the present invention are largely
20 analogous to those described above in connection with the first embodiment. However, some additional features will be discussed.

According to an embodiment of the solid state light emitting device according to the present invention, the base structures may advantageously protrude above the mask layer. The grown base structures are not necessarily limited by the thickness of the mask
25 layer, on the contrary, they may instead protrude above and extend beyond the openings in the mask layer. For continued growth after the structures have protruded above the mask layer the structures may also extend in a lateral direction. Allowing extended growth provides another possibility to tune the size and geometry of the base structures and quantum wells in addition to the geometrical disposition of the openings discussed in relation to the first aspect
30 of the present invention.

According to one embodiment of the present invention, the growth surface may advantageously comprise a GaN or InGaN growth layer arranged on the carrier substrate. From the growth layer a GaN or InGaN base structure may be grown followed by an InGaN quantum well layer. It would also be possible to use other material combinations,

preferably from the III-V group of semiconductor-based materials, and more preferably from the subset of nitride based III-N materials.

BRIEF DESCRIPTION OF THE DRAWINGS

5 These and other aspects of the present invention will now be described in more detail with reference to the appended drawings showing exemplary embodiments of the invention, wherein:

 Fig. 1 is a flow-chart schematically illustrating an exemplary manufacturing method according to an exemplary embodiment of the present invention;

10 Figs. 2a-h schematically illustrate the steps of the method illustrated by the flow-chart in fig 1;

 Figs. 3a-c schematically illustrate an intermediate step in the fabrication method for making a solid state light emitting device according to an exemplary embodiment of the present invention; and

15 Figs. 4a-b schematically illustrates alternative light source patterns for solid state light emitting device according to various embodiments of the present invention.

DETAILED DESCRIPTION

 In the following detailed description, various embodiments of the method for
20 manufacturing solid state light emitting devices according to the present invention are mainly discussed with reference to a method based on growth of relaxed semiconductor structures as a base for light emitting diodes.

 It should be noted that this by no means limits the scope of the present invention which is equally applicable to passive devices emitting light through
25 photoluminescent emission. Manufacturing methods using variations of the processing steps described below are also possible. As an example, other mask patterning methods such as photolithography or e-beam lithography may be used. Furthermore, the method is equally applicable for other material combinations, primarily comprising materials from the III-V group of semiconductor-based material. Also, growth methods may be selected from a range
30 of methods enabling epitaxial growth, for instance, MBE may be used instead of MOVPE.

 An exemplary method according to an embodiment of the present invention will now be described with reference to the flow-chart shown in Fig. 1 together with Fig. 2 schematically illustrating the device in different stages of the manufacturing process.

In a first step 101, a substrate 201 having a growth surface 204 is provided as shown in Fig 2a. A suitable substrate can be a sapphire or a doped silicon carbide (SiC) wafer. As an example, a GaN layer 203 is deposited on the surface of the sapphire wafer 202 to form a growth surface 204 as shown in Fig 2a. Growth surfaces consisting of a so called
5 buffer layer of relaxed GaN obtained by hetero-epitaxial growth of GaN on commonly used substrates are well-suited. At least the top of this GaN-layer is n-doped for fabricating an electroluminescent device.

In the next step 102, a mask layer 205 is provided as illustrated in Fig 2b. A deformable precursor layer to the mask layer is deposited on the GaN growth surface. The
10 deformable precursor is in this embodiment sol-gel derived SiO₂.

In the following step 103, the mask layer 205 is patterned. Patterning is done by imprinting the precursor layer over the entire area of the wafer in a single step using surface conformal nano imprinting (SCIL), resulting in depressions in the form of squares in the silica layer as shown in Fig. 2c. The largest lateral dimension of each of the depressions is
15 less than 0.3 μm. As a result of imprinting, there may be a thin residual layer of silica at the bottom of the depressions. The remaining silica at the bottom of the depressions can be removed through reactive ion etching, forming openings 206 exposing the GaN growth surface 204. The etching of the silica is preferably selective with respect to the GaN growth surface 204.

In the subsequent step 104 of growing the base structures 207, as is schematically illustrated in Fig 2d, InGaN base structures 207 are grown on the exposed GaN growth surface 204 in each of the openings 206 of the mask layer 205. InGaN growth may, for example, be done in a metalorganic vapor phase epitaxy (MOVPE) reactor and the In content is determined by the trimethylindium (TMI) to triethylgallium (TEG) precursor ratio.
25 A variation in In content may also be achieved by adapting the temperature during growth. The epitaxially grown InGaN base structures 207 only nucleate in the openings 206 at the GaN surface 204 and no growth takes place on the surface of the silica mask layer. Due to the limited dimensions of the openings 206, the resulting InGaN base structures 207 have a relaxed crystal structure. The shape of the base structures 207, when grown in the manner as
30 described in the present embodiment using square openings, is a square pyramid. Depending on growth time the top of the pyramid might be flat. The shape of the top is not critical to the function of the light emitting device and shapes such as conventional pyramids are equally possible. The base structures 207 may or may not protrude above the mask layer 205 depending on the mask layer thickness and growth time of the base structures 207. In the

present embodiment, base structure growth is stopped before coalescence, but it would in principle be equally possible to fabricate light emitting devices from coalesced structures, provided that the base structures remain crystallographically relaxed.

5 In the next step 105, illustrated in Fig. 2e, a thin light-generating quantum well layer 208 is grown on the surface of the base structures 207. The epitaxially grown quantum well layer 208 only grows on the base structure 207 and no growth takes place on the surface of the mask layer 205. In this embodiment, the quantum well layer 208 comprises InGaN having a higher In content than the base structure 207. The relaxed crystal structure of the base structure 207 leads to the incorporation of a higher In content in the quantum well layer 10 208 compared to what is incorporated on non-relaxed base structures under the same conditions. By increasing the In content, the band gap is reduced sufficiently so as to allow the emission of green or red light. In another embodiment, the base structures 207 can be made of GaN with an InGaN quantum well for fabrication of light sources emitting blue light.

15 The next step 106, illustrated in Fig. 2f, is the deposition of a charge carrier confinement layer 209. In the present embodiment, the charge carrier confinement layer 209 comprises an aluminum gallium nitride (AlGaN) electron blocking layer.

In the next step 107 illustrated in Fig. 2g a conducting layer 210 is deposited. The deposition of a conducting layer 210 comprises deposition of a p-doped InGaN layer and 20 followed by a p⁺⁺-doped InGaN layer.

The final step 108 in the method according to an embodiment of the present invention is illustrated in Fig. 2h where a contact layer 211 is deposited in the form of an electrically conductive contact material such as ITO (Indium Tin Oxide) or Pd/Au. Conventional processing can subsequently be used to define the p-contacts and n-contacts. 25 Contacts to the n-doped side of the device may be achieved either through holes etched in the top-layers or via substrate removal and contacts at the n-doped side. The derived solid state lighting device itself may be continuous or segmented to enable differentiated contacting to individual (base) structures over the device area.

Fig. 3a illustrates device having a pattern 301 where the size and separation 30 distance of the openings 206 in the mask layer varies over the surface of the device. By varying the size and separation distance of the openings 206 as outlined it is possible to tailor the resulting light sources to emit different wavelengths on the same wafer without adding any process steps. In general, having a smaller opening to mask ratio, as illustrated in the top part 302 of Fig. 3a, result in a thicker quantum well layer which in turn gives emission at a

higher wavelength compared to an area with a larger opening to mask ratio 303. As an example, by combining multiple wavelengths it is possible to fabricate devices emitting white light. As another example, by segmenting and separately contacting areas emitting different wavelengths, a color tunable device can be made.

5 Fig. 3b illustrates the openings 206 in the mask layer 205 exposing the growth surface 204 prior to growth of base structures.

Fig. 3c schematically illustrates a device having openings of the same size but where the separation distance of the openings is different in different regions of the device. In particular, in a first region (302) the distance between the openings are larger than in a
10 second region (303) which leads to a different density of openings.

Fig. 4a schematically illustrates a possible shape of the openings in the mask layer where a hexagonal shape 402 enables alignment along specific crystal directions in the underlying growth surface. As an example, two schematic crystal directions of the growth surface, c_1 and c_2 , are shown. It is also shown that a hexagonal opening may be aligned so
15 that it has sides (404, 405) substantially parallel to the crystal directions. By aligning the sides of the grown base structures to a desired underlying crystallographic orientation, making all sides of the structure equivalent, it is possible to achieve a higher uniformity and thereby more controlled emission properties. An even higher degree of uniformity can be obtained when the hexagonal openings 402 are packed in a hexagonal pattern 403 as
20 illustrated in Fig. 4b, as then also the distances between adjacent hexagons can be chosen constant.

As an example, aligning a hexagonal configuration of openings along the low-index orientation on a GaN surface implies that all opening walls will be either along the (10-10) or (11-20) direction.

25 As another example, triangular openings oriented along the major low-index crystallographic axis on the C-plane of GaN will lead to well defined crystallographic growth of equivalent crystal planes.

As yet another example, when growing structures on the M-plane, A-plane or R-plane of sapphire, all exhibiting a rectangular symmetry, at least two different sets of
30 planes are initially grown and the ratio between the planes can be tuned by selecting the size shape and orientation of the opening.

The person skilled in the art realizes that the present invention by no means is limited to the preferred embodiments described above. On the contrary, many modifications and variations are possible within the scope of the appended claims. For example, the method

according to the present invention may also be used to fabricate vertical cavity emitting lasers (VCSELs) and laser diodes (LDs). Additionally, LEDs having been fabricated according to the method described above but with different material compositions are equally possible. Also, by omitting the n-type and p-type doping as well as the contacting layers, the resulting structure is well suited to act as a photoluminescent emitter with most of the properties with respect to wavelength tuning and selection as described above. Such a material could be directly illuminated by a suitable UV or blue emitting light source or through a waveguide structure. Furthermore, the basic principle of the present invention may also be applied to the fabrication of group III-V based semiconductor-based devices in general by providing a surface for growth having the desired properties related to lattice parameters and strain levels.

CLAIMS:

1. A method for manufacturing a solid state light emitting device having a plurality of light sources, the method comprising the steps of:
 - providing a substrate (201) having a growth surface (204);
 - providing a mask layer (205) on said growth surface, said mask layer having a
 - 5 plurality of openings (206) through which said growth surface (204) is exposed, wherein a largest lateral dimension of each of said openings (206) is less than 0.3 μm and wherein said mask layer (205) comprises a first mask layer portion (302) and a second mask layer portion, (303) each comprising a plurality of openings (206) exposing said growth surface (204),
 - wherein said first mask layer portion (302) exhibits a first ratio between an
 - 10 exposed area of said growth surface (204) and an unexposed area of said growth surface (204), and wherein said second mask layer portion (303) exhibits a second ratio between an exposed area of said growth surface (204) and an unexposed area of said growth surface (204), said second ratio being different from said first ratio;
 - growing a base structure (207) on said growth surface (204) in each of said
 - 15 openings (206) of said mask layer (205); and
 - growing at least one light-generating quantum well layer (208) on the surface of each of said base structures (207).
2. The method according to claim 1, wherein said plurality of openings are of
- 20 substantially the same size and wherein the distance between adjacent openings is greater in said second mask layer portion (303) than in said first mask layer portion (302).
3. The method according to any one of the preceding claims, wherein each
- 25 opening in the plurality of openings (206) has a polygon shape, wherein at least one side of said opening is aligned substantially in parallel to a crystallographic orientation of said growth surface (204).
4. The method according to any one of the preceding claims, wherein said
- opening is hexagonal.

5. The method according to any one of the preceding claims, further comprising the step of providing a first contacting structure on the light-generating quantum well layer (207) of each of said base structures and a second contacting structure electrically contacting the base structure.
6. The method according to any claim 5, wherein the step of providing a first contacting structure comprises the steps of:
- growing a charge carrier confinement layer (209) on the surface of said light-generating quantum well layer (208);
 - providing a conducting layer (210) on the surface of said charge carrier confinement layer (209); and
 - providing contacts to the conducting layer.
7. The method according to any one of the preceding claims, wherein said step of providing a mask layer (205) comprises the steps of:
- depositing a mask layer material on said growth surface; and
 - selectively removing mask layer material to form said openings (206).
8. The method according to claim 7, wherein said step of selectively removing comprises the steps of:
- patterning said mask layer (205) by producing a plurality of depressions in said mask layer (205) through nano-imprinting; and
 - removing said mask layer material at the bottom of said depressions by selectively etching said mask layer material with respect to said growth surface material to form said openings (206) exposing said growth surface (204).
9. A solid state light emitting device comprising:
- a substrate (201) having a growth surface (204);
 - a mask layer (205) on said growth surface (204), said mask layer (205) having a plurality of openings (206), wherein a largest lateral dimension of each of said openings is less than 0.3 μm and wherein said mask layer (205) comprises a first mask layer portion (302) and a second mask layer portion, (303) each comprising a plurality of openings (206), wherein said first mask layer portion (302) exhibits a first ratio between the

opening area and the mask layer area, and wherein said second mask layer portion (303) exhibits a second ratio between the opening area and the mask area, said second ratio being different from said first ratio;

5 an at least partially crystallographically relaxed base structure (207) grown on said growth surface (204) in each of said openings (206) of said mask layer (205); and
a light-generating quantum well layer (208) grown on the surface of each of said base structures (207).

10. A solid state light emitting device according to claim 9, wherein said plurality
10 of openings are of substantially the same size and wherein the distance between adjacent openings is greater in said second mask layer portion (303) than in said first mask layer portion (302).

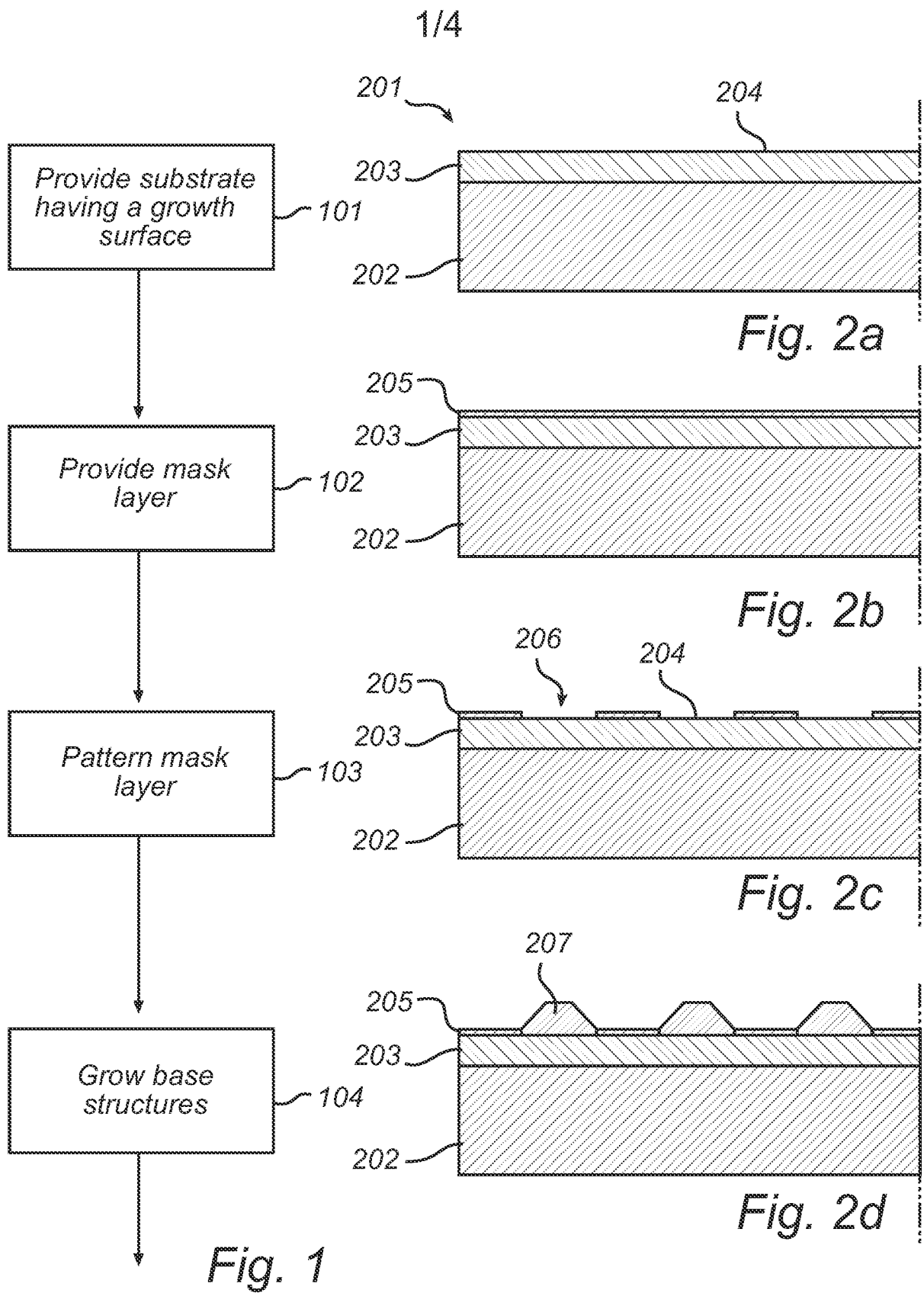
11. A solid state light emitting device according to claim 9 or 10, wherein each of
15 the plurality base structures (207) has a polygon shape, where at least one side of said polygon is aligned substantially in parallel to a crystallographic orientation of said growth surface (204).

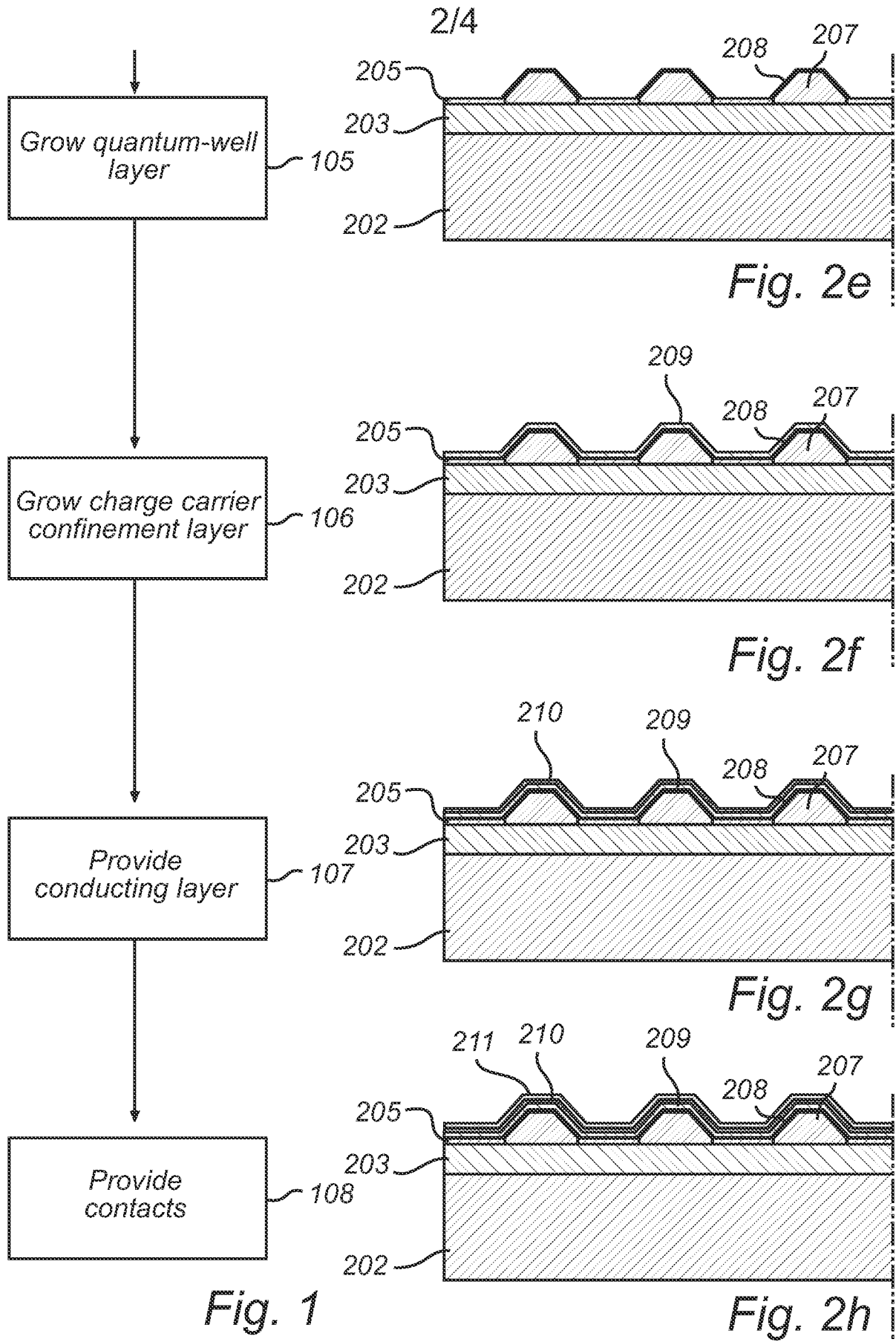
12. A solid state light emitting device according to any one of claims 9 to 11,
20 further comprising a first contacting structure arranged on the light-generating quantum well layer (208) of each of said base structures (207) and a second contacting structure electrically contacting the base structure.

13. The solid state light emitting device according to any one of claims 9 to 12,
25 wherein each of said base structures (207) protrudes above said mask layer (205).

14. The solid state light emitting device according to any one of claims 9 to 13,
wherein at least one of said growth surface (204) and base structures (207) comprises GaN or
30 InGaN.

15. The solid state light emitting device according to any one of claims 9 to 14,
wherein said quantum well layer (208) comprises InGaN.





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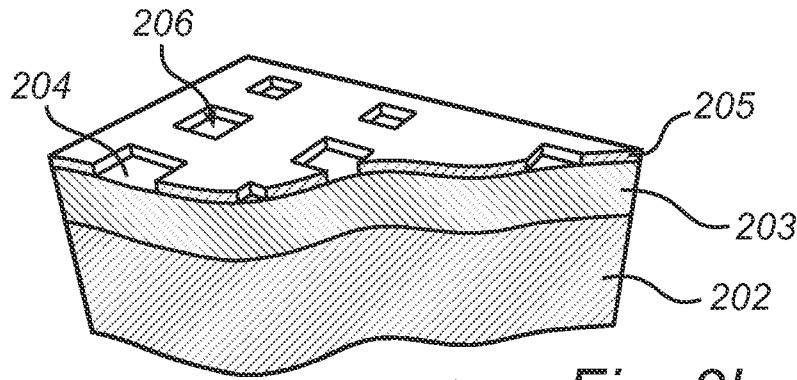


Fig. 3b

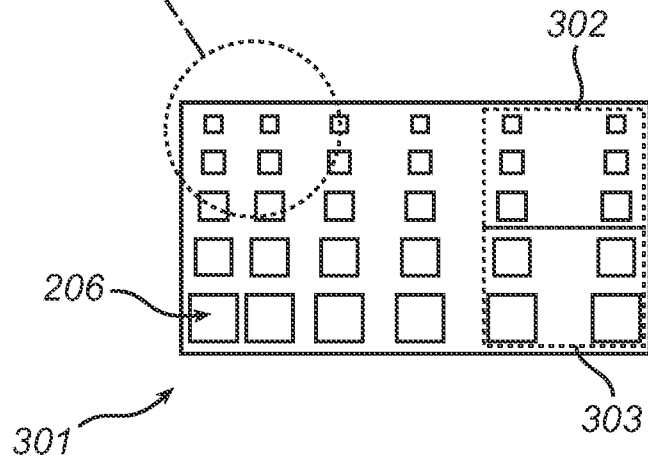


Fig. 3a

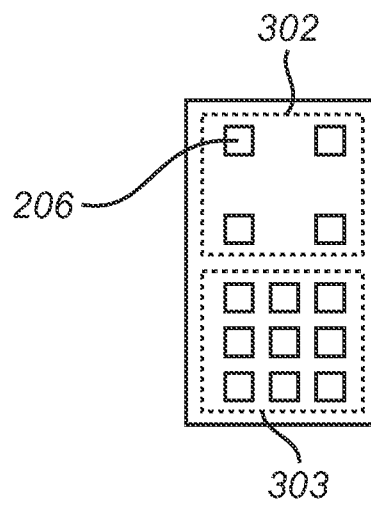
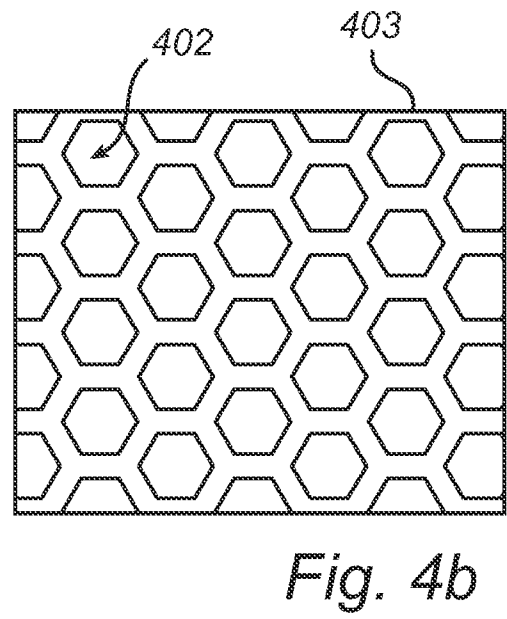
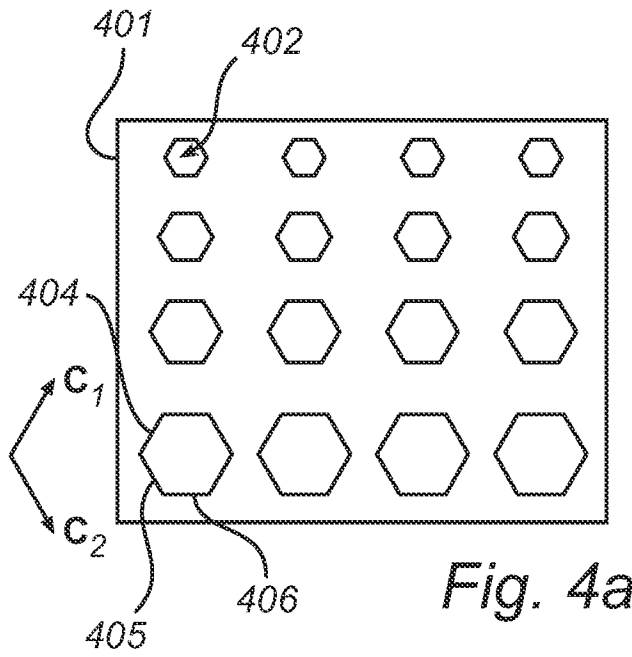


Fig. 3c



INTERNATIONAL SEARCH REPORT

International application No PCT/IB2011/054680

A. CLASSIFICATION OF SUBJECT MATTER INV. H01L33/24 H01L33/08 H01L21/02 ADD.				
According to International Patent Classification (IPC) or to both national classification and IPC				
B. FIELDS SEARCHED				
Minimum documentation searched (classification system followed by classification symbols) H01L				
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched				
Electronic data base consulted during the international search (name of data base and, where practical, search terms used) EPO-Internal				
C. DOCUMENTS CONSIDERED TO BE RELEVANT				
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.		
X	US 2008/149946 A1 (KIM JAMES C [US] ET AL) 26 June 2008 (2008-06-26) cited in the application	1,3-9, 11-15		
Y	abstract paragraphs [0005], [0030], [0035], [0037], [0039] - [0044], [0050] - [0056] figures claims 1,4,5	2,10		
Y	----- US 2010/148147 A1 (BOUR DAVID P [US] ET AL) 17 June 2010 (2010-06-17)	2,10		
A	the whole document	1,9		
A	----- US 2008/012030 A1 (YOON SANG HO [KR] ET AL) 17 January 2008 (2008-01-17) abstract paragraphs [0006], [0043] - [0045] figure 7 -----	1,3-7,9, 11-15		
<input type="checkbox"/> Further documents are listed in the continuation of Box C. <input checked="" type="checkbox"/> See patent family annex.				
* Special categories of cited documents : <table style="width: 100%; border: none;"> <tr> <td style="width: 50%; border: none; vertical-align: top;"> "A" document defining the general state of the art which is not considered to be of particular relevance "E" earlier document but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed </td> <td style="width: 50%; border: none; vertical-align: top;"> "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art. "&" document member of the same patent family </td> </tr> </table>			"A" document defining the general state of the art which is not considered to be of particular relevance "E" earlier document but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed	"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art. "&" document member of the same patent family
"A" document defining the general state of the art which is not considered to be of particular relevance "E" earlier document but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed	"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art. "&" document member of the same patent family			
Date of the actual completion of the international search	Date of mailing of the international search report			
17 February 2012	24/02/2012			
Name and mailing address of the ISA/ European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Authorized officer Gijsbertsen, Hans			

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Information on patent family members

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