May 6, 1969 F. R. BRADLEY 3,443,206

COMPENSATION CIRCUITS FOR VOLTAGE DIVIDERS

Filed July 5, 1966 Sheet 1 of 4

FIG. 1

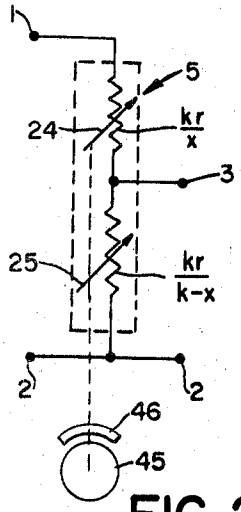


FIG. 2

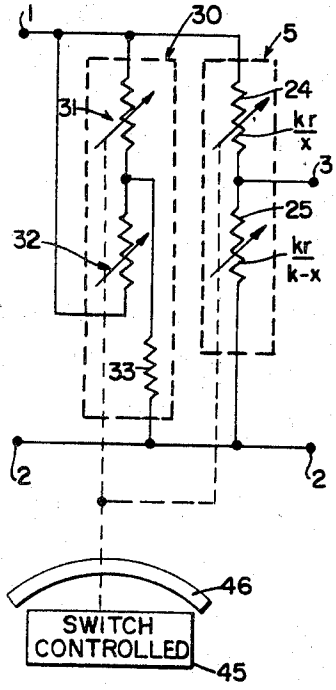
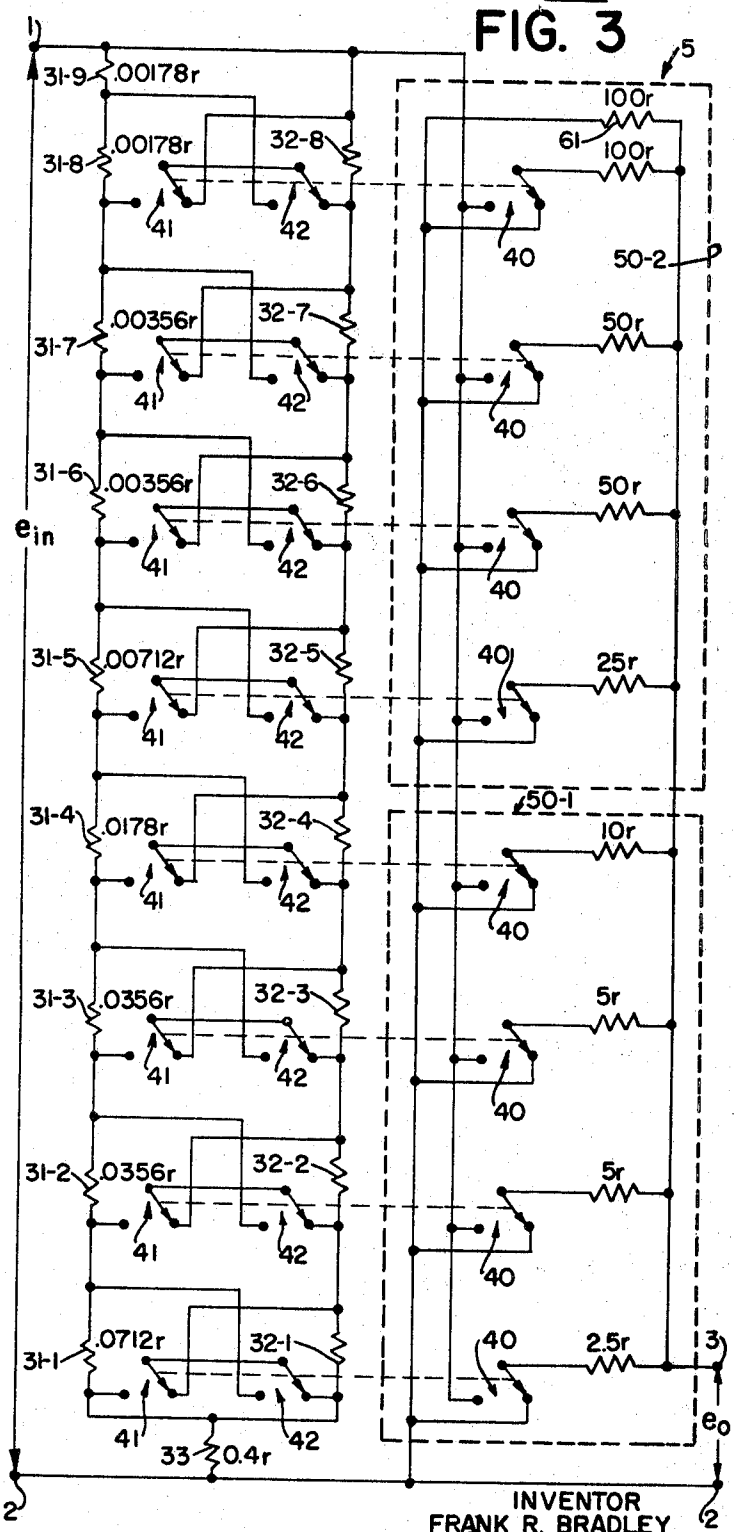
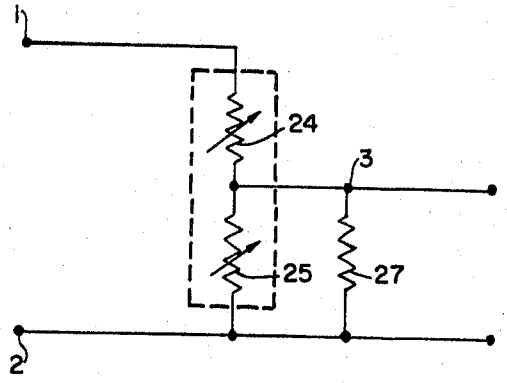


FIG. 3



INVENTOR
FRANK R. BRADLEY
BY Darby & Darby
ATTORNEYS

FIG. 4



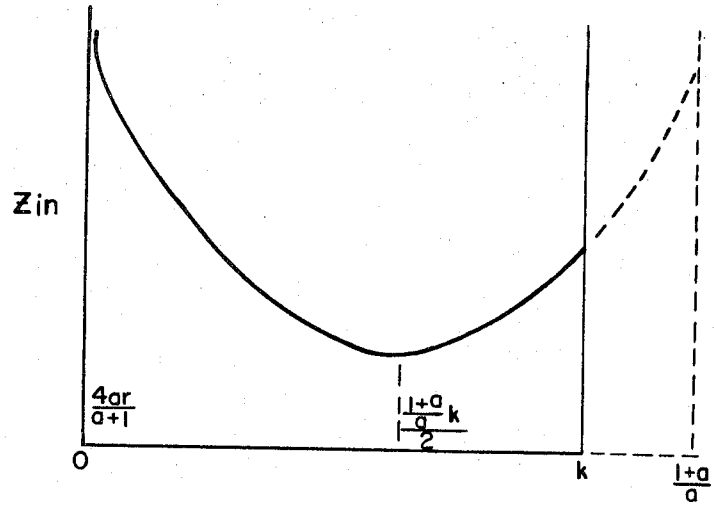
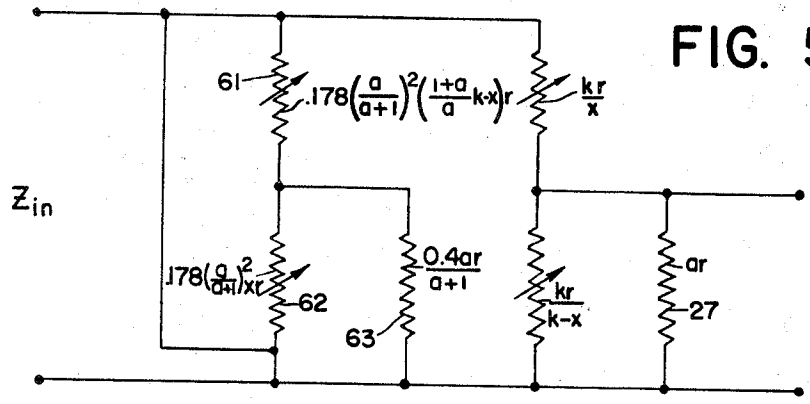


FIG. 4A

FIG. 5



INVENTOR
FRANK R. BRADLEY

BY Berry & Berry

ATTORNEYS

May 6, 1969 F. R. BRADLEY 3,443,206

COMPENSATION CIRCUITS FOR VOLTAGE DIVIDERS

Filed July 5, 1966 Sheet 3 of 4

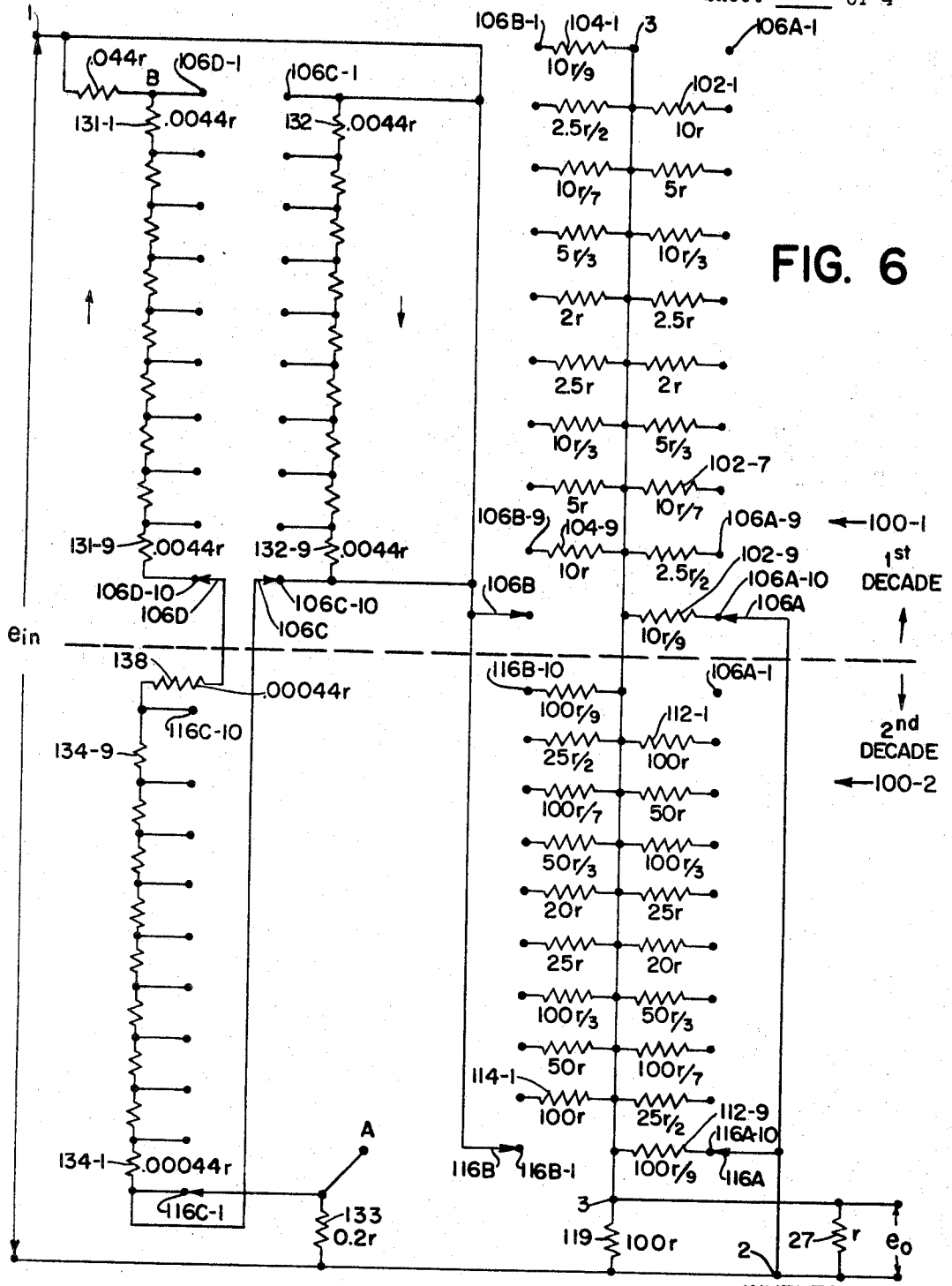


FIG. 6

INVENTOR
FRANK R. BRADLEY

BY Cushman, Darby & Cushman

ATTORNEYS

May 6, 1969 F. R. BRADLEY 3,443,206

COMPENSATION CIRCUITS FOR VOLTAGE DIVIDERS

Filed July 1966 Sheet 4 of 4

FIG. 7

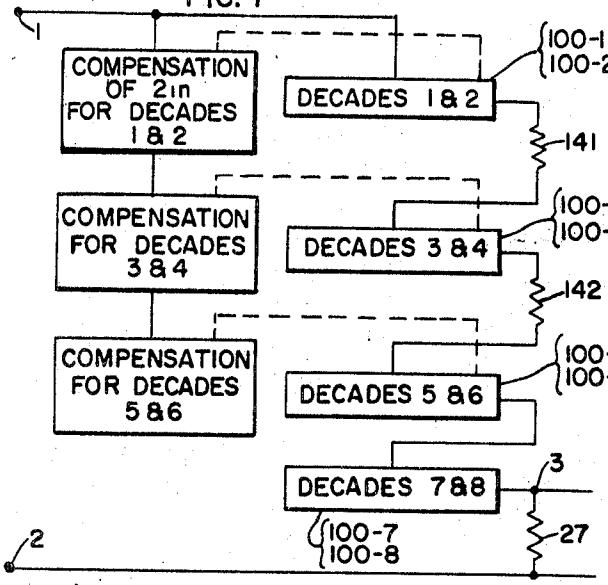


FIG. 10

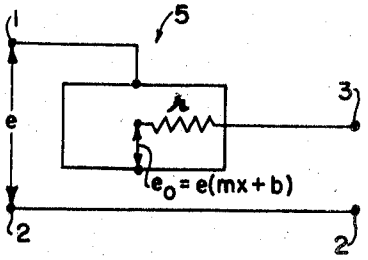


FIG. 8

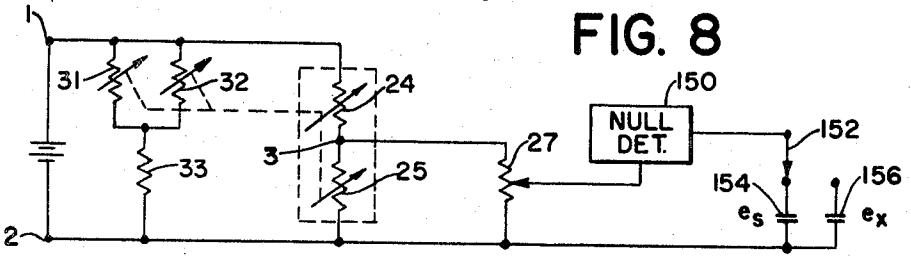
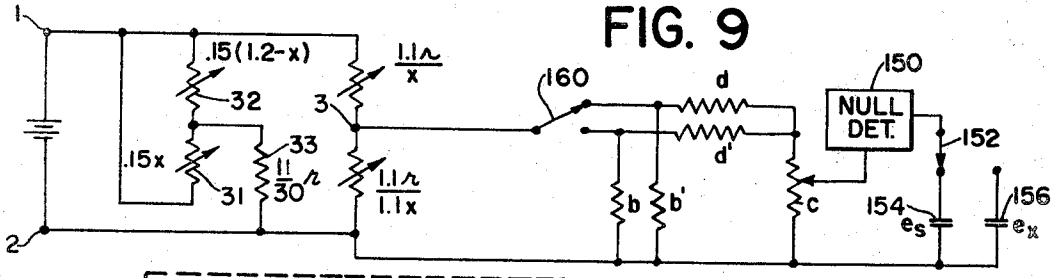


FIG. 9



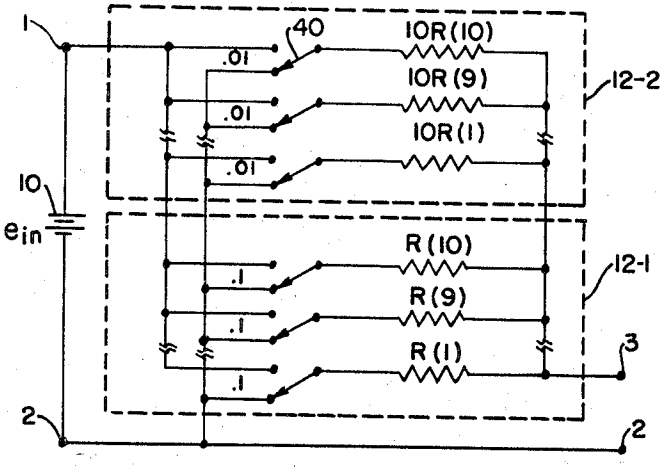


FIG. 11

INVENTOR
FRANK R. BRADLEY
BY Clarke, Clarke
ATTORNEYS

United States Patent Office 3,443,206
Patented May 6, 1969

3,443,206

COMPENSATION CIRCUITS FOR VOLTAGE DIVIDERS

Frank R. Bradley, 9 Dash Place,
Bronx, N.Y. 10463

Filed July 5, 1966, Ser. No. 562,846
Int. Cl. H02m 3/04, 5/06; H02p 13/00
U.S. Cl. 323—74 26 Claims

ABSTRACT OF THE DISCLOSURE

Compensating circuits for voltage dividers of the conductance type for maintaining the input impedance of the divider within a given range over the operating range of division ratios of the divider. Scaling circuits for the output of the divider which maintain a constant output impedance are also disclosed.

This invention relates to voltage dividers and more particularly to compensation circuits for voltage conductance dividers of the constant source impedance type.

There exists a class of voltage dividers known as conductance dividers of the constant source impedance type. These dividers produce a linearly varying output voltage in accordance with the divider ratio setting and a constant source impedance, that is, the output impedance of the divider remains constant, over the range of its voltage division ratios.

While the output impedance of this type of divider remains constant, the input impedance varies over the range of division ratios. This is tolerable in many situations but a number of applications exist where it is desirable to hold the divider input impedance as constant as possible over the complete range of division ratios. One such application exists in a potentiometer measuring instrument where it is desirable to increase allowable battery source impedance.

In accordance with the present invention, novel compensating circuits are provided for voltage dividers of the conductance type. These circuits are effective in maintaining the input impedance of the divider within a tolerable range of variation over the full operating range of division ratios of the divider. In the preferred embodiment of the invention the compensating circuits are additional impedances operated by, or concurrently with, the switching arrangement of the divider used for changing its division ratio. The additional impedances are connected in the compensating circuit to maintain a predetermined relationship to the voltage division ratio.

It is therefore an object of the present invention to provide circuits for reducing the input impedance variation of voltage dividers of the conductance type.

Another object is to provide input impedance compensating circuits in which the compensation circuitry is operated by the same controls which set the division ratio.

A further object is to provide input impedance compensation circuits as above for constant source impedance dividers in which additional impedances are connected in shunt with the divider output.

A further object of this invention is to provide a constant input-constant output impedance divider in combination with "permissible combination" scale switching for potentiometer application.

Other objects and advantages of the present invention will become more apparent upon reference to the following specification and annexed drawings, in which:

FIG. 1 is a schematic diagram of an unloaded constant source impedance divider;

FIG. 2 is a schematic of the voltage divider of FIG. 1 with an input impedance compensation circuit in accordance with the present invention;

FIG. 3 is a schematic diagram of a two decade divider utilizing the compensating circuit principles of FIG. 2 and showing the switching arrangement;

FIG. 4 is a schematic diagram representing a loaded constant source impedance divider;

FIG. 4A is a graph which shows the input impedance variation for a loaded divider;

FIG. 5 is a schematic diagram of the voltage divider of FIG. 4 with an input impedance compensation circuit in accordance with the present invention;

FIG. 6 is a schematic diagram of a two decade divider utilizing the compensating circuit principles of FIG. 5 and showing the switching arrangement;

FIG. 7 is a block diagram representation of a multiple decade divider with multiple compensation circuits;

FIG. 8 is a schematic diagram of a constant source impedance divider with input impedance compensating circuits used in a potentiometer;

FIG. 9 is a schematic diagram of a constant source impedance voltage divider used in a potentiometer with both voltage scaling and input impedance compensating circuits;

FIG. 10 is a schematic diagram illustrating the principles of the constant source impedance divider; and

FIG. 11 is a schematic diagram of one form of constant source impedance divider.

FIG. 10 illustrates the general principles of the type of conductance (constant source impedance) voltage divider **5** used with the present invention. The divider is a three (four) terminal network and has a pair of input terminals **1** and **2**, the latter terminal **2** being common and serving as one of a pair of output terminals **2** and **3**. Divider **5** is constructed with one or more fixed or variable impedances, such as resistors, therein which can be adjusted and/or interconnected by any suitable means (not shown in FIG. 10) in a manner such that when the impedances of the divider are set by a switching arrangement to produce any particular voltage division ratio x between the input and output terminals, and a voltage e is applied to input terminals **1** and **2**, the output voltage e_o across output terminals **2** and **3** varies as a linear function of e given by:

$$e_o = e(mx+b) \quad (1)$$

Here, m is the slope of a straight line function and b is the zero intercept on the abscissa of a Cartesian coordinate $(x-y)$ graph. Both m and x are determined by the divider component values and their interconnection. The intercept b is normally (but not necessarily) made equal to zero in potentiometer devices.

The divider **5** is also constructed so that the voltage e_o of Equation 1 has a fixed source impedance r looking into terminals **2** and **3** for any ratio setting x of the divider. The value of the source impedance r of the divider is also determined by its design. Another way of describing the characteristics of the divider **5** is that when input terminals **1** and **2** are shorted, the impedance measured between output terminals **2** and **3** or terminals **1** and **3** is constant and equal to r, independent of the ratio setting x. Many types of suitable dividers having these characteristics are currently in use including those commonly called conductance dividers.

FIG. 11 shows one type of constant source impedance divider constructed according to FIG. 10, and using a plurality of resistors for producing a decimally weighted output. The divider input terminals **1** and **2** are connected across a source **10** of input voltage e_{in}. A separate single pole, double throw switch **40** is provided for each resistor and the upper contact of each switch is connected to divider input terminal **1** while the lower contact is

connected to input terminal 2. The center arm of each switch has a resistor connected thereto and one end of each of these resistors is connected to common summing point terminal 3.

Depending upon the setting of its respective switch 40, an impedance is either connected in series between terminals 1 and 2 or across terminals 2 and 3 of the divider. It is understood that these switches 40 may be multiply-controlled by a decade or other switching means such as a rotary switch type, for example, which is wired to simultaneously connect any selected number of the resistors in a decade to either terminal 1 or 2, for example, connect the first five resistors of a decade to terminal 1 and the other resistors to terminal 2. Each decade of the divider preferably has its own switch. The decade switching arrangement is represented diagrammatically in FIG. 10. In FIG. 1, one switch 45 is shown symbolically for all of the decade switches operating adjacent a scale 46 which is preferably linearly calibrated in accordance with Equation 1. Preferably, in all embodiments of the invention each of the switches 40 or their decade operating switches, is of the conventional break-before-make type so that one connection is broken when a resistor is being switched to avoid shorting out the power supply. In all of the embodiments of the invention described below, the controls, scale, and break-before-make switches are preferably used, although not specifically described. It also should be understood that while x, the division ratio of the divider, varies between zero and one, that the scale 46 can be calibrated differently, for example, a scale of from 0 to 1.1.

The divider of FIG. 11 illustratively is to produce one hundred and ten steps of one unit each. To do this, two decades 12–1 and 12–2 are used. The first decade 12–1 includes 10 divider resistors of value R, designated R(1) through R(10), one end of each of which is connected to the movable contact arm of a respective switch 40. The second decade 12–2 has ten resistors each of value 10R, designated 10R(1) through 10R(10), one end of each of which is also connected to a respective switch 40. The ratio of e_o to e_{in} of the divider of FIG. 9 is:

$$\frac{e_o}{e_{in}}=\frac{n}{110} \tag{2}$$

where $0 \leq n \leq 110$ and n is the number of switch "weightings" for those switches 40 returned to the high side (up-position) terminal 1 of the divider. The "weighting" is shown adjacent each switch 40. It should be clear that each resistor of value R contributes a weighting of 10 parts (.1) of the 110 available while each resistor of value 10R contributes 1 part (.01). By selectively operating switches 40 the value of e_o can be selected in steps of e_{in} 110. For example, where e_o is to be 87/110 of e_{in}, resistors R(1) through R(8) and 10R(1) through 10R(7) eacht has its respective switch 40 connected to the high side terminal 1.

The number of output voltage steps available from a divider of the type shown in FIG. 11 can be increased by adding other decades of proportionately higher value resistors, or by adding other decades of the same or lower value resistors and a resistor in series in the line to the summing terminal 3. All of these techniques are conventional in the art.

FIGURE 1 shows a constant source impedance divider in generalized form with the resistor 24 corresponding to the total value of the resistors connected between terminals 1 and 3. Resistor 25 corresponds to the total value of the resistors connected between terminals 2 and 3. The value of resistor 24 is designated by the generalized formula kr/x while the value of resistor 25 is designated as

$$\frac{kr}{k-x}$$

where r is the source impedance of the divider 5, x is the division ratio set in to the divider, and k is the multiplier factor of the full scale ratio of the divider, a function of dial scale 46, and is any real number.

With divider 5 of FIG. 1 unloaded at terminals 2 and 3, its input impedance looking into terminals is

$$Z_{in}=\frac{kr}{x}+\frac{kr}{k-x}=\frac{k^2r}{x(k-x)} \tag{3}$$

An unloaded divider is defined more specifically as one in which there are no impedances, such as resistors, returned from divider summing terminal 3 to either of the other terminals 1 or 2 other than the conductance-weighted switch-programmed resistors of the divider itself.

Using Equation 3, it can be shown that for the full range of variation of x from zero to k in an unloaded divider that Z_{in} varies as a hyperbolic function with asymptotes at zero and k. The minimum value of Z_{in} occurs at $k/2$ and is equal to $4r$.

It should be understood that the variation of Z_{in} effects the impedance that a voltage source connected across terminals 1 and 2 sees as the divider scale ratio is changed. This is undesirable if the voltage across the divider should remain fixed and if the source impedance of the voltage is not zero.

FIG. 2 shows in generalized schematic form one type of compensation network connected in shunt with input terminals 1 and 2, which can be used to make the input impedance Z_{in} substantially constant, within reasonable limits, over the entire dividing ratio range x of the divider. The divider 5 is again drawn in generalized form with the resistors 24 and 25. Here, a compensating network 30 formed by resistors 31, 32 and 33 is connected across input terminals 1 and 2. Resistors 31 and 32 are connected in series with the upper end of resistor 31 connected to terminal 1, together with the lower end of resistor 32. Resistor 33 is connected between the junction of resistors 31 and 32 and divider terminal 2. The purpose of resistors 31, 32 and 33 is to produce an approximating function which will counteract the variation of Z_{in}.

Resistors 31 and 32 are preferably linearly variable resistors whose values are preferably controlled by the divider switching circuits, so that as the ratio x is changed, the values of both resistors 31 and 32 are changed simultaneously. To illustrate the switch 45, which represents all of the switching for the divider and compensating circuits, is shown ganged to operate both divider 5 and the resistors 31 and 32 of the compensating circuit 30. A predetermined relationship is maintained between the value of x and these compensating resistors 31 and 32, as is described below in greater detail. The value of resistor 33 remains fixed over the complete range of x and it has a predetermined relationship to the source impedance r.

It has been found that the variation of the input impedance Z_{in} can be reduced to an acceptable amount over the complete range of x by making resistor 31 equal to approximately $0.178r(k-x)$ and resistors 32 equal to approximately $0.178rx$. The value of fixed resistor 33 is preferably made approximately $.4r$. In any constant source impedance divider the value of r is constant and is determined by the divider design, while x is programmed in a known manner by the switches connecting the internal divider impedances between either of terminals 1 or 2. The values of resistors 31, 32 and 33 are selected as a result of determining the input impedance of the divider with the compensating network of FIG. 2 and optimizing these values to smooth the combined Z_{in} curve from 0 to k for the various settings of x made available by the switch program.

Using the compensating network of FIG. 2 for various divider settings of x with the values for resistors 31, 32 and 33 given above, the following table can be constructed

giving the input impedance as a function of r in terms of the setting x:

TABLE 1

Value of kx:	Z_{in}
0	.4000r
0.05	.4007r
.1	.4010r
.15	.4011r
.2	.4010r
.25	.4008r
.3	.4006r
.35	.4004r
.4	.4002r
.45	.4001r
.5	.4000r

the values are symmetrical about .5 and repeat.

It can be seen that by using the compensation arrangement of FIG. 2 that Z_{in} no longer varies over an infinite range but is now held over a nominal $\pm\frac{1}{8}\%$ above .4r. This obviously is a marked reduction in input impedance variation using a constant source divider and the relative stability of Z_{in} permits instruments using the divider to be constructed taking this into effect and enabling higher accuracy results to be obtained. Values other than those previously given for resistors **31**, **32** and **33** can be used but it is believed that those given result in a relatively good error curve fit to restrict the input impedance variation to within a tolerable range.

FIGURE 3 is a schematic diagram showing the details of one form of an input impedance compensated constant source impedance divider compensated in accordance with the arrangement of FIG. 2. The same reference numerals are used where applicable as in FIGS. 1 and 2. While only a two decade divider is shown, it should be understood that the switching circuit arrangement of FIG. 3 can be extended to a greater number of decades. Each of the two divider decades **50–1** and **50–2** has four resistors and their respective switches **40** for connecting these resistors between either pair of terminals **1** and **3**, or **2** and **3**. A resistor **61** of value 100r is shunted across terminals **2** and **3** of the divider. The respective value of each resistor in a decade is shown adjacent together with the weighting of each of the respective switches **40**. It should be noted that the values of the resistors in decade **50–2** are ten times greater that the corresponding resistors of decade **50–1**. The divider of FIGURE 3 has a range of k from .00 to .99 in steps of .01 in accordance with the setting of the switches **40**.

Each of the switches **40** of divider **5** has a respective two-deck, single-pole, double-throw switch mechanically ganged to it. The switch decks are labelled **41** and **42**. Two separate chains of series connected resistors **31–1** through **31–9** and **32–1** through **32–8** are connected from divider terminal **1** to the upper end of fixed value resistor **33**. The lower end of the latter resistor is connected to divider terminal **2**. It should be clear that the total series resistance value of resistors **31–1** through **31–9** correspond to the value of resistor **31** of FIG. 2, while the total series resistance value of resistors **32–1** through **32–8** corresponds to the value of resistor **32** of FIG. 2.

Each pair of switch decks **41** and **42** ganged to a respective divider switch **40** controls a corresponding pair of resistors **31** and **32** to alternately short out one of the resistors of the pair and place the other resistor in the compensating circuit. For example, when the upper resistor of decade **50–2** has its switch **40** set to terminal **2**, as shown, the ganged switches **41** and **42** are thrown to their right-hand contacts, as shown. This shorts out resistor **32–8**, leaving resistor **31–8** in the compensating circuit. With the same switch **40** connected to divider terminal **1** and the ganged switches **41** and **42** to the left, resistor **32–8** is in the compensating circuit and resistor **31–8** is shorted out. Each of the switches **40** controls one pair of resistors **31** and **32** in a similar manner.

With the circuit of FIG. 3, it can be shown that whatever the setting of the various divider switches **40** to produce a given division ratio x, that the total series resistance values of each chain of resistors **31** and **32** varies as a function of x and maintains a predetermined relationship thereto. Using the values shown adjacent each resistor **31** and **32** of FIG. 3, this variation is such that the value of the chain of resistors **31** is always $0.178r(k-x)$ and that of the chain of resistors **32** is $0.178r(x)$. Here, $k=1.0$. Thus, the advantageous results of the compensating circuit of FIG. 2 are achieved so that the divider of FIG. 3 has a constant output impedance and, within the limits of the approximating function produced by resistors **31**, **32** and **33**, constant input impedance. This, of course is a desirable result since the voltage at the divider input terminals remains substantially constant.

In one use, such as disclosed in my copending application Ser. No. 546,822, filed May 2, 1966 entitled "Potentiometer Devices," a divider of the constant source impedance type such as the divider **5** of FIGS. 1–3, and 5–11 disclosed herein, is used in a potentiometer circuit. In this use a load is connected across terminals **2** and **3**, which terminals in a potentiometer device also provide one input to a null detector or to a voltage scaling circuit as described in my copending application Ser. No. 546,846, filed May 2, 1966 entitled "Scaling Circuits for Voltage Dividers." Such an arrangement is shown in FIG. 4 where the load resistor is designated **27** and has a value ar, where a is any positive number.

It is shown in FIG. 4A that the input impedance Z_{in} of the loaded divider of FIG. 4 over the complete range of the division ratio x from zero to k is also hyperbolic in form. The input impedance curve has an asymptote at zero and another asymptote at

$$\frac{1+a}{a}k$$

The divider scale however, does not reach a value

$$\frac{1+a}{a}k$$

The minimum Z_{in} is at

$$\frac{\frac{1+a}{a}k}{2} \text{ and is } \frac{4ar}{a+1}$$

The Z_{in} of the loaded divider of FIG. 4 can be compensated by a network connected in shunt with input terminals **1** and **2** in much the same manner as the compensation arrangement of FIG. 3. This is shown in FIG. 5. Here, the compensating resistors **61**, **62** and **63** of linearly varying value correspond to resistors **31**, **32** and **33** of FIG. 3. The preferred values of these resistors are as follows:

$$61 - .178\left(\frac{a}{a+1}\right)^2\left(\frac{1+a}{a}k-x\right)r - \text{variable}$$

$$62 - .178\left(\frac{a}{a+1}\right)^2 xr \quad - \text{variable}$$

$$63 - \frac{0.4ar}{a+1} \quad - \text{fixed}$$

Using the above values for resistors **61**, **62** and **63**, the range of Z_{in} variation is reduced to tolerable limits similar to those of the divider of FIG. 3. The compensated input impedance curve is much the same as that produced with the values of Table 1 above but with an expansion along the horizonal scale. Here, the lowest value of Z_{in} is

$$\frac{.4ar}{a+1}$$

for k equal to zero, increasing to a maximum of

$$\frac{.401ar}{a+1}$$

The curve is symmetrical about the point

$$\frac{\frac{1+a}{a}k}{2}$$

Thus, the compensated divider of FIG. 5 also has a constant output impedance with an input impedance which is relatively constant within the range established by the compensating network.

From the foregoing description of the loaded divider case, it should be understood that the unloaded divider of FIGS. 1–3 is a special case of the loaded divider where the value of ar is very high, or infinite.

FIGURE 6 shows a two-decade loaded divider compensated in accordance with the arrangement of FIG. 5. Here, $a=1$ so that the value of load resistor **27** is r and k goes from 00 to 1.0. The divider portion of upper decade **100–1** is formed by first and second sets of resistors **102** and **104**. There are nine resistors in each set, with each resistor of both sets having one end directly connected to divider terminal **3**. The other end of each resistor **102** terminates at a respective stationary contact of deck A of a four-deck ten-position switch **106**. Similarly, the other end of each resistor **104** terminates at a respective stationary contact of deck B of switch **106**.

The movable contacts of the switch decks **106A** to **106D** are ganged to move together. For the sake of clarity, the usual dashed lines indicating this are omitted in FIG. 6. For each setting of switch **106**, one resistor **102** is connected between divider terminals **2** and **3** by switch deck **106A** and one resistor **104** between divider terminals **1** and **3** by switch deck **106B**. The values of the resistors **102** and **104** are selected to produce the desired voltage division ratio and the constant source impedance r at any setting of switch **106**. A typical set of values for these resistors is shown in FIG. 6.

The second decade **100–2** of the divider is constructed like the first decade. Here, two sets each of nine resistors **112** and **114** are used, which correspond to resistors **102** and **104** of decade **100–1**, and a three-deck ten-position ganged switch **116**, corresponding to switch **106**. The movable contact of switch **116A** operates to place a pair of resistors **112** and **114** between terminals **2** and **3** and **1** and **3**, respectively. One typical set of values for these resistors is shown in FIG. 6. A scaling resistor **119** is connected across terminals **2** and **3**.

The two decade divider of FIG. 6 operates in the same manner as the divider of FIG. 9, with the switching circuit and resistor connections being somewhat different, to produce any desired division ratio x in steps of .01 unit. The compensating circuit includes first and second sets each of nine serially connected resistors **131** and **132** whose connection into the compensating circuit is controlled by the respective decks C and D of switch **106**, which are ganged for operation with switch decks **106A** and **106B**. Resistors **131** are wired with the upper end of resistor **131–1** connected to stationary contact **106D–1** and the junction of each successively higher numbered pair of series connected resistors connected to the next higher numbered contact of switch decks **106D**. The lower end of the last resistor **131–9** is connected to contact **106D–10**. The upper end of the resistor **131–1** is connected to switch contact **106D–1** and through a fixed value resistor **136** to divider terminal **1**. A similar arrangement is used for resistors **132** which are connected into the compensating circuit by switch deck **106C**. The upper end of resistor **132–1** is connected only to switch contact **106C–1**.

The movable contact of switch deck **106D** is connected to the upper end of the fixed value compensating resistor **133**, through a fixed value resistor **138** and a set of nine series connected resistors **134–1** through **134–9**. The lower end of resistor **133** is connected to divider terminal **2** while movable switch arm **106C** of the upper decade is connected to the lower end of resistor **134–1**. Resistors **134** are selectively connected into the compensating circuit by a third deck (C) of second decade switch **116** whose movable contact is mechanically ganged to the movable contacts of decks **116A** and **116B**. The movable, center arm of second decade switch deck **116C** is connected directly to the upper end of fixed value compensating resistor **133**.

The value of compensating resistance corresponding to resistor **31** of FIG. 5 for any setting of first decade switch **106** and second decade switch **116**, includes fixed value resistor **136**, those of resistors **131** in series between resistor **136** and movable switch contact **106D**, fixed value resistor **138** and those of resistors **134** above the movable contact arm of second decade switch deck **116C**. Similarly, the value of compensating resistance corresponding to resistor **32** includes those resistors **132** connected in series above the contact where the movable contact of first decade switch deck **106C** is positioned and those resistors below the movable arm of switch **116C**.

In the condition shown in FIG. 6 with maximum divider ratio setting, the value of the resistance corresponding to resistor **31** is maximum and that corresponding to resistor **32** is minimum. As the divider ratio setting decreases, that is either or both switches **106** and **116** are moved upwardly in FIG. 6, the values of the two variable compensating resistors change in accordance with the error correction curve established by the compensation network. This is the same action obtained with the different type of switching circuit of the divider of FIG. 3. A typical set of values for the resistors are shown to produce the desired compensation of $.044x$ and $.044(2-x)$, since the divider output is loaded. It should be noted that the divider of FIG. 6 is decimally coded as contrasted to the binary coded decimal divider of FIG. 3.

It should be understood that many compensating circuit arrangements are possible using the concept of controlling the compensating impedances by the ratio switches of the basic divider. Also, improvements in the fit of the compensating impedance curve to make the divider input impedance more nearly constant may be obtained by making the mmultiplying factor (e.g. $.4r$ or

$$\left(\frac{0.4ar}{a+1}\right)$$

of the fixed resistor variable or by non-linearizing the values of the other two compensating resistors of the divider's most significant decade and thus drawing an n segment fit to the Z_{in} curves of the dividers of FIGS. 2 and 4, where n is the number of steps in the most significant decade. The latter means that at various steps in the divider ratio setting, for example those which produce the larger input impedance variations about a certain level, the normal multiplying factors or resistors **31** or **131** and **32** or **132** are departed from to make Z_{in} deviate less.

An improvement in the constancy of Z_{in} can also be realized by making the compensating circuits more sophisticated. For example, connecting a resistor of value $.017r$ between points A and B of the divider of FIG. 6 gives a slight improvement (about 15%) in the input impedance constancy.

In the construction of certain types of constant source impedance dividers, such as multi-section or rescaled dividers, scaling resistors are sometimes used after the first few decades to avoid the necessity of using resistors of very high values in the least significant decades. For example, in the case where the divider resistors of the most significant decade are of a value $10r$, at the sixth decade the resistors would have to be in the order of 10^6r in a binary coded decimal or decimally coded divider. Resistors of the higher magnitudes are, of course,

more expensive to produce. In such cases to achieve Z_{in} compensation, multiple versions of the compensating circuit are preferably used if the rescaled resistors, those in the lesser significant decades, are not of sufficiently high value to have an insignificant effect on the input impedance.

FIG. 7 shows a multi-section compensated divider with scaling resistors in block diagram form. A scaling resistor **141** is connected between the summing point, corresponding to divider terminal **3**, of the first two pairs of divider decades **100–1**, **100–2** and **100–3**, **100–4**. Similarly, a scaling resistor **142** is connected between decades **100–3**, **100–4** and **100–5**, **100–6** while summing points of connected decades **100–5**, **100–6** and **100–7**, **100–8** are connected directly together.

Each of the first three pairs of decades **100–1**, **100–2**; **100–3**, **100–4**; and **100–5**, **100–6** has its own compensating circuit which is independently controlled by the corresponding divider switches of the respective decade pair. This is shown by the dotted line indicating the ganging of the switches. The switching for the compensating circuits can be any suitable configuration, such as those previously described. Decades **100–7** and **100–8**, the least significant, may be left uncompensated if the values of their resistors are relatively high, and thus do not seriously affect Z_{in}, due to the absence of a scaling resistor between the last two pairs of decades. Of course, in accordance with the invention, a single compensating circuit can be constructed to operate with any number of decades, for example one, two, three or four. Two decade compensating circuits only are described since they illustrate all the principles of this type of arrangement.

The compensated divider of FIGS. 5 and 6 lends itself particularly well to a potentiometer application, as is shown in FIG. 8. Here, the load resistor **27** always sees a constant source impedance r and Z_{in} varies only over the range permitted by the compensating circuit **31**, **32**, **33**, thus raising the permissible level of battery (and associated lead) source impedance. A null detector **150** receives one input through a switch **152** from either a standard reference source **154** of known voltage e_s for an unknown voltage e_x from a source **156**. The other input is the voltage tapped off from load resistor **27**. The center arm of resistor **27** is used to normalize the potentiometer to the reference voltage e_s. For a detailed explanation of the operation of the potentiometer devices, reference is made to my aforesaid copending applications.

The compensating circuit heretofore discussed for FIGS. 5, 6 and 8, made use of a load resistor **27** connected between the summing terminal **3** of the divider and the low side terminal **2**. An analysis of the Z_{in} deviation for loads returned to the high side terminal **1** from terminal **3**, or for loads returned to both terminals **1** and **3**, shows that the compensating scheme may be extended.

The compensating circuits of FIGS. 5, 6 and 8 also permit construction of a potentiometer in which load resistance **27** of value ar is a constant input impedance network with a stepwise variable attenuator for scaling or ranging. Such a circuit is shown in FIG. 9, and reference is made to the latter of my aforesaid copending applications for a more detailed explanation of the scaling circuit shown in FIG. 9 and other scaling circuits.

In FIG. 9, the resistors of the compensating network **31**, **32**, **33** have values somewhat different from those previously considered but the principle of operation is similar. For the divider shown, $k=1.1$. The output voltage of the divider is applied through a switch **160** to one of two sets of ranging resistors, the first set comprising resistors b, d and c and the second set resistors b', d' and c. The load impedance presented to the divider by the first set is:

$$\frac{b(d+c)}{b+d+c}$$

and of the second set:

$$\frac{b'(d'+c)}{b'+d'+c}$$

Each set of resistors forms a load resistor for the divider. By making the values of the first and second sets equal, load resistance ar is the same for both settings of switch **160**. At the same time the values of resistors b, b' and c, c' can be chosen, while still making ar constant, so that a desired scaling of the output voltage across resistor c, which is potentiometrically tapped for the normalization adjustment of the potentiometer, can be produced with the two settings of switch **160**. Of course, any number of sets of scaling resistors can be used to produce a number of scaling steps.

The compensated divider and potentiometer circuits of the present invention also can be used in scaling circuits in which so-called "permissible combinations" of resistors are used for scaling. This is also described in my aforesaid co-pending application S.N. 546,846. It is known that a matched set of n resistors of average value R, where n has factors a_1, a_2 . . . a_k, can be connected in k series, parallel and series-parallel combinations to synthesize resistance values ranging from R/n (all resistors in parallel) to Rn (all resistors in series) where the individual values of the combinations thus synthesized are correct relative to each other within an error which is less than the sum of the squares of the deviation of individual resistors from the arithmetic mean value resistor R_M. This error compensation and relative value prevails as long as theoretically equal current flows through each of the n resistors of the set and as long as leakage and differential lead resistance effects are negligible. Such a connection of the resistors in a set to satisfy these requirements is herein called a "permissible combination." The error theory for the resistor sets is described in the National Bureau of Standards Circular 470 entitled "Precision Resistors and Their Measurement," issued Oct. 8, 1948, by the United States Government Printing Office.

Referring back now to FIG. 9, a circuit is described in which certain of the scaling resistors b, b', d and d' are formed by a "permissible combination" of resistors. Consider here that the combination comprises four resistors which can be connected into any series ar series-parallel, or parallel combination by any conventional switching circuit (not shown) and that 4:1 range switching is desired by switch **160**.

To begin the analysis, consider that $d'=16d$. Since, for example, d' and d can be the shunt and series connections respectively of four resistors of value $4d$, the ratio 16 is established with great accuracy. For 4 to 1 ranging:

$$\frac{c}{d+c}=\frac{4c}{16d+c}$$

and, therefore, $c=4d$.

This means that resistor c is equal to a series-parallel "permissible combination" of the four $4d$ resistors and therefore may be inter-compared to this combination with great accuracy using substitution methods.

For a constant load ar on the divider

$$\frac{b(d+c)}{b+d+c}=\frac{b'(d'+c)}{b'+d'+c}$$

Since $c=4d$ and $d'=16r$.

Therefore,

$$\frac{b(d+4d)}{b+d+4d}=\frac{b'(16d+4d)}{b'+16d+3d}$$

Choosing $b'=d$, makes $b=d/4$.

Since

$$\frac{b(d+c)}{b+d+c}=ar$$

if we make $a=5/21$, then $d=r$.

In summary, to produce 4 to 1 ranging $b=r/4$, $c=4r$, $d=r$, $b'=r$, $d'=16r$. Resistors d and d' each is one permissible combination of four resistors of value $4d$ in series or in parallel, resistor c, b' and the divider source impedance r are equal to a permissible combination value of the four $4d$ resistors and may be intercompared by substitution methods. Resistor b is adjusted by observing the voltage at the divider arm while range switching and adjusting b so that there is no change in this voltage.

Values of range switching other than 4 to 1 are equally feasible. For example the following set of values results in a 10 to 1 range change with the d and d' resistor remaining in the ratio 16 to 1—

$$d=r,\ b=2r/3,\ c=2r/3,\ b'=500r/1020,\ d'=16r$$

It should again be noted that two of the resistors of the scaling circuit, d and d' in this case, are both equal to a permissible combination of the same set of resistors.

While the preferred embodiments of the invention have been described above, it will be understood that these are illustrative only, and the invention is limited solely by the appended claims.

What is claimed is:

1. The combination comprising a variable voltage divider having an input and an output and a plurality of impedance means, means for connecting said divider input to a source of voltage, said voltage divider including switching means for linearly varying its voltage division ratio by changing the relationships of the impedance means of said divider to produce a correspondingly varying output voltage at said output and a substantially constant output impedance of a known value at said output irrespective of the relationships of the divider impedance means, and means connected to said voltage divider for compensating the impedance looking into said input by holding it within a predetermined range as the voltage division ratio of the divider is changed.

2. The combination of claim **1** wherein said compensating means comprises a plurality of impedances which are interconnected to produce linearly varying impedance elements corresponding to change in the division ratio of the divider.

3. The combination of claim **1** wherein said compensating means comprises a plurality of impedance means, means interconnecting said impedance means to form a number of impedance elements the value of at least one of which varies non-linearly corresponding to a change in the division ratio of the divider.

4. The combination of claim **1** further comprising means connecting said switching means to said compensating means for operating said compensating means as the voltage division ratio of the divider is changed.

5. The combination of claim **4** wherein said voltage divider has a pair of input terminals and a pair of output terminals, and said compensating means is connected across said input terminals.

6. The combination of claim **5** wherein said compensating means comprises first and second networks of impedances and a fixed value impedance, means connecting said first and second networks in series and the unconnected ends thereof to one of the input terminals and means connecting one end of the fixed value impedance to the junction of said first and second networks and the other end to the other input terminal.

7. The combination of claim **6** wherein the values of said first and second impedance networks vary linearly as the division ratio of the divider is changed.

8. The combination of claim **6** wherein the value of at least one of said first and second impedance networks varies in a non-linear manner as the division ratio of the divider is changed.

9. The combination of claim **6** wherein the impedances of said first and second networks are interconnected by said switching means to maintain an impedance of about

$$.178\left(\frac{a}{a+1}\right)^2 xr$$

for one of said networks and about

$$.178\left(\frac{a}{a+1}\right)^2\left(\frac{1+a}{a}k-x\right)r$$

for the other of said networks as the division ratio is changed for a divider with a load across its output terminals, where x is the division ratio of the divider, k is the divider operating scale factor, r is the value of the divider constant output impedance and a is a constant multiplied with r to determine the value of the load on the divider output terminals.

10. The combination of claim **9** wherein the value of said fixed impedance is about

$$\frac{0.4ar}{a+1}$$

11. The combination of claim **6** wherein the impedances of said first and second networks are interconnected by said switching means to maintain an impedance of about $0.178rx$ for one of said networks and about $0.178r(k-x)$ for the other of said networks as the division ratio is changed for a divider having a high impedance load across its output terminals, where x is the division ratio of the divider, k is the divider operating scale factor, and r is the value of the divider constant output impedance.

12. The divider of claim **1** further comprising a plurality of scaling impedance means connected to the divider output for scaling its output voltage, means connected to said scaling impedance means for selecting a set thereof to produce a desired scaling factor, the impedance presented to the divider of each selectable set of impedances being substantially the same.

13. The combination of claim **12** wherein each set of impedances comprises a plurality of resistor means at least one of said resistor means of one set of impedances comprising a plurality of resistors connected as a "permissible combination."

14. The combination of claim **13** wherein one of the resistor means of the other set of impedance means also is formed as a "permissible combination" of said plurality of resistors.

15. The divider of claim **4** further comprising a plurality of scaling impedance means connected to the divider output for scaling its output voltage, means connected to said scaling impedance means for selecting a set thereof to produce a desired scaling factor, the impedance presented to the divider of each selectable set of impedances being substantially the same.

16. The combination of claim **15** wherein each set of impedances comprises a plurality of resistor means at least one of said resistor means of one set of impedances comprising a plurality of resistors connected as a "permissible combination."

17. The combination of claim **16** wherein one of the resistor means of the other set of impedance means also is formed as a "permissible combination" of said plurality of resistors.

18. The divider of claim **6** further comprising a plurality of scaling impedance means connected to the divider output for scaling its output voltage, means connected to said scaling impedance means for selecting a set thereof to produce a desired scaling factor, the impedance presented to the divider of each selectable set of impedances being substantially the same.

19. The combination of claim **18** wherein each set of impedances comprises a plurality of resistor means at least one of said resistor means comprising a plurality of resistors connected as a "permissible combination."

20. The combination of claim **19** wherein one of the resistor means of the other set of impedance means also

is formed as a "permissible combination" of said plurality of resistors.

21. The combination of claim 14 in which at least one impedance element other than that formed by the set of impedances connected in a "permissible combination" is equal to a "permissible combination" of said set.

22. The combination of claim 17 in which at least one impedance element other than that formed by the set of impedances connected in a "permissible combination" is equal to a "permissible combination" of said set.

23. The combination of claim 20 in which at least one impedance element other than that formed by the set of impedances connected in a "permissible combination" is equal to a "permissible combination" of said set.

24. A circuit for scaling the voltage from a source comprising first and second sets of resistor means, means for connecting one of said sets to the voltage source to produce an output voltage for the set across one of the resistor means in accordance with the values of the respective resistor means forming the set, one of said resistor means of said one set formed by a first plurality of resistors each of a given value connected in a "permissible combination" and one of the resistor means of the other set also formed by a "permissible combination" of a second plurality of resistors having the same given value as the resistors of said first plurality.

25. The combination of claim 24 wherein at least one resistor means of a set other than a resistor means formed by a "permissible combination" of a plurality of resistors is equal in value to a "permissible combination" of the said plurality of resistors.

26. A circuit for scaling the voltage from a source comprising first and second sets of resistor means, means for connecting one of said sets to the voltage source to produce an output voltage for the set across one of the resistor means in accordance with the values of the respective resistor means forming the set, one of said resistor means of one set formed by a plurality of resistors each of a given value connected in a "permissible" combination," and another resistor means of said one set other than (a) the one resistor means formed by a "permissible combination" of a plurality of resistors is equal in value to a "permissible combination" of said plurality of resistors of said one resistor means of said one set.

References Cited

UNITED STATES PATENTS

2,999,202	9/1961	Ule	323—74
3,238,443	3/1966	Julie	324—98 X
3,305,769	2/1967	Julie	323—74
3,315,152	4/1967	Lindley	323—74
2,184,104	12/1939	Smith	323—79
2,536,501	1/1951	Hood et al.	333—81

JOHN F. COUCH, *Primary Examiner.*

G. GOLDBERG, *Assistant Examiner.*

U.S. Cl. X.R.

323—79, 94; 333—81