(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
20 April 2017 (20.04.2017)

WIPO | PCT

(10) International Publication Number
WO 2017/066309 A1

(51) International Patent Classification:
H01L 49/02 (2006.01) *H01L 21/768* (2006.01)
H01L 27/24 (2006.01)

(21) International Application Number:
PCT/US2016/056621

(22) International Filing Date:
12 October 2016 (12.10.2016)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
62/240,277 12 October 2015 (12.10.2015) US
15/288,594 7 October 2016 (07.10.2016) US

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

(54) Title: STRUCTURE AND METHOD OF FABRICATING THREE-DIMENSIONAL (3D) METAL-INSULATOR-METAL (MIM) CAPACITOR AND RESISTOR IN SEMI-ADDITIVE PLATING METAL WIRING

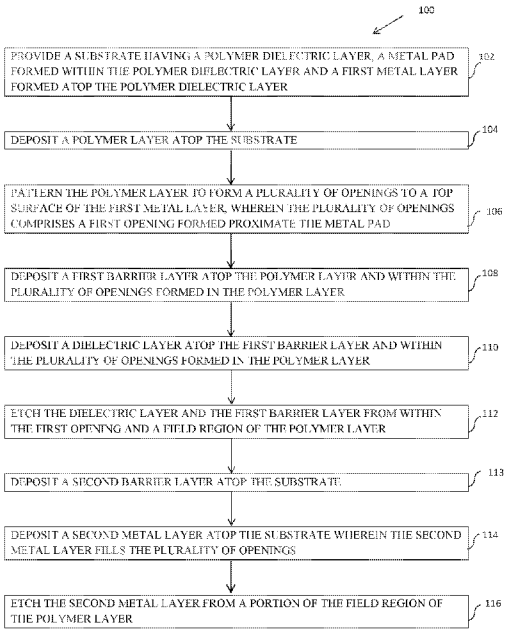

FIGURE 1

(57) Abstract: Methods of processing a substrate include: providing a substrate having a polymer dielectric layer, a metal pad formed within the polymer dielectric layer and a first metal layer formed atop the polymer dielectric layer; depositing a polymer layer atop the substrate; patterning the polymer layer to form a plurality of openings, wherein the plurality of openings comprises a first opening formed proximate the metal pad; depositing a first barrier layer atop the polymer layer; depositing a dielectric layer atop the first barrier layer; etching the dielectric layer and the first barrier layer from within the first opening and a field region of the polymer layer; depositing a second barrier layer atop the substrate; depositing a second metal layer atop the substrate wherein the second metal layer fills the plurality of openings; and etching the second metal layer from a portion of the field region of the polymer layer.

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STRUCTURE AND METHOD OF FABRICATING THREE-DIMENSIONAL (3D) METAL-INSULATOR-METAL (MIM) CAPACITOR AND RESISTOR IN SEMI-ADDITIVE PLATING METAL WIRING

FIELD

[0001] Embodiments of the present disclosure generally relate to three-dimensional metal-insulator-metal ("3D MIM") capacitors and resistors in integrated circuits.

BACKGROUND

[0002] A semiconductor memory device generally comprises a plurality of memory cells which are used to store a large quantity of information. Each memory cell includes a capacitor for storing electric charge and a corresponding field effect transistor for opening and closing charging and discharging passages of the capacitor. As the size of semiconductor devices continues to shrink, the area occupied by each component of a semiconductor device should be decreased. Capacitors are one component that can occupy considerable area on a semiconductor die depending on the size of the capacitor and/or the number of capacitors on the die.

[0003] One example of a capacitor used in a semiconductor memory device is a metal-insulator-metal (MIM) capacitor. A traditional MIM capacitor is two-dimensional (2D). A 2D MIM capacitor has two facing metal plates which are planar and substantially parallel to each other and to the substrate. One method of increasing the capacitance of a MIM capacitor is to increase the sizes of the metal plates. However, increasing the sizes of the metal plates will consume more surface area of the substrate. Accordingly, a need exists to reduce the surface area on the substrate occupied by a capacitor without sacrificing the capacitance.

[0004] Accordingly, the inventors have developed an improved 3-dimensional metal-insulator-metal (3D MIM) capacitor and method of forming a 3D MIM capacitor.

SUMMARY

[0005] Methods for processing a substrate are provided herein. In some embodiments, a method of processing a substrate includes: providing a substrate having a polymer dielectric layer, a metal pad formed within the polymer dielectric layer and a first metal layer formed atop the polymer dielectric layer; depositing a polymer layer atop the substrate; patterning the polymer layer to form a plurality of openings to a top surface of the first metal layer, wherein the plurality of openings comprises a first opening formed proximate the metal pad; depositing a first barrier layer atop the polymer layer and within the plurality of openings formed in the polymer layer; depositing a dielectric layer atop the first barrier layer and within the plurality of openings formed in the polymer layer; etching the dielectric layer and the first barrier layer from within the first opening and a field region of the polymer layer; depositing a second barrier layer atop the substrate; depositing a second metal layer atop the substrate wherein the second metal layer fills the plurality of openings; and etching the second metal layer from a portion of the field region of the polymer layer.

[0006] In some embodiments, a method of processing a substrate, includes: providing a substrate having a patterned polymer dielectric layer comprising a plurality of openings; depositing a first barrier layer atop the substrate; depositing a dielectric layer atop the first barrier layer; depositing a second barrier layer atop the dielectric layer; and depositing a metal pad atop a portion of a field region of the patterned polymer dielectric layer.

[0007] A substrate includes: a polymer dielectric layer; a metal pad filling an opening in the polymer dielectric layer; a patterned first metal layer atop the polymer dielectric layer and conductively coupled to the metal pad; a polymer layer atop the substrate, wherein the polymer layer comprises a plurality of openings etched to a top surface of the patterned first metal layer, wherein the plurality of openings comprises a first opening formed proximate the metal pad; a barrier layer atop the polymer layer and within the plurality of openings in the polymer layer; a dielectric layer atop the barrier layer and within the plurality of openings in the polymer layer; a second barrier layer atop the substrate; and a second metal layer atop the substrate wherein the second metal layer fills the plurality of openings, and wherein the barrier

layer, the dielectric layer and the second metal layer are not formed atop a portion of a field region of the substrate.

[0008] Other and further embodiments of the present disclosure are described below.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] Embodiments of the present disclosure, briefly summarized above and discussed in greater detail below, can be understood by reference to the illustrative embodiments of the disclosure depicted in the appended drawings. However, the appended drawings illustrate only typical embodiments of the disclosure and are therefore not to be considered limiting of scope, for the disclosure may admit to other equally effective embodiments.

[0010] Figure 1 depicts a flow chart of a method for processing a substrate in accordance with some embodiments of the present disclosure.

[0011] Figures 2A-G depict the stages of processing a substrate in accordance with some embodiments of the present disclosure.

[0012] Figures 3A-3G depict embodiments of forming a 3-dimensional resistor in accordance with some embodiments of the present disclosure.

[0013] Figure 4 depicts a flow chart of a method for processing a substrate in accordance with some embodiments of the present disclosure.

[0014] Figure 5 depicts a flow chart of a method for processing a substrate in accordance with some embodiments of the present disclosure.

[0015] To facilitate understanding, identical reference numerals have been used, where possible, to designate identical elements that are common to the figures. The figures are not drawn to scale and may be simplified for clarity. Elements and features of one embodiment may be beneficially incorporated in other embodiments without further recitation.

DETAILED DESCRIPTION

[0016] Methods for processing a substrate are provided herein. The inventive methods advantageously facilitate an improved 3-dimensional (3D) metal-insulator-

metal (MIM) capacitor and method of forming a 3D MIM capacitor having reduced resistance, enhanced system performance of overall system (i.e. of die connection to pad), and enhanced surface area over the same footprint in view of traditional 2-dimensional MIM structures.

[0017] Figure 1 depicts a flow chart of a method 100 for processing a substrate in accordance with some embodiments of the present disclosure. The method 100 is described herein with respect to the structure depicted in Figures 2A-2G. The method 100 of the present disclosure may be performed in a single process chamber capable of performing both etching and deposition. Such a suitable process chamber may be a standalone process chamber, or part of a cluster tool. Alternatively, the inventive methods disclosed herein may be performed in separate chambers that also may be standalone or part of a cluster tool.

[0018] The method 100 generally begins at 102, as depicted in Figure 2A, by providing a substrate 200 having a polymer dielectric layer 202, a metal pad 206 formed within the polymer dielectric layer 202 and a first metal layer 204 formed atop the polymer dielectric layer 202. The metal pad 206 is formed within an opening 224 in the polymer dielectric layer 202. In some embodiments, the metal pad 206 fills the opening 224 to a top surface of the substrate 200. In some embodiments, a die 226 is optionally embedded in the substrate 200. The die can be any known suitable die material, such as silicon, used in wafer packaging. The substrate 200 may be any suitable substrate material used in semiconductor manufacturing processes. For example, the substrate 200 may be one of silicon, glass, ceramic, or dielectric. The polymer dielectric layer 202 may comprise any suitable polymer dielectric material such as polyimide or polybenzoxazole, or the like. The metal pad 206 and the first metal layer 204 may comprise any suitable conductive material used to form a metal interconnect such as copper (Cu), aluminum (Al), or the like. The first metal layer 204 is a redistribution layer (*i.e.* a layer to redirect connectivity to the pad) provided over the polymer dielectric layer 202. In some embodiments, the first metal layer 204 may be formed using a plating process or deposition process, such as a physical vapor deposition process, used in a semiconductor manufacturing processes.

[0019] Next at 104, and as depicted in Figure 2B, a polymer layer 208 is spin-coated over the substrate 200. The polymer layer 208 may be deposited using any suitable spin-coating process or lithographic process. In some embodiments, the polymer layer 208 is a polybenzoxazole (PBO) layer, a polyimide layer, a benzocyclobutene (BCB) layer, an epoxy layer, or a photo-sensitive material layer

[0020] Next, at 106, and as depicted in Figure 2C, the polymer layer 208 is patterned to form a plurality of openings 210. The plurality of openings 210 are formed to a top surface 216 of the first metal layer 204. The plurality of openings 210 comprises a first opening 218 formed proximate the metal pad 206. In some embodiments, the patterning process may be any suitable lithographic process for forming openings in the polymer layer 208. In some embodiments, the plurality of openings 210 may be a feature such as a via, a trench, or the like.

[0021] Next at 108, and as depicted in Figure 2D, a first barrier layer 212 is conformally deposited atop the substrate 200. The first barrier layer 212 is deposited atop, or directly atop, the polymer layer 208 and within the plurality of openings 210 formed in the polymer layer 208. The first barrier layer 212 is deposited atop the field region of the polymer layer 208 and along the sidewalls of the plurality of openings 210 and the bottom of the plurality of openings 210. The first barrier layer 212 may be deposited using any suitable deposition process, for example a physical vapor deposition process (PVD), a chemical vapor deposition process (CVD), an atomic layer deposition process (ALD), or the like. In some embodiments, the first barrier layer 212 is a conductive material, such as titanium (Ti) or titanium nitride (TiN).

[0022] Next, at 110, and as depicted in Figure 2D, a dielectric layer 214 is conformally deposited over the first barrier layer 212. The dielectric layer 214 is deposited atop, or directly atop, the first barrier layer 212 and within the plurality of openings 210 formed in the polymer layer 208. The dielectric layer 214 is deposited atop the field region of the first barrier layer 212 and along the sidewalls of the plurality of openings 210 and the bottom of the plurality of openings 210. The dielectric layer 214 may be deposited using any suitable deposition process, for example a physical vapor deposition process (PVD), a chemical vapor deposition

process (CVD), an atomic layer deposition process (ALD), or the like. In some embodiments, the dielectric layer 214 is a nitride film or a high-k dielectric material, such as hafnium oxide (HfO_2), silicon nitride (Si_3N_4), or tantalum oxide (Ta_2O_5).

[0023] Next, at 112, and as depicted in Figure 2E, the dielectric layer 214 and the first barrier layer 212 are etched from within the first opening 218 and from a field region 220 of the polymer layer 208. In some embodiments, the dielectric layer 214 and the first barrier layer 212 may be etched using a patterned photoresist layer (not shown). For example, a photoresist material can be deposited on the substrate 200 and then exposed to light filtered by a reticle, such as a glass plate that is patterned with exemplary feature geometries that block light from propagating through the reticle. After passing through the reticle, the light contacts the surface of the photoresist material and changes the chemical composition of the photoresist material such that a developer can remove a portion of the photoresist material. In the case of positive photoresist materials, the exposed regions are removed, and in the case of negative photoresist materials, the unexposed regions are removed. The photoresist layer may comprise any photoresist materials suitable to provide a template to facilitate etching the layers 212, 214 from within the first opening 218 and from a field region 220 of the polymer layer 208. For example, in some embodiments, the photoresist material may be a positive or negative photoresist and/or a DUV or EUV (deep ultraviolet or extreme ultraviolet) photoresist and may comprise one or more of polymers, organic compounds (e.g., comprising carbon, hydrogen and oxygen), an amorphous carbon, such as Advanced Patterning Film (APF), available from Applied Materials, Inc., located in Santa Clara, California, a tri-layer resist (e.g., a photoresist layer, a Si-rich anti-reflective coating (ARC) layer, and a carbon-rich ARC, or bottom ARC (BARC) layer), a spin-on hardmask (SOH), or the like. Thereafter, the layers 212, 214 are etched to remove the material from the areas that are no longer protected by the photoresist material. The photoresist material is then completely stripped from the substrate 200.

[0024] Next, at 113 and 114, and as depicted in Figure 2F, a second barrier layer 228 and a second metal layer 222, are deposited atop the substrate 200. The second barrier layer 228 is conformally deposited atop the substrate 200 and within the plurality of openings 210 formed in the polymer layer 208. The second barrier

layer 228 may be deposited using any suitable deposition process, for example a physical vapor deposition process (PVD), a chemical vapor deposition process (CVD), an atomic layer deposition process (ALD), or the like. In some embodiments, the second barrier layer 228 is a conductive material, such as titanium (Ti) or titanium nitride (TiN). The second metal layer 222 is deposited atop the substrate 200 and fills the plurality of openings 210. The second metal layer 222 may be deposited using any suitable deposition process, for example a electroplating process. The second metal layer 222 may comprise any suitable conductive material used to form a metal interconnect such as copper (Cu), aluminum (Al), or the like.

[0025] Next, at 116, and depicted in Figure 2G, the layers 212, 214, 228, 222 are etched from a portion of the field region 220 of the polymer layer 208. In some embodiments, the layers 212, 214, 228, 222 may be etched using a patterned photoresist layer (not shown) as described above. The photoresist layer may comprise any photoresist materials suitable to provide a template to facilitate etching the layers 212, 214, 228, 222. The layers 212, 214, 228, 222 are etched to remove the material from the areas that are no longer protected by the photoresist material. The photoresist material is then completely stripped from the substrate 200.

[0026] Figure 4 depicts a flow chart of a method 400 for processing a substrate in accordance with some embodiments of the present disclosure. The method 400 is described herein with respect to the structure depicted in Figures 3A-3C. The method 400 of the present disclosure may be performed in a single process chamber capable of performing both etching and deposition. Such a suitable process chamber may be a standalone process chamber, or part of a cluster tool. Alternatively, the inventive methods disclosed herein may be performed in separate chambers that also may be standalone or part of a cluster tool.

[0027] Figures 3A-3C depicts one embodiment of forming a 3-dimensional resistor in accordance with some embodiments of the present disclosure. The method 400 generally begins at 402, as depicted in Figure 3A by providing a substrate 300 having a patterned polymer dielectric layer 302 comprising a plurality of openings 304. In some embodiments, the substrate 300 may be any suitable substrate

material used in semiconductor manufacturing processes. For example, the substrate 300 may be one of silicon, glass, ceramic, or dielectric. The patterned polymer dielectric layer 302 may comprise any suitable polymer dielectric material such as polyimide or polybenzoxazole, or the like. In some embodiments, the patterned polymer dielectric layer 302 may be patterned using any suitable etch lithographic process, such as a plasma etching process, for forming openings in a polymer material.

[0028] Next, at 404, and as depicted in Figure 3B a first barrier layer 306 is deposited atop the substrate 300. The first barrier layer 306 is deposited atop the patterned polymer dielectric layer 302 and within the plurality of openings 304 formed in the patterned polymer dielectric layer 302. The first barrier layer 306 is deposited atop the field region of the patterned polymer dielectric layer 302 and along the sidewalls of the plurality of openings 304 and the bottom of the plurality of openings 304. The first barrier layer 306 may be deposited using any suitable deposition process, for example a physical vapor deposition process (PVD), a chemical vapor deposition process (CVD), an atomic layer deposition process (ALD), or the like. In some embodiments, the first barrier layer 306 is a conductive material, such as titanium (Ti) or titanium nitride (TiN).

[0029] Next, at 406, and as depicted in Figure 3C, a dielectric layer 308 is deposited over the first barrier layer 306. The dielectric layer 308 is deposited atop the first barrier layer 306 and within the plurality of openings 304 formed in the patterned polymer dielectric layer 302. The dielectric layer 308 may be deposited using any suitable deposition process, for example a physical vapor deposition process (PVD), a chemical vapor deposition process (CVD), an atomic layer deposition process (ALD), or the like. In some embodiments, the dielectric layer 308 is a nitride film or a high-k dielectric material, such as hafnium oxide (HfO_2), silicon nitride (Si_3N_4), tantalum oxide (Ta_2O_5).

[0030] Next, at 407, following deposition of the dielectric layer 308 a second barrier layer 318 is conformally deposited atop the substrate 200, for example directly atop the dielectric layer 308, and within the plurality of openings 210 formed in the polymer layer 208. The second barrier layer 318 may be deposited using any

suitable deposition process, for example a physical vapor deposition process (PVD), a chemical vapor deposition process (CVD), an atomic layer deposition process (ALD), or the like. In some embodiments, the second barrier layer is a conductive material, such as titanium (Ti) or titanium nitride (TiN). Next, the layers 306, 308, 318 are etched from a portion of the field region 314 of the patterned polymer dielectric layer 302. In some embodiments, the layers 306, 308, 318 may be etched using a patterned photoresist layer (not shown) as described above.

[0031] Next at 408, and as depicted in Figure 3C a metal pad 310 connection is formed atop a portion of the field region of the patterned polymer dielectric layer 302. The metal pad 310 may comprise any suitable conductive material used to form a metal interconnect such as copper (Cu).

[0032] Figure 5 depicts a flow chart of a method 500 for processing a substrate in accordance with some embodiments of the present disclosure. The method 500 is described herein with respect to the structure depicted in Figures 3D-3G. The method 500 of the present disclosure may be performed in a single process chamber capable of performing both etching and deposition. Such a suitable process chamber may be a standalone process chamber, or part of a cluster tool. Alternatively, the inventive methods disclosed herein may be performed in separate chambers that also may be standalone or part of a cluster tool.

[0033] Figures 3D-3G depict one embodiment of forming a 3-dimensional resistor in accordance with some embodiments of the present disclosure. The method 500 generally begins at 502, and as depicted in Figure 3D by providing a substrate 300 with a patterned metal layer 312. In some embodiments, the substrate 300 may be any suitable substrate material used in semiconductor manufacturing processes. For example, the substrate 300 may be one of silicon, glass, ceramic, or dielectric. In some embodiments, the patterned metal layer 312 may comprise any suitable conductive material used to form a metal interconnect such as copper (Cu).

[0034] Next, at 504, and as depicted in Figure 3E, a patterned polymer dielectric layer 302 comprising a plurality of openings 304 is formed atop the substrate 300. A portion of the plurality of openings 304 is formed atop the patterned metal layer 312 such that a portion of the plurality of openings 304 exposes a top surface of the

patterned metal layer 312. The patterned polymer dielectric layer 302 may comprise any suitable polymer dielectric material such as polyimide or polybenzoxazole, or the like. In some embodiments, the patterned polymer dielectric layer 302 may be patterned using any suitable etch lithographic process, such as a plasma etching process, for forming openings in a polymer material.

[0035] Next, at 506, and as depicted in Figure 3F a first barrier layer 306 is deposited atop the substrate 300. The first barrier layer 306 is deposited atop the patterned polymer dielectric layer 302 and within the plurality of openings 304 formed in the patterned polymer dielectric layer 302. The first barrier layer 306 is deposited atop the field region of the patterned polymer dielectric layer 302 and along the sidewalls of the plurality of openings 304 and the bottom of the plurality of openings 304. The first barrier layer 306 may be deposited using any suitable deposition process, for example a physical vapor deposition process (PVD), a chemical vapor deposition process (CVD), an atomic layer deposition process (ALD), or the like. In some embodiments, the first barrier layer 306 is a conductive material, such as titanium (Ti) or titanium nitride (TiN).

[0036] Next, at 508, and as depicted in Figure 3F, a dielectric layer 308 is deposited over the first barrier layer 306. The dielectric layer 308 is deposited atop the first barrier layer 306 and within the plurality of openings 304 formed in the patterned polymer dielectric layer 302. The dielectric layer 308 may be deposited using any suitable deposition process, for example a physical vapor deposition process (PVD), a chemical vapor deposition process (CVD), an atomic layer deposition process (ALD), or the like. In some embodiments, the dielectric layer 308 is a nitride film or a high-k dielectric material, such as hafnium oxide (HfO_2), silicon nitride (Si_3N_4), tantalum oxide (Ta_2O_5). The dielectric layer 308 and the first barrier layer 306 are then removed from within a first opening 316 of the patterned polymer dielectric layer 302. In some embodiments, the layers 306, 308, may be etched from within a first opening 316 of the patterned polymer dielectric layer 302 using a patterned photoresist layer (not shown) as described above.

[0037] Following deposition of the dielectric layer 308 a second barrier layer 318 is conformally deposited atop the substrate 200 and within the plurality of openings

304 formed in the patterned polymer dielectric layer 302. The second barrier layer 318 may be deposited using any suitable deposition process, for example a physical vapor deposition process (PVD), a chemical vapor deposition process (CVD), an atomic layer deposition process (ALD), or the like. In some embodiments, the second barrier layer is a conductive material, such as titanium (Ti) or titanium nitride (TiN). Next, the layers 306, 308, 318 are etched from within a first opening 316 of the patterned polymer dielectric layer 302 using a patterned photoresist layer (not shown) as described above.

[0038] Next at 510, and as depicted in Figure 3G, a metal pad 310 connection is formed to the patterned metal layer 312. The metal pad 310 is formed atop a portion of the field region of the patterned polymer dielectric layer 302. The metal pad 310 may comprise any suitable conductive material used to form a metal interconnect such as copper (Cu). The conductive material of the metal pad 310 is deposited within the first opening 316 of the patterned polymer dielectric layer 302 to fill the first opening 316.

[0039] While the foregoing is directed to embodiments of the present disclosure, other and further embodiments of the disclosure may be devised without departing from the basic scope thereof.

Claims:

1. A method of processing a substrate, comprising:

providing a substrate having a polymer dielectric layer, a metal pad formed within the polymer dielectric layer and a first metal layer formed atop the polymer dielectric layer;

depositing a polymer layer atop the substrate;

patterning the polymer layer to form a plurality of openings to a top surface of the first metal layer, wherein the plurality of openings comprises a first opening formed proximate the metal pad;

depositing a first barrier layer atop the polymer layer and within the plurality of openings formed in the polymer layer;

depositing a dielectric layer atop the first barrier layer and within the plurality of openings formed in the polymer layer;

etching the dielectric layer and the first barrier layer from within the first opening and a field region of the polymer layer;

depositing a second barrier layer atop the substrate;

depositing a second metal layer atop the substrate wherein the second metal layer fills the plurality of openings; and

etching the second metal layer from a portion of the field region of the polymer layer.

2. The method of claim 1, wherein the substrate is one of silicon, glass, ceramic, or dielectric.

3. The method of claim 1, wherein the metal pad is copper.

4. The method of any of claims 1 to 3, wherein at least one of the first metal layer or the second metal layer is a copper or aluminum layer.

5. The method of any of claims 1 to 3, wherein the polymer dielectric layer is polyimide or polybenzoxazole.

6. The method of any of claims 1 to 3, wherein the polymer layer is one of a polybenzoxazole (PBO) layer, a polyimide layer, a benzocyclobutene (BCB) layer, an epoxy layer, or a photo-sensitive material layer.

7. The method of any of claims 1 to 3, wherein the first barrier layer is titanium.

8. The method of any of claims 1 to 3, wherein the dielectric layer is hafnium oxide (HfO_2), silicon nitride (Si_3N_4), or tantalum oxide (Ta_2O_5).

9. A method of processing a substrate, comprising:

providing a substrate having a patterned polymer dielectric layer comprising a plurality of openings;

depositing a first barrier layer atop the substrate;

depositing a dielectric layer atop the first barrier layer;

depositing a second barrier layer atop the dielectric layer; and

depositing a metal pad atop a portion of a field region of the patterned polymer dielectric layer.

10. The method of claim 9, wherein at least one of:

the substrate is one of silicon, glass, ceramic, or dielectric;

the metal pad is copper;

the patterned polymer dielectric layer is one of a polybenzoxazole (PBO) layer, a polyimide layer, a benzocyclobutene (BCB) layer, an epoxy layer, or a photo-sensitive material layer;

wherein the first barrier layer is titanium; or

the dielectric layer is one of hafnium oxide (HfO_2), silicon nitride (Si_3N_4), tantalum oxide (Ta_2O_5).

11. A substrate, comprising:

a polymer dielectric layer;

a metal pad filling an opening in the polymer dielectric layer;

a patterned first metal layer atop the polymer dielectric layer and conductively coupled to the metal pad;

a polymer layer atop the substrate, wherein the polymer layer comprises a plurality of openings etched to a top surface of the patterned first metal layer, wherein the plurality of openings comprises a first opening formed proximate the metal pad;

a barrier layer atop the polymer layer and within the plurality of openings in the polymer layer;

a dielectric layer atop the barrier layer and within the plurality of openings in the polymer layer;

a second barrier layer atop the substrate; and

a second metal layer atop the substrate wherein the second metal layer fills the plurality of openings, and wherein the barrier layer, the dielectric layer and the second metal layer are not formed atop a portion of a field region of the substrate.

12. The substrate of claim 11, wherein the polymer dielectric layer is polyimide or polybenzoxazole.

13. The substrate of claim 11, wherein the polymer layer is one of a polybenzoxazole (PBO) layer, a polyimide layer, a benzocyclobutene (BCB) layer, an epoxy layer, or a photo-sensitive material layer.

14. The substrate of claim 11, wherein the second metal layer is a copper or aluminum layer.

15. The substrate of claim 11, wherein the dielectric layer is hafnium oxide (HfO_2), silicon nitride (Si_3N_4), or tantalum oxide (Ta_2O_5).

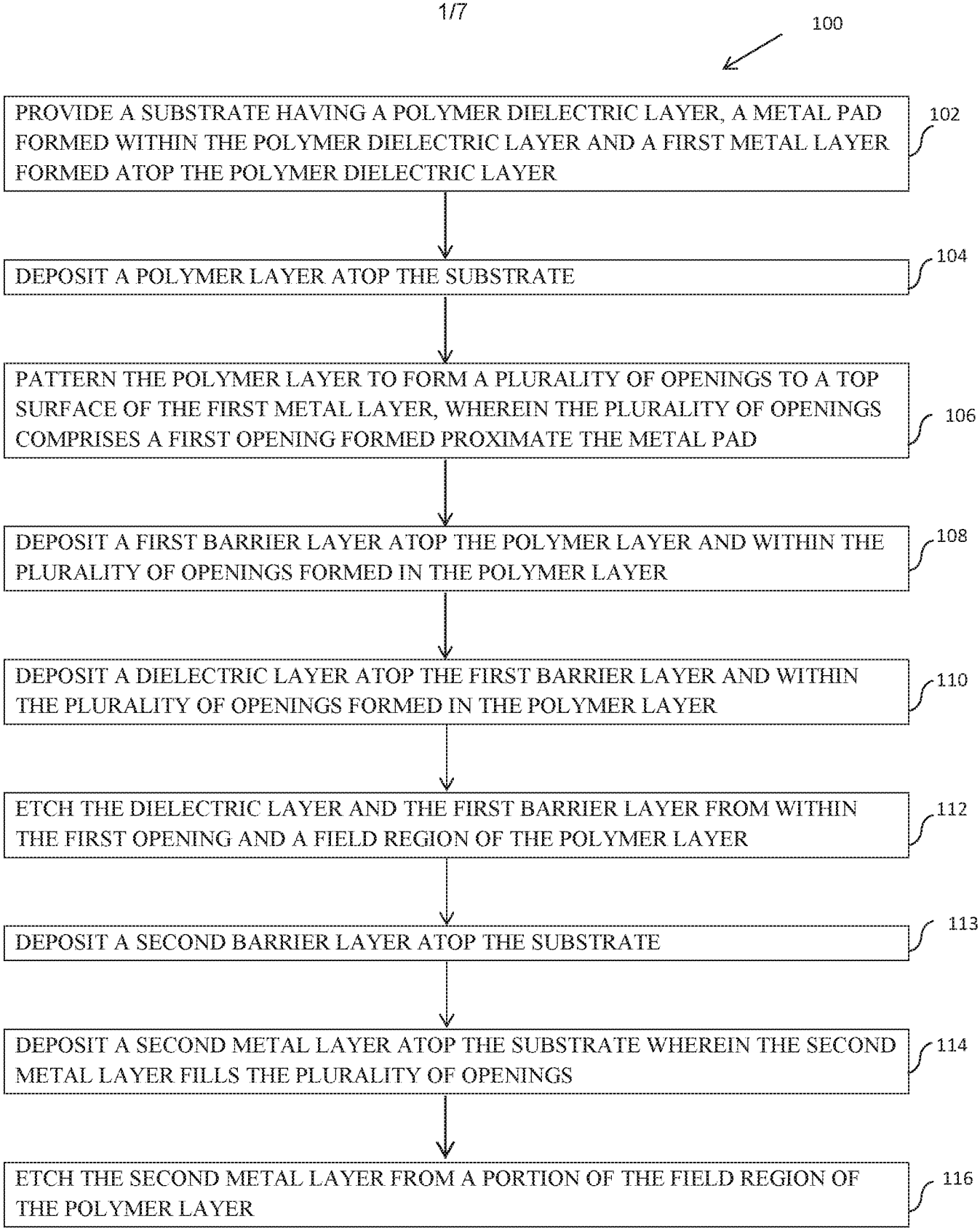
100
PROVIDE A SUBSTRATE HAVING A POLYMER DIELECTRIC LAYER, A METAL PAD FORMED WITHIN THE POLYMER DIELECTRIC LAYER AND A FIRST METAL LAYER FORMED ATOP THE POLYMER DIELECTRIC LAYER
102
DEPOSIT A POLYMER LAYER ATOP THE SUBSTRATE
104
PATTERN THE POLYMER LAYER TO FORM A PLURALITY OF OPENINGS TO A TOP SURFACE OF THE FIRST METAL LAYER, WHEREIN THE PLURALITY OF OPENINGS COMPRISES A FIRST OPENING FORMED PROXIMATE THE METAL PAD
106
DEPOSIT A FIRST BARRIER LAYER ATOP THE POLYMER LAYER AND WITHIN THE PLURALITY OF OPENINGS FORMED IN THE POLYMER LAYER
108
DEPOSIT A DIELECTRIC LAYER ATOP THE FIRST BARRIER LAYER AND WITHIN THE PLURALITY OF OPENINGS FORMED IN THE POLYMER LAYER
110
ETCH THE DIELECTRIC LAYER AND THE FIRST BARRIER LAYER FROM WITHIN THE FIRST OPENING AND A FIELD REGION OF THE POLYMER LAYER
112
DEPOSIT A SECOND BARRIER LAYER ATOP THE SUBSTRATE
113
DEPOSIT A SECOND METAL LAYER ATOP THE SUBSTRATE WHEREIN THE SECOND METAL LAYER FILLS THE PLURALITY OF OPENINGS
114
ETCH THE SECOND METAL LAYER FROM A PORTION OF THE FIELD REGION OF THE POLYMER LAYER
116

FIGURE 1

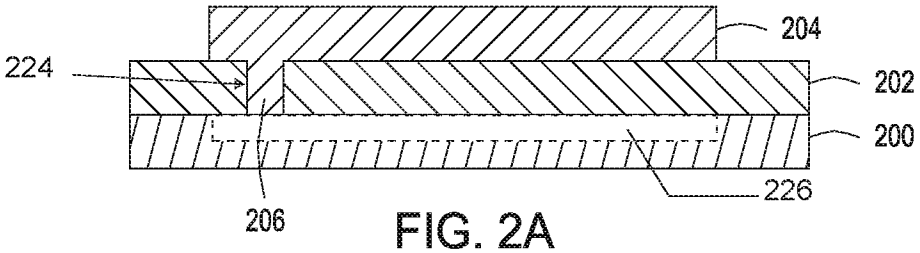

FIG. 2A

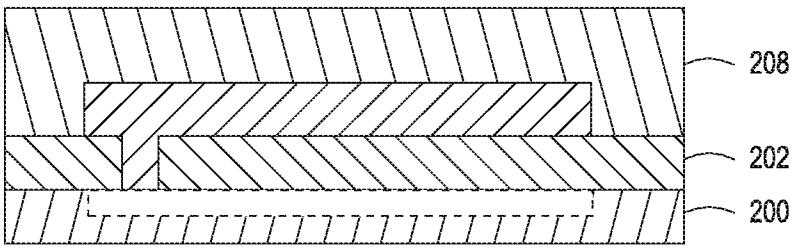

FIG. 2B

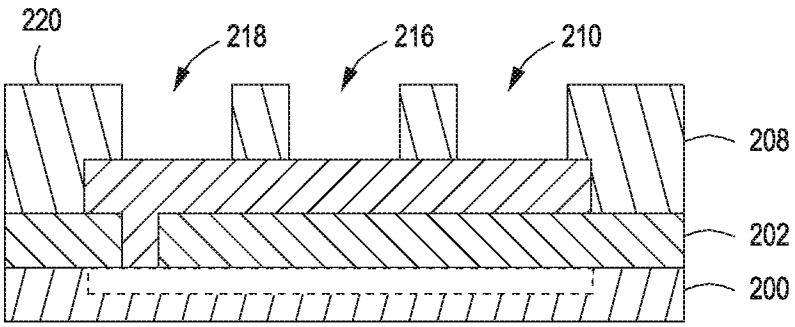

FIG. 2C

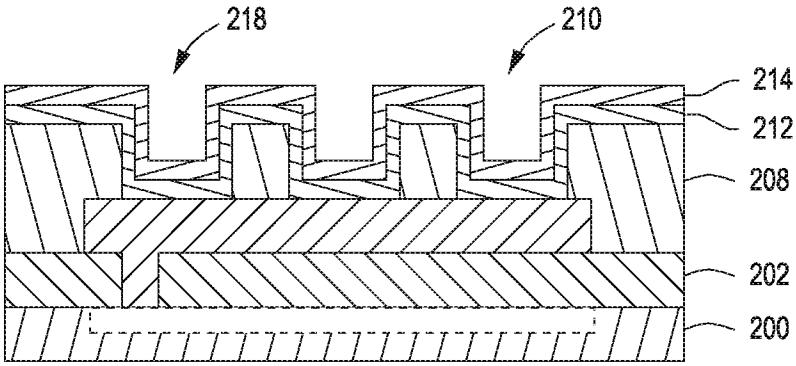

FIG. 2D

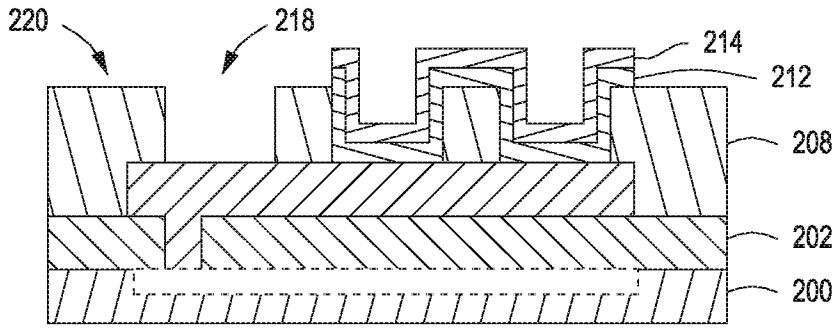

FIG. 2E

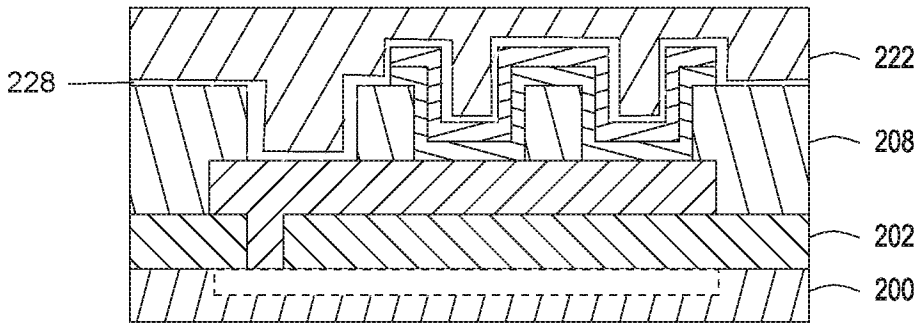

FIG. 2F

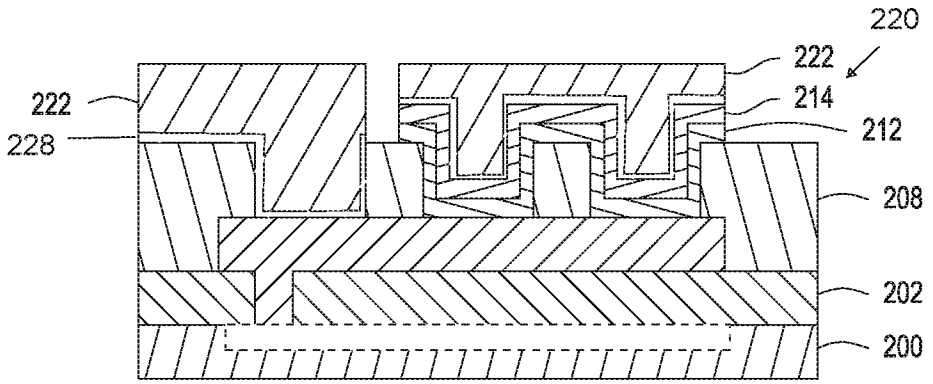

FIG. 2G

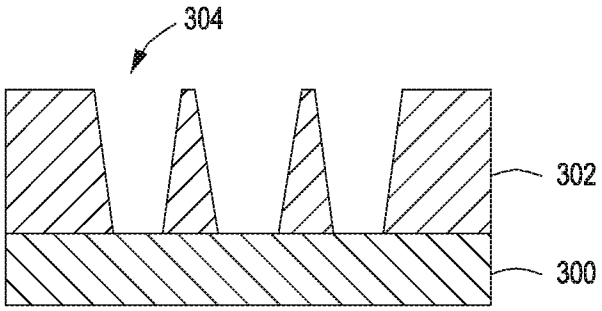

FIG. 3A

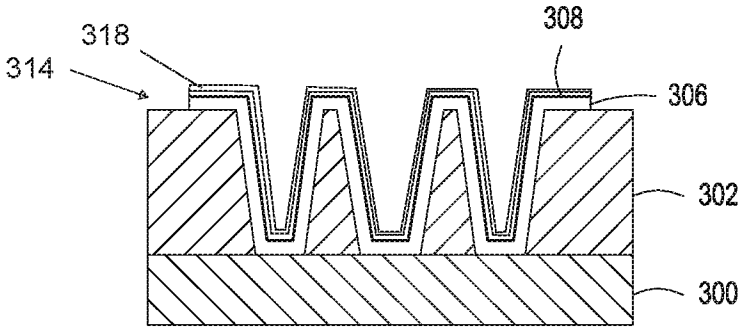

FIG. 3B

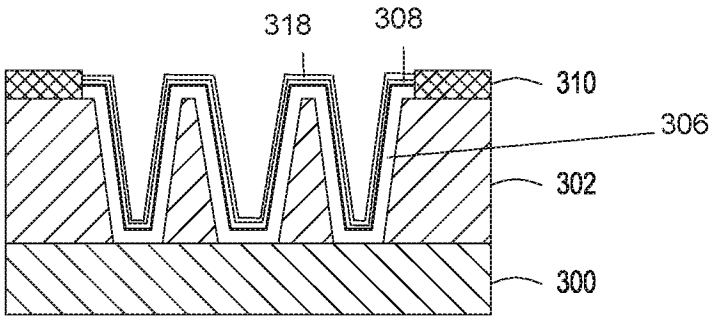

FIG. 3C

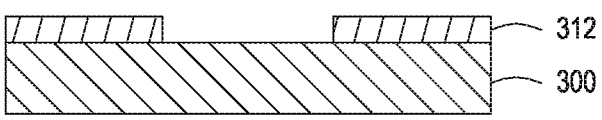

FIG. 3D

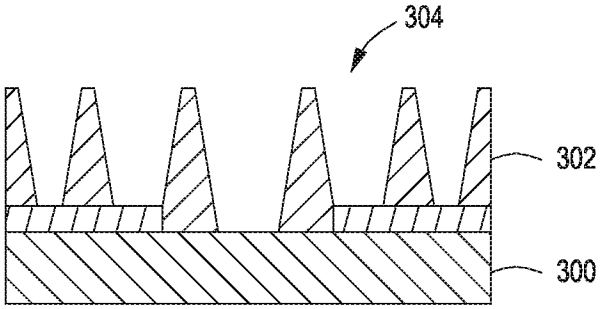

FIG. 3E

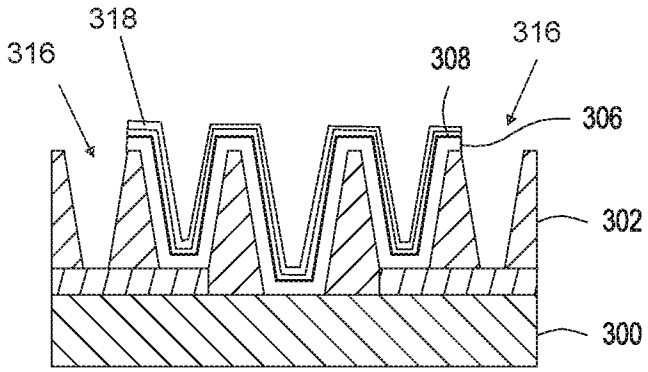

FIG. 3F

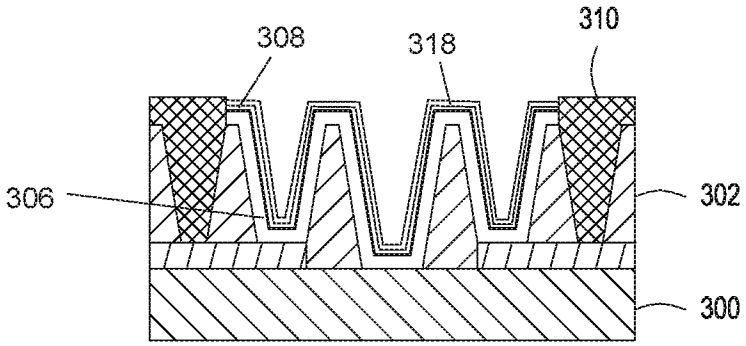

FIG. 3G

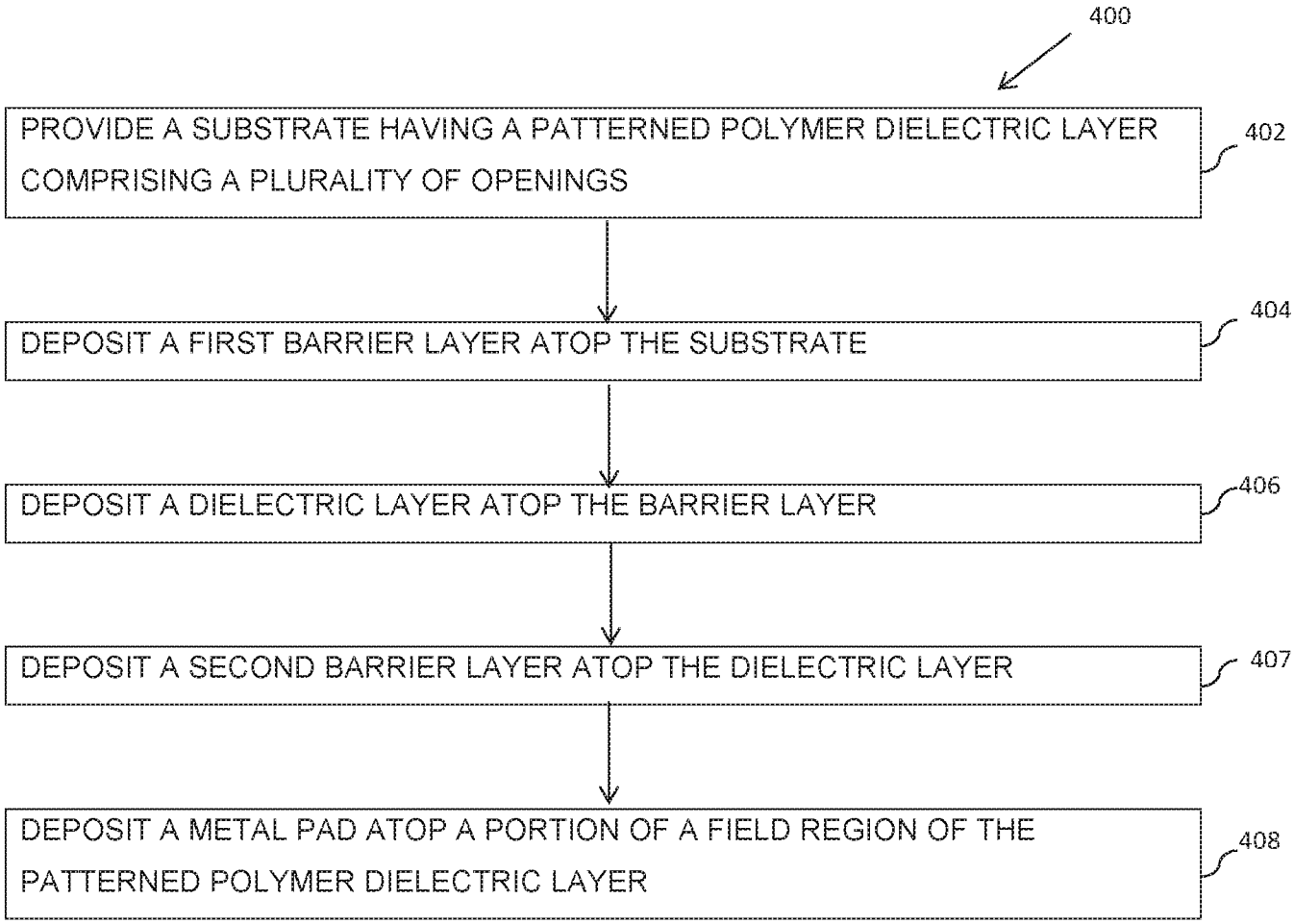
400
PROVIDE A SUBSTRATE HAVING A PATTERNED POLYMER DIELECTRIC LAYER COMPRISING A PLURALITY OF OPENINGS
402
DEPOSIT A FIRST BARRIER LAYER ATOP THE SUBSTRATE
404
DEPOSIT A DIELECTRIC LAYER ATOP THE BARRIER LAYER
406
DEPOSIT A SECOND BARRIER LAYER ATOP THE DIELECTRIC LAYER
407
DEPOSIT A METAL PAD ATOP A PORTION OF A FIELD REGION OF THE PATTERNED POLYMER DIELECTRIC LAYER
408

Figure 4

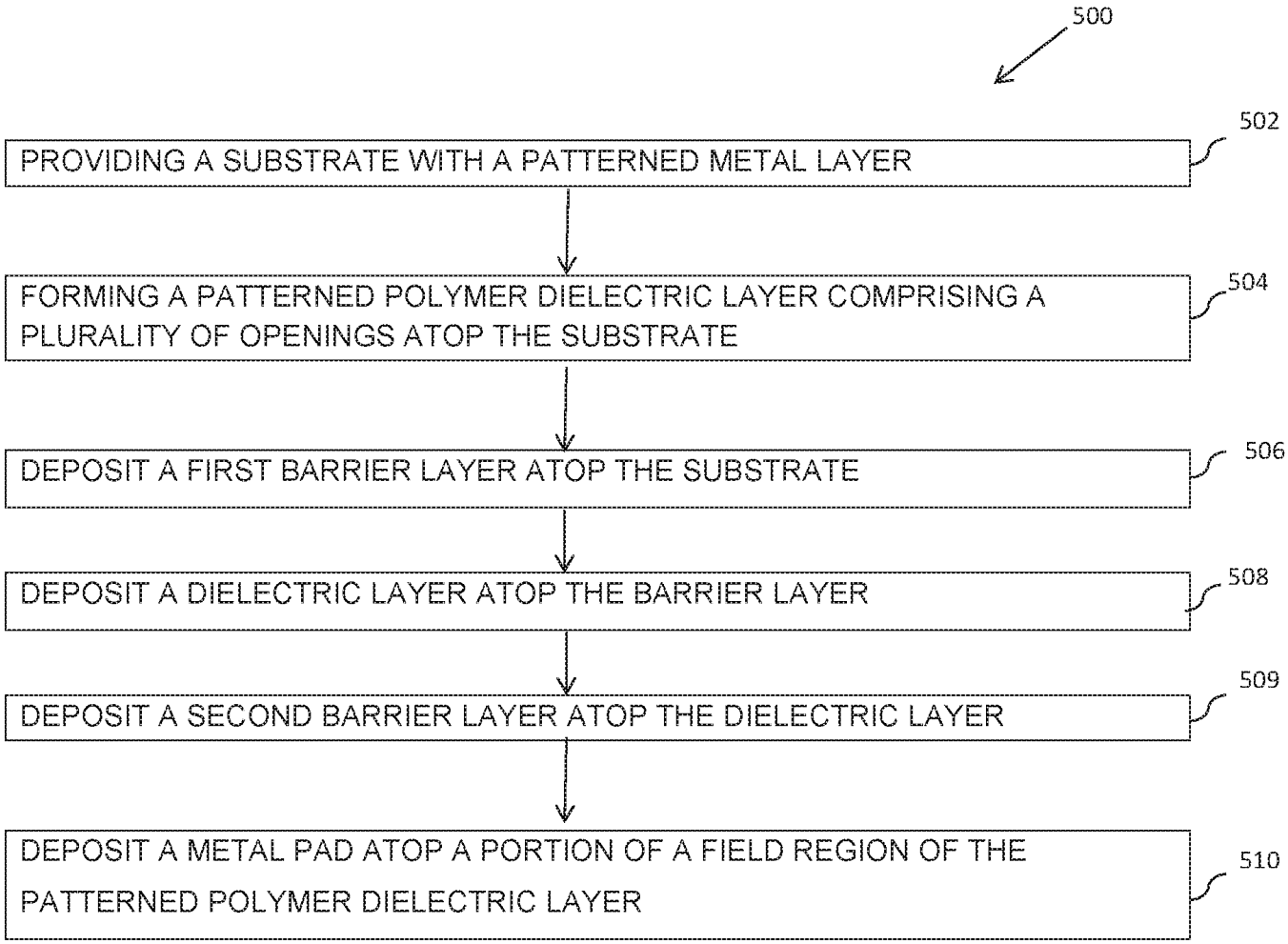
500
PROVIDING A SUBSTRATE WITH A PATTERNED METAL LAYER
502
FORMING A PATTERNED POLYMER DIELECTRIC LAYER COMPRISING A PLURALITY OF OPENINGS ATOP THE SUBSTRATE
504
DEPOSIT A FIRST BARRIER LAYER ATOP THE SUBSTRATE
506
DEPOSIT A DIELECTRIC LAYER ATOP THE BARRIER LAYER
508
DEPOSIT A SECOND BARRIER LAYER ATOP THE DIELECTRIC LAYER
509
DEPOSIT A METAL PAD ATOP A PORTION OF A FIELD REGION OF THE PATTERNED POLYMER DIELECTRIC LAYER
510

Figure 5

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2016/056621

A. CLASSIFICATION OF SUBJECT MATTER

H01L 49/02(2006.01)i, H01L 27/24(2006.01)i, H01L 21/768(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 49/02; H01L 21/20; H01L 29/40; H05K 1/00; H01L 29/76; H01L 29/423; G06T 1/00; H01L 29/02; H01L 27/24; H01L 21/768

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: metal-insulator-metal (MIM) capacitor, resistor, barrier layer, dielectric layer, polymer layer, polymer dielectric layer

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2014-0264743 A1 (TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD.) 18 September 2014 See paragraphs [0025]-[0027], [0033]; claim 1; and figures 3-5, 8.	9,10
A		1-8,11-15
A	US 2003-0201476 A1 (WEI HUA CHENG et al.) 30 October 2003 See paragraphs [0018]-[0024]; and figures 2-4.	1-15
A	US 2014-0264624 A1 (TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD.) 18 September 2014 See paragraphs [0020]-[0049]; and figures 1-10.	1-15
A	US 2013-0241939 A1 (JON BRADLEY LASITER et al.) 19 September 2013 See paragraphs [0077]-[0100]; and figures 10A-10H.	1-15
A	US 2013-0168816 A1 (CHIH-KAI KANG et al.) 04 July 2013 See paragraphs [0024]-[0036]; and figures 1-12.	1-15

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
20 January 2017 (20.01.2017)	**23 January 2017 (23.01.2017)**

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Authorized officer
KIM, Do Weon
Telephone No. +82-42-481-5560

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2016/056621

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