(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
31 December 2003 (31.12.2003)

PCT

(10) International Publication Number
WO 2004/000718 A2

(51) International Patent Classification[7]: B81B 7/00

(21) International Application Number:
PCT/US2003/018306

(22) International Filing Date: 10 June 2003 (10.06.2003)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
10/174,935 19 June 2002 (19.06.2002) US

(71) Applicant: **INTEL CORPORATION** [US/US]; 2200 Mission College Boulevard, Santa Clara, CA 95052 (US).

(72) Inventors: **MA, Qing**; 919 Brentwood Drive, San Jose, CA 95129 (US). **CHOU, Tsung-Kuan**; 4861 Montreal Drive, San Jose, CA 95130 (US).

(74) Agent: **TROP, Timothy, N.**; Trop, Pruner & Hu, P.C., Suite 100, 8554 Katy Freeway, Houston, TX 77024 (US).

(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NI, NO, NZ, OM, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *without international search report and to be republished upon receipt of that report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: BRIDGES FOR MICROELECTROMECHANICAL STRUCTURES

(57) Abstract: A conductive bridge (16) in a second conductive layer may be utilized to join a pair of spaced apart conductive strips (12) in a first conductive layer. A gap (44) between the first and second strips (12) may be bridged by the bridge (16) while isolating both the 5 first and second strips (12) and the bridge (16) itself from another conductor (18) which extends through the gap (44) between the first and second strips (12).

WO 2004/000718 A2

Bridges For Microelectromechanical Structures

Background

This invention relates generally to microelectro-mechanical structures (MEMS).

Microelectromechanical structures are physical structures which may be fabricated using microelectronic fabrication techniques. In the fabrication of MEMS devices, it is often desirable to isolate different structures electrically from one another. To this end, an air gap may be positioned underneath an electrical connector. Such a structure may be called a bridge since it allows an electrical connection over an air gap and provides for isolation from underlying devices.

For example, for multi-mode multi-band cell phone applications, an antenna switch multiplexer switches the antenna to a different mode or band, as well as between transmission and receiving. The multiplexer consists of many individual switches. To route the signal lines, ground lines, and actuation control lines across each other, more that two metal layers are needed.

For example, an in-line cantilever beam metal contact series switch generally requires two metal lines in order to allow the connection. A first signal line may be in a first layer, a second signal line may also be in the first layer, an actuation element may be in the first layer, but the cantilever beam metal contact switch itself must be in at least a second layer.

Thus, there is a need for better ways to allow connections in MEMS devices.

Brief Description of the Drawings

Figure 1 is a top plan view of one embodiment of the present invention;

Figure 2 is a top plan view of a second embodiment of the present invention;

Figure 3 is a top plan view of a third embodiment of the present invention;

Figure 4 is an enlarged cross-sectional view of a technique in accordance with one embodiment of the present invention;

Figure 5 is an enlarged cross-sectional view of the embodiment shown in Figure 4 at a subsequent stage in accordance with one embodiment of the present invention;

Figure 6 is an enlarged cross-sectional view at a subsequent stage in accordance with one embodiment of the present invention;

Figure 7 is an enlarged cross-sectional view at a subsequent stage in accordance with one embodiment of the present invention;

Figure 8 is an enlarged cross-sectional view at a subsequent stage in accordance with one embodiment of the present invention;

Figure 9 is an enlarged cross-sectional view of a subsequent stage in accordance with one embodiment of the present invention;

Figure 10 is an enlarged cross-sectional view of a subsequent stage in accordance with one embodiment of the present invention;

Figure 11 is an enlarged cross-sectional view of a subsequent stage in accordance with one embodiment of the present invention;

Figure 12 is an enlarged cross-sectional view of a stage subsequent to the stage depicted in Figure 8 in accordance with another embodiment of the present invention; and

Figure 13 is an enlarged cross-sectional view of a subsequent stage to that shown in Figure 12 in accordance with one embodiment of the present invention.

Detailed Description

Referring to Figure 1, a basic switch/transmission line co-planar waveguide (CPW) 10 includes a control voltage line 18 that is routed under a bridge 16e across a ground line 12a, including two strips separated by a gap 22, in accordance with one embodiment of the present invention. The ground lines 12a, 12b, and 12c may be formed in a first conductive layer. The signal line 16 may be made in a second, separate conductive layer. The control voltage line 18 may also be in the first conductive layer.

The width of the CPW 10 generally scales with the width of the signal line 16. The width of the signal line 16 may be reduced by using both of the first and second conductive layers in order to have the necessary conductivity. Thus, the ground lines 12 may be made using a thin bottom metal layer in one embodiment.

The width "W" of the bridge 16e may be small enough so that a sacrificial layer (not shown in Figure 1) underneath the bridge 16e may be removed during a release step. In one embodiment, the span of the bridge 16e may be smaller than approximately five times the thickness of the second, upper conductive layer so that the bridge 16e is stiff enough not to collapse under voltage between the two conductive layers.

Figure 2 shows a multiplexer 10a which includes ground lines 12, signal lines 16f and 16g, as well as the signal lines 16a through 16g in accordance with another

embodiment of the present invention. The bridge 20a bridges the ground lines 12c, the bridge 26 bridges the elements 16f and 16g, and the bridge 20 bridges the ground lines 12a. Thus, the control voltage line 18a may span all the way through three separate ground lines, 12a, 12b, and 12c, to reach the ground line 12d.

Referring to Figure 3, in accordance with still another embodiment of the present invention, the ground lines 12a, 12b, and 12c may be crossed by control lines 18b and 18c. The control voltage line 18b goes under a bridge 34 and the control voltage line 18c goes under a bridge 35. The signal lines 32 and 36 are joined by the bridge 34. The signal lines 36 and 38 are joined by the bridge 35. By keeping the span of each bridge 34 and 35 relatively small, multiple bridges may be needed in some embodiments. Thus, the intermediate signal line portion 36 may provide an island which allows the length of the bridges 34 and 35 to be limited to the desired length.

In accordance with one embodiment of the present invention, a bridge, such as a bridge 16e, 16c, 20, 26, 20a, 16c, 34, or 35, may be formed by forming a dielectric layer 42 over a semiconductor substrate 40. The dielectric layer may be silicon dioxide or silicon nitride, as two examples.

Then, as shown in Figure 5, a first or bottom conductive layer 12 may be deposited on the dielectric layer 42 and patterned. The patterning of the layer 12 forms the central island 46 and the gaps 44. The bottom conductive layer 12 may be a composite of titanium, nickel, and gold, in one embodiment.

Referring to Figure 6, the structure may then be covered with a sacrificial layer 48. The sacrificial layer 48 may be deposited or spun-on in some embodiments. In one embodiment, the sacrificial layer 48 may be made of polymeric materials, such as polyimide, resist, or flowable glasses, that reflow, shrink, melt, or vaporize at elevated temperatures.

Next, referring to Figure 7, after lithography and etching, anchor holes 50 may be formed in the sacrificial layer 48.

A seed layer 52, for facilitating plating, may then be coated over the structure shown in Figure 7 to achieve the structure shown in Figure 8. A thick resist 54 may be patterned as a mold for plating as shown in Figure 9. Next, a bridge 16 may be plated, using the seed layer 52 to facilitate adherence of the bridge 16, and using the resist 54 as a

mold for defining the bridge 16. The second or top conductive layer forming the bridge 16 may be gold in one embodiment of the present invention.

After plating the bridge 16, the resist 54 may be removed. The seed layer 52 may be etched away and the material 48 may be released, forming a void 58 under the bridge 16. In one embodiment, the sacrificial material 48 is released through the application of heat.

In another embodiment of the present invention, after the structure shown in Figure 8 is formed, etching may be used to form the U-shaped metal structure 52, as shown in Figure 12. Instead of plating a seed layer, a heavier metal layer 52 may be formed in this embodiment. Thereafter, the air bridge may be formed by releasing the material 48, forming the void 60.

While the present invention has been described with respect to a limited number of embodiments, those skilled in the art will appreciate numerous modifications and variations therefrom. It is intended that the appended claims cover all such modifications and variations as fall within the true spirit and scope of this present invention.

What is claimed is:

1. A method comprising:

forming a pair of conductive strips in a first conductive layer, said strips separated by a gap;

extending a conductor through said gap in the first conductive layer; and

forming, in a second conductive layer, a conductive bridge that electrically couples said first and second strips in isolation from said conductor.

2. The method of claim 1 including forming a co-planar waveguide.

3. The method of claim 1 including forming a multiplexer.

4. The method of claim 1 including forming said second conductive layer over said first conductive layer.

5. The method of claim 4 including forming a release material under said conductive bridge and releasing said release material.

6. The method of claim 5 including releasing said release material by applying heat.

7. The method of claim 1 including forming said bridge with a span less than approximately five times the thickness of said second conductive layer.

8. The method of claim 1 including enabling a control voltage line to extend through a plurality of ground lines formed by the same first conductive layer by providing gaps for said control voltage line to extend through said ground lines.

9. The method of claim 8 including forming a plurality of bridges to connect each ground line across each of said gaps.

10. The method of claim 1 including depositing an insulator on a semiconductor structure, forming a release material on said insulator, and forming a seed layer on said release layer.

11. The method of claim 10 including forming a mold layer over said seed layer to define the shape of said bridge.

12. An integrated circuit comprising:

a semiconductor structure;

a first conductive layer formed on said semiconductor structure, said first conductive layer including a pair of conductive strips separated by a gap, said first conductive layer further including a line extending across said gap in isolation from said strips; and

a second conductive layer over said first conductive layer, said second conductive layer including a bridge which couples said first strip to said second strip in electrical isolation from said line.

13. The circuit of claim 12 wherein said circuit includes a co-planar waveguide.

14. The circuit of claim 12 wherein said circuit includes a multiplexer.

15. The circuit of claim 12 wherein said bridge has a span less than approximately five times the thickness of said second conductive layer.

16. The circuit of claim 12 wherein said line is a control voltage line that extends completely through a plurality of ground lines, each of said ground lines including a gap allowing the passage of said control line, said circuit including a plurality of bridges that connect each of said ground lines across said gaps over said control voltage line.

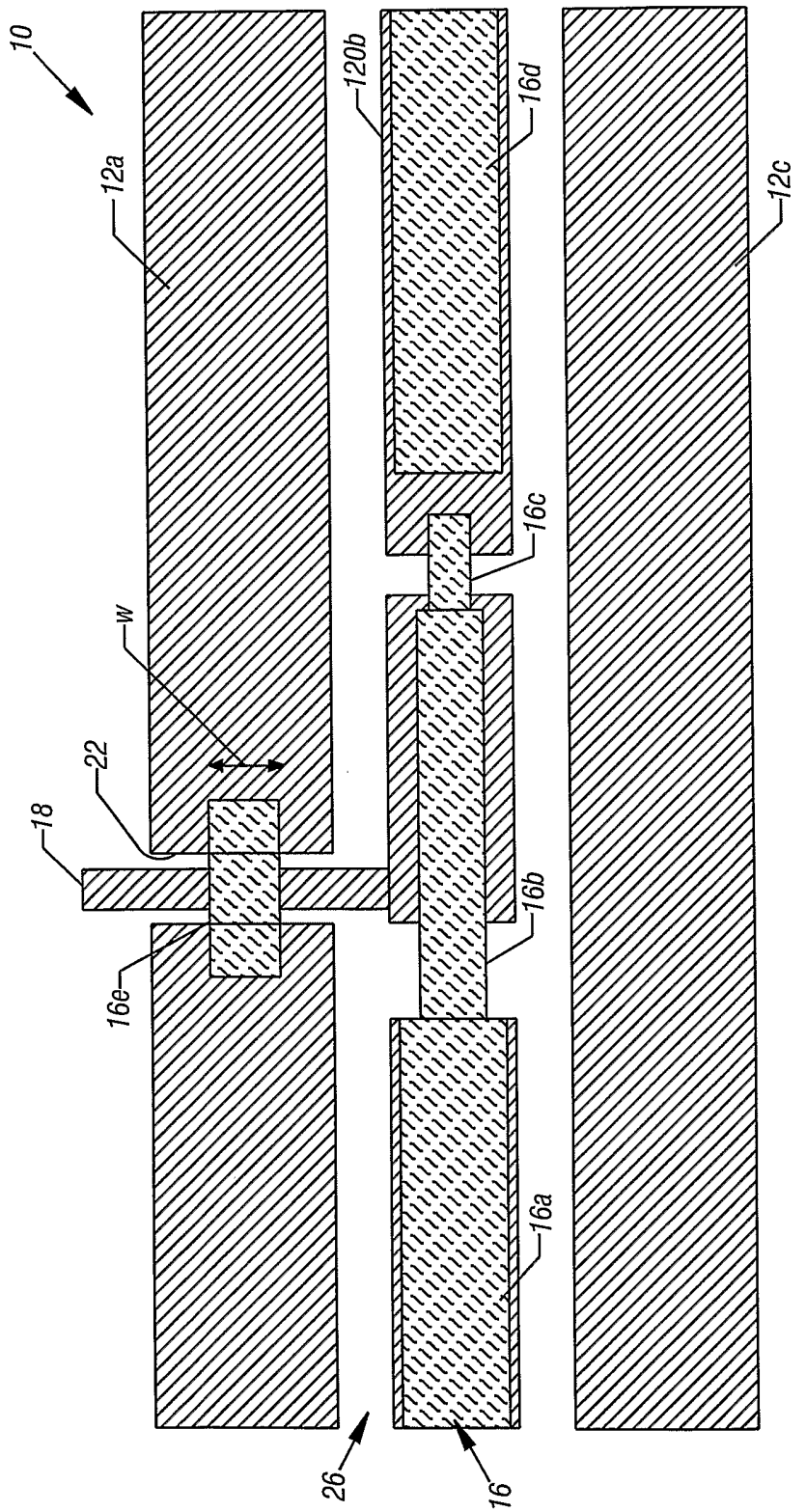

FIG. 1

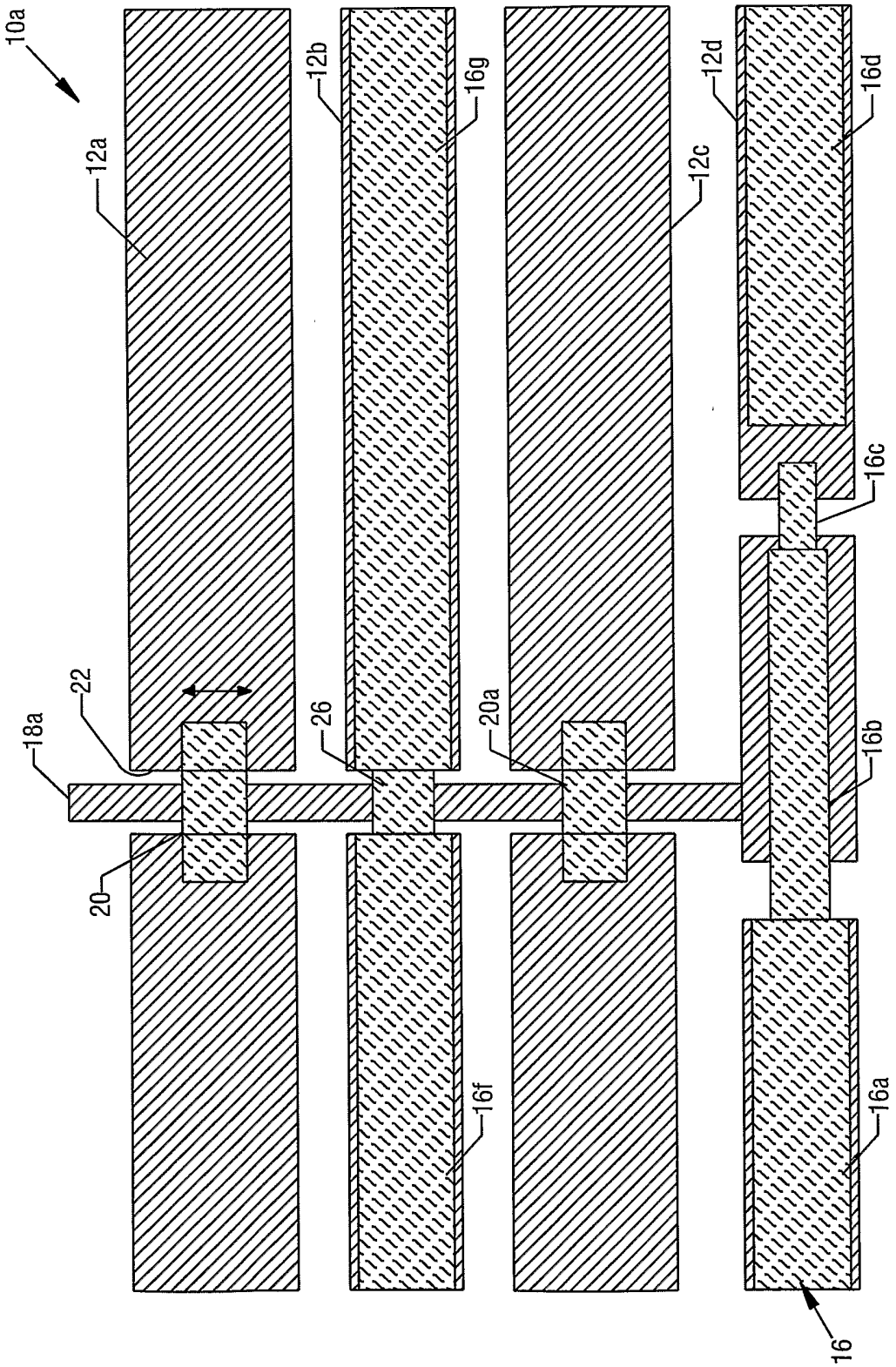

FIG. 2

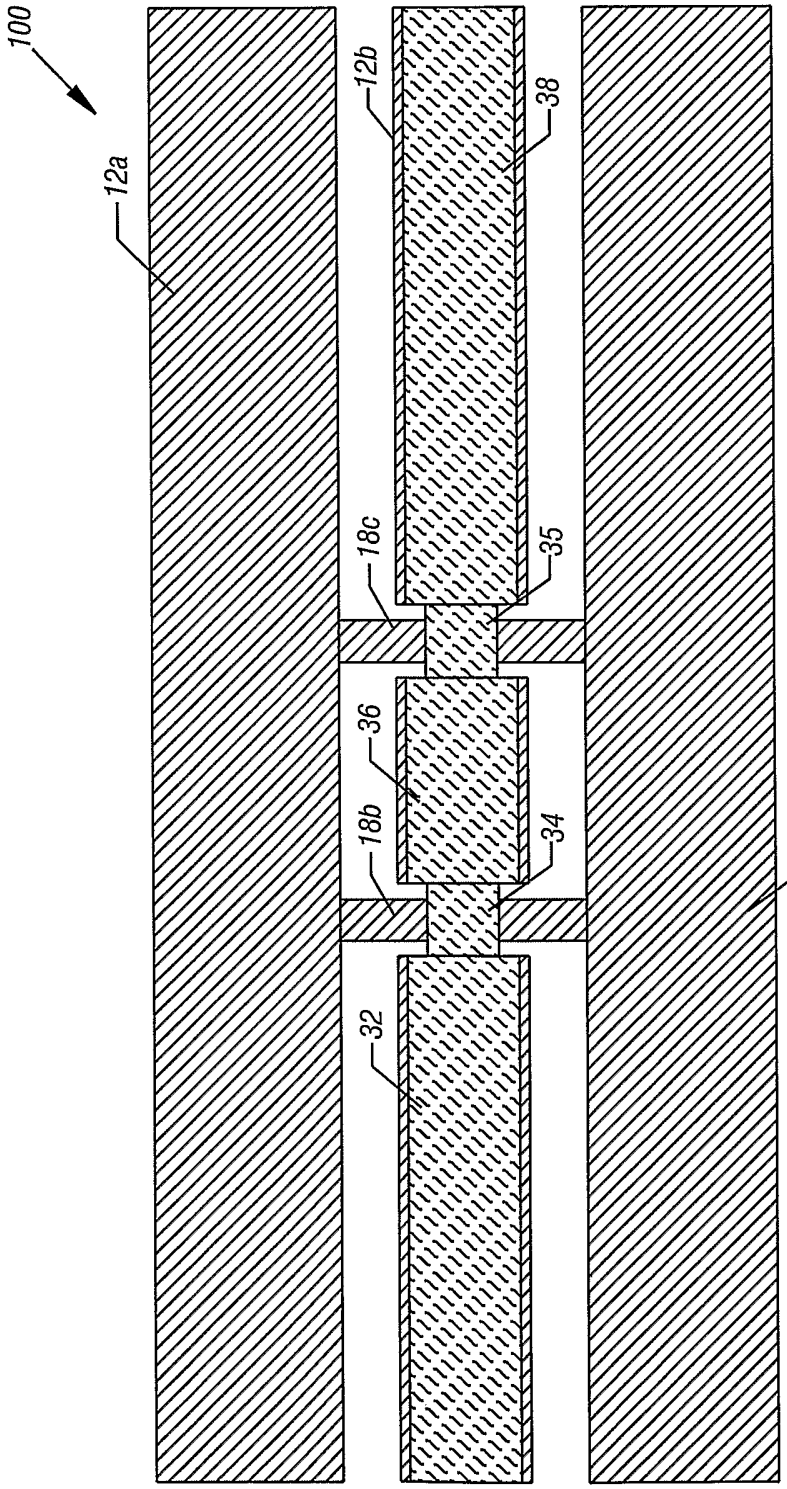

FIG. 3

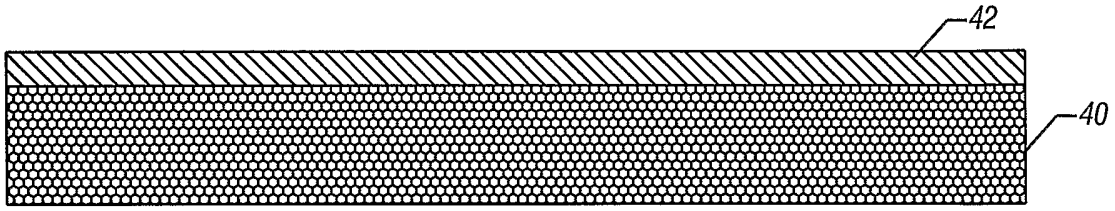

FIG. 4

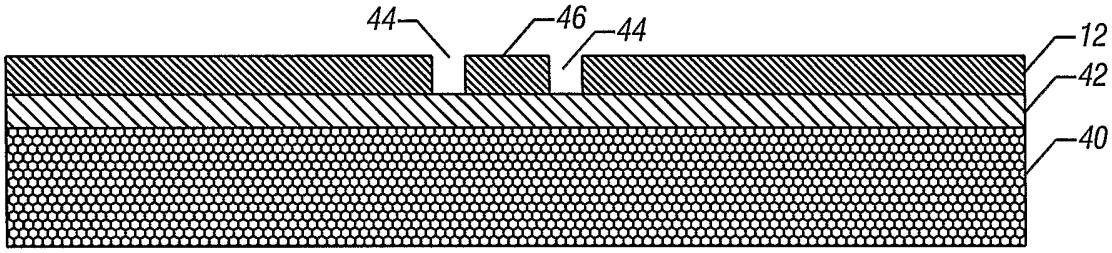

FIG. 5

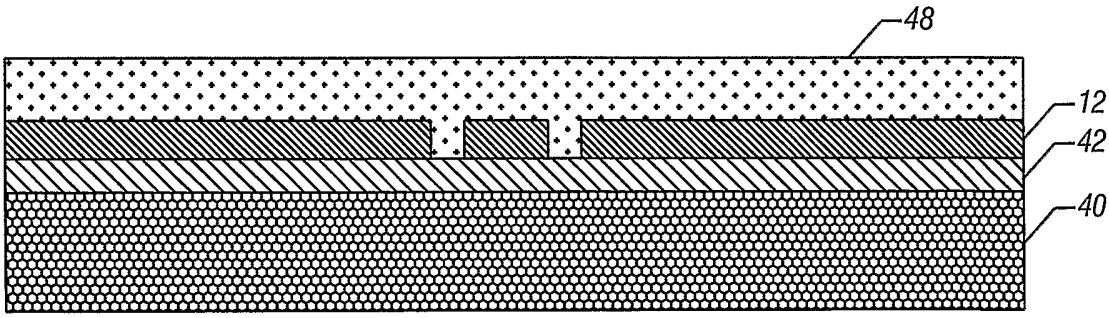

FIG. 6

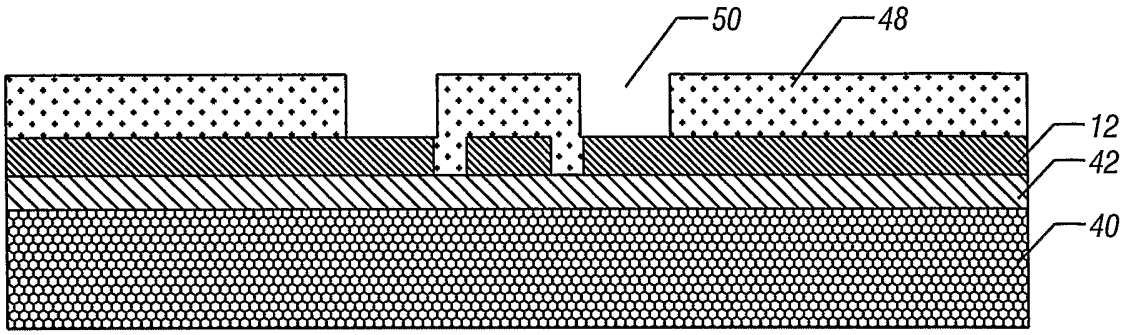

FIG. 7

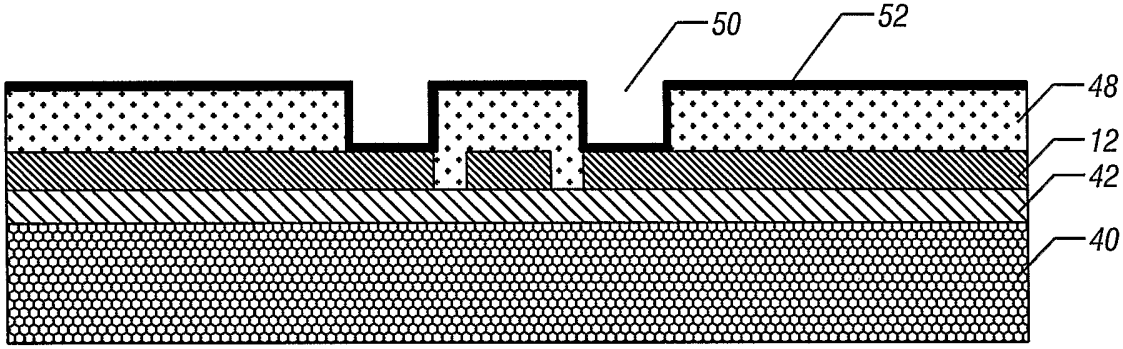

FIG. 8

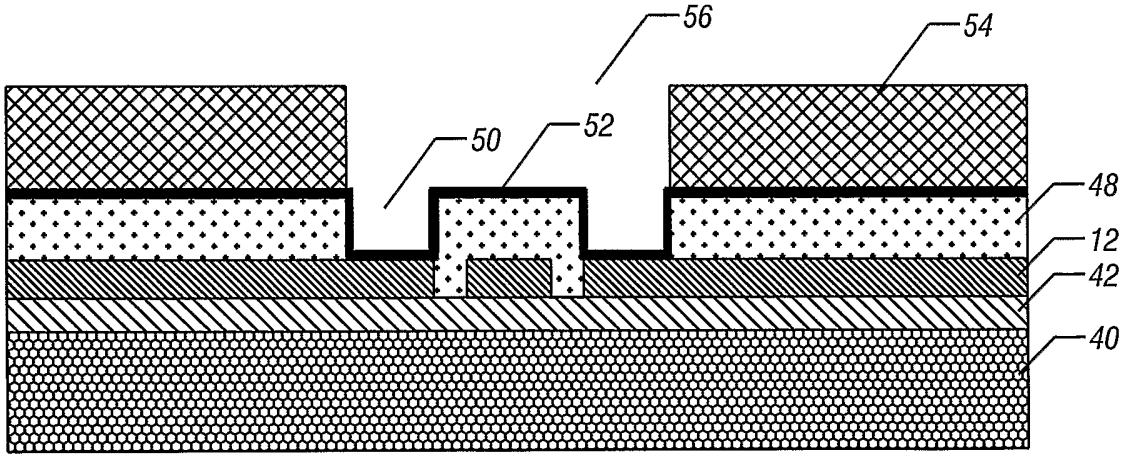

FIG. 9

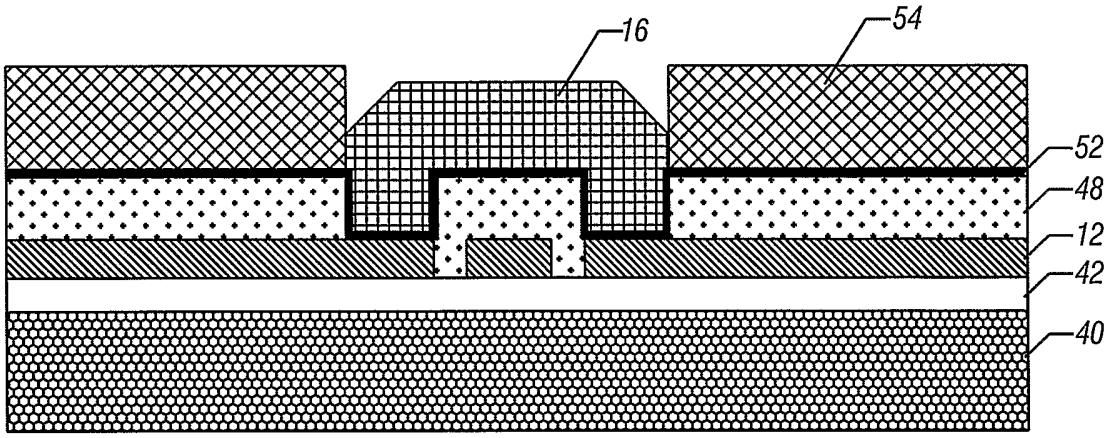

FIG. 10

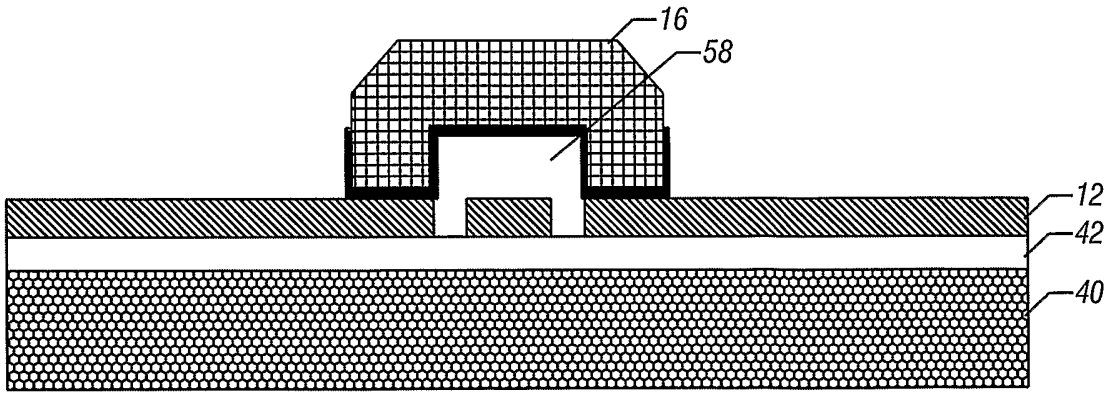

FIG. 11

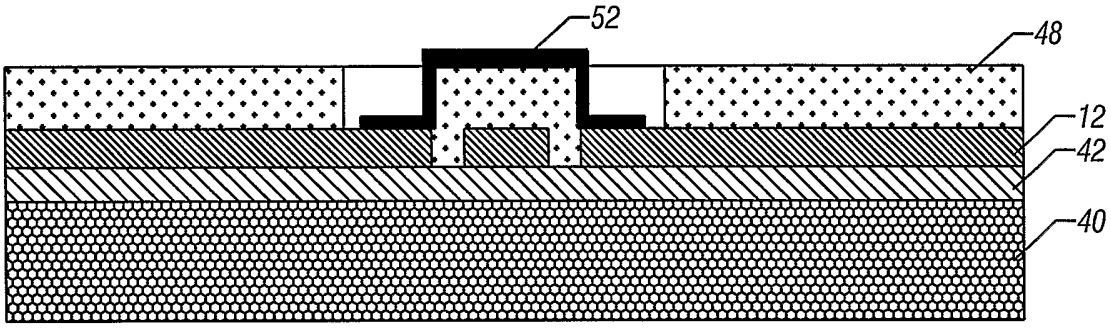

FIG. 12

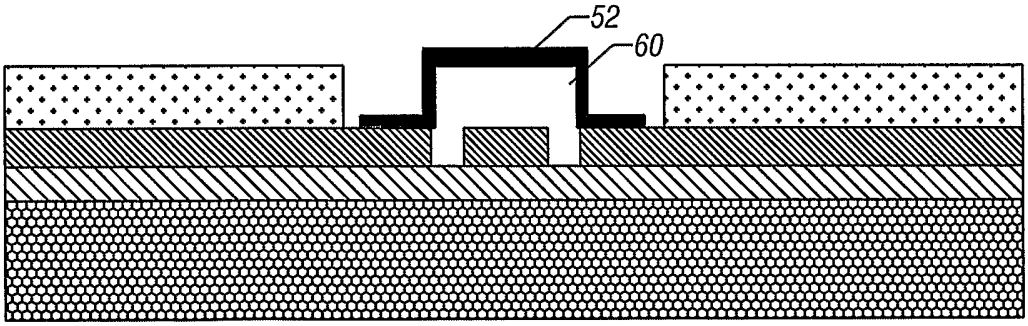

FIG. 13