A silicon dioxide etch stop layer (30) is formed on an inner surface (28b) of a monocrystalline silicon layer (28), and a silicon carrier wafer (52) is bonded to the etch stop layer. The exposed inner surface (28a) of the monocrystalline layer (28) is uniformly thinned to approximately 4 micrometers. Front electrodes (20) in the form of heavily doped areas, and microelectronic transistor driver devices (42) for the electrodes (20) are integrally formed on the outer surface (28a) of the monocrystalline layer (28). A front plate (12) is bonded to the outer surface (28a) of the monocrystalline layer (28), and the carrier (52) is removed. The central portion of the etch stop layer (30) is removed from the inner surface (28b) of the monocrystalline layer (28), and the exposed central portion (28c) of the layer (28) is uniformly thinned to approximately 400 angstroms using plasma assisted chemical etching. A back plate (14) having a back electrode (16) formed thereon is adhered to the unetched peripheral portion (28d) of the inner surface (28b) of the monocrystalline layer (28) to define a sealed space (24) between the front and back electrodes (12, 14) which is filled with liquid crystal material (26).
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LIQUID CRYSTAL DISPLAY INCLUDING ELECTRODES AND DRIVER DEVICES INTEGRALLY FORMED IN MONOCRYSTALLINE SEMICONDUCTOR_LAYER AND METHOD OF FABRICATING THE DISPLAY

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention generally relates to the field of liquid crystal devices, and more specifically to a high speed liquid crystal display and fabrication method in which electrodes and microelectronic electrode driver devices are integrally formed in a transparent monocrystalline semiconductor layer.

Description of the Related Art

A liquid crystal display includes a sealed space which is filled with a liquid crystal material. Front and back electrodes are disposed on opposite sides of the space and are selectively energized to apply electric fields to the liquid crystal material to cause it to locally switch between two discrete polarization states in which it appears either light or dark respectively.

Liquid crystal displays can have either transmissive or reflective configurations. The front electrodes can be arranged in segments to provide an alphanumeric display for a calculator or clock, or in a rectangular matrix to provide a continuous graphic image for television, computer and other applications.

U.S. Patent No. 4,239,346, entitled "COMPACT LIQUID
CRYSTAL DISPLAY SYSTEM", issued Dec. 16, 1980 to R. Lloyd discloses an Active-Matrix Liquid-Crystal Display (AMLCD) including transparent front and back plates which define a sealed space therebetween which is filled with liquid crystal material. A common back electrode is formed on the inner surface of the back plate, whereas a semiconductor layer is formed on the inner surface of the front plate.

Front electrodes of transparent indium tin oxide (ITO) are formed in a rectangular matrix pattern on the inner surface of the semiconductor layer. Thin film MOSFET electrode driver transistors and polycrystalline silicon bus lines are also formed on the inner surface of the semiconductor layer, and are operatively connected to the electrodes. Electrical potentials are selectively applied between the individual front electrodes and the back electrode via the bus lines and driver transistors to locally polarize the liquid crystal material and form a graphic image.

The preferred material for the front and back plates is glass, due to its negligible reactivity with liquid crystal materials and low cost. Although epitaxial deposition of monocrystalline (single crystalline or bulk) silicon is possible on various materials such as sapphire, the temperature required for deposition is on the order of 1,000°C, which is far in excess of the melting point of glass. In addition, the crystalline structure of glass is highly irregular, and non-conducive to the growth of an epitaxial silicon layer.

For these reasons, the silicon layer on the front plate of Lloyd's display is formed by chemical vapor deposition (CVD) of amorphous or polycrystalline silicon. CVD of these materials can be performed at low temperatures and is not adversely affected by the irregular crystalline structure of the glass material of the plate.

However, the carrier mobility of polycrystalline
silicon is one-eighth that of monocrystalline silicon, and the mobility of amorphous silicon is one-hundredth that of monocrystalline silicon. The operating speed of a micro-electronic device is linearly proportional to the mobility. The low mobility of polycrystalline and amorphous silicon limits the operating speed of the electrode driver transistors and thereby the displays in which they are incorporated.

**SUMMARY OF THE INVENTION**

In accordance with the present invention, a silicon dioxide etch stop layer is formed on an inner surface of a monocrystalline silicon layer, and a silicon carrier wafer is bonded to the etch stop layer. The exposed outer surface of the monocrystalline layer is uniformly thinned to approximately 4 micrometers.

Front electrodes in the form of heavily doped areas, and transistor drivers for the electrodes are integrally formed on the outer surface of the monocrystalline layer. A front plate is bonded to the outer surface of the monocrystalline layer, and the carrier wafer is removed.

The central portion of the etch stop layer is removed from the inner surface of the monocrystalline layer, and the exposed central portion of the monocrystalline layer is thinned to a uniform thickness of approximately 400 angstroms using plasma assisted chemical etching. A back plate having a back electrode formed thereon is adhered to the unetched peripheral portion of the inner surface of the monocrystalline layer to define a sealed space between the front and back electrodes which is filled with liquid crystal material.

The electrode driver transistors which are formed in the present monocrystalline silicon layer have much higher carrier mobility than comparable transistors formed in polycrystalline and amorphous silicon as described above.
The higher mobility enables higher current per junction area, allowing the size of the transistors to be reduced and provide an increase in resolution and fill factor (ratio of active area to total area of display).

In addition, the front electrodes which are composed of highly doped areas of the thinned, monocrystalline silicon layer are more durable than the ITO electrodes of the prior art, providing the present display with improved reliability and ease of fabrication.

These and other features and advantages of the present invention will be apparent to those skilled in the art from the following detailed description, taken together with the accompanying drawings, in which like reference numerals refer to like parts.

DESCRIPTION OF THE DRAWINGS

FIG. 1 is a simplified sectional view illustrating a liquid crystal display embodying the present invention;
FIG. 2 is a diagram illustrating the arrangement of front electrodes, electrode driver transistors and bus lines of the display;
FIG. 3 is a diagram illustrating a unit cell of the display at enlarged scale;
FIG. 4 is a diagram illustrating the arrangement of a single electrode driver transistor of the display;
FIGs. 5 to 9 are simplified sectional views illustrating the method of fabricating the present display; and
FIG. 10 is a simplified sectional view illustrating a modified embodiment of the present display.

DETAILED DESCRIPTION OF THE INVENTION

As illustrated in FIGs. 1 to 3, a liquid crystal display 10 embodying the present invention includes a glass front plate 12 (which faces a viewer) having a front or outer surface 12a and back or inner surface 12b, and a
glass back plate 14 having a front or inner surface 14a and back or outer surface 14b. A back electrode 16 is formed on the inner surface 14a of the back plate 14, whereas a plurality of unit cells 18 including transparent front electrodes 20 are adhered to the inner surface 12b of the front plate 12 by a transparent adhesive 22 such as epoxy.

The plates 12 and 14 are sandwiched together with a predetermined spacing therebetween, and sealed at their peripheral edges to define a sealed space 24 therebetween which is filled with a liquid crystal material 26. The display 10 can be transmissive, in which case the plate 14 and back electrode 16 are transparent. Alternatively, the display 10 can be reflective, in which case the back electrode 16 is made reflective or a reflector (not shown) is provided behind the electrode 16.

The back electrode 16 and cells 18 can be arranged in any desired configuration within the scope of the invention. In the preferred configuration as illustrated in FIG. 2, the cells 18 are arranged in a rectangular grid array to form an Active-Matrix Liquid-Crystal Display (AMLCD). Alternatively, although not illustrated, the electrodes can be arranged as segments which are selectively switched to form numerals or alphanumeric characters.

The electrodes 20 are individually and selectively switched between two discrete voltages such that the electric field between the electrodes 20 and the electrode 16 causes the local polarization of the liquid crystal material 26 to switch between two discrete states. One or more polarizer plates (not shown) are provided for polarizing light passing through the material 26 such that the material 26 appears light or dark in the two polarization states respectively.

In accordance with the invention, a monocrystalline (single crystalline or bulk) semiconductor layer 28 is sandwiched between the plates 12 and 14 and has a front or
outer surface 28a and back or inner surface 28b. The preferred material for the semiconductor layer 28 is silicon, although other semiconductor materials such as gallium arsenide or cadmium telluride can be used within the scope of the invention.

The outer surface 28a of the semiconductor layer 28 is adhered to the inner surface 12b of the front plate 12 by the adhesive 22. The inner surface 28b of the layer 28 has a thinned central portion 28c and a thick peripheral portion 28d which constitutes a continuous protrusion extending toward the back plate 14. A thin silicon dioxide layer 30 is formed on the peripheral portion 28d which is sealingly adhered to the inner surface 14a of the back plate 14 by an adhesive 32.

The peripheral portion 28d acts as a peripheral seal such that the space 24 is defined between the central and peripheral portions 28c, 28d of the inner surface 28b of the semiconductor layer 28 and the inner surface 14a of the back plate 14 (with the back electrode 16 formed thereon), with the liquid crystal material 24 being disposed between the electrodes 16 and 20.

The peripheral portion 28d also constitutes a spacer, having a predetermined height which is selected such that the spacing between the inner surfaces 12b and 14a of the plates 12 and 14 respectively and the thickness of the space 24 will have predetermined selected values.

As illustrated in FIG. 2, the unit cells 18 are arranged in a rectangular matrix configuration. Sixteen cells 18 (one cell 18 is illustrated in FIG. 3) are arranged in a 4 x 4 matrix. The number of cells 18 is not limited within the scope of the invention. A practical display will include, for example, 262,144 unit cells arranged in a 512 x 512 matrix.

The display 10 as viewed in FIG. 2 includes four row select bus lines 34 and four column select bus lines 36.
which are formed on the outer surface 28a of the semiconductor layer 28. The lines 34 and 36 may be aluminum metallizations as illustrated, or alternatively be formed as electrically conductive polycrystalline lines in the material of the semiconductor layer 28.

An external row driver 38 sequentially applies a select signal to the row select lines 34. A column driver 40 applies signals to the column select lines 36 which designate the polarization states (light or dark display areas) for the individual cells 18 in the selected row. In this manner, the rows are sequentially scanned to generate a pixelized graphic image.

As illustrated in FIG. 3, an exemplary row select line 34 is connected to the gate of a microelectronic thin film MOSFET electrode driver device transistor 42 of the respective cell 18, whereas the column select line 36 is connected to the source of the transistor 42. The drain of the transistor 42 is connected to the electrode 20. Although not illustrated, a storage capacitor may be provided which is connected to the drain of the transistor 42.

The row select signal turns on the transistor 42, which gates the column select signal from the source to the drain and thereby to the electrode 20. The column select signal has one of two discrete values which causes the electrodes 16 and 20 to create a local electric field therebetween which polarizes the liquid crystal material 26 to a corresponding state in which it appears light or dark in accordance with the value of the column select signal.

The electrodes 20 are preferably formed as respective areas in the front surface 28a of the semiconductor layer 28 which are highly doped to a level of electrical conductivity. It is, however, within the scope of the invention to chemically deposit the electrodes 20 on the surface 28a.

The electrode driver transistors 42 are also formed on
the front surface 28a of the semiconductor layer 28 as thin film enhancement MOSFETs to constitute an integral micro-electronic structure with the electrodes 20 and select lines 34 and 36. An exemplary configuration of the transistor 42 is illustrated in FIG. 4, and includes a channel 42a which is doped to N or P conductivity type by a suitable process such as ion implantation.

An insulative gate oxide layer 42b is deposited over the channel 42a. A tab 34a extends from the row select line 34 over the oxide layer 42b to constitute the gate of the transistor 42. A tab 36a extends from the column select line 36 over the left end (as viewed in FIG. 4) of the channel 42a to constitute the source. A tab 20a extends from the electrode 20 over the right end of the channel 42a to constitute the drain.

As further illustrated in FIG. 1, holes may be etched through the semiconductor layer 28 to enable connection of the select lines 34 and 36 to the drivers 38 and 40 respectively. In the example shown, a diagonal hole 28e is formed through the left end portion of the layer 28 to enable a wirebond 44 to be connected to the leftmost row select line 36.

The electrode driver transistors 42 which are formed in the present monocrystalline silicon layer 28 have much higher carrier mobility than comparable transistors formed in polycrystalline and amorphous silicon as in the prior art. The higher mobility enables higher current per junction area, allowing the size of the transistors to be reduced and provide an increase in resolution and fill factor (ratio of active area to total area of display).

The front electrodes 20 which are composed of highly doped areas of the thinned, central portion 28c of the monocrystalline silicon layer 28 are more durable than the ITO electrodes of the prior art, providing the present display 10 with improved reliability and ease of fabrica-
tion. In addition, the electrodes 20, select lines 34 and 36 and transistors 42 are hermetically sealed by the plate 12 and adhesive 22, thereby protecting them from chemical reaction with the liquid crystal material 26.

A method of fabricating the display 10 is illustrated in FIGs. 5 to 10. In FIG. 5, a bonded structure 50 is provided as including the monocrystalline silicon layer 28, with the silicon dioxide layer 30 formed on the inner surface 28b thereof. A sacrificial carrier wafer 52 is bonded to the oxide layer 30.

The monocrystalline silicon layer 28 has a thickness of 3.7 - 6 micrometers, with the preferred value being 4 micrometers. The carrier wafer 52 is preferably formed of silicon and has a thickness of 525 micrometers, making it sufficiently durable to support the monocrystalline silicon layer 28 through standard silicon processing steps. The silicon dioxide layer 30 is typically one micrometer thick.

The structure 50 is fabricated by initially providing the monocrystalline silicon layer 28 in the form of a wafer having a thickness on the order of that of the carrier wafer 52. The layer 28 is then oxidized to form the silicon dioxide layer 30. The wafers are then pressed together with or without the intermediary of an adhesive, and the outer surface 28a of the layer 28 is thinned to the desired thickness.

The preferred method of thinning the monocrystalline silicon layer 28 is Plasma Assisted Chemical Etching (FACE) as disclosed in U.S. Patent No. note: insert reference for FACE process, which enables the outer surface 28a to be planarized and the thickness of the layer 28 to be made highly uniform. Structures 50 which are suitable for practicing the present invention are commercially available from, for example, Shin-Etsu Handotai (SEH) of Tokyo, Japan.

In the step of FIG. 6, the unit cells 18 and select
lines 34 and 36 are formed on the front surface 28a of the layer 28 as indicated by arrows 54 using standard silicon processing technology. The step of FIG. 6 may include the formation of additional microelectronic devices or structures, such as light blocking shields for the transistors 42, although not explicitly illustrated.

FIG. 7 illustrates how the structure 50 is inverted from the orientation of FIG. 6, and bonded to the front plate 12 using the adhesive 32.

In FIG. 8, the carrier wafer 52 is removed using an etchant to which the silicon dioxide layer 30 is resistant. The preferred etchant is potassium hydroxide (KOH), with the layer 30 acting as a etch stop layer. A photoresist layer 56 is formed around the periphery of the layer 30 using standard photolithographic techniques, and the central portion of the silicon dioxide layer 30 is etched away as indicated by arrows 58 to expose the silicon layer 28.

As illustrated in FIG. 9, the central portion 28c of the monocrystalline silicon layer 28 is thinned to approximately 300 - 600 angstroms, preferably 400 angstroms, using the PACE process as indicated by arrows 60. The final thickness of the portion 28c depends on the desired color of the display 10. The diagonal hole 44 is etched through the layer 28, and the wirebond 44 is connected to the column select line 36.

The back plate 14 is then adhered to the peripheral portion 28d of the layer 28 as illustrated in FIG. 9, and the space 24 is filled with the liquid crystal material 26 to produce the display 10 as illustrated in FIG. 1. The silicon dioxide layer 30 may be removed prior to assembly of the back plate 14, or may remain as shown.

FIG. 10 illustrates a modified liquid crystal display 70 embodying the present invention in which the monocrystalline silicon layer is designated as 72. In the display
70, a photoresist pattern (not shown) is formed on the layer 72, and portions of the layer 72 and adhesive 32 are etched away completely in the step of FIG. 9 to produce islands 74 on which the driver transistors 42 and select lines 34 and 36 are formed, and openings 76 between the islands 74.

Transparent electrodes 78 are formed on the inner surface 12b of the plate 12 by deposition of ITO in the openings 76 and operatively connected to the transistors 42. The display 70 is desirable in an application in which the ITO electrodes 78 can be made more transmissive than the doped silicon electrodes 20.

While several illustrative embodiments of the invention have been shown and described, numerous variations and alternate embodiments will occur to those skilled in the art, without departing from the spirit and scope of the invention. Accordingly, it is intended that the present invention not be limited solely to the specifically described illustrative embodiments. Various modifications are contemplated and can be made without departing from the spirit and scope of the invention as defined by the appended claims.
WE CLAIM:

1. A liquid crystal display, comprising:
   a transparent first plate having an inner surface and an outer surface;
   a monocrystalline semiconductor layer having an inner surface and an outer surface, said outer surface of the semiconductor layer being transparently adhered to said inner surface of the first plate;
   a transparent first electrode which is adhered to said inner surface of the first plate;
   a microelectronic driver device which is formed on said outer surface of the semiconductor layer and operatively connected to the first electrode;
   a second plate having an inner surface and an outer surface;
   a second electrode formed on said inner surface of the second plate;
   spacer means for spacing said inner surfaces of the first and second plates from each other by a predetermined spacing;
   sealing means for providing a peripheral seal around the first and second plates to define a sealed space between the first and second electrodes; and
   a liquid crystal material provided in said space.

2. A display as in claim 1, in which the first electrode comprises a heavily doped area formed in said outer surface of the semiconductor layer.

3. A display as in claim 1, in which the semiconductor layer comprises an island in which the driver device is formed.

4. A display as in claim 3, in which:
the semiconductor layer has an opening formed therethrough which is laterally spaced from said island; and

the first electrode is adhered to said inner surface of the first plate in said opening.

5. A display as in claim 1, in which a central portion of the semiconductor layer which defines said space has a thickness of approximately 300 - 600 angstroms.

6. A display as in claim 1, in which the semiconductor layer is formed of silicon.

7. A display as in claim 1, in which the spacer means comprises a protrusion which extends from said inner surface of the semiconductor layer toward said inner surface of the second plate and has a height corresponding to said predetermined spacing.

8. A display as in claim 1, in which the spacer means and the sealing means in combination comprise a continuous peripheral protrusion which extends from said inner surface of the semiconductor toward said inner surface of the second plate and has a height corresponding to said predetermined spacing.

9. A microelectronic structure, comprising:
   a plate;
   a monocrystalline semiconductor layer;
   an adhesive which bonds a surface of the semiconductor layer to the plate; and
   microelectronic circuit means formed on said surface of the semiconductor layer.

10. A structure as in claim 9, in which the micro-
electronic circuit means comprises:
   an electrode; and
   a microelectronic driver device which is opera-
5   tively connected to the electrode.

11. A structure as in claim 10, in which the elec-
trode comprises a heavily doped area formed in said surface
of the semiconductor layer.

12. A structure as in claim 9, in which a central
portion of the semiconductor layer has a thickness of
approximately 300 - 600 angstroms.

13. A structure as in claim 9, in which the semi-
conductor layer is formed of silicon.

14. A method of fabricating a semiconductor struc-
ture, comprising the steps of:
   (a) providing a material including:
   a carrier; and
      a monocristalline semiconductor layer having
     a first surface and a second surface, said second surface
     of the semiconductor layer being bonded to the carrier;
   (b) forming a microelectronic device on said
      first surface of the semiconductor layer;
   (c) adhering said first surface of the semi-
      conductor layer to a plate; and
   (d) removing the carrier from said second surface
      of the semiconductor layer.

15. A method as in claim 14, further comprising the
step, performed after step (d), of:
   (e) thinning at least a central portion of said
second surface of the semiconductor layer.
16. A method as in claim 15, in which step (e) comprises plasma assisted chemical etching.

17. A method as in claim 15, in which:
   step (e) comprises thinning said second surface of the semiconductor layer to a thickness of approximately 300 - 600 angstroms.

18. A method as in claim 17, in which step (a) comprises providing the material such that the semiconductor layer has a thickness of at least one micrometer.

19. A method as in claim 17, in which step (a) comprises providing the material such that the carrier has a thickness of approximately 525 micrometers.

20. A method as in claim 17, in which step (a) comprises providing the material such that the semiconductor layer is formed of silicon.

21. A method as in claim 14, in which:
   step (a) comprises providing the material as further including an etch stop layer formed on said second surface of the semiconductor layer; and
   step (d) comprises etching away the carrier using an etchant to which the etch stop layer is resistant.

22. A method as in claim 21, further comprising the steps, performed after step (d), of:
   (e) removing the etch stop layer from a central portion of said second surface of the semiconductor layer; and
   (f) thinning said central portion using an etchant to which the etch stop layer is resistant.
23. A method as in claim 22, in which step (f) comprises plasma assisted chemical etching.

24. A method as in claim 21, in which:
   step (a) comprises providing the carrier as being formed of silicon and the etch stop layer as being formed of silicon dioxide.

25. A method as in claim 24, in which step (d) comprises etching away the carrier using potassium hydroxide.
FIG. 2.

FIG. 3.
A. CLASSIFICATION OF SUBJECT MATTER
IPC 5 G02F1/136 H01L27/12 H01L21/20

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 5 G02F H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic database consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

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<td>PATENT ABSTRACTS OF JAPAN vol. 16, no. 371 (P-1399) 10 August 1992 &amp; JP, A, 04 116 624 (SEIKO) 17 April 1992 see abstract</td>
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<td>US, A, 3 765 747 (PANKRATZ) 16 October 1973 see figures 18, 21B</td>
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Further documents are listed in the continuation of box C. Patent family members are listed in annex.

* Special categories of cited documents:
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Date of the actual completion of the international search
6 May 1994

Date of mailing of the international search report
18. 05. 94

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