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- *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*
- *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

Published:

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INTERCONNECT FOR ELECTRONIC DEVICE

BACKGROUND

[0001] This relates to interconnects for electronic devices.

SUMMARY

[0002] In one example, a semiconductor die includes a substrate and an integrated circuit provided on the substrate and having contacts. An electrically conductive layer is provided on the integrated circuit and defines electrically conductive elements electrically connected to the contacts. Electrically conductive interconnects coupled with respective electrically conductive elements. The electrically conductive interconnects have at least one of different sizes or shapes from one another.

[0003] In another example, an electronic package includes a die having a substrate and an integrated circuit provided on the substrate. The integrated circuit includes contacts. An electrically conductive layer is provided on the integrated circuit and defines electrically conductive elements electrically connected to the contacts. Electrically conductive interconnects coupled with respective electrically conductive elements. The electrically conductive interconnects have at least one of different sizes or shapes from one another. A leadframe is secured to the electrically conductive interconnects.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] FIG. 1 is a perspective view of an example wafer for forming an electronic device.

[0005] FIG. 2 is a section view taken along line 2-2 of FIG. 1 and showing a die.

[0006] FIG. 3A is a schematic illustration of electrically conductive elements contacted by electrically conductive interconnects in the die.

[0007] FIG. 3B is a perspective view of FIG. 3A.

[0008] FIG. 4 is a top view of another example electronic device

[0009] FIG. 5 is a top view of another example electronic device.

[0010] FIG. 6 is a section view of yet another example electronic device.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0011] FIG. 1 illustrates an example wafer 90 used to form an electronic device. The electronic device can be, for example, a wafer-level chip scale package (WLCSP) of integrated circuits. Alternatively, the electronic device can be on the chip or die scale, PCB scale or panel scale or an electronic package. Consequently, the electronic device can be on the millimeter size scale or up to several feet in size.

[0012] As shown, the wafer 90 includes a substrate 110 having a first side 112 and a second side 114. The substrate 110 can be circular and have a diameter of about, for example, 200 or 300 mm. Alternatively, the substrate 110 can be square or rectangular (not shown). The substrate 110 can be formed from a semiconductor material, such as silicon. The wafer 90 is diced, *e.g.*, by stealth dicing, to singulate the wafer into individual dies 94 (FIG. 2). The dies 94 when connected to a leadframe 147, form an electronic package or device 100.

[0013] Within each die 94 integrated circuits 120 are fabricated or otherwise provided on the second side 114 of the substrate 110. The integrated circuits 120 include one or more contacts shown schematically at 121. The integrated circuits 120 can be arranged in a grid or array equidistantly spaced from one another about the second side 114. Depending on the sizes of the substrate 110 and integrated circuits 120, thousands or tens of thousands of integrated circuits can be fabricated on the second side 114 of the substrate. Each integrated circuit 120 includes a surface or side 108 facing away from the substrate 110.

[0014] Referring to FIGS. 2 and 3A, a layer 130 of electrically conductive material is provided on the side 108 of the integrated circuits 120 and defines one or more electrically conductive first, second, and third elements 131, 133, 135 for redistributing and/or routing power. The layer 130 can be formed from a metal, such as copper or aluminum. The elements 131, 133, 135 can include electrically conductive lines and/or electrically conductive contacts formed in different patterns.

[0015] As shown in FIG. 3A, the elements 131, 133 are formed as first and second lines. The elements 135 are formed as contacts. Other permutations and combinations of lines and contacts are contemplated. Each element 131, 133 is electrically connected to one or more of the contacts 121 through vias (not shown) in the integrated circuit. Each element 131, 133 can include at least one base 134 and a plurality of fingers 136 extending from each base in one or more directions. The base 134 can have a polygonal shape, *e.g.*, square, rectangular or trapezoidal. The fingers

136 can be generally rectangular and have a length extending away from the base 134 that greater than the width. The element 131 shown includes a pair of bases 134 and fingers 136 extending between the bases. At least some fingers 136 extend between and interconnect the bases 134.

[0016] Each element 133 includes a base 134 and fingers 136 extending from the base. In one example, the fingers 136 extend in opposite directions from the base 134. The base 134 can have a polygonal shape, *e.g.*, square, rectangular or trapezoidal. The fingers 136 can be generally rectangular and have a length extending away from the base 134 that greater than the width. The elements 133 are positioned between the fingers 136 of the element 131 and are electrically isolated from one another and from the element 131. In one example, the elements 133 are interdigitated with the fingers 136 of the element 131. The elements 135 can be round or square and are each electrically connected to a corresponding contact 121 in the integrated circuit 120 through a via (not shown). The elements 135 are electrically isolated from one another and from the elements 131, 133.

[0017] Referring to FIG. 2, a layer 140 of material extends over the layer 130 and covers the entire side 108 of each integrated circuit 120. The layer 140 is formed from an electrically insulating material such as polyimide. One or more slots or openings 142 extend entirely through the insulating layer 140 to expose portions of the layer 130, namely, to expose the elements 135 and portions of the elements 131, 133. It will be appreciated, however, that the layer 140 can be omitted (not shown).

[0018] The openings 142 can be sized and shaped to expose different portions of the same element 131 or 133 or portions of different elements 131, 133. To this end, the openings 142 can be aligned with the bases 134 and/or fingers 136 of the elements 131, 133. Each opening 142 can have a cross-sectional area that varies along its depth or have a constant cross-sectional area (not shown). As shown, each opening 142 has a cross-sectional area that increases in a direction extending away from the layer 130.

[0019] Referring to FIG. 3B, electrically conductive interconnects 150 extend through each opening 142 (when present) into contact with the elements 135 and the exposed portions of the elements 131, 133. Each interconnect 150 includes a first portion or bump 152 and a second portion or post 154 positioned between the first portion and the respective elements 131, 133, 135. Alternatively, the first portion 152 can be omitted (not shown). Each second portion 154

engages an element 135 or portions of the elements 131, 133 exposed by the associated opening 142. It will be appreciated that although interconnects 150 are only illustrated on a single integrated circuit 120 in FIG. 1 any number of the integrated circuits on the substrate 110 can include any number of interconnects.

[0020] The first portion 152 can be formed from a conductive material such as tin solder, *e.g.*, SnAg or NiSnAg, that undergoes solder reflow to secure the die 94 to the leadframe 147. With this in mind, the leadframe 147 can be secured to the dies 94 prior to singulation of the wafer 90 into dies. As a result, portions of the leadframe 147 are cut off during singulation and the remainder of the leadframe remains in the electronic device after singulation. The leadframe 147 may therefore not have a frame shape in the electronic device.

[0021] In any case, the second portion 154 can be formed from a conductive material such as copper. The first portion 152 can have a thickness t_1 of about 5 - 30 μm . The second portion 154 can have a thickness t_2 of about 25 - 55 μm . The interconnect 150 can have an overall thickness T of about 60 μm . The thickness T of the interconnect 150 can be different from the width, which extends perpendicular to the thickness (left to right as shown), *i.e.*, the thickness can be greater or less than the width. The interconnect 150 can be formed by electroplating the first and second portions 152, 154 directly onto the insulating layer 140 and through the openings 142 into contact with the elements 135 and the exposed portions of the elements 131, 133. The interconnect 150 can have an overhang or lip 160 that engages the insulating layer 140 outside the opening 142. In other words, the interconnect 150 can have a larger footprint than the opening 142 and extend entirely around or encircle the opening from above (as shown). The lip 160 can have a width w of about 25 μm relative to the smallest cross-sectional area of the opening 142 at the layer 130.

[0022] The interconnects 150 can have a wide range of shapes and sizes on each integrated circuit 120. In particular, the interconnect 150 can have any shape or cross-section, *e.g.*, square or rectangular (*see* FIG. 3), circular, polygonal and/or elongated, with any number of straight and/or curved sides. The interconnects 150 associated with a single integrated circuit 120 can have different sizes and/or different shapes from one another. In one example, the interconnect 150 can have a width of about 150 - 500 μm and a length of about 150 - 500 μm . The interconnect 150 can have an aspect ratio of at least 1:1 and up to about 5:1. Regardless, the interconnect 150 completely fills each opening 142 and the shape of the interconnect is defined

by the shape of the opening. That said, configuring an opening 142 to expose particular portions of the elements 131, 133 readily enables the interconnect 150 extending into the opening to contact those exposed portions.

[0023] With this in mind, the shapes of the openings 142 in the insulating layer 140 allow the interconnects 150 to contact to any number of elements 131, 133, 135. In the example shown in FIG. 3A, five openings 142 in the insulating layer 140 allow five interconnects 150 to contact the individual, exposed elements 135 formed as contacts. The interconnects 150 contacting the elements 135 can be circular, round or square (not shown).

[0024] Another, elongated opening 142 exposes the fingers 136 on the element 131 and the bases 134 of multiple elements 133. The interconnect 150 electroplated through this opening 142 therefore contacts the fingers 136 on the element 131 as well as the bases 134 of the elements 133. Consequently, the elements 131, 133, which would otherwise be electrically isolated from one another, are now electrically connected to one another by the interconnect 150. Accordingly, multiple contacts 121 within the same integrated circuit 120 that are electrically connected to the exposed elements 131, 133 are electrically connected to one another. This is desirable when, for example, multiple integrated circuits 120 are intended for the same integrated circuit once the electronic device 100 is diced or when it is desirable to increase power delivery to one or more integrated circuits.

[0025] It will be appreciated that a single interconnect 150 can extend into multiple, discrete openings 142 to electrically connect spaced-apart portions of the elements 131, 133 (not shown). In any case, the openings 142 throughout the insulating layer 140 are sized and shaped to expose portions of the layer 130 such that providing interconnects 150 in the openings will electrically connect contacts 121 within a single integrated circuit 120. This is repeated across all the integrated circuits 120 on the electronic device 100 in a desired manner.

[0026] To this end, in another example die 94 shown in FIG. 4, a pair of interconnects 150 are provided on the surface 108 for three contacts 121 in the die. A first, generally square interconnect 150 extends through a similarly shaped opening 142 in the insulating layer 140 to allow the interconnect to contact an exposed element 135 aligned with the opening (not shown). A second, generally rectangular interconnect 150 extends through a similarly shaped opening 142 in the insulating layer 140 to allow the interconnect to contact portions of multiple elements 131, 133 aligned with the opening (not shown).

[0027] In another example electronic device configuration shown in FIG. 5, the electronic device is a die 200 formed by segmenting the wafer 90 by dicing, *e.g.*, by stealth dicing. Nine interconnects 150 are provided on the surface 108 for thirteen contacts 121 in the die 94. Five interconnects 150 are square and contact the elements 135. The remaining interconnects 150 are elongated and contact portions of multiple elements 131, 133.

[0028] In another example shown in FIG. 6, the electronic device is a WLCSP 300 for a high current application. Consequently, the conductive material is formed in multiple layers 230 within the substrate 110. The layers 230 can be formed from damascene copper and define one or more field effect transistors including a gate (not shown), drain (D), and source (S). The layers 230 are arranged through the thickness of the integrated circuit 120 and cooperate with vias (not shown) to electrically connect contacts 121 within the integrated circuits 120 to one another and electrically connect the structures to the interconnects 250.

[0029] The ability to form the interconnects 150, 250 into multiple sizes and/or shapes advantageously allows the interconnects to transfer power to the integrated circuits 120 at an increased level. More specifically, a single interconnect 150 can contact the conductive layer 130 over a larger surface area than conventional spherical solder balls, thereby allowing more power to flow through a single interconnect to the contacts 121 in the integrated circuit 120 electrically connected therewith. The frequency of the encoded messages that can be passed through the layer 130/interconnect 150, 250 interface is therefore increased.

[0030] In one example, the interconnects 150, 250 can increase the V_{ss} area by at least 80%, the I/O area by at least 30%, the V_{in} area by at least 100% and the V_{sw} area by at least 120% compared to the area afforded by spherical solder balls. As a result, the interconnects 150, 250 can be designed to maximize the size of power and logic interconnections in the electronic device without increasing the size of the associated integrated circuit(s) 120 or violating surface mount technology capability. The interconnects 150 described herein can therefore used for power devices.

[0031] The non-circular interconnects 150, 250 described herein can also advantageously alleviate or substantially reduce the conductive layer routing within the substrate normally required by conventional, spherical solder connections. In particular, some existing electronic devices require multi-level conductive metal routing within the substrate to electrically connect multiple integrated circuits on the opposing side of the substrate. On the other hand, the

conductive interconnects described herein are capable of contacting multiple, electrically isolated contacts or structures within a single integrated circuit in an efficient, cost-effective manner.

[0032] Also, the interconnects 150, 250 can have a reduced thickness compared to spherical interconnects, which results in improved thermal performance as greater heat transfer occurs through the thinner, non-circular interconnect. More specifically, a shorter interconnect provides less resistance and produces less heat loss. Consequently, the interconnects 150, 250 described herein can increase the flexibility in electrical routing to improve the electromigration resistance and thermal efficiency of the electronic device while increasing key interconnection areas between the interconnects and electrical elements. The interconnects also allow for a more efficient use of the substrate space for functional devices.

[0033] Modifications are possible in the described embodiments, and other embodiments are possible, within the scope of the claims.

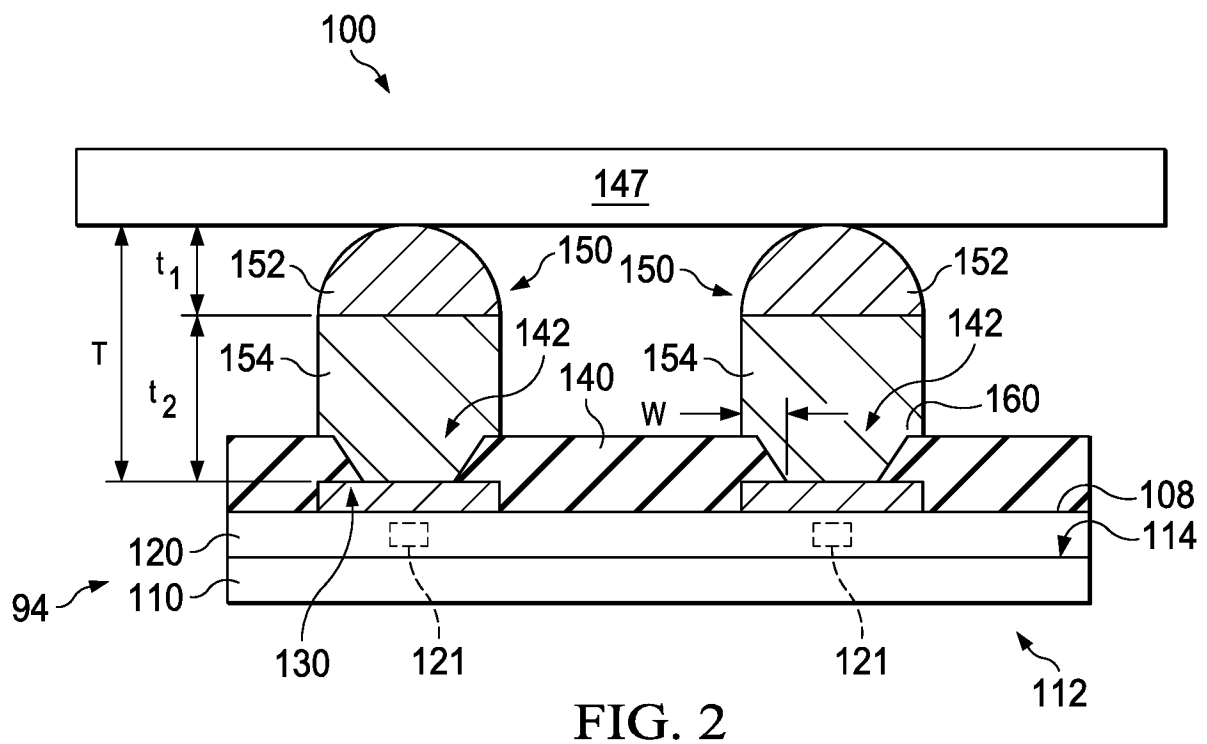
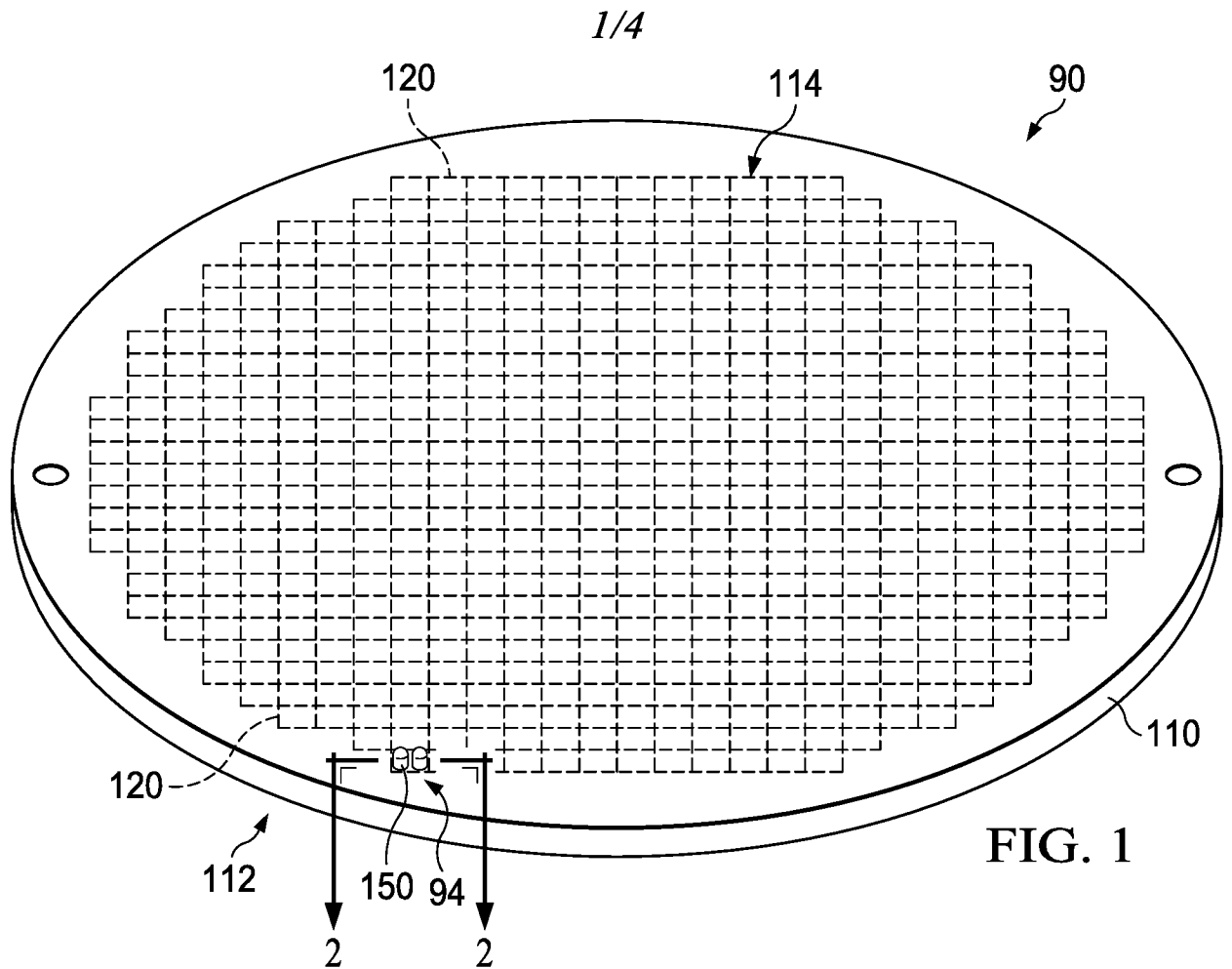
CLAIMS

What is claimed is:

1. A semiconductor die comprising:
a substrate;
an integrated circuit provided on the substrate and having contacts;
an electrically conductive layer provided on the integrated circuit and defining electrically conductive elements electrically connected to the contacts; and
electrically conductive interconnects coupled to respective electrically conductive elements, the electrically conductive interconnects having at least one of different sizes or shapes from one another.
2. The die of claim 1, wherein at least one of the electrically conductive interconnects has a thickness extending away from the electrically conductive elements greater than a width extending perpendicular to the thickness.
3. The die of claim 1, wherein at least one of the electrically conductive interconnects is polygonal in shape.
4. The die of claim 1, wherein at least one of the electrically conductive interconnects has an aspect ratio greater than 1:1.
5. The die of claim 1, further comprising an insulating layer provided over the electrically conductive layer and including openings exposing the electrically conductive elements.
6. The die of claim 5, wherein the electrically conductive interconnects extend through the openings into contact with the electrically conductive elements.
7. The die of claim 1, wherein each electrically conductive interconnect comprises a first portion including tin and a second portion including copper and positioned between the first portion and the electrically conductive layer.
8. The die of claim 7, wherein the second portion has a thickness of about 25-55 μm .
9. The die of claim 7, wherein at least one of the electrically conductive interconnects has a thickness of about 60 μm .
10. The die of claim 1, wherein the plurality of electrically conductive elements comprises first and second elements interdigitated with one another with the electrically conductive interconnect contacting the first and second elements.

11. An electronic package comprising:
a die comprising:
a substrate;
an integrated circuit provided on the substrate and having contacts;
an electrically conductive layer provided on the integrated circuit and defining electrically conductive elements electrically connected to the contacts;
electrically conductive interconnects coupled to respective electrically conductive elements, the electrically conductive interconnects having at least one of different sizes or shapes from one another;
a leadframe secured to the electrically conductive interconnects.
12. The electronic package of claim 11, wherein at least one of the electrically conductive interconnects has a thickness extending away from the electrically conductive elements greater than a width extending perpendicular to the thickness.
13. The electronic package of claim 11, wherein at least one of the electrically conductive interconnects is polygonal in shape.
14. The electronic package of claim 11, wherein at least one of the electrically conductive interconnects has an aspect ratio greater than 1:1.
15. The electronic package of claim 11, further comprising an insulating layer provided over the electrically conductive layer and including openings exposing the electrically conductive elements.
16. The electronic package of claim 15, wherein the electrically conductive interconnects extending through the openings into contact with the electrically conductive elements.
17. The electronic package of claim 11, wherein each electrically conductive interconnect comprises a first portion including tin and a second portion including copper and positioned between the first portion and the electrically conductive layer.
18. The electronic package of claim 17, wherein the second portion has a thickness of about 25-55 μm .
19. The electronic package of claim 17, wherein at least one of the electrically conductive interconnects has a thickness of about 60 μm .

20. The electronic package of claim 11, wherein the plurality of electrically conductive elements comprises first and second elements interdigitated with one another with the electrically conductive interconnect contacting the first and second elements.



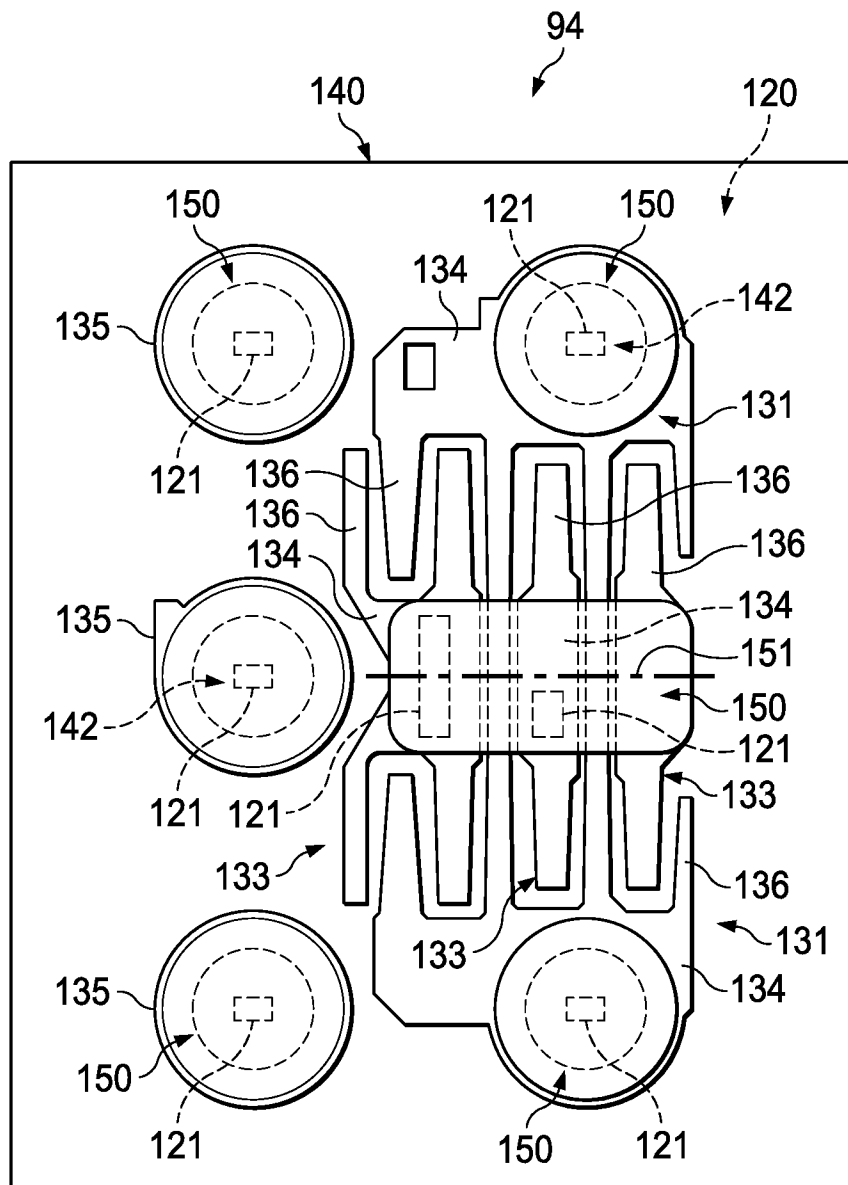


FIG. 3A

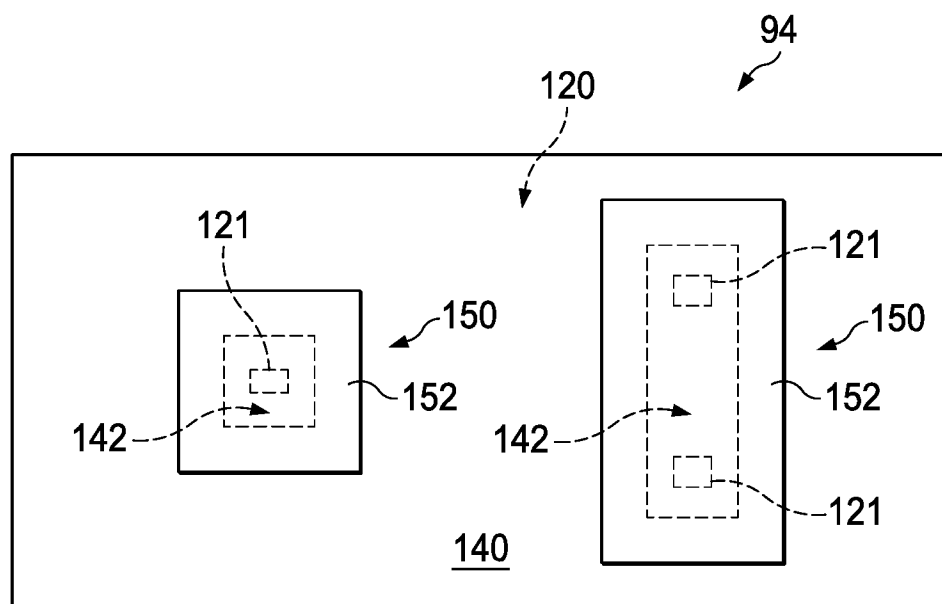
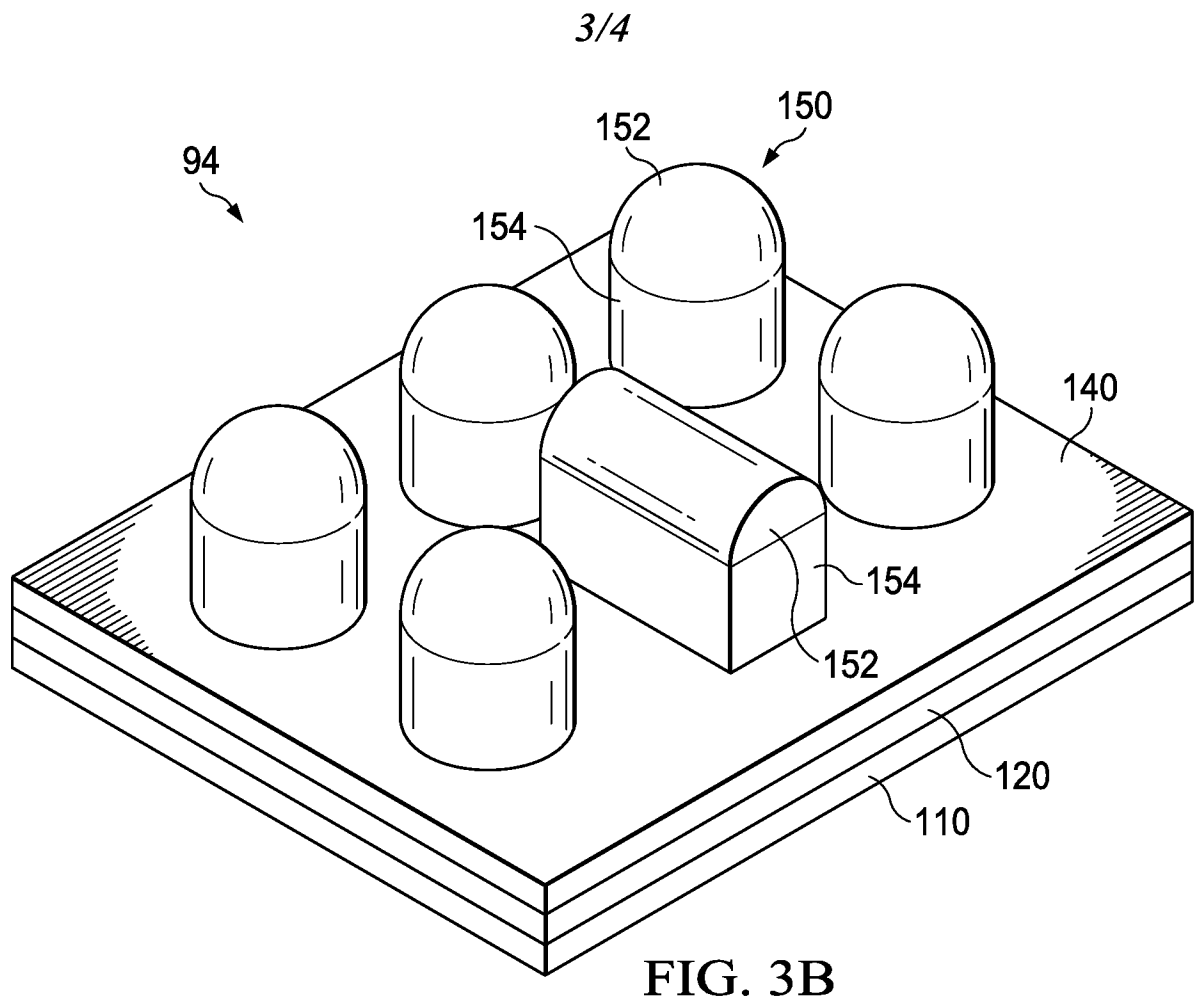


FIG. 4

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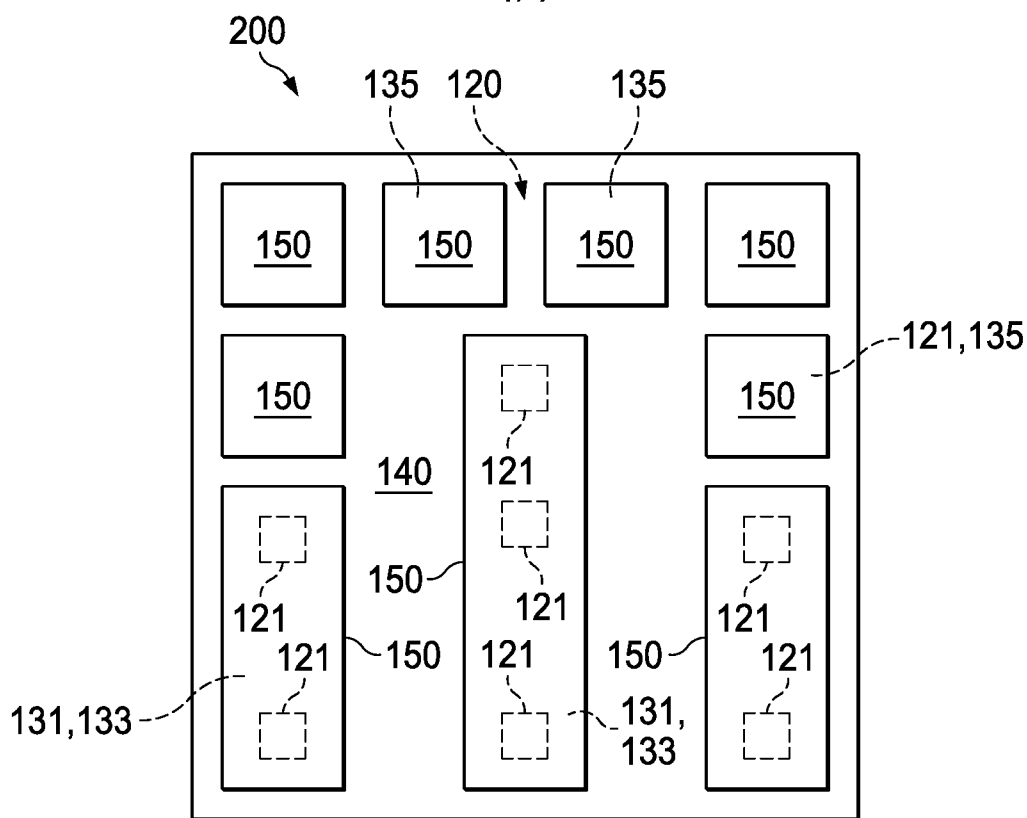


FIG. 5

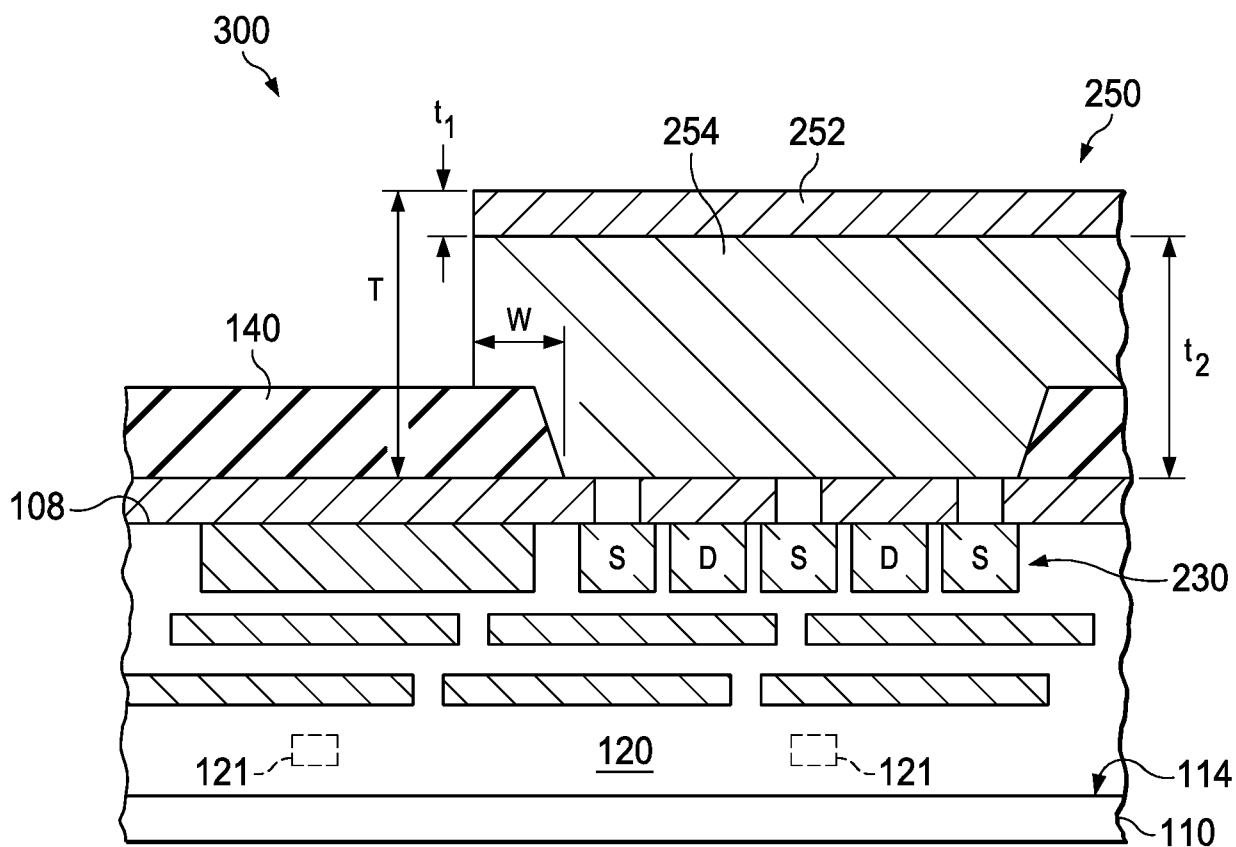


FIG. 6

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INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 2019/068046

A. CLASSIFICATION OF SUBJECT MATTER		
H01L 21/768 (2006.01) H01L 23/482 (2006.01)		
According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED		
Minimum documentation searched (classification system followed by classification symbols)		
H01L 21/00, 21/70, 21/71, 21/768, H01L 23/00, 23/48, 23/482, 23/485, 23/488, 23/495		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched		
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)		
PatSearch (RUPTO internal), USPTO, PAJ, Esp@cenet, DWPI, EAPATIS, PATENTSCOPE, Information Retrieval System of FIPS		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2012/0061823 A1 (TAIWAN SEMICONDUCTOR MFG) 15.03.2012	1-20
A	US 2012/0153458 A1 (TEXAS INSTRUMENTS INCORPORATED) 21.01.2012	1-20
A	US 2014/0231992 A1 (IBM) 21.08.2014	1-20
A	US 2016/0307826 A1 (GAN SYSTEMS INC) 20.10.2016	1-20
A	US 2016/0284629 (GREAT WALL SEMICONDUCTOR CORP) 29.09.2016	1-20
☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.		
* Special categories of cited documents: “A” document defining the general state of the art which is not considered to be of particular relevance “E” earlier document but published on or after the international filing date “L” document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) “O” document referring to an oral disclosure, use, exhibition or other means “P” document published prior to the international filing date but later than the priority date claimed “T” later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention “X” document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone “Y” document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art “&” document member of the same patent family		
Date of the actual completion of the international search		Date of mailing of the international search report
25 March 2020 (25.03.2020)		26 March 2020 (26.03.2020)
Name and mailing address of the ISA/RU: Federal Institute of Industrial Property, Berezhkovskaya nab., 30-1, Moscow, G-59, GSP-3, Russia, 125993 Facsimile No: (8-495) 531-63-18, (8-499) 243-33-37		Authorized officer M. Adireeva Telephone No. (499) 240-25-91